

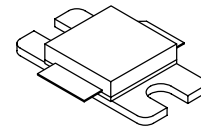
The RF MOSFET Line  
**RF Power Field Effect Transistors**  
**N-Channel Enhancement-Mode Lateral MOSFETs**

**MRF21030LR3**  
**MRF21030LSR3**

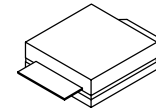
Designed for PCN and PCS base station applications with frequencies from 2.0 to 2.2 GHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB for PCN-PCS/cellular radio and WLL applications.

- Wideband CDMA Performance: -45 dB ACPR @ 4.096 MHz, 28 Volts  
 Output Power — 3.5 Watts  
 Power Gain — 14 dB  
 Efficiency — 15%
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 28 Vdc, 2.11 GHz, 30 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Low Gold Plating Thickness on Leads, 40μ" Nominal.
- In Tape and Reel. R3 Suffix = 250 Units per 32 mm, 13 Inch Reel.

**2.2 GHz, 30 W, 28 V**  
**LATERAL N-CHANNEL**  
**RF POWER MOSFETs**



**CASE 465E-04, STYLE 1**  
**NI-400**  
**MRF21030LR3**



**CASE 465F-04, STYLE 1**  
**NI-400S**  
**MRF21030LSR3**

**MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Drain-Source Voltage	V <sub>DSS</sub>	65	Vdc
Gate-Source Voltage	V <sub>GS</sub>	-0.5, +15	Vdc
Total Device Dissipation @ T <sub>C</sub> = 25°C Derate above 25°C	P <sub>D</sub>	83.3 0.48	Watts W/°C
Storage Temperature Range	T <sub>stg</sub>	- 65 to +150	°C
Operating Junction Temperature	T <sub>J</sub>	200	°C

**ESD PROTECTION CHARACTERISTICS**

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	M3 (Minimum)

**THERMAL CHARACTERISTICS**

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	R <sub>θJC</sub>	2.1	°C/W

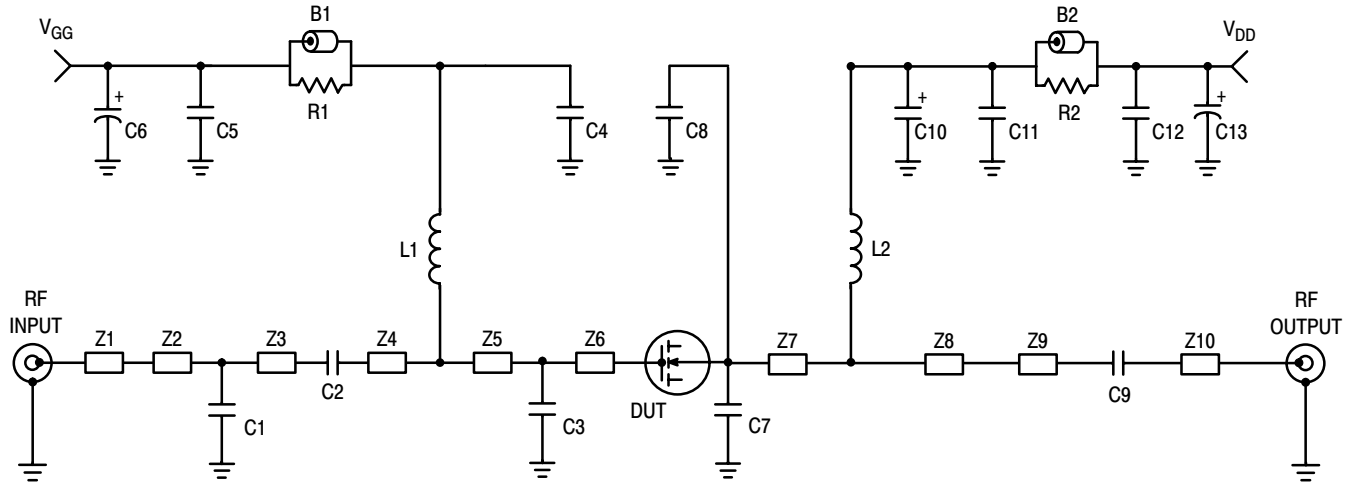
**NOTE - CAUTION** - MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

# Freescale Semiconductor, Inc.

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Drain-Source Breakdown Voltage (V <sub>GS</sub> = 0 Vdc, I <sub>D</sub> = 20 μA)	V <sub>(BR)DSS</sub>	65	—	—	Vdc
Zero Gate Voltage Drain Current (V <sub>DS</sub> = 28 Vdc, V <sub>GS</sub> = 0 Vdc)	I <sub>DSS</sub>	—	—	1	μAdc
Gate-Source Leakage Current (V <sub>GS</sub> = 5 Vdc, V <sub>DS</sub> = 0 Vdc)	I <sub>GSS</sub>	—	—	1	μAdc
<b>ON CHARACTERISTICS</b>					
Gate Threshold Voltage (V <sub>DS</sub> = 10 Vdc, I <sub>D</sub> = 100 μAdc)	V <sub>GS(th)</sub>	2	3	4	Vdc
Gate Quiescent Voltage (V <sub>DS</sub> = 28 Vdc, I <sub>D</sub> = 250 mA)	V <sub>GS(Q)</sub>	2	3.3	4.5	Vdc
Drain-Source On-Voltage (V <sub>GS</sub> = 10 Vdc, I <sub>D</sub> = 1 Adc)	V <sub>DS(on)</sub>	—	0.29	0.4	Vdc
Forward Transconductance (V <sub>DS</sub> = 10 Vdc, I <sub>D</sub> = 1 Adc)	g <sub>fs</sub>	—	2	—	S
<b>DYNAMIC CHARACTERISTICS</b>					
Input Capacitance (Including Input Matching Capacitor in Package) (1) (V <sub>DS</sub> = 28 Vdc, V <sub>GS</sub> = 0, f = 1 MHz)	C <sub>iss</sub>	—	98.5	—	pF
Output Capacitance (1) (V <sub>DS</sub> = 28 Vdc, V <sub>GS</sub> = 0, f = 1 MHz)	C <sub>oss</sub>	—	37	—	pF
Reverse Transfer Capacitance (V <sub>DS</sub> = 28 Vdc, V <sub>GS</sub> = 0, f = 1 MHz)	C <sub>rss</sub>	—	1.3	—	pF
<b>FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system)</b>					
Two-Tone Common-Source Amplifier Power Gain (V <sub>DD</sub> = 28 Vdc, P <sub>out</sub> = 30 W PEP, I <sub>DQ</sub> = 250 mA, f <sub>1</sub> = 2140.0 MHz, f <sub>2</sub> = 2140.1 MHz)	G <sub>ps</sub>	—	13	—	dB
Two-Tone Drain Efficiency (V <sub>DD</sub> = 28 Vdc, P <sub>out</sub> = 30 W PEP, I <sub>DQ</sub> = 250 mA, f <sub>1</sub> = 2140.0 MHz, f <sub>2</sub> = 2140.1 MHz)	η	—	33	—	%
3rd Order Intermodulation Distortion (V <sub>DD</sub> = 28 Vdc, P <sub>out</sub> = 30 W PEP, I <sub>DQ</sub> = 250 mA, f <sub>1</sub> = 2140.0 MHz, f <sub>2</sub> = 2140.1 MHz)	IMD	—	-30	—	dBc
Input Return Loss (V <sub>DD</sub> = 28 Vdc, P <sub>out</sub> = 30 W PEP, I <sub>DQ</sub> = 250 mA, f <sub>1</sub> = 2140.0 MHz, f <sub>2</sub> = 2140.1 MHz)	IRL	—	-13	—	dB
Two-Tone Common-Source Amplifier Power Gain (V <sub>DD</sub> = 28 Vdc, P <sub>out</sub> = 30 W PEP, I <sub>DQ</sub> = 250 mA, f <sub>1</sub> = 2110.0 MHz, f <sub>2</sub> = 2110.1 MHz and f <sub>1</sub> = 2170.0 MHz, f <sub>2</sub> = 2170.1 MHz)	G <sub>ps</sub>	12	13	—	dB
Two-Tone Drain Efficiency (V <sub>DD</sub> = 28 Vdc, P <sub>out</sub> = 30 W PEP, I <sub>DQ</sub> = 250 mA, f <sub>1</sub> = 2110.0 MHz, f <sub>2</sub> = 2110.1 MHz and f <sub>1</sub> = 2170.0 MHz, f <sub>2</sub> = 2170.1 MHz)	η	31	33	—	%
3rd Order Intermodulation Distortion (V <sub>DD</sub> = 28 Vdc, P <sub>out</sub> = 30 W PEP, I <sub>DQ</sub> = 250 mA, f <sub>1</sub> = 2110.0 MHz, f <sub>2</sub> = 2110.1 MHz and f <sub>1</sub> = 2170.0 MHz, f <sub>2</sub> = 2170.1 MHz)	IMD	—	-30	-27.5	dBc
Input Return Loss (V <sub>DD</sub> = 28 Vdc, P <sub>out</sub> = 30 W PEP, I <sub>DQ</sub> = 250 mA, f <sub>1</sub> = 2110.0 MHz, f <sub>2</sub> = 2110.1 MHz and f <sub>1</sub> = 2170.0 MHz, f <sub>2</sub> = 2170.1 MHz)	IRL	—	-13	-9	dB
Output Mismatch Stress (V <sub>DD</sub> = 28 Vdc, P <sub>out</sub> = 30 W CW, I <sub>DQ</sub> = 250 mA, f = 2110 MHz, VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.



B1, B2	Short Ferrite Beads	Z1	0.153" x 0.087" Microstrip
C1	1 pF Chip Capacitor	Z2	0.509" x 0.156" Microstrip
C2	4.7 pF Chip Capacitor	Z3	0.572" x 0.087" Microstrip
C3	0.5 pF Chip Capacitor	Z4	0.509" x 0.232" Microstrip
C4	3.9 pF Chip Capacitor	Z5	0.277" x 0.143" Microstrip
C5, C12	0.1 $\mu$ F Chip Capacitors	Z6	0.200" x 0.305" Microstrip
C6, C13	470 $\mu$ F, 63 V Electrolytic Chip Capacitors	Z7	0.200" x 0.511" Microstrip
C7, C8	0.3 pF Chip Capacitors	Z8	0.510" x 0.328" Microstrip
C9	3.6 pF Chip Capacitor	Z9	0.608" x 0.081" Microstrip
C10	22 $\mu$ F Tantalum Chip Capacitor	PCB	Taconic TLX8, 30 mils, $\epsilon_r = 2.55$
C11	5.1 pF Chip Capacitor		
L1, L2	12.5 nH Inductors		
R1, R2	12 $\Omega$ Chip Resistors (1206)		

Figure 1. MRF21030LR3( LSR3) Test Circuit Schematic

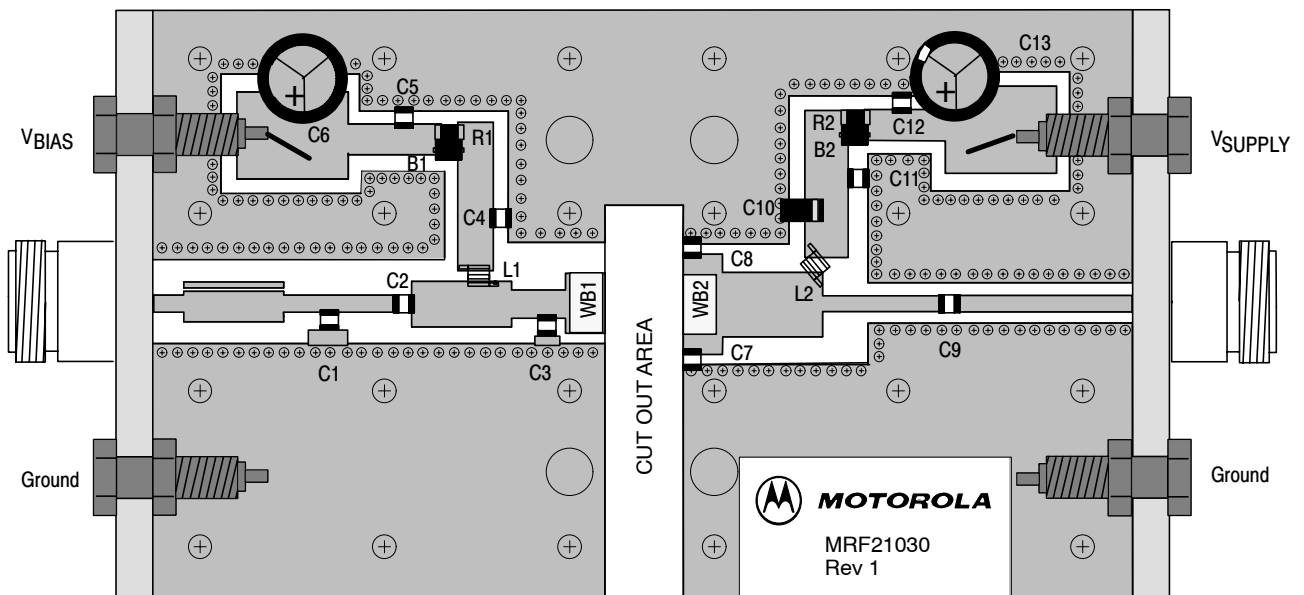


Figure 2. MRF21030LR3( LSR3) Test Circuit Component Layout

## TYPICAL CHARACTERISTICS

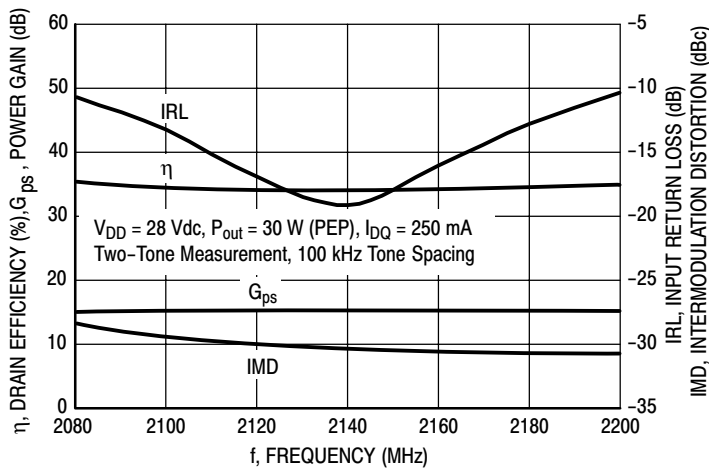


Figure 3. Class AB Broadband Circuit Performance

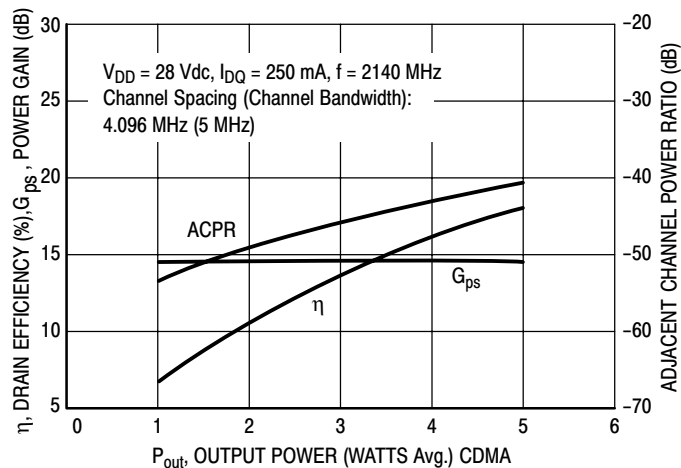


Figure 4. CDMA ACPR, Power Gain and Drain Efficiency versus Output Power

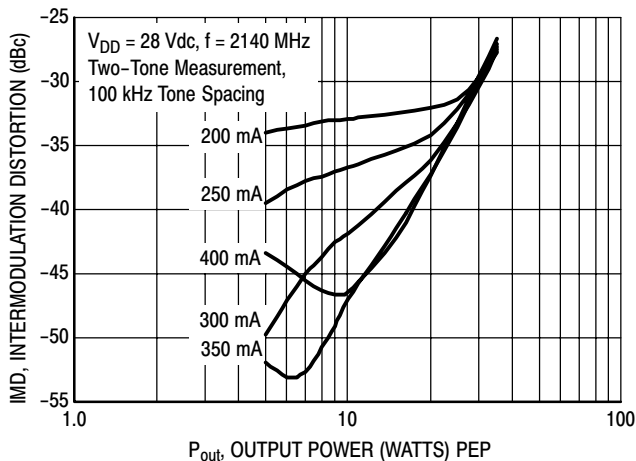


Figure 5. Intermodulation Distortion versus Output Power

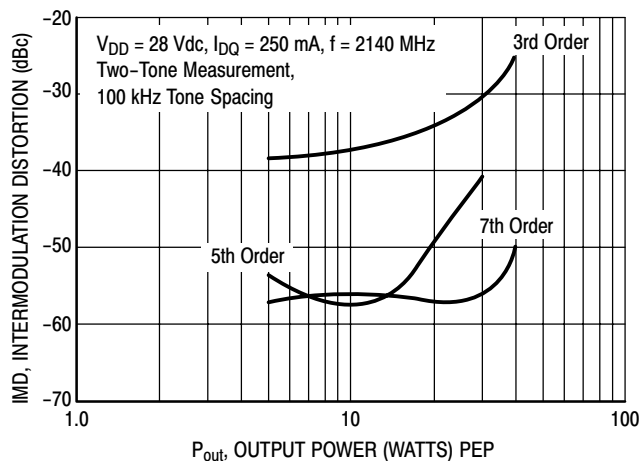


Figure 6. Intermodulation Distortion Products versus Output Power

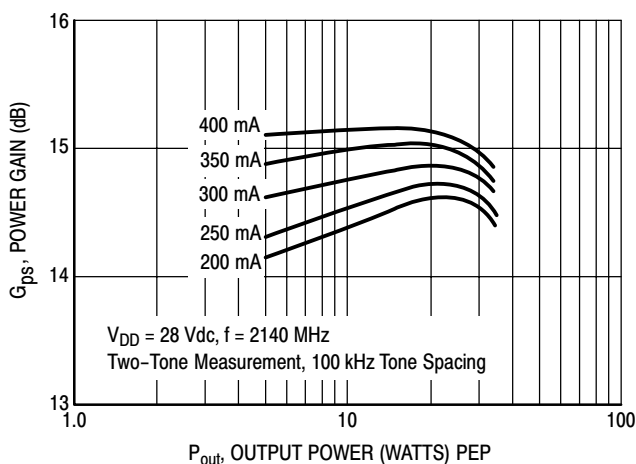


Figure 7. Power Gain versus Output Power

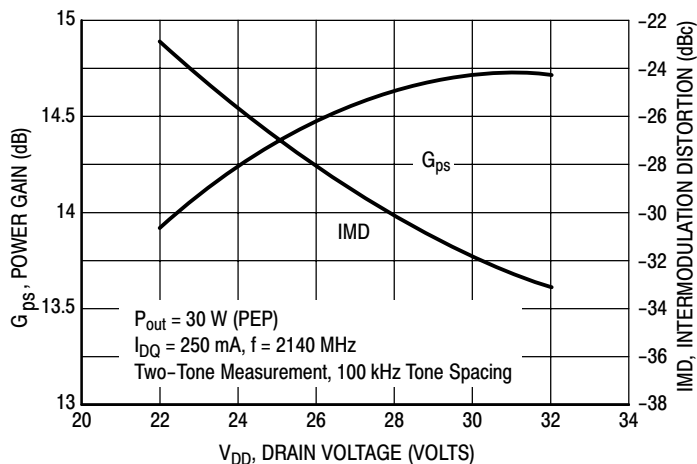
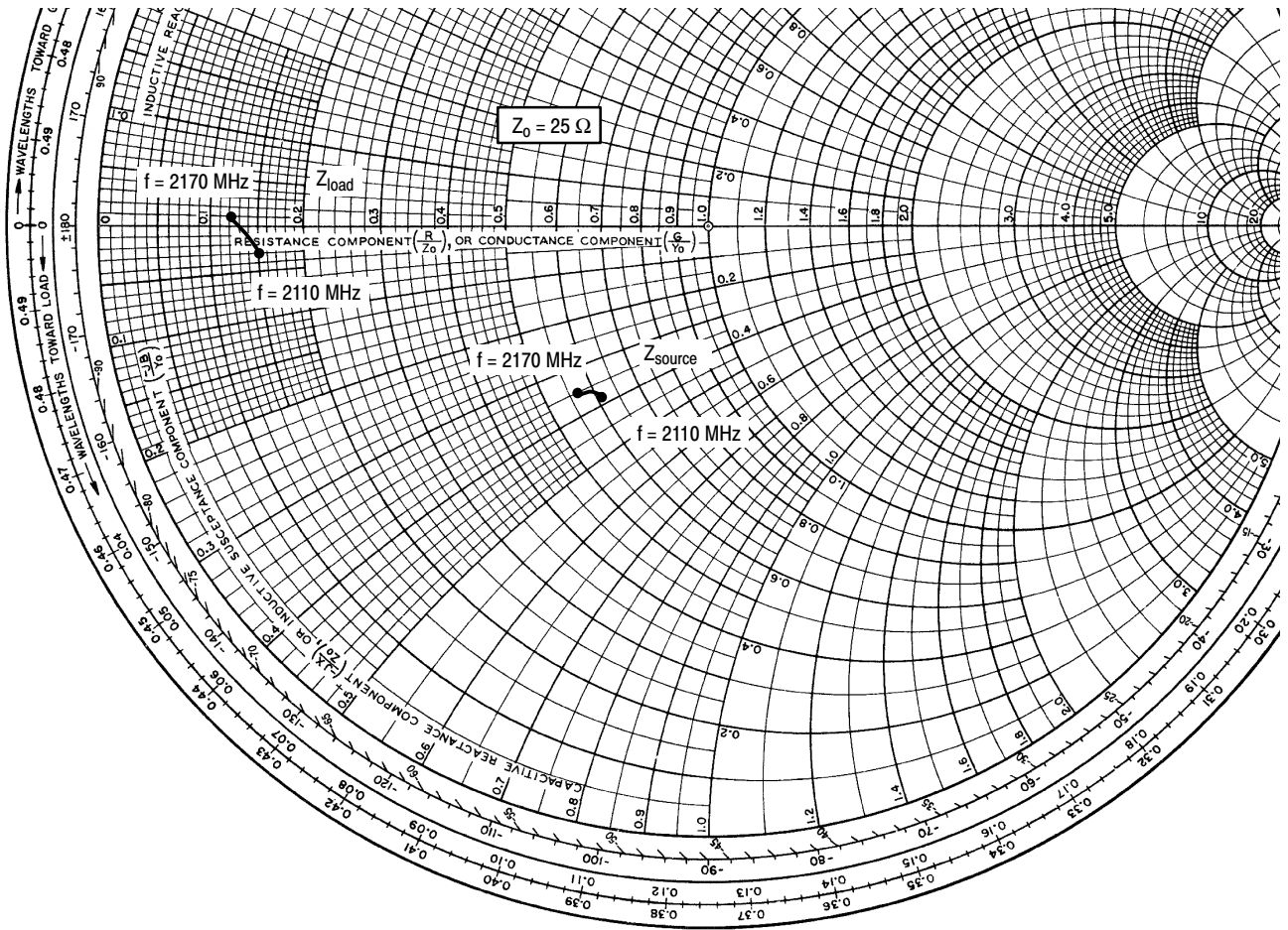


Figure 8. Power Gain and Intermodulation Distortion versus Supply Voltage



$V_{DD} = 28\text{ V}$ ,  $I_{DQ} = 250\text{ mA}$ ,  $P_{out} = 30\text{ W PEP}$

f MHz	Z <sub>source</sub> Ω	Z <sub>load</sub> Ω
2110	15.3 - j9.4	3.7 - j0.78
2140	14.6 - j9.4	3.4 - j0.37
2170	14.3 - j8.8	3.0 + j0.13

Z<sub>source</sub> = Test circuit impedance as measured from gate to ground.

Z<sub>load</sub> = Test circuit impedance as measured from drain to ground.

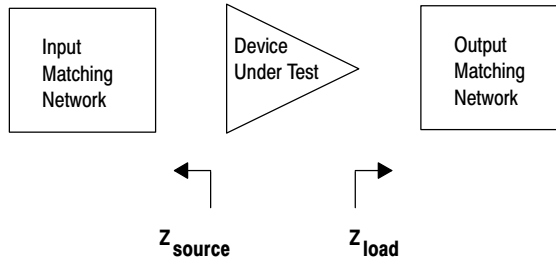


Figure 9. Series Equivalent Source and Load Impedance

**NOTES**



Information in this document is provided solely to enable system and software implementers to use Motorola products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Motorola data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part.

MOTOROLA and the Stylized M Logo are registered in the US Patent and Trademark Office. All other product or service names are the property of their respective owners. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

© Motorola Inc. 2004

#### HOW TO REACH US:

**USA/EUROPE/LOCATIONS NOT LISTED:**  
Motorola Literature Distribution  
P.O. Box 5405, Denver, Colorado 80217  
1-800-521-6274 or 480-768-2130

**JAPAN:** Motorola Japan Ltd.; SPS, Technical Information Center,  
3-20-1, Minami-Azabu, Minato-ku, Tokyo 106-8573, Japan  
81-3-3440-3569

**ASIA/PACIFIC:** Motorola Semiconductors H.K. Ltd.; Silicon Harbour Centre,  
2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong  
852-26668334

**HOME PAGE:** <http://motorola.com/semiconductors>



**MOTOROLA**

**For More Information On This Product,  
Go to: [www.freescale.com](http://www.freescale.com)**

**MRF21030/D**