

Document Title**32Kx8 bit Low Power and Low Voltage CMOS Static RAM****Revision History**

<u>Revision No.</u>	<u>History</u>	<u>Draft Data</u>	<u>Remark</u>
0.0	Initial draft	April 1, 1997	Preliminary
1.0	Finalize - Add 70ns part in KM62U256D Family - Show Icc read only, and increased value Icc = 2mA → Icc Read = 5mA - Separate Icc1 read and write Icc1 = 5mA → Icc1 Read = 5mA, Icc1 Write = 10mA - Improved standby current (I _{SB1}) Commercial part: 10μA → 5μA Extended and Industrial part: 20μA → 5μA - Improved V _{IL} (Min.): 0.4V → 0.6V - Improved power dissipation: 0.7W → 1W	November 12, 1997	Final
1.01	Errata correction - Removed 'TTL Compatible' from Features - Errata correction from 4.5V to 3.0/2.7V for DATA RETENTION WAVE FORM	October 24, 2001	Final

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32Kx8 bit Low Power and Low Voltage CMOS Static RAM

FEATURES

- Process Technology: 0.4μm CMOS
- Organization: 32Kx8
- Power Supply Voltage
K6T0808V1D family: 3.0~3.6V
K6T0808U1D family: 2.7~3.3V
- Low Data Retention Voltage: 2V(Min)
- Three State Outputs
- Package Type: 28-SOP-450, 28-TSOP1-0813.4F/R

GENERAL DESCRIPTION

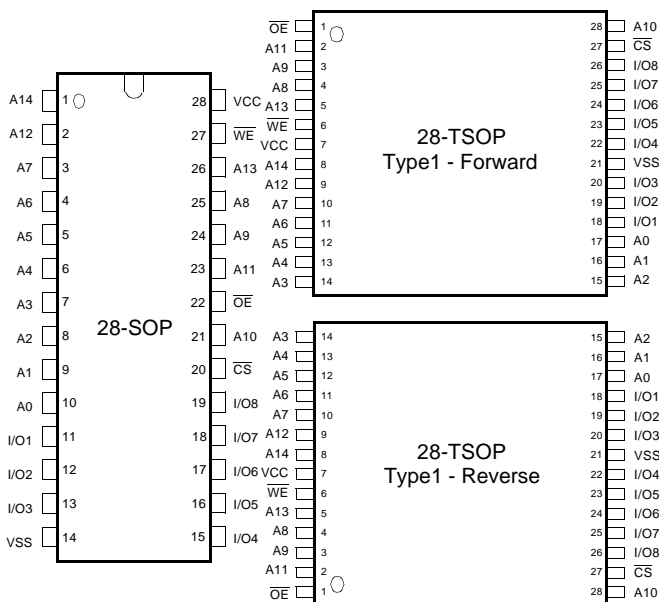
The K6T0808V1D and K6T0808U1D families are fabricated by SAMSUNG's advanced CMOS process technology. The families support various operating temperature range and have various package types for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (I _{SB1} , Max)	Operating (I _{CC2} , Max)	
K6T0808V1D-B K6T0808U1D-B	Commercial(0~70°C)	3.0V ~3.6V 2.7V ~ 3.3V	70 ¹⁾ /100ns 70 ¹⁾ /85/100ns	5μA	35mA	28-SOP-450 ²⁾ 28-TSOP1-0813.4F/R
K6T0808V1D-D K6T0808U1D-D	Extended(-25~85°C)	3.0V ~3.6V 2.7V ~ 3.3V	70 ¹⁾ /100ns 70 ¹⁾ /85/100ns			
K6T0808V1D-F K6T0808U1D-F	Industrial(-40~85°C)	3.0V ~3.6V 2.7V ~ 3.3V	70 ¹⁾ /100ns 70 ¹⁾ /85/100ns			

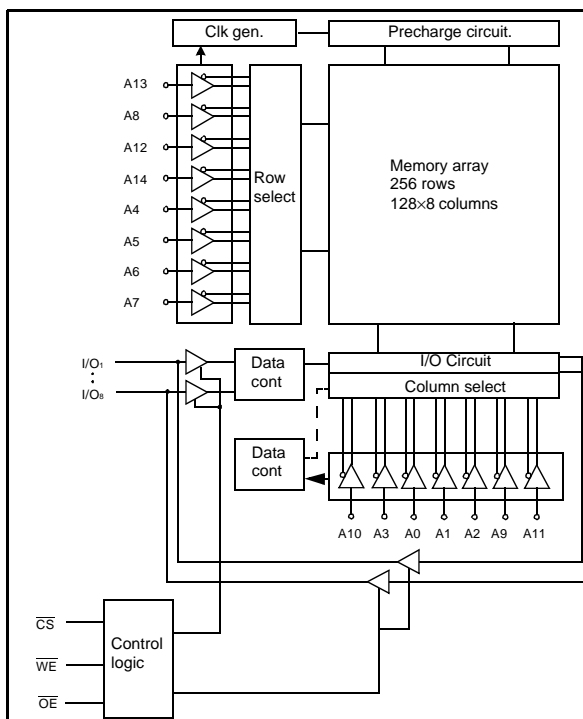
1. The parameter is measured with 30pF test load.
2. K6T0808V1D Family support SOP package without 100ns speed bin.

PIN DESCRIPTION



Pin Name	Function	Pin Name	Function
A ₀ -A ₁₄	Address Inputs	I/O ₁ -I/O ₈	Data Inputs/Outputs
\overline{WE}	Write Enable Input	Vcc	Power
\overline{CS}	Chip Select Input	Vss	Ground
\overline{OE}	Output Enable Input	NC	No connect

FUNCTIONAL BLOCK DIAGRAM



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PRODUCT LIST

Commercial Temp. Product (0~70°C)		Extended Temp. Products (-25~85°C)		Industrial Temp Products (-40~85°C)	
Part Name	Function	Part Name	Function	Part Name	Function
K6T0808V1D-GB70	28-SOP, 70ns, 3.3V	K6T0808V1D-GD70	28-SOP, 70ns, 3.3V	K6T0808V1D-GF70	28-SOP, 70ns, 3.3V
K6T0808V1D-TB70	28-TSOP-F, 70ns, 3.3V	K6T0808V1D-TD70	28-TSOP F, 70ns, 3.3V	K6T0808V1D-TF70	28-TSOP F, 70ns, 3.3V
K6T0808V1D-TB10	28-TSOP-F, 100ns, 3.3V	K6T0808V1D-TD10	28-TSOP F, 100ns, 3.3V	K6T0808V1D-TF10	28-TSOP F, 100ns, 3.3V
K6T0808V1D-RB70	28-TSOP-R, 70ns, 3.3V	K6T0808V1D-RD70	28-TSOP R, 70ns, 3.3V	K6T0808V1D-RF70	28-TSOP R, 70ns, 3.3V
K6T0808V1D-RB10	28-TSOP-R, 100ns, 3.3V	K6T0808V1D-RD10	28-TSOP R, 100ns, 3.3V	K6T0808V1D-RF10	28-TSOP R, 100ns, 3.3V
K6T0808U1D-GB70	28-SOP, 70ns, 3.0V	K6T0808U1D-GD70	28-SOP, 70ns, 3.0V	K6T0808U1D-GF70	28-SOP, 70ns, 3.0V
K6T0808U1D-GB85	28-SOP, 85ns, 3.0V	K6T0808U1D-GD85	28-SOP, 85ns, 3.0V	K6T0808U1D-GF85	28-SOP, 85ns, 3.0V
K6T0808U1D-GB10	28-SOP, 100ns, 3.0V	K6T0808U1D-GD10	28-SOP, 100ns, 3.0V	K6T0808U1D-GF10	28-SOP, 100ns, 3.0V
K6T0808U1D-TB70	28-TSOP-F, 70ns, 3.0V	K6T0808U1D-TD70	28-TSOP-F, 70ns, 3.0V	K6T0808U1D-TF70	28-TSOP-F, 70ns, 3.0V
K6T0808U1D-TB85	28-TSOP-F, 85ns, 3.0V	K6T0808U1D-TD85	28-TSOP-F, 85ns, 3.0V	K6T0808U1D-TF85	28-TSOP-F, 85ns, 3.0V
K6T0808U1D-TB10	28-TSOP-F, 100ns, 3.0V	K6T0808U1D-TD10	28-TSOP-F, 100ns, 3.0V	K6T0808U1D-TF10	28-TSOP-F, 100ns, 3.0V
K6T0808U1D-RB70	28-TSOP-R, 70ns, 3.0V	K6T0808U1D-RD70	28-TSOP-R, 70ns, 3.0V	K6T0808U1D-RF70	28-TSOP-R, 70ns, 3.0V
K6T0808U1D-RB85	28-TSOP-R, 85ns, 3.0V	K6T0808U1D-RD85	28-TSOP-R, 85ns, 3.0V	K6T0808U1D-RF85	28-TSOP-R, 85ns, 3.0V
K6T0808U1D-RB10	28-TSOP-R, 100ns, 3.0V	K6T0808U1D-RD10	28-TSOP-R, 100ns, 3.0V	K6T0808U1D-RF10	28-TSOP-R, 100ns, 3.0V

FUNCTIONAL DESCRIPTION

\overline{CS}	\overline{OE}	\overline{WE}	I/O	Mode	Power
H	X ¹⁾	X ¹⁾	High-Z	Deselected	Standby
L	H	H	High-Z	Output Disabled	Active
L	L	H	Dout	Read	Active
L	X ¹⁾	L	Din	Write	Active

1. X means don't care (Must be in high or low states)

ABSOLUTE MAXIMUM RATINGS¹⁾

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-0.5 to V _{CC} +0.5	V	-
Voltage on Vcc supply relative to Vss	V _{CC}	-0.5 to 4.6	V	-
Power Dissipation	P _D	1.0	W	-
Storage temperature	T _{STG}	-65 to 150	°C	-
Operating Temperature	T _A	0 to 70	°C	K6T0808V1D-B, K6T0808U1D-B
		-25 to 85	°C	K6T0808V1D-D, K6T0808U1D-D
		-40 to 85	°C	K6T0808V1D-F, K6T0808U1D-F
Soldering temperature and time	T _{SOLDER}	260°C, 10sec (Lead Only)	-	-

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS¹⁾

Item	Symbol	Product	Min	Typ	Max	Unit
Supply voltage	V _{CC}	K6T0808V1D Family	3.0	3.3	3.6	V
		K6T0808U1D Family	2.7	3.0	3.3	
Ground	V _{SS}	ALL	0	0	0	V
Input high voltage	V _{IH}	K6T0808V1D, K6T0808U1D Family	2.2	-	V _{CC} +0.3	V
Input low voltage	V _{IL}	K6T0808V1D, K6T0808U1D Family	-0.3 ³⁾	-	0.6	V

Note:

- Commercial Product: T_A=0 to 70°C, otherwise specified
Industrial Product: T_A=-40 to 85°C, otherwise specified
- Overshoot: V_{CC}+3.0V in case of pulse width≤30ns
- Undershoot: -3.0V in case of pulse width≤30ns
- Overshoot and undershoot are sampled, not 100% tested

CAPACITANCE¹⁾ (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C _{IN}	V _{IN} =0V	-	8	pF
Input/Output capacitance	C _{IO}	V _{IO} =0V	-	10	pF

- Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

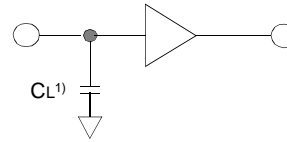
Item	Symbol	Test Conditions	Min	Typ	Max	Unit	
Input leakage current	I _{LI}	V _{IN} =V _{SS} to V _{CC}	-1	-	1	μA	
Output leakage current	I _{LO}	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$, V _{IO} =V _{SS} to V _{CC}	-1	-	1	μA	
Operating power supply current	I _{CC}	I _{IO} =0mA, $\overline{CS}=V_{IL}$, V _{IN} =V _{IH} or V _{IL} , Read	-	2	5	mA	
Average operating current	I _{CC1}	Cycle time=1μs, 100% duty, I _{IO} =0mA $\overline{CS} \leq 0.2V$, V _{IN} ≤0.2V, V _{IN} ≥V _{CC} -0.2V	Read	-	1.5	5	mA
			Write	-	6	10	
	I _{CC2}	Cycle time=Min, 100% duty, I _{IO} =0mA, $\overline{CS}=V_{IL}$, V _{IN} =V _{IH} or V _{IL}	-	23	35	mA	
Output low voltage	V _{OL}	I _{OL} =2.1mA	-	-	0.4	V	
Output high voltage	V _{OH}	I _{OH} =-1.0mA	2.4	-	-	V	
Standby Current(TTL)	I _{SB}	$\overline{CS}=V_{IH}$, Other inputs = V _{IL} or V _{IH}	-	-	0.3	mA	
Standby Current (CMOS)	I _{SB1}	$\overline{CS} \geq V_{CC}-0.2V$, Other inputs=0~V _{CC}	-	0.1	5	μA	

AC OPERATING CONDITIONS

TEST CONDITIONS (Test Load and Test Input/Output Reference)

Input pulse level: 0.4 to 2.4V
 Input rising and falling time: 5ns
 Input and output reference voltage: 1.5V
 Output load (See right): $C_L=100\text{pF}+1\text{TTL}$
 $C_L^1=30\text{pF}+1\text{TTL}$

1. Refer to AC CHARACTERISTICS



1. Including scope and jig capacitance

AC CHARACTERISTICS

(K6T0808V1D Family: $V_{CC}=3.0\sim 3.6\text{V}$, , K6T0808U1D Family: $V_{CC}=2.7\sim 3.3\text{V}$
 Commercial product: $T_A=0$ to 70°C , Extended product: $T_A=-25$ to 85°C , Industrial product: $T_A=-40$ to 85°C)

Parameter List		Symbol	Speed Bins						Units
			70 ¹ ns		85ns		100ns		
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	t _{RC}	70	-	85	-	100	-	ns
	Address access time	t _{AA}	-	70	-	85	-	100	ns
	Chip select to output	t _{CO}	-	70	-	85	-	100	ns
	Output enable to valid output	t _{OE}	-	35	-	40	-	50	ns
	Chip select to low-Z output	t _{LZ}	10	-	10	-	10	-	ns
	Output enable to low-Z output	t _{OLZ}	5	-	5	-	5	-	ns
	Chip disable to high-Z output	t _{HZ}	0	30	0	30	0	35	ns
	Output disable to high-Z output	t _{OHZ}	0	30	0	30	0	35	ns
	Output hold from address	t _{OH}	5	-	10	-	15	-	ns
Write	Write cycle time	t _{WC}	70	-	85	-	100	-	ns
	Chip select to end of write	t _{CW}	60	-	70	-	80	-	ns
	Address set-up time	t _{AS}	0	-	0	-	0	-	ns
	Address valid to end of write	t _{AW}	60	-	70	-	80	-	ns
	Write pulse width	t _{WP}	50	-	60	-	70	-	ns
	Write recovery time	t _{WR}	0	-	0	-	0	-	ns
	Write to output high-Z	t _{WHZ}	0	25	0	25	0	35	ns
	Data to write time overlap	t _{DW}	30	-	35	-	40	-	ns
	Data hold from write time	t _{DH}	0	-	0	-	0	-	ns
	End write to output low-Z	t _{OW}	5	-	10	-	10	-	ns

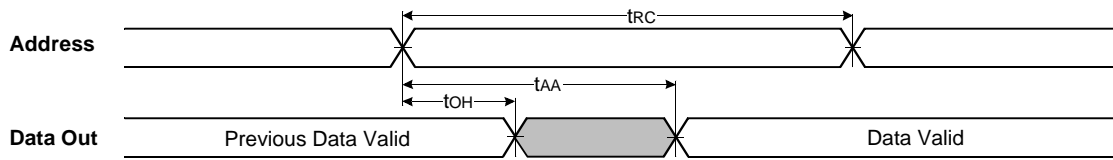
1. The parameter is measured with 30pF test load

DATA RETENTION CHARACTERISTICS

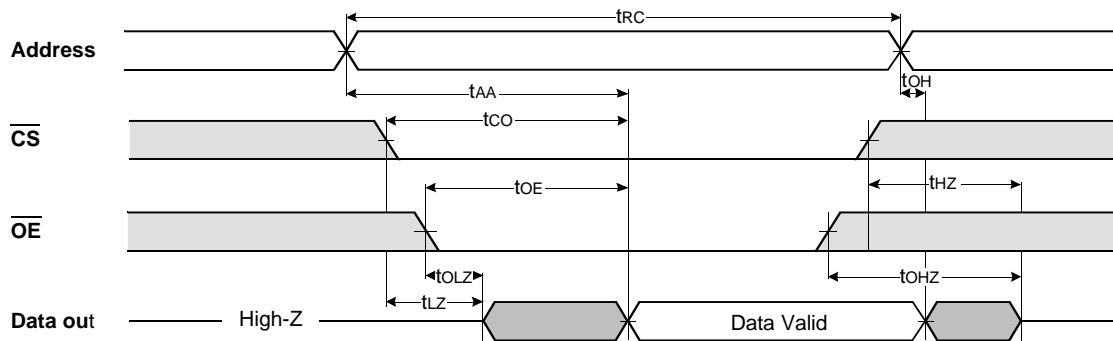
Item	Symbol	Test Condition	Min	Typ	Max	Unit
V _{CC} for data retention	V _{DR}	$\overline{CS} \geq V_{CC}-0.2\text{V}$	2.0	-	3.6	V
Data retention current	I _{DR}	$V_{CC}=3.0\text{V}$, $\overline{CS} \geq V_{CC}-0.2\text{V}$	-	-	5	μA
Data retention set-up time	t _{SDR}	See data retention waveform	0	-	-	ms
Recovery time	t _{RDR}		5	-	-	

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$)



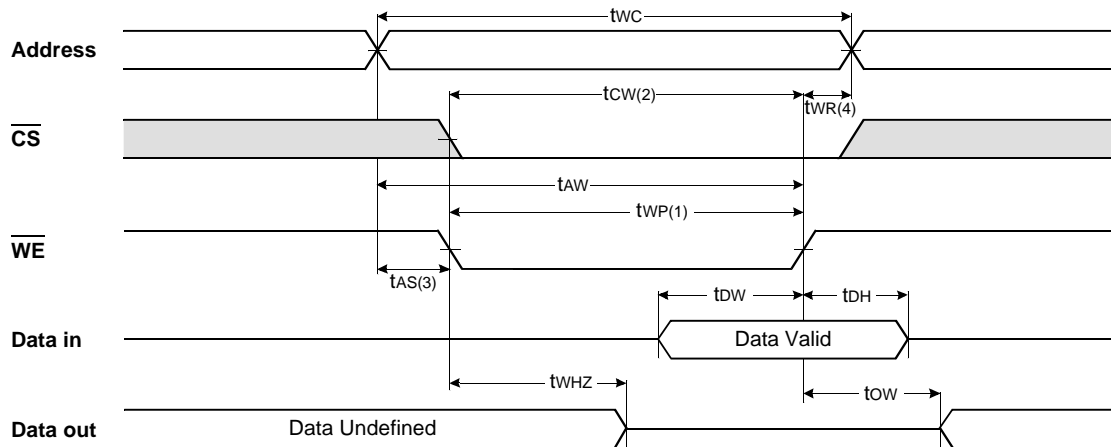
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}=V_{IH}$)



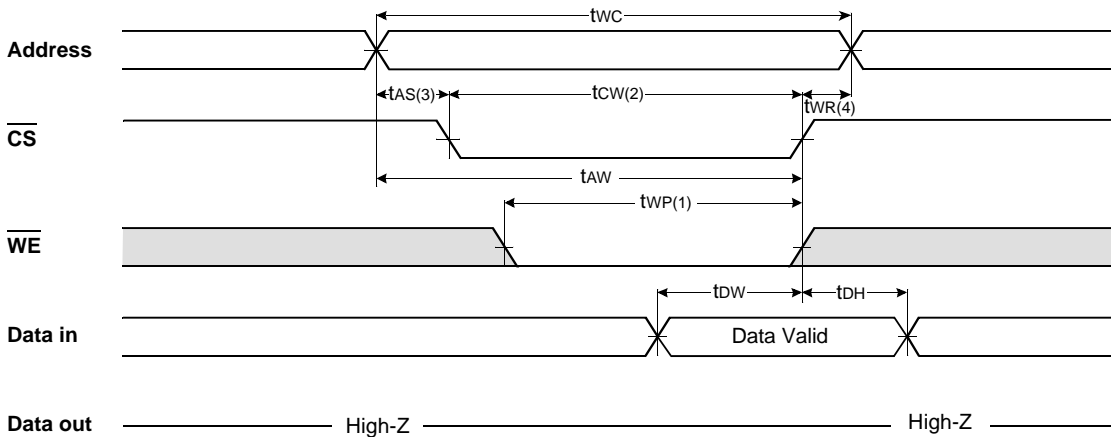
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.

TIMING WAVEFORM OF WRITE CYCLE(1) (\overline{WE} Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) (\overline{CS} Controlled)

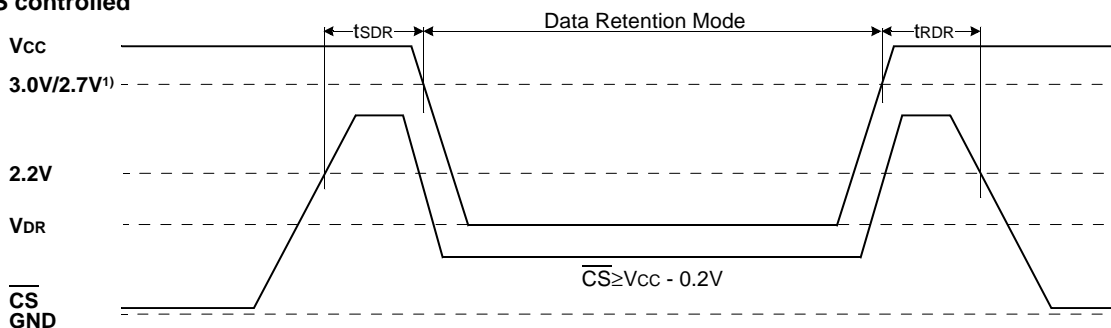


NOTES (WRITE CYCLE)

1. A write occurs during the overlap of a low \overline{CS} and a low \overline{WE} . A write begins at the latest transition among \overline{CS} going Low and \overline{WE} going low : A write end at the earliest transition among CS going high and WE going high, t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the \overline{CS} going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} is applied in case a write ends with \overline{CS} or \overline{WE} going high.

DATA RETENTION WAVE FORM

\overline{CS} controlled

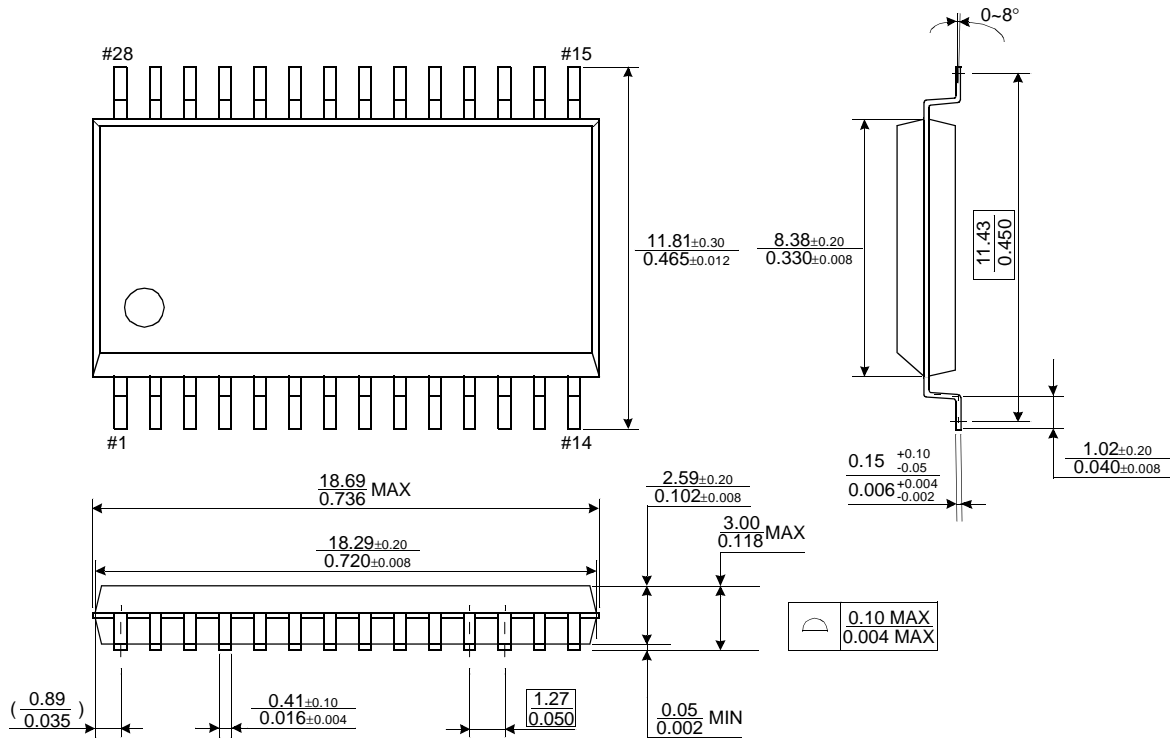


1. 3.0V for K6T0808V1D Family, 2.7V for K6T0808U1D Family

PACKAGE DIMENSIONS

Units: millimeter(inch)

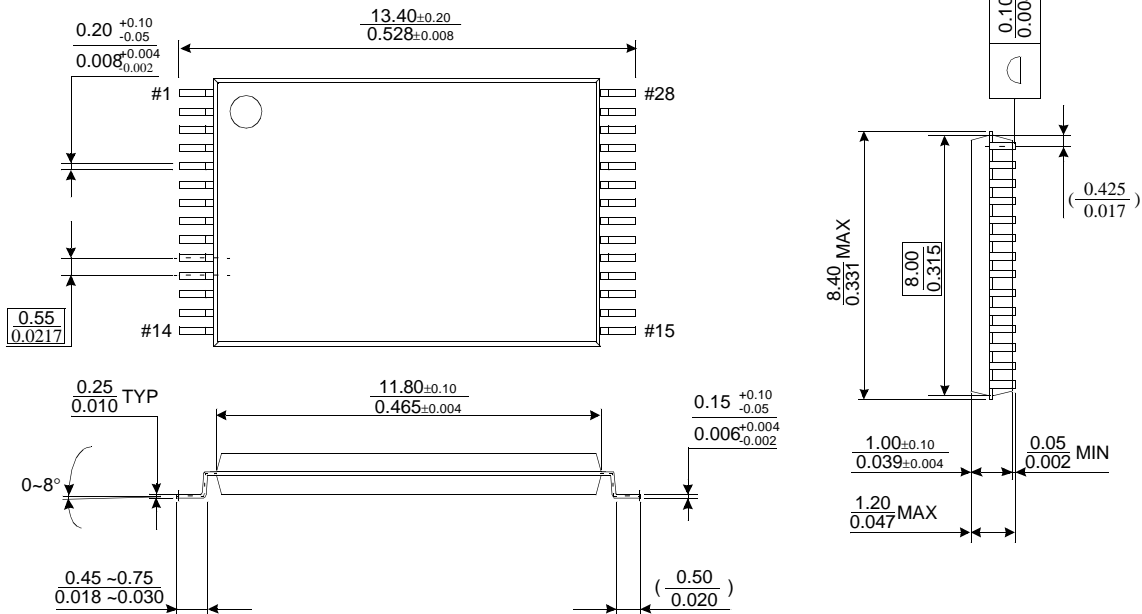
28 PIN PLASTIC SMALL OUTLINE PACKAGE(450mil)



PACKAGE DIMENSIONS

28 PIN THIN SMALL OUTLINE PACKAGE TYPE1 (0813.4F)

Units: millimeter(inch)



28 PIN THIN SMALL OUTLINE PACKAGE TYPE1 (0813.4R)

