

# IGLOO PLUS Low-Power Flash FPGAs with Flash\*Freeze Technology



## Features and Benefits

### Low Power

- 1.2 V to 1.5 V Core Voltage Support for Low Power
- Supports Single-Voltage System Operation
- 5  $\mu$ W Power Consumption in Flash\*Freeze Mode
- Low-Power Active FPGA Operation
- Flash\*Freeze Technology Enables Ultra-Low Power Consumption while Maintaining FPGA Content
- Configurable Hold Previous State, Tristate, HIGH, or LOW State per I/O in Flash\*Freeze Mode
- Easy Entry To / Exit From Ultra-Low-Power Flash\*Freeze Mode

### Feature Rich

- 30 k to 125 k System Gates
- Up to 36 kbits of True Dual-Port SRAM
- Up to 212 User I/Os

### Reprogrammable Flash Technology

- 130-nm, 7-Layer Metal, Flash-Based CMOS Process
- Live-at-Power-Up (LAPU) Level 0 Support
- Single-Chip Solution
- Retains Programmed Design When Powered Off

### In-System Programming (ISP) and Security

- Secure ISP Using On-Chip 128-Bit Advanced Encryption Standard (AES) Decryption via JTAG (IEEE 1532-compliant)<sup>†</sup>
- FlashLock<sup>®</sup> to Secure FPGA Contents

### High-Performance Routing Hierarchy

- Segmented, Hierarchical Routing and Clock Structure

### Advanced I/O

- 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V Mixed-Voltage Operation
- Bank-Selectable I/O Voltages—4 Banks per Chip on All IGLOO<sup>®</sup> PLUS Devices
- Single-Ended I/O Standards: LVTTTL, LVCMOS 3.3 V / 2.5 V / 1.8 V / 1.5 V / 1.2 V
- Selectable Schmitt Trigger Inputs
- I/O Registers on Input, Output, and Enable Paths
- Hot-Swappable and Cold-Sparing I/Os
- Programmable Output Slew Rate and Drive Strength
- Weak Pull-Up/-Down
- IEEE 1149.1 (JTAG) Boundary Scan Test
- Pin-Compatible Small-Footprint Packages across the IGLOO PLUS Family

### Clock Conditioning Circuit (CCC) and PLL<sup>†</sup>

- Six CCC Blocks, One with an Integrated PLL
- Configurable Phase Shift, Multiply/Divide, Delay Capabilities, and External Feedback
- Wide Input Frequency Range (1.5 MHz up to 250 MHz)

### Embedded Memory

- 1 kbit of FlashROM User Nonvolatile Memory
- SRAMs and FIFOs with Variable-Aspect-Ratio 4,608-Bit RAM Blocks (x1, x2, x4, x9, and x18 organizations)<sup>†</sup>
- True Dual-Port SRAM (except x18)<sup>†</sup>

Table 1-1 • IGLOO PLUS Product Family

IGLOO PLUS Devices	AGLP030	AGLP060	AGLP125
System Gates	30 k	60 k	125 k
Typical Equivalent Macrocells	256	512	1,024
VersaTiles (D-flip-flops)	792	1,584	3,120
Flash*Freeze Mode (typical, $\mu$ W)	5	10	16
RAM kbits (1,024 bits)	–	18	36
4,608-Bit Blocks	–	4	8
Secure (AES) ISP	–	Yes	Yes
FlashROM Bits	1 k	1 k	1 k
Integrated PLL in CCCs <sup>1</sup>	–	1	1
VersaNet Globals <sup>2</sup>	6	18	18
I/O Banks	4	4	4
Maximum User I/Os	120	157	212
Package Pins			
CS	CS201, CS289	CS201, CS289	CS281, CS289
VQ	VQ128	VQ176	

Notes:

1. AGLP060 in CS201 does not support the PLL.
2. Six chip (main) and twelve quadrant global networks are available for AGLP060 and AGLP125.

<sup>†</sup> The AGLP030 device does not support this feature.

## I/Os Per Package <sup>1</sup>

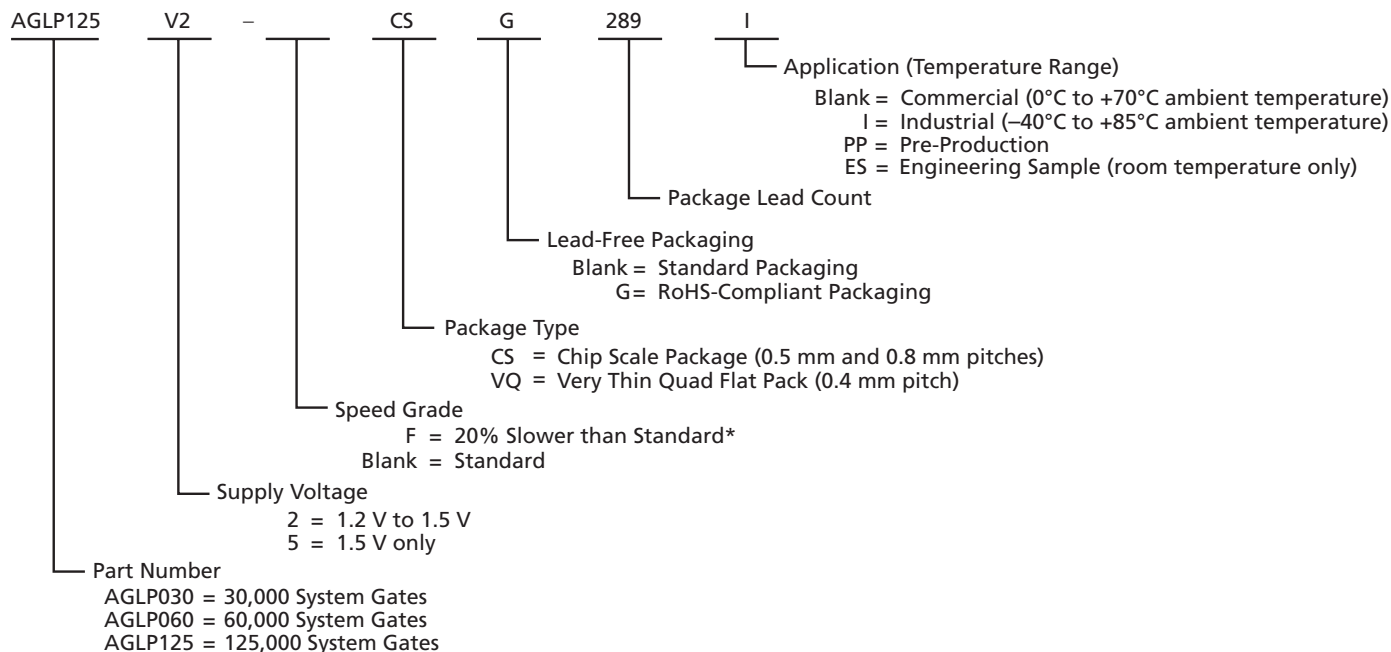
IGLOO PLUS Devices	AGLP030	AGLP060	AGLP125
Package	Single-Ended I/Os		
CS201	120	157	–
CS281	–	–	212
CS289	120	157	212
VQ128	101	–	–
VQ176	–	137	–

*Note:* When the Flash\*Freeze pin is used to directly enable Flash\*Freeze mode and not used as a regular I/O, the number of single-ended user I/Os available is reduced by one.

**Table 1-2 • Package Dimensions**

Package	CS201	CS281	CS289	VQ128	VQ176
Length × Width (mm/mm)	8 × 8	10 × 10	14 × 14	14 × 14	20 × 20
Nominal Area (mm <sup>2</sup> )	64	100	196	196	400
Pitch (mm)	0.5	0.5	0.8	0.4	0.4
Height (mm)	0.89	1.05	1.20	1.0	1.0

## IGLOO PLUS Ordering Information



### Notes:

1. Marking information: IGLOO PLUS V2 devices do not have a V2 marking, but IGLOO PLUS V5 devices are marked accordingly.
2. The DC and switching characteristics for the -F speed grade targets are based only on simulation. The characteristics provided for the -F speed grade are subject to change after establishing FPGA specifications. Some restrictions might be added and will be reflected in future revisions of this document. The -F speed grade is only supported in the Commercial temperature range.
3. "G" indicates RoHS-compliant packages.

## Temperature Grade Offerings

Package	AGLP030	AGLP060	AGLP125
CS201	C, I	C, I	–
CS281	–	–	C, I
CS289	C, I	C, I	C, I
VQ128	C, I	–	–
VQ176	–	C, I	–

**Notes:**

1. C = Commercial temperature range: 0°C to 70°C ambient temperature.
2. I = Industrial temperature range: –40°C to 85°C ambient temperature.

## Speed Grade and Temperature Grade Matrix

Temperature Grade	–F <sup>1</sup>	Std.
C <sup>2</sup>	✓	✓
I <sup>3</sup>	–	✓

**Notes:**

1. The characteristics provided for the –F speed grade are subject to change after establishing FPGA specifications. Some restrictions might be added and will be reflected in future revisions of this document. The –F speed grade is only supported in the Commercial temperature range.
2. C = Commercial temperature range: 0°C to 70°C ambient temperature.
3. I = Industrial temperature range: –40°C to 85°C ambient temperature.

Contact your local Actel representative for device availability:  
<http://www.actel.com/company/contact/default.aspx>.

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# 1 – IGLOO PLUS Device Family Overview

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## General Description

The IGLOO PLUS family of flash FPGAs, based on a 130 nm flash process, offers the lowest power FPGA, a single-chip solution, small-footprint packages, reprogrammability, and an abundance of advanced features.

The Flash\*Freeze technology used in IGLOO PLUS devices enables entering and exiting an ultra-low-power mode that consumes as little as 5  $\mu$ W while retaining the design information, SRAM content, registers, and I/O states. Flash\*Freeze technology simplifies power management through I/O and clock management with rapid recovery to operation mode.

The Low Power Active capability (static idle) allows for ultra-low-power consumption while the IGLOO PLUS device is completely functional in the system. This allows the IGLOO PLUS device to control system power management based on external inputs (e.g., scanning for keyboard stimulus) while consuming minimal power.

Nonvolatile flash technology gives IGLOO PLUS devices the advantage of being a secure, low-power, single-chip solution that is live at power-up (LAPU). IGLOO PLUS is reprogrammable and offers time-to-market benefits at an ASIC-level unit cost.

These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

IGLOO PLUS devices offer 1 kbit of on-chip, reprogrammable, nonvolatile FlashROM storage as well as clock conditioning circuitry based on an integrated phase-locked loop (PLL). IGLOO PLUS devices have up to 125 k system gates, supported with up to 36 kbits of true dual-port SRAM and up to 212 user I/Os. The AGLP030 devices have no PLL or RAM support.

### Flash\*Freeze Technology

The IGLOO PLUS device offers unique Flash\*Freeze technology, allowing the device to enter and exit ultra-low-power Flash\*Freeze mode. IGLOO PLUS devices do not need additional components to turn off I/Os or clocks while retaining the design information, SRAM content, registers, and I/O states. Flash\*Freeze technology is combined with in-system programmability, which enables users to quickly and easily upgrade and update their designs in the final stages of manufacturing or in the field. The ability of IGLOO PLUS V2 devices to support a wide range of core and I/O voltages (1.2 V to 1.5 V) allows further reduction in power consumption, thus achieving the lowest total system power.

During Flash\*Freeze mode, each I/O can be set to the following configurations: hold previous state, tristate, or set as HIGH or LOW.

The availability of low-power modes, combined with reprogrammability, a single-chip and single-voltage solution, and availability of small-footprint, high-pin-count packages, make IGLOO PLUS devices the best fit for portable electronics.

### Flash Advantages

#### **Low Power**

IGLOO PLUS devices exhibit power characteristics similar to those of an ASIC, making them an ideal choice for power-sensitive applications. IGLOO PLUS devices have only a very limited power-on current surge and no high-current transition period, both of which occur on many FPGAs.

IGLOO PLUS devices also have low dynamic power consumption to further maximize power savings; power is even further reduced by the use of a 1.2 V core voltage.

Low dynamic power consumption, combined with low static power consumption and Flash\*Freeze technology, gives the IGLOO PLUS device the lowest total system power offered by any FPGA.

## **Security**

The nonvolatile, flash-based IGLOO PLUS devices do not require a boot PROM, so there is no vulnerable external bitstream that can be easily copied. IGLOO PLUS devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer.

IGLOO PLUS devices (except AGLP030) utilize a 128-bit flash-based lock and a separate AES key to secure programmed intellectual property and configuration data. In addition, all FlashROM data in IGLOO PLUS devices can be encrypted prior to loading, using the industry-leading AES-128 (FIPS192) bit block cipher encryption standard. AES was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the 1977 DES standard. IGLOO PLUS devices have a built-in AES decryption engine and a flash-based AES key that make them the most comprehensive programmable logic device security solution available today. IGLOO PLUS devices with AES-based security allow for secure, remote field updates over public networks such as the Internet, and ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves. The contents of a programmed IGLOO PLUS device cannot be read back, although secure design verification is possible.

Security, built into the FPGA fabric, is an inherent component of the IGLOO PLUS family. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. The IGLOO PLUS family, with FlashLock and AES security, is unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected and secure, making remote ISP possible. An IGLOO PLUS device provides the most impenetrable security for programmable logic designs.

## **Single Chip**

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based IGLOO PLUS FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.

The IGLOO PLUS devices can be operated with a 1.2 V or 1.5 V single-voltage supply for core and I/Os, eliminating the need for additional supplies while minimizing total power consumption.

## **Live at Power-Up**

The Actel flash-based IGLOO PLUS devices support Level 0 of the LAPU classification standard. This feature helps in system component initialization, execution of critical tasks before the processor wakes up, setup and configuration of memory blocks, clock generation, and bus activity management. The LAPU feature of flash-based IGLOO PLUS devices greatly simplifies total system design and reduces total system cost, often eliminating the need for CPLDs and clock generation PLLs. In addition, glitches and brownouts in system power will not corrupt the IGLOO PLUS device's flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM, expensive voltage monitor, brownout detection, and clock generator devices from the PCB design. Flash-based IGLOO PLUS devices simplify total system design and reduce cost and design risk while increasing system reliability and improving system initialization time.

IGLOO PLUS flash FPGAs allow the user to quickly enter and exit Flash\*Freeze mode. This is done almost instantly (within 1  $\mu$ s), and the device retains configuration and data in registers and RAM. Unlike SRAM-based FPGAs, the device does not need to reload configuration and design state from external memory components; instead, it retains all necessary information to resume operation immediately.

## **Reduced Cost of Ownership**

Advantages to the designer extend beyond low unit cost, performance, and ease of use. Unlike SRAM-based FPGAs, flash-based IGLOO PLUS devices allow all functionality to be live at power-up; no external boot PROM is required. On-board security mechanisms prevent access to all the programming information and enable secure remote updates of the FPGA logic. Designers can perform secure remote in-system reprogramming to support future design iterations and field

upgrades with confidence that valuable intellectual property cannot be compromised or copied. Secure ISP can be performed using the industry-standard AES algorithm. The IGLOO PLUS family device architecture mitigates the need for ASIC migration at higher user volumes. This makes the IGLOO PLUS family a cost-effective ASIC replacement solution, especially for applications in the consumer, networking/communications, computing, and avionics markets.

### **Firm-Error Immunity**

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. These errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not exist in the configuration memory of IGLOO PLUS flash-based FPGAs. Once it is programmed, the flash cell configuration element of IGLOO PLUS FPGAs cannot be altered by high-energy neutrons and is therefore immune to them. Recoverable (or soft) errors occur in the user data SRAM of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

### **Advanced Flash Technology**

The IGLOO PLUS family offers many benefits, including nonvolatility and reprogrammability, through an advanced flash-based, 130 nm LVCMOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

IGLOO PLUS family FPGAs utilize design and process techniques to minimize power consumption in all modes of operation.

### **Advanced Architecture**

The proprietary IGLOO PLUS architecture provides granularity comparable to standard-cell ASICs. The IGLOO PLUS device consists of five distinct and programmable architectural features (Figure 1-1 on page 1-4):

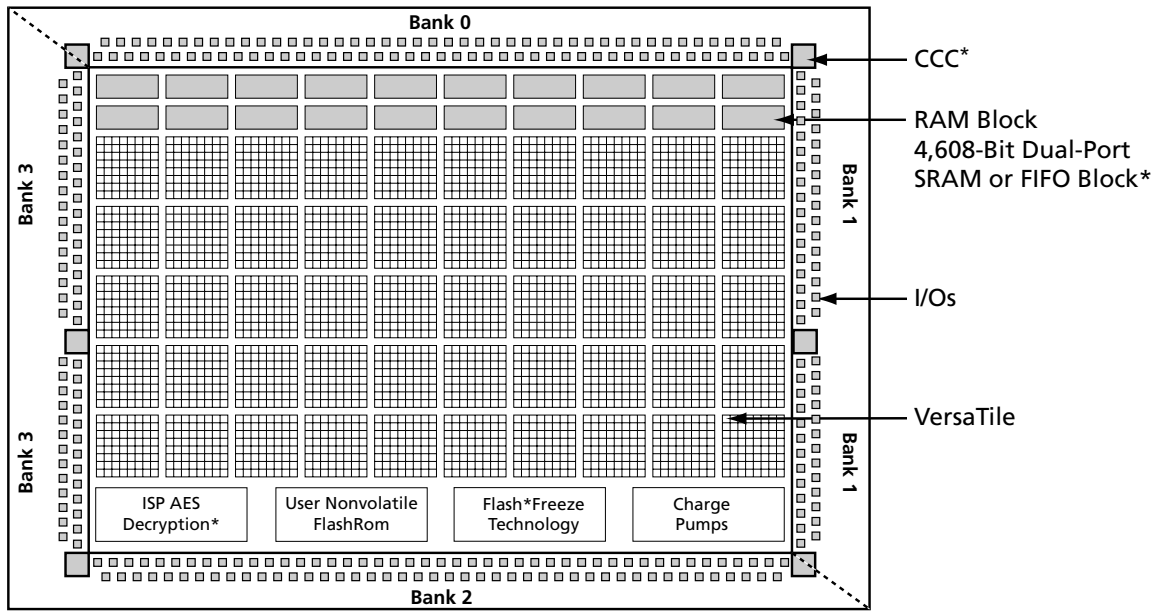
- Flash\*Freeze technology
- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory<sup>†</sup>
- Extensive CCCs and PLLs<sup>†</sup>
- Advanced I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate flash switch interconnections. The versatility of the IGLOO PLUS core tile as either a three-input lookup table (LUT) equivalent or a D-flip-flop/latch with enable allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the Actel ProASIC family of third-generation-architecture flash FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

In addition, extensive on-chip programming circuitry allows for rapid, single-voltage (3.3 V) programming of IGLOO PLUS devices via an IEEE 1532 JTAG interface.

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<sup>†</sup> The AGLP030 device does not support PLL or SRAM.



\* Not supported by AGLP030 devices

Figure 1-1 • IGLOO PLUS Device Architecture Overview with Four I/O Banks (AGLP030, AGLP060, and AGLP125)

### Flash\*Freeze Technology

The IGLOO PLUS device has an ultra-low-power static mode, called Flash\*Freeze mode, which retains all SRAM and register information and can still quickly return to normal operation. Flash\*Freeze technology enables the user to quickly (within 1  $\mu$ s) enter and exit Flash\*Freeze mode by activating the Flash\*Freeze pin while all power supplies are kept at their original values. In addition, I/Os and global I/Os can still be driven and can be toggling without impact on power consumption, clocks can still be driven or can be toggling without impact on power consumption, and the device retains all core registers, SRAM information, and I/O states. I/Os can be individually configured to either hold their previous state or be tristated during Flash\*Freeze mode. Alternatively, they can be set to a certain state using weak pull-up or pull-down I/O attribute configuration. No power is consumed by the I/O banks, clocks, JTAG pins, or PLL, and the device consumes as little as 5  $\mu$ W in this mode.

Flash\*Freeze technology allows the user to switch to Active mode on demand, thus simplifying the power management of the device.

The Flash\*Freeze pin (active low) can be routed internally to the core to allow the user's logic to decide when it is safe to transition to this mode. Refer to Figure 1-2 for an illustration of



entering/exiting Flash\*Freeze mode. It is also possible to use the Flash\*Freeze pin as a regular I/O if Flash\*Freeze mode usage is not planned.

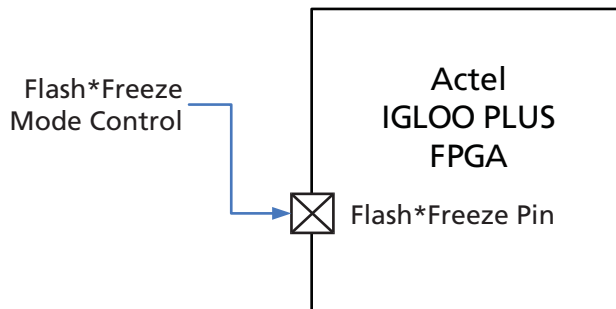


Figure 1-2 • IGLOO PLUS Flash\*Freeze Mode

### VersaTiles

The IGLOO PLUS core consists of VersaTiles, which have been enhanced beyond the ProASIC<sup>PLUS</sup>® core tiles. The IGLOO PLUS VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set

Refer to Figure 1-3 for VersaTile configurations.

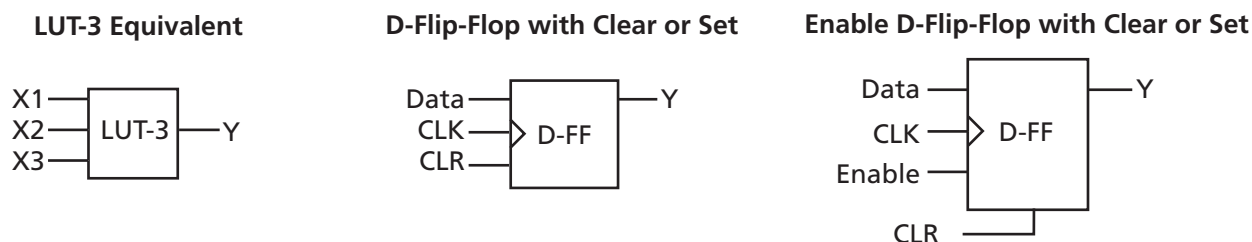


Figure 1-3 • VersaTile Configurations

### User Nonvolatile FlashROM

Actel IGLOO PLUS devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard IGLOO PLUS IEEE 1532 JTAG programming interface. The core can be individually programmed (erased and written), and on-chip AES decryption can be used selectively to securely load data over public networks (except in AGLP030 devices), as in security keys stored in the FlashROM for a user design.

The FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

The FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

The Actel IGLOO PLUS development software solutions, Libero® Integrated Design Environment (IDE) and Designer, have extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Actel Libero IDE and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

### **SRAM and FIFO**

IGLOO PLUS devices (except AGLP030 devices) have embedded SRAM blocks along their north side. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a 4-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode) using the UJTAG macro (except in AGLP030 devices).

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal Empty and Full flags. The embedded FIFO control unit contains the counters necessary for generation of the read and write address pointers. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

### **PLL and CCC**

IGLOO PLUS devices provide designers with very flexible clock conditioning circuit (CCC) capabilities. Each member of the IGLOO PLUS family contains six CCCs. One CCC (center west side) has a PLL. The AGLP030 device does not have a PLL or CCCs; it contains only inputs to six globals.

The six CCC blocks are located at the four corners and the centers of the east and west sides. One CCC (center west side) has a PLL.

The four corner CCCs and the east CCC allow simple clock delay operations as well as clock spine access.

The inputs of the six CCC blocks are accessible from the FPGA core or from one of several inputs located near the CCC that have dedicated connections to the CCC block.

The CCC block has these key features:

- Wide input frequency range ( $f_{IN\_CCC}$ ) = 1.5 MHz up to 250 MHz
- Output frequency range ( $f_{OUT\_CCC}$ ) = 0.75 MHz up to 250 MHz
- 2 programmable delay types for clock skew minimization
- Clock frequency synthesis (for PLL only)

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°. Output phase shift depends on the output divider configuration (for PLL only).
- Output duty cycle = 50% ± 1.5% or better (for PLL only)
- Low output jitter: worst case < 2.5% × clock period peak-to-peak period jitter when single global network used (for PLL only)
- Maximum acquisition time is 300 μs (for PLL only)

- Exceptional tolerance to input period jitter—allowable input jitter is up to 1.5 ns (for PLL only)
- Four precise phases; maximum misalignment between adjacent phases of  $40 \text{ ps} \times 250 \text{ MHz} / f_{\text{OUT\_CCC}}$  (for PLL only)

### **Global Clocking**

IGLOO PLUS devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there is a comprehensive global clock distribution network.

Each VersaTile input and output port has access to nine VersaNets: six chip (main) and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via multiplexers (MUXes). The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high-fanout nets.

### ***I/Os with Advanced I/O Standards***

The IGLOO PLUS family of FPGAs features a flexible I/O structure, supporting a range of voltages (1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V). IGLOO PLUS FPGAs support many different I/O standards.

The I/Os are organized into four banks. All devices in IGLOO PLUS have four banks. The configuration of these banks determines the I/O standards supported.

Each I/O module contains several input, output, and output enable registers.

## **Part Number and Revision Date**

Part Number 51700102-001-3

Revised December 2008

## **List of Changes**

The following table lists critical changes that were made in the current version of the document.

<b>Previous Version</b>	<b>Changes in Current Version (v1.3)</b>	<b>Page</b>
v1.2 (August 2008)	A note was added to <a href="#">Table 1-1 · IGLOO PLUS Product Family</a> : "AGLP060 in CS201 does not support the PLL."	I
	<a href="#">Table 1-2 · Package Dimensions</a> was updated to change the nominal size of VQ176 from 100 to 400 mm <sup>2</sup> .	II
v1.1 (July 2008)	The VQ128 and VQ176 packages were added to <a href="#">Table 1-1 · IGLOO PLUS Product Family</a> , the " <a href="#">I/Os Per Package</a> <sup>1</sup> " table, <a href="#">Table 1-2 · Package Dimensions</a> , " <a href="#">IGLOO PLUS Ordering Information</a> ", and the " <a href="#">Temperature Grade Offerings</a> " table.	I to IV
v1.0 (March 2008)	As a result of the Libero IDE v8.4 release, Actel now offers a wide range of core voltage support. The document was updated to change 1.2 V / 1.5 V to 1.2 V to 1.5 V.	N/A

## Datasheet Categories

### ***Categories***

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advance," "Preliminary," and "Production." The definitions of these categories are as follows:

### ***Product Brief***

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

### ***Advance***

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

### ***Preliminary***

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

### ***Unmarked (production)***

This version contains information that is considered to be final.

## **Export Administration Regulations (EAR)**

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