Approved Product

CY25811 / CY25812 / CY25814

Spread Spectrum Clock Generator

FEATURES

- 4 to 32 MHz Input Frequency Range
- 4 to 128 MHz Output Frequency Range
- Accepts Clock, Crystal and Resonator Inputs
- 1x, 2x and 4x Frequency Multiplication:
  CY25811: 1x CY25812: 2x CY25814: 4x
- Center and Down Spread Modulation
- Frequency Range Selection
- Low Power Dissipation :
  3.3V = 52 mW-typ @ 6MHz
  3.3V = 60 mW-typ @ 12MHz
  3.3V = 72 mW-typ @ 24MHz
- Low Cycle-to Cycle Jitter:
  8MHz = 195 ps-typ
  16MHz = 175 ps-typ
  32MHz = 100 ps-typ
- Available in 8-pin (150 mil.) SOIC package

APPLICATIONS

- Printers and MFPs
- LCD Panels
- Digital Copiers
- PDAs
- Automotive
- CD-ROM, VCD and DVD
- Networking, LAN/WAN
- Scanners
- Modems
- Embedded Digital Systems

BENEFITS

- Peak EMI reduction by 8 to 16dB
- Fast Time to Market
- Cost Reduction

GENERAL DESCRIPTION

The CY25811/12/14 products are Spread Spectrum Clock Generator (SSCG) ICs used for the purpose of reducing Electro Magnetic Interference (EMI) found in today's high-speed digital electronic systems.

The devices use a Cypress proprietary Phase-Locked Loop (PLL) and Spread Spectrum Clock (SSC) technology to synthesize and modulate the frequency of the input clock. By frequency modulating the clock, the measured EMI at the fundamental and harmonic frequencies is greatly reduced.
This reduction in radiated energy can significantly reduce the cost of complying with regulatory agency requirements and improve time to market without degrading system performance.

The input frequency range is 4 to 32 MHz and accepts clock, crystal and ceramic resonator inputs. The output clock can be selected to produce 1x, 2x or 4x multiplication of the input frequency with Spread Spectrum Frequency Modulation.

The use of 2x or 4x frequency multiplication eliminates the need for higher order crystals and enables the user to generate up to 128 MHz Spread Spectrum Clock (SSC) by using only first order crystals. This will reduce the cost while improving the system clock accuracy, performance and complexity

Center Spread or Down Spread frequency modulation can be selected by the user based on 4 discrete values of Spread % for each Spread Mode with the option of a Non-Spread mode for system test and verification purposes.

The CY25811/12/14 products are available in an 8 pin SOIC (150-mil.) package with a commercial operating temperature range of 0 to 70°C. Contact Cypress for availability of -25 to +85°C Industrial Temperature Range Operation. Refer to CY25568 for multiple clock output options such as modulated and unmodulated clock outputs or Power Down function.

BLOCK DIAGRAM

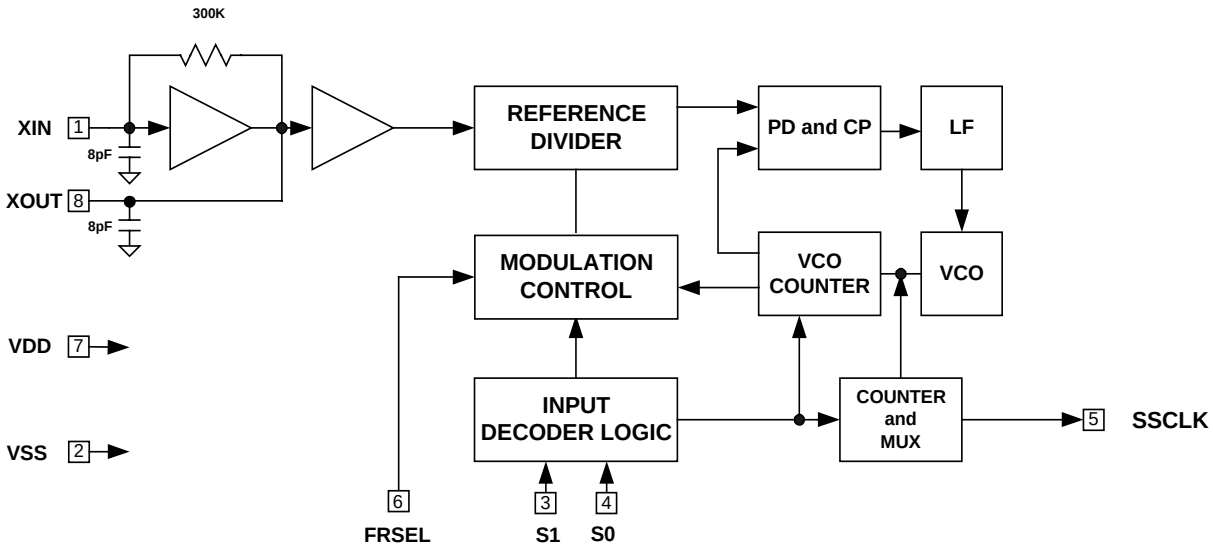


Figure 1. Block Diagram

ORDERING INFORMATION

Part No.	Frequency Multiplication	Package	Operating Temperature Range
CY25811SC	1x	8 Pin SOIC	0 to 70°C
CY25812SC	2x	8 Pin SOIC	0 to 70°C
CY25814SC	4x	8 Pin SOIC	0 to 70°C

Table 1. Ordering Information

PIN CONFIGURATION

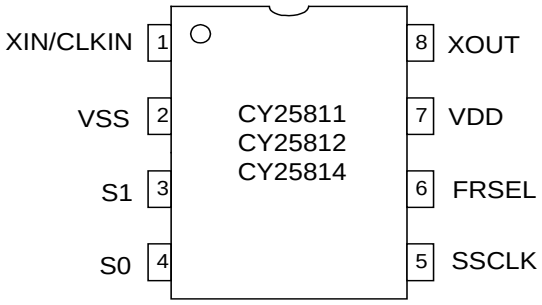


Figure 2. 8 Pin SOIC Package Pin Assignment

PIN DESCRIPTION

Pin	Function	Description
1	**Xin/CLK**	Crystal, Ceramic Resonator or Clock input pin.
2	**VSS**	Power Supply Ground.
3	**S1**	Digital Spread % control pin. 3-Level input (H-M-L). Default=M.
4	**S0**	Digital Spread % control pin. 3-Level input (H-M-L). Default=M.
5	**SSCLK**	Spread Spectrum Output Clock
6	**FRSEL**	Input Frequency Range Selection digital control input. 3-Level input (H-M-L). Default=M.
7	**VDD**	Positive Power Supply.
8	**XOUT**	Crystal or Ceramic Resonator Output pin.

Table 2. Pin Description

ABSOLUTE MAXIMUM RATINGS:

Power Supply Voltage (VDD): +5.5V
Input Voltage Relative to VDD: VDD+0.3V
Input Voltage Relative to VSS: VSS-0.3V

Operating Temperature: 0 to 70°C
Storage Temperature: -65 to +150°C

Note: Operation at any Absolute Maximum Rating is not implied.

DC ELECTRICAL CHARACTERISTICS:

Test Conditions: VDD=3.3V, T=25°, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
VDD	Power Supply Range	2.90	3.3	3.60	V	
VINH	Input High Voltage	0.85VDD	VDD	VDD	V	S0, S1 and FRSEL Inputs
VINM	Input Middle Voltage	0.40VDD	0.50VDD	0.60VDD	V	S0, S1 and FRSEL Inputs
VINL	Input Low Voltage	0.0	0.0	0.15VDD	V	S0, S1 and FRSEL Inputs
VOH1	Output High Voltage	2.4	-	-	V	IOH = 4 ma, SSCLK Output
VOH2	Output High Voltage	2.0	-	-	V	IOH = 6 ma, SSCLK Output
VOL1	Output Low Voltage	-	-	0.4	V	IOL = 4 ma, SSCLK Output
VOL2	Output Low Voltage	-	-	1.2	V	IOL = 10 ma, SSCLK Output
Cin1	Input Capacitance	6.0	7.5	9.0	pF	XIN (Pin 1) and XOUT (Pin 8)
Cin2	Input Capacitance	3.5	4.5	6.0	pF	All Digital Inputs
IDD1	Power Supply Current	-	16.6	19.6	mA	Fin=6MHz, no load
IDD2	Power Supply Current	-	18.6	22.0	mA	Fin=12MHz, no load
IDD3	Power Supply Current	-	23.0	27.2	mA	Fin=24MHz, no load

Table 3

TIMING ELECTRICAL CHARACTERISTICS:

Test Conditions: VDD=3.3V, T=25°C, CL=15pF. Rise/Fall time @ 0.4 and 2.4V, duty cycle at 1.5 V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
ICLKFR	Input Frequency Range	4		32	MHz	Clock, Crystal or Ceramic Resonator Input
trise1	Clock Rise Time	2.4	3.2	4.0	ns	SSCLK, SM811 and SM812
tfall1	Clock Fall Time	2.4	3.2	4.0	ns	SSCLK, SM811 and SM812
trise2	Clock Rise Time	1.2	1.6	2.0	ns	SSCLK, only SM814 when FRSEL=M
tfall2	Clock Fall Time	1.2	1.6	2.0	ns	SSCLK, only SM814 when FRSEL=M
CDCin	Input Clock Duty Cycle	20	50	80	%	XIN
CDCout	Output Clock Duty Cycle	45	50	55	%	SSCLK
CCJ1	Cycle-to-Cycle Jitter	-	540	675	ps	Fin=4MHz, Fout=4MHz, CY25811
CCJ2	Cycle-to-Cycle Jitter	-	195	260	ps	Fin=8MHZ, Fout=8MHz, CY25811
CCJ3	Cycle-to-Cycle Jitter	-	195	260	ps	Fin=8MHz, Fout=16MHz, CY25812
CCJ4	Cycle-to-Cycle Jitter	-	170	225	ps	Fin=16MHz, Fout=32MHz, CY25812
CCJ5	Cycle-to-Cycle Jitter	-	170	225	ps	Fin=16MHz, Fout=64MHz, CY25814
CCJ6	Cycle-to-Cycle Jitter	-	100	150	ps	Fin=32MHz, Fout=128MHz, CY25814

Table 4

INPUT FREQUENCY RANGE AND SELECTION

The CY25811/12/14 input frequency range is 4 to 32 MHz. This range is divided into 3 segments and controlled by 3-Level FRSEL pin as given in Table 5.

FRSEL	INPUT FREQUENCY RANGE
0	4.0 to 8.0 MHz
1	8.0 to 16.0 MHz
M	16.0 to 32.0 MHz

Table 5 – Input Frequency Selection

SPREAD % SELECTION

The CY25811/12/14 SSCG products provide Center-Spread, Down-Spread and No-Spread functions. The amount of Spread % is selected by using 3-Level S0 and S1 digital inputs and Spread % values are given in Table 6.

XIN (MHz)	FRSEL	S1=0 S0=0	S1=0 S0=M	S1=0 S0=1	S1=M S0=0	S1=1 S0=1	S1=1 S0=0	S1=M S0=1	S1=1 S0=M	S1=M S0=M
		CENTER (%)	CENTER (%)	CENTER (%)	CENTER (%)	DOWN (%)	DOWN (%)	DOWN (%)	DOWN (%)	NO SPREAD
4-5	0	+/-1.4	+/-1.2	+/-0.6	+/-0.5	-3.0	-2.2	-1.9	-0.7	0
5-6	0	+/-1.3	+/-1.1	+/-0.5	+/-0.4	-2.7	-1.9	-1.7	-0.6	0
6-7	0	+/-1.2	+/-0.9	+/-0.5	+/-0.4	-2.5	-1.8	-1.5	-0.6	0
7-8	0	+/-1.1	+/-0.9	+/-0.4	+/-0.3	-2.3	-1.7	-1.4	-0.5	0
8-10	1	+/-1.4	+/-1.2	+/-0.6	+/-0.5	-3.0	-2.2	-1.9	-0.7	0
10-12	1	+/-1.3	+/-1.1	+/-0.5	+/-0.4	-2.7	-1.9	-1.7	-0.6	0
12-14	1	+/-1.2	+/-0.9	+/-0.5	+/-0.4	-2.5	-1.8	-1.5	-0.6	0
14-16	1	+/-1.1	+/-0.9	+/-0.4	+/-0.3	-2.3	-1.7	-1.4	-0.5	0
16-20	M	+/-1.4	+/-1.2	+/-0.6	+/-0.5	-3.0	-2.2	-1.9	-0.7	0
20-24	M	+/-1.3	+/-1.1	+/-0.5	+/-0.4	-2.7	-1.9	-1.7	-0.6	0
24-28	M	+/-1.2	+/-0.9	+/-0.5	+/-0.4	-2.5	-1.8	-1.5	-0.6	0
28-32	M	+/-1.1	+/-0.9	+/-0.4	+/-0.3	-2.3	-1.7	-1.4	-0.5	0

Table 6 – Spread % Selection

3-LEVEL DIGITAL INPUTS

S0, S1, and FRSEL digital inputs are designed to sense 3 different logic levels designated as High “1”, Low “0” and Middle “M”. With this 3-Level digital input logic, the 3-Level Logic is able to detect 9 different logic states.

S0, S1 and FRSEL pins include an on chip 20K (10K /10K) resistor divider. No external application resistors are needed to implement the 3-Level logic levels as shown below:

Logic Level “0” : 3-Level logic pin connected to GND.

Logic Level “M” : 3-Level logic pin left floating (no connection.)

Logic Level “1” : 3-Level logic pin connected to VDD.

The Figure 3 illustrates how to implement 3-Level Logic.

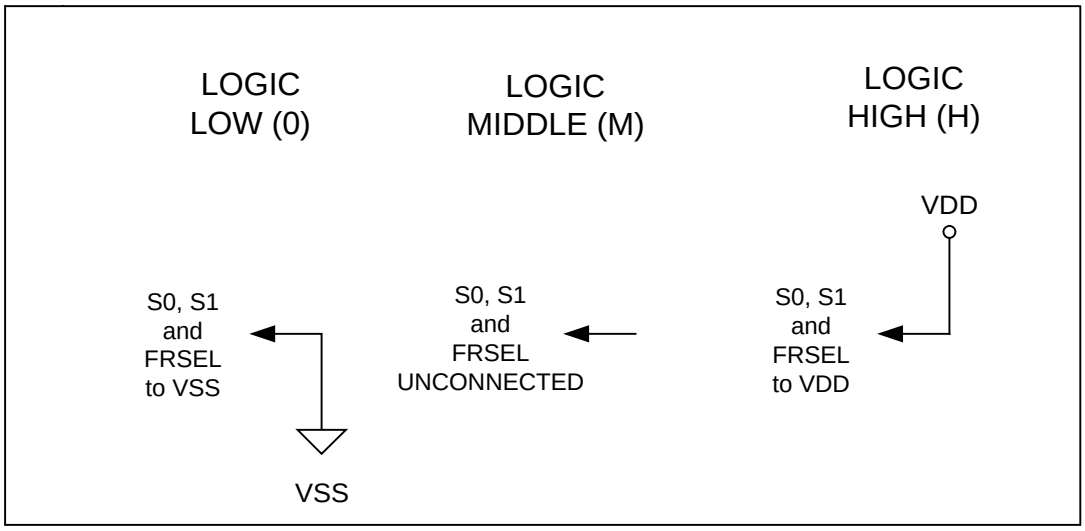


Figure 3. 3-Level Logic

MODULATION RATE

Spread Spectrum Clock Generators utilize frequency modulation (FM) to distribute energy over a specific band of frequencies. The maximum frequency of the clock (fmax) and minimum frequency of the clock (fmin) determine this band of frequencies. The time required to transition from fmin to fmax and back to fmin is the period of the Modulation Rate. The Modulation Rate of SSCG clocks are generally referred to in terms of frequency, or fmod = 1/Tmod.
The input clock frequency, fin, and the internal divider determine the Modulation Rate.

In the case of CY25811/2/4 devices, the (Spread Spectrum) Modulation Rate, fmod, is given by the following formula:

$$fmod = fin/DR$$

Where; fmod is the Modulation Rate, fin is the Input Frequency and DR is the Divider Ratio as given in Table 7. Notice that Input Frequency Range is set by FRSEL.

FRSEL	INPUT FREQUENCY RANGE (MHz)	DIVIDER RATIO (DR)
0	4 to 8	128
1	8 to 16	256
M	16 to 32	512

Table 7. Modulation Rate Divider Ratios

INPUT AND OUTPUT FREQUENCY SELECTION

The relationship between input frequency versus output frequency in terms of device selection and FRSEL setting is given in Table 8. As shown, the input frequency range is selected by FRSEL and is the same for CY25811, CY25812 and CY25814. The selection of CY25811 (1x), CY25812 (2x) or CY25814 (4x) determines the frequency multiplication at the output (SSCLK, Pin 5) with respect to input frequency (XIN, Pin-1).

INPUT FREQUENCY RANGE (MHz)	FRSEL	PRODUCT	MULTIPLICATION	OUTPUT FREQUENCY RANGE (MHz)
4 to 8	0	**SM811**	1x	4 to 8
8 to 16	1	**SM811**	1x	8 to 16
16 to 32	M	**SM811**	1x	16 to 32
4 to 8	0	**SM812**	2x	8 to 16
8 to 16	1	**SM812**	2x	16 to 32
16 to 32	M	**SM812**	2x	32 to 64
4 to 8	0	**SM814**	4x	16 to 32
8 to 16	1	**SM814**	4x	32 to 64
16 to 32	M	**SM814**	4x	64 to 128

Table 8. Input and Output Frequency Selection

CHARACTERISTIC CURVES

The following curves demonstrate the characteristic behavior of the CY25811/12/14 when tested over a number of environmental and application specific parameters. These are typical performance curves and are not meant to replace any parameter specified in tables 3 and 4.

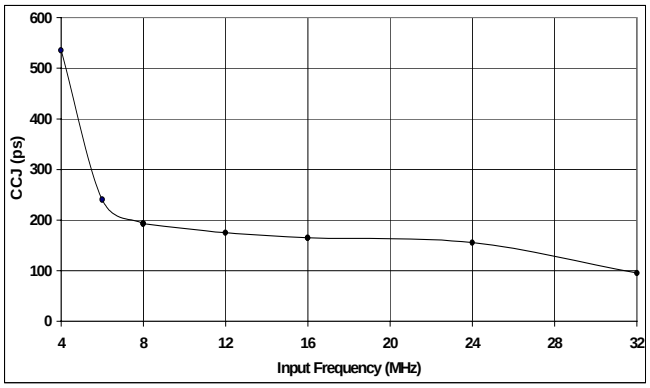


Figure 4A. Jitter vs. Input Frequency (No Load)

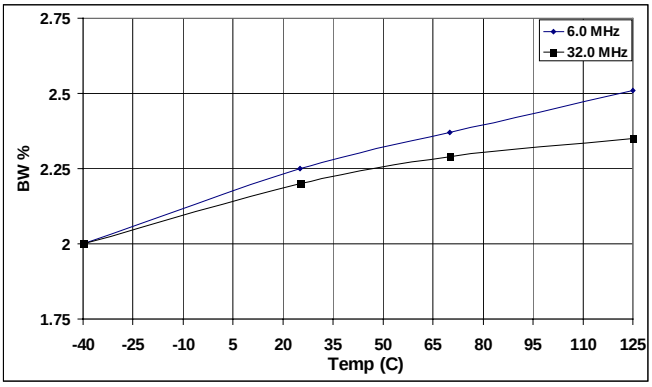


Figure 4B. Bandwidth % vs. Temperature

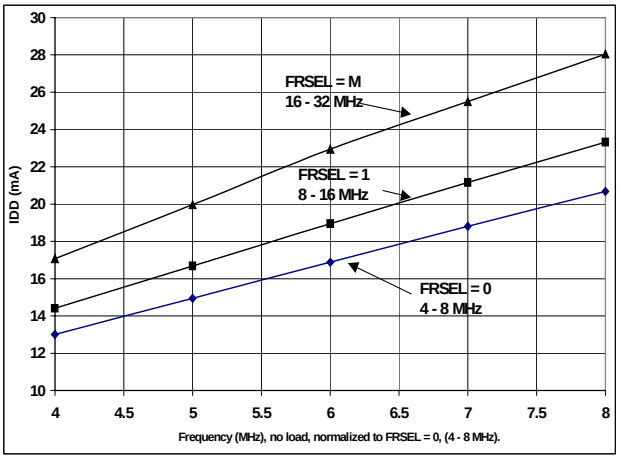


Figure 4C. IDD vs. Frequency (FRSEL = 0, 1, M)

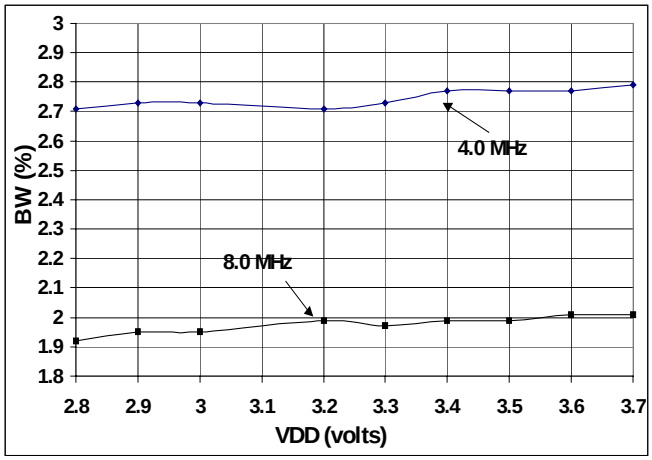
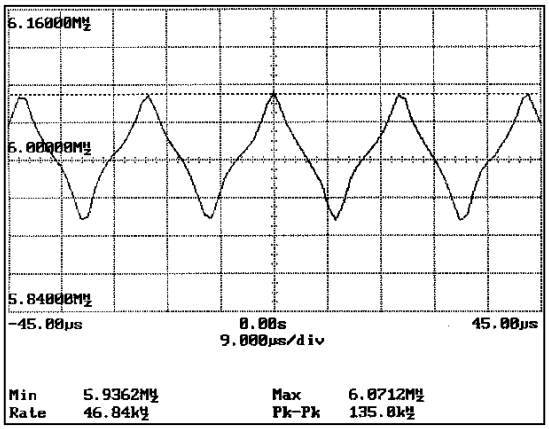


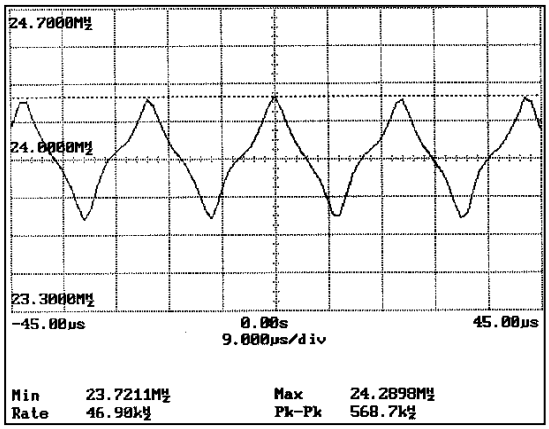
Figure 4D. Bandwidth % vs. VDD

SSCG PROFILES

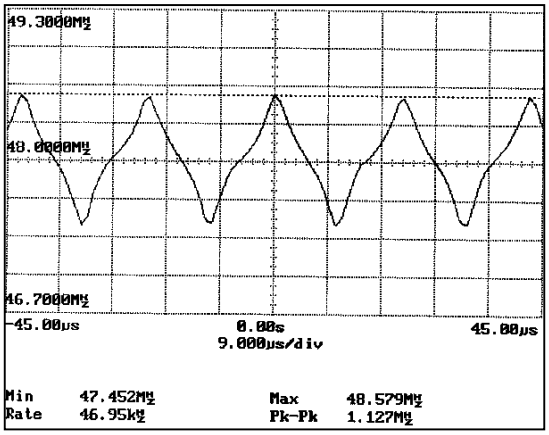
CY25811/12/14 SSCG products use a non-linear “optimized” frequency profile as shown In Figure 5. The use of Cypress proprietary “optimized” frequency profile maintains flat energy distribution over the fundamental and higher order harmonics. This results in additional EMI reduction in electronic systems.



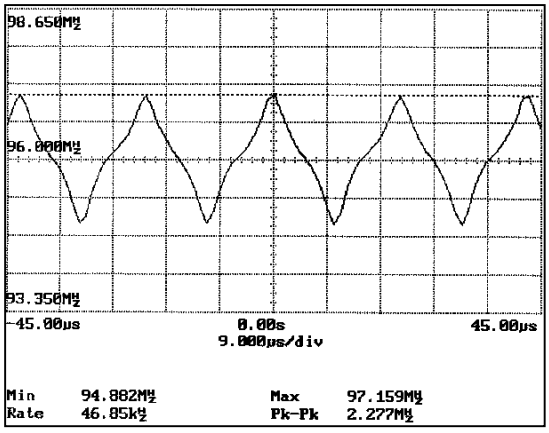
Xin = 6.0 MHz	SSCLK1 = 6.0 MHz
S1, S0 = 0	
FRSEL = 0	P/N = CY25811SC



Xin = 24.0 MHz	SSCLK1 = 24.0 MHz
S1, S0 = 0	
FRSEL = M	P/N = CY25811SC



Xin = 12.0 MHz	SSCLK1 = 48.0 MHz
S1, S0 = 0	
FRSEL = 1	P/N = CY25814SC



Xin = 24.0 MHz	SSCLK1 = 96.0 MHz
S1, S0 = 0	
FRSEL = M	P/N = CY25814SC

Figure 5. Spread Spectrum Profiles (Frequency versus Time)

APPLICATION SCHEMATIC

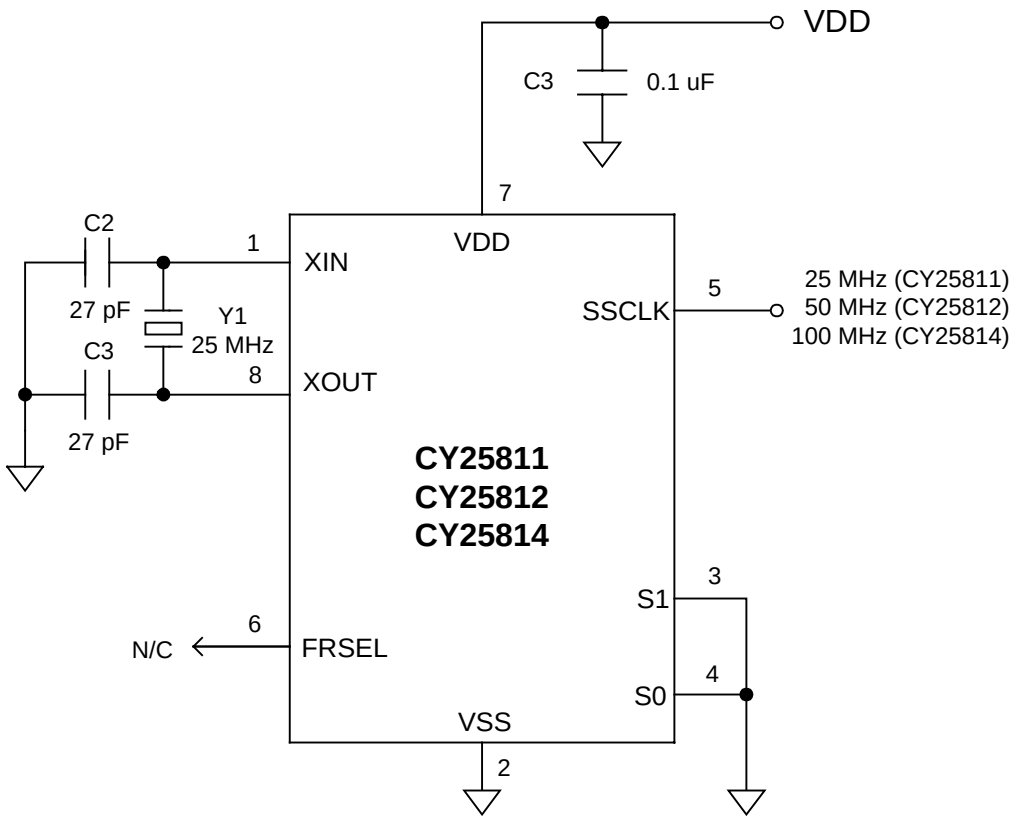


Figure 6. Typical Application Schematic

8 PIN SOIC PACKAGE DRAWING AND OUTLINE

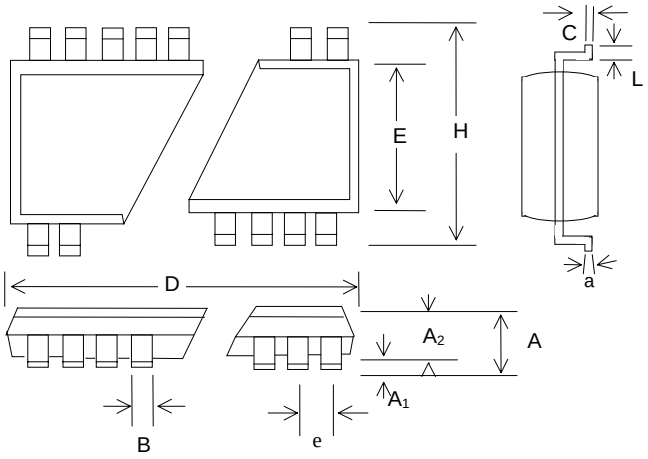


Figure 7. Package Drawing

8 Pin SOIC Outline Dimensions (150 mil)

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	0.053	-	0.069	1.35	-	1.75
A_1	0.004	-	0.010	0.10	-	0.25
A2	0.047	-	0.059	1.20	-	1.50
B	0.013	-	0.020	0.33	-	0.51
C	0.007	-	0.010	0.19	-	0.25
D	0.189	-	0.197	4.80	-	5.00
E	0.150	-	0.157	3.80	-	4.00
e	0.050 BSC			1.27 BSC		
H	0.228	-	0.244	5.80	-	6.20
L	0.016	-	0.050	0.40	-	1.27
a	0º	-	8º	0º	-	8º

Table 9. Package Outline

Notice

Cypress Semiconductor Corporation reserves the right to make changes to its products in order to improve design, performance or reliability. Cypress Semiconductor Corporation assumes no responsibility for the use of its products in life supporting and medical applications where the failure or malfunction of the product could cause failure of the life supporting and medical systems. Products are not authorized for use in such applications unless a written approval is requested by the manufacturer and an approval is given in writing by Cypress Semiconductor Corporation for the use of its products in the life supporting and medical applications.

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Document Title: CY25811, CY25812, CY25814 Spread Spectrum Clock Generator **Document Number:** 38-07112				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	107516	06/14/01	NDP	Convert from IMI to Cypress
*A	108002	06/29/01	NDP	Delete “Junction Temp.” in Absolute Maximum Ratings.