# Switched-Capacitor Voltage Converter with Regulator

## FEATURES

- **Available in Space Saving SO-8 Package**
- **Output Current: 100mA (LT1054)**
  **125mA (LT1054L)**
- Low Loss: 1.1V at 100mA
- Operating Range: 3.5V to 15V (LT1054)
  3.5V to 7V (LT1054L)
- **Reference and Error Amplifier for Regulation**
- External Shutdown
- External Oscillator Synchronization
- Can Be Paralleled
- Pin Compatible with the LTC®1044/LTC7660

## APPLICATIONS

- Voltage Inverter
- Voltage Regulator
- Negative Voltage Doubler
- Positive Voltage Doubler



## DESCRIPTION

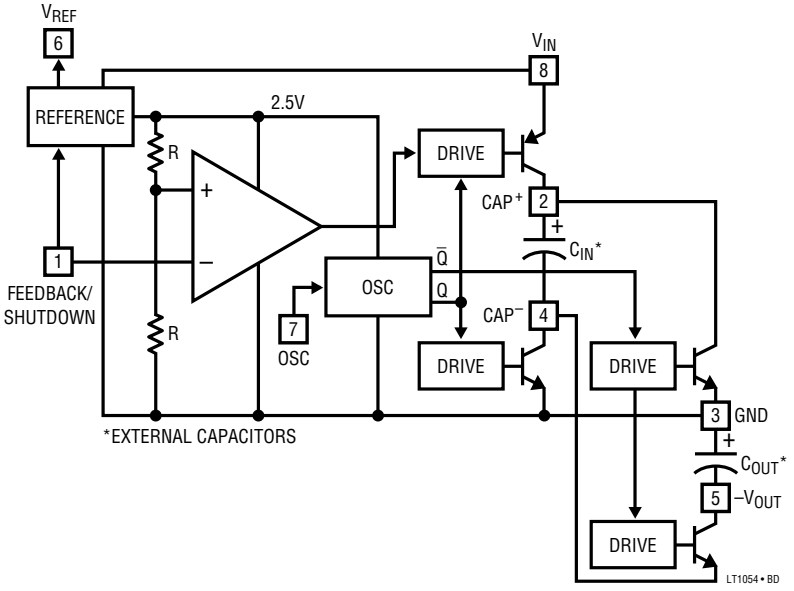
The LT®1054 is a monolithic, bipolar, switched-capacitor voltage converter and regulator. The LT1054 provides higher output current than previously available converters with significantly lower voltage losses. An adaptive switch driver scheme optimizes efficiency over a wide range of output currents. Total voltage loss at 100mA output current is typically 1.1V. This holds true over the full supply voltage range of 3.5V to 15V. Quiescent current is typically 2.5mA.

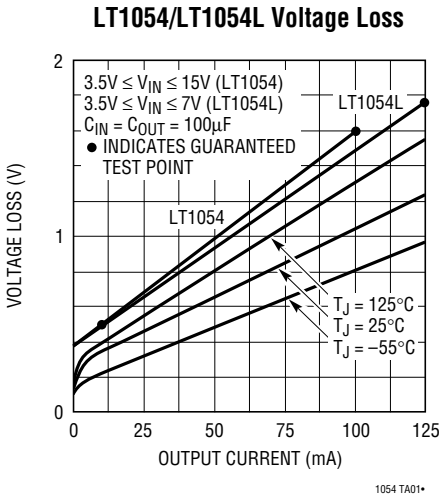
The LT1054 also provides regulation, a feature not previously available in switched-capacitor voltage converters. By adding an external resistive divider a regulated output can be obtained. This output will be regulated against changes in both input voltage and output current. The LT1054 can also be shut down by grounding the feedback pin. Supply current in shutdown is less than 100µA.

The internal oscillator of the LT1054 runs at a nominal frequency of 25kHz. The oscillator pin can be used to adjust the switching frequency or to externally synchronize the LT1054.

The LT1054 is pin compatible with previous converters such the LTC1044/LTC7660.

## BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (Note 2)
- LT1054 ..... 16V
- LT1054L ..... 7V

Input Voltage
- Pin 1 ..... $0V \le V_{PIN1} \le V^+$
- Pin 3 (S Package) ..... $0V \le V_{PIN3} \le V^+$
- Pin 7 ..... $0V \le V_{PIN7} \le V_{REF}$
- Pin 13 (S Package) ..... $0V \le V_{PIN13} \le V_{REF}$

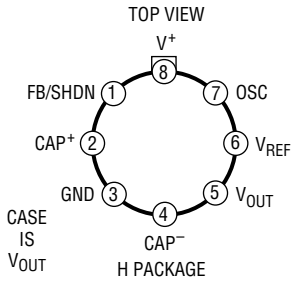
Operating Junction Temperature Range
- LT1054C/LT1054LC ..... 0°C to 100°C
- LT1054I ..... –40°C to 100°C
- LT1054M ..... –55°C to 125°C

Maximum Junction Temperature (Note 3)
- LT1054C/LT1054LC ..... 125°C
- LT1054I ..... 125°C
- LT1054M ..... 150°C

Storage Temperature Range
- H, J8, N8 and S8 Packages ..... –55°C to 150°C
- S Package ..... –65°C to 150°C

Lead Temperature (Soldering, 10 sec) ..... 300°C

## PACKAGE/ORDER INFORMATION (Note 6)

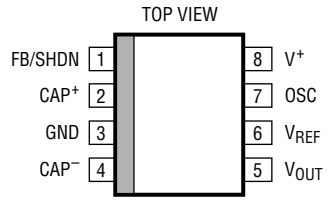



H PACKAGE
8-LEAD TO-5 METAL CAN

$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 150°C, $\theta_{JC}$ = 45°C/W

ORDER PART NUMBER

LT1054CH
LT1054MH




S8 PACKAGE
8-LEAD PLASTIC SO

$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 120°C/W

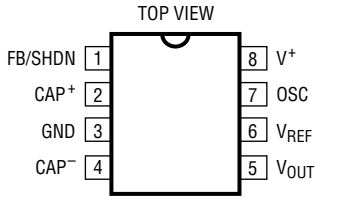
SEE REGULATION AND CAPACITOR SELECTION SECTIONS IN THE APPLICATIONS INFORMATION FOR IMPORTANT INFORMATION ON THE S8 DEVICE

ORDER PART NUMBER

LT1054CS8
LT1054LCS8

S8 PART MARKING

1054
1054L



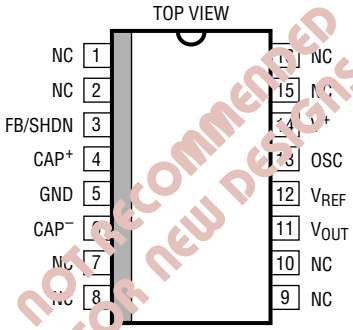

J8 PACKAGE
8-LEAD CERAMIC DIP

N8 PACKAGE
8-LEAD PLASTIC DIP

$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 100°C/W (J8)
$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 130°C/W (N8)

ORDER PART NUMBER

LT1054CJ8
LT1054CN8
LT1054IN8
LT1054MJ8






SW PACKAGE
16-LEAD PLASTIC SO

$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 150°C/W

ORDER PART NUMBER

LT1054CSW
LT1054ISW

## ELECTRICAL CHARACTERISTICS (Note 7)

| PARAMETER | CONDITIONS | | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Supply Current | $I_{LOAD}$ = 0mA | LT1054: $V_{IN}$ = 3.5V | ● | | 2.5 | 4.0 | mA |
| | | $V_{IN}$ = 15V | ● | | 3.0 | 5.0 | mA |
| | | LT1054L: $V_{IN}$ = 3.5V | ● | | 2.5 | 4.0 | mA |
| | | $V_{IN}$ = 7V | ● | | 3.0 | 5.0 | mA |
| Supply Voltage Range | LT1054 | | ● | 3.5 | | 15 | V |
| | LT1054L | | ● | 3.5 | | 7 | V |
| Voltage Loss ($V_{IN}$ – $\lvert V_{OUT} \rvert$) | $C_{IN}$ = $C_{OUT}$ = 100µF Tantalum (Note 4) | | | | | | |
| | $I_{OUT}$ = 10mA | | ● | | 0.35 | 0.55 | V |
| | $I_{OUT}$ = 100mA | | ● | | 1.10 | 1.60 | V |
| | $I_{OUT}$ = 125mA (LT1054L) | | ● | | 1.35 | 1.75 | V |
| Output Resistance | $\Delta I_{OUT}$ = 10mA to 100mA (Note 5) | | ● | | 10 | 15 | Ω |
| Oscillator Frequency | LT1054: 3.5V ≤ $V_{IN}$ ≤ 15V | | ● | 15 | 25 | 35 | kHz |
| | LT1054L: 3.5V ≤ $V_{IN}$ ≤ 7V | | ● | 15 | 25 | 35 | kHz |
| Reference Voltage | $I_{REF}$ = 60µA, $T_J$ = 25°C | | | 2.35 | 2.50 | 2.65 | V |
| | | | ● | 2.25 | | 2.75 | V |
| Regulated Voltage | $V_{IN}$ = 7V, $T_J$ = 25°C, $R_L$ = 500Ω (Note 6) | | | –4.70 | –5.00 | –5.20 | V |
| Line Regulation | LT1054: 7V ≤ $V_{IN}$ ≤ 12V, $R_L$ = 500Ω (Note 6) | | ● | | 5 | 25 | mV |
| Load Regulation | $V_{IN}$ = 7V, 100Ω ≤ $R_L$ ≤ 500Ω (Note 6) | | ● | | 10 | 50 | mV |
| Maximum Switch Current | | | | | 300 | | mA |
| Supply Current in Shutdown | $V_{PIN1}$ = 0V | | ● | | 100 | 200 | µA |

The ● denotes specifications which apply over the full operating temperature range.

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:** The absolute maximum supply voltage rating of 16V is for unregulated circuits using LT1054. For regulation mode circuits using LT1054 with $V_{OUT}$ ≤ 15V at Pin 5 (Pin 11 on S package), this rating may be increased to 20V. The absolute maximum supply voltage for LT1054L is 7V.

**Note 3:** The devices are guaranteed by design to be functional up to the absolute maximum junction temperature.

**Note 4:** For voltage loss tests, the device is connected as a voltage inverter, with pins 1, 6, and 7 (3, 12, and 13 S package) unconnected. The voltage losses may be higher in other configurations.

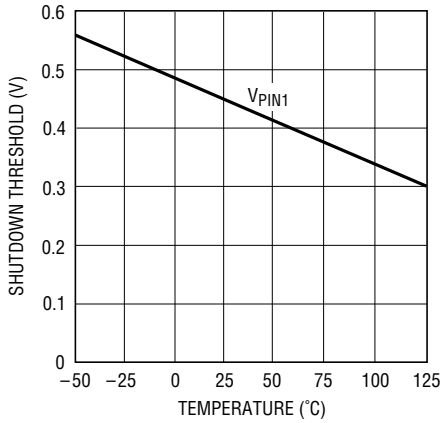
**Note 5:** Output resistance is defined as the slope of the curve, ($\Delta V_{OUT}$ vs $\Delta I_{OUT}$), for output currents of 10mA to 100mA. This represents the linear portion of the curve. The incremental slope of the curve will be higher at currents <10mA due to the characteristics of the switch transistors.

**Note 6:** All regulation specifications are for a device connected as a positive-to-negative converter/regulator with R1 = 20k, R2 = 102.5k, C1 = 0.002µF, (C1 = 0.05µF S package) $C_{IN}$ = 10µF tantalum, $C_{OUT}$ = 100µF tantalum.

**Note 7:** The S8 package uses a different die than the H, J8, N8 and S packages. The S8 device will meet all the existing data sheet parameters. See Regulation and Capacitor Selection in the Applications Information section for differences in application requirements.

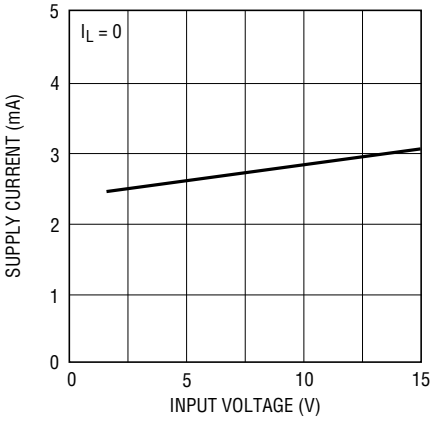
# TYPICAL PERFORMANCE CHARACTERISTICS

### Shutdown Threshold



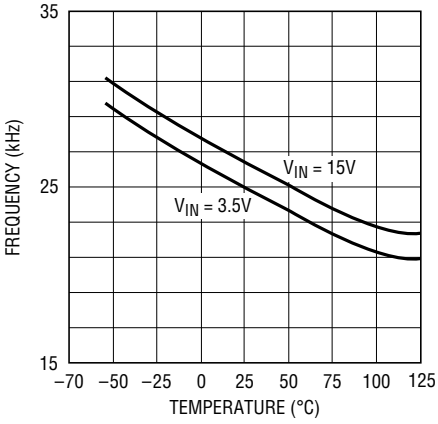

LT1054 • TPC01

### Supply Current



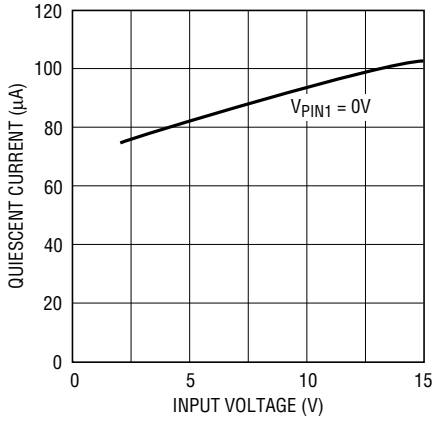

LT1054 • TPC02

### Oscillator Frequency



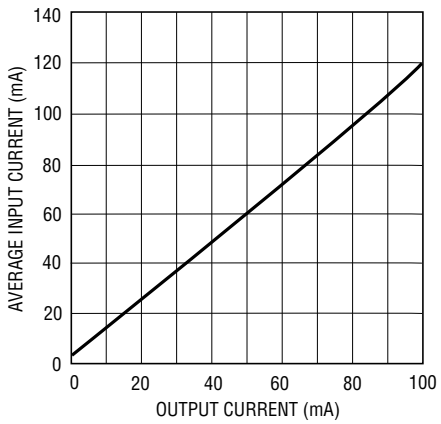

LT1054 • TPC03

### Supply Current in Shutdown



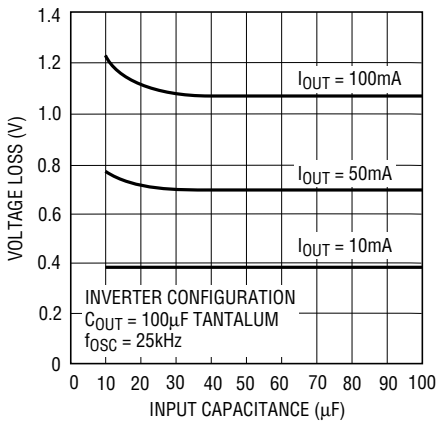

LT1054 • TPC04

### Average Input Current



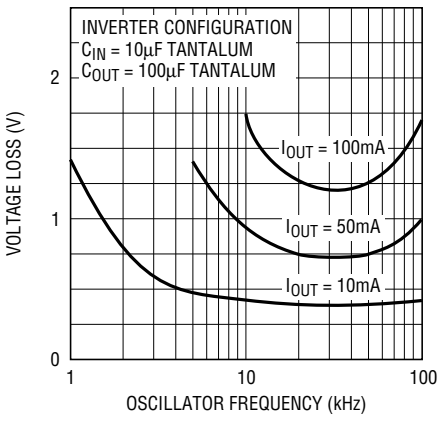

LT1050 • TPC05

### Output Voltage Loss



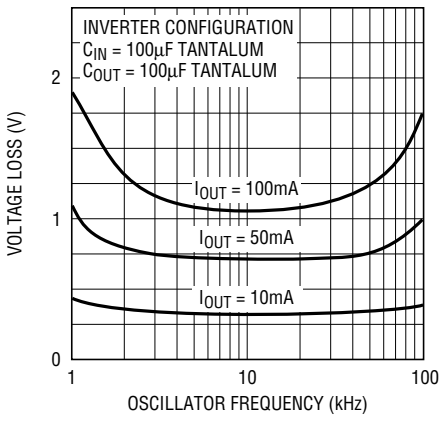

LT1054 • TPC06

### Output Voltage Loss




LT1054 • TPC07

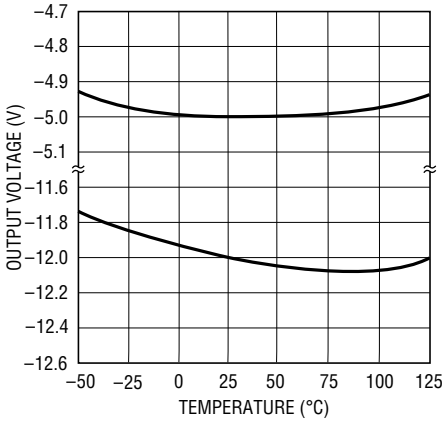
### Output Voltage Loss




LT1054 • TPC08

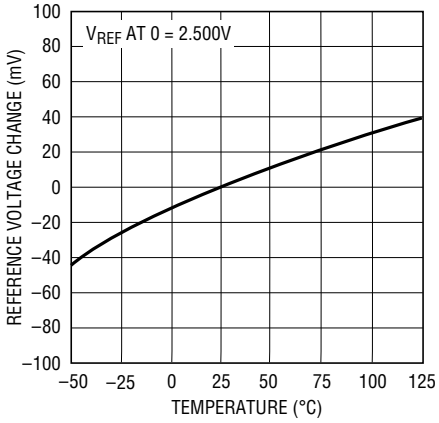
## TYPICAL PERFORMANCE CHARACTERISTICS

**Regulated Output Voltage**




LT1054 • TPC09

**Reference Voltage Temperature Coefficient**




LT1054 • TPC10

## PIN FUNCTIONS

**FB/SHDN (Pin 1):** Feedback/Shutdown Pin. This pin has two functions. Pulling Pin 1 below the shutdown threshold (≈0.45V) puts the device into shutdown. In shutdown the reference/regulator is turned off and switching stops. The switches are set such that both $C_{IN}$ and $C_{OUT}$ are discharged through the output load. Quiescent current in shutdown drops to approximately 100µA (see Typical Performance Characteristics). Any open-collector gate can be used to put the LT1054 into shutdown. For normal (unregulated) operation the device will start back up when the external gate is shut off. In LT1054 circuits that use the regulation feature, the external resistor divider can provide enough pull-down to keep the device in shutdown until the output capacitor ($C_{OUT}$) has fully discharged. For most applications where the LT1054 would be run intermittently, this does not present a problem because the discharge time of the output capacitor will be short compared to the off-time of the device. In applications where the device has to start up before the output capacitor ($C_{OUT}$) has fully discharged, a restart pulse must be applied to Pin 1 of the LT1054. Using the circuit of Figure 5, the restart signal can be either a pulse ($t_p$ > 100µs) or a logic high. Diode coupling the restart signal into Pin 1 will allow the output voltage to come up and regulate without overshoot. The resistor divider R3/R4 in Figure 5 should be chosen to provide a signal level at pin 1 of 0.7V to 1.1V.

Pin 1 is also the inverting input of the LT1054's error amplifier and as such can be used to obtain a regulated output voltage.

**CAP⁺/CAP⁻ (Pin 2/Pin 4):** Pin 2, the positive side of the input capacitor ($C_{IN}$), is alternately driven between $V^+$ and ground. When driven to $V^+$, Pin 2 sources current from $V^+$. When driven to ground Pin 2 sinks current to ground. Pin 4, the negative side of the input capacitor, is driven alternately between ground the $V_{OUT}$. When driven to ground, Pin 4 sinks current to ground. When driven to $V_{OUT}$ Pin 4 sources current from $C_{OUT}$. In all cases current flow in the switches is unidirectional as should be expected using bipolar switches.

**$V_{OUT}$ (Pin 5):** In addition to being the output pin this pin is also tied to the substrate of the device. **Special care must be taken in LT1054 circuits to avoid pulling this pin positive with respect to any of the other pins**. Pulling Pin 5 positive with respect to Pin 3 (GND) will forward bias the substrate diode which will prevent the device from starting. This condition can occur when the output load driven by the LT1054 is referred to its positive supply (or to some other positive voltage). Note that most op amps present just such a load since their supply currents flow from their $V^+$ terminals to their $V^-$ terminals. To prevent start-up problems with this type of load an external transistor must be added as shown in Figure 1. This will prevent $V_{OUT}$ (Pin 5)

## PIN FUNCTIONS

from being pulled above the ground pin (Pin 3) during start-up. Any small, general purpose transistor such as 2N2222 or 2N2219 can be used. $R_X$ should be chosen to provide enough base drive to the external transistor so that it is saturated under nominal output voltage and maximum output current conditions. In some cases an N-channel enhancement mode MOSFET can be used in place of the transistor.

$$R_X \leq \frac{(|V_{OUT}|)\beta}{I_{OUT}}$$

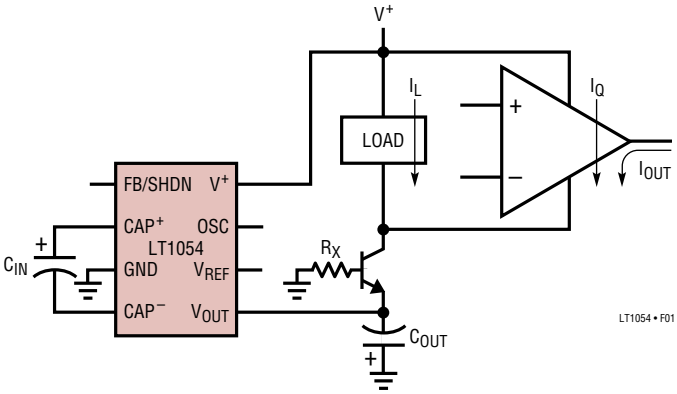



**Figure 1**

**$V_{REF}$ (Pin 6):** Reference Output. This pin provides a 2.5V reference point for use in LT1054-based regulator circuits. The temperature coefficient of the reference voltage has been adjusted so that the temperature coefficient of the regulated output voltage is close to zero. This requires the reference output to have a positive temperature coefficient as can be seen in the typical performance curves. This nonzero drift is necessary to offset a drift term inherent in the internal reference divider and comparator network tied to the feedback pin. The overall result of these drift terms is a regulated output which has a slight positive temperature coefficient at output voltages below 5V and a slight negative TC at output voltages above 5V. Reference output current should be limited, for regulator feedback networks, to approximately 60µA. The reference pin will draw ≈100µA when shorted to ground and will not affect the internal reference/regulator, so that this pin can also be used as a pull-up for LT1054 circuits that require synchronization.

**OSC (Pin 7):** Oscillator Pin. This pin can be used to raise or lower the oscillator frequency or to synchronize the device to an external clock. Internally Pin 7 is connected to the oscillator timing capacitor ($C_t \approx 150pF$) which is alternately charged and discharged by current sources of ±7µA so that the duty cycle is ≈50%. The LT1054 oscillator is designed to run in the frequency band where switching losses are minimized. However the frequency can be raised, lowered, or synchronized to an external system clock if necessary.

The frequency can be lowered by adding an external capacitor (C1, Figure 2) from Pin 7 to ground. This will increase the charge and discharge times which lowers the oscillator frequency. The frequency can be increased by adding an external capacitor (C2, Figure 2, in the range of 5pF to 20pF) from Pin 2 to Pin 7. This capacitor will couple charge into $C_T$ at the switch transitions, which will shorten the charge and discharge time, raising the oscillator frequency. Synchronization can be accomplished by adding an external resistive pull-up from Pin 7 to the reference pin (Pin 6). A 20k pull-up is recommended. An open collector gate or an NPN transistor can then be used to drive the oscillator pin at the external clock frequency as shown in Figure 2. Pulling up Pin 7 to an external voltage is **not recommended**. For circuits that require both frequency synchronization and regulation, an external reference can be used as the reference point for the top of the R1/R2 divider allowing Pin 6 to be used as a pull-up point for Pin 7.

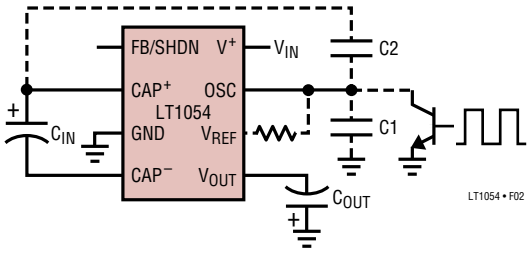



**Figure 2**

**$V^+$ (Pin 8):** Input Supply. The LT1054 alternately charges $C_{IN}$ to the input voltage when $C_{IN}$ is switched in parallel with the input supply and then transfers charge to $C_{OUT}$ when $C_{IN}$ is switched in parallel with $C_{OUT}$. Switching occurs at

## PIN FUNCTIONS

the oscillator frequency. During the time that $C_{IN}$ is charging, the peak supply current will be approximately equal to 2.2 times the output current. During the time that $C_{IN}$ is delivering charge to $C_{OUT}$ the supply current drops to approximately 0.2 times the output current. An input supply bypass capacitor will supply part of the peak input current drawn by the LT1054 and average out the current drawn from the supply. A minimum input supply bypass capacitor of 2µF, preferably tantalum or some other low ESR type is recommended. A larger capacitor may be desirable in some cases, for example, when the actual input supply is connected to the LT1054 through long leads, or when the pulse current drawn by the LT1054 might affect other circuitry through supply coupling.

## APPLICATIONS INFORMATION

### Theory of Operation

To understand the theory of operation of the LT1054, a review of a basic switched-capacitor building block is helpful.

In Figure 3 when the switch is in the left position, capacitor C1 will charge to voltage V1. The total charge on C1 will be q1 = C1V1. The switch then moves to the right, discharging C1 to voltage V2. After this discharge time the charge on C1 is q2 = C1V2. Note that charge has been transferred from the source V1 to the output V2. The amount of charge transferred is:

$$\Delta q = q1 - q2 = C1(V1 - V2)$$

If the switch is cycled f times per second, the charge transfer per unit time (i.e., current) is:

$$I = (f)(\Delta q) = (f)[C1(V1 - V2)]$$

To obtain an equivalent resistance for the switched-capacitor network we can rewrite this equation in terms of voltage and impedance equivalence:

$$I = \frac{V1 - V2}{(1/fC1)} = \frac{V1 - V2}{R_{EQUIV}}$$

A new variable $R_{EQUIV}$ is defined such that $R_{EQUIV} = 1/fC1$. Thus the equivalent circuit for the switched-capacitor network is as shown in Figure 4. The LT1054 has the same switching action as the basic switched-capacitor building block. Even though this simplification doesn't include finite switch on-resistance and output voltage ripple, it provides an intuitive feel for how the device works.

These simplified circuits explain voltage loss as a function of frequency (see Typical Performance Characteristics). As frequency is decreased, the output impedance will eventu-

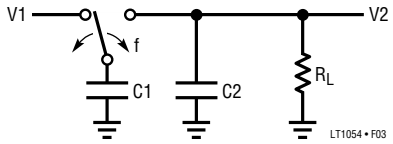



**Figure 3. Switched-Capacitor Building Block**

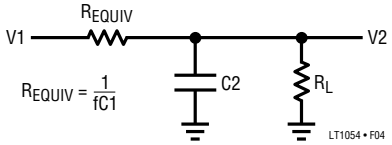



**Figure 4. Switched-Capacitor Equivalent Circuit**

ally be dominated by the 1/fC1 term and voltage losses will rise.

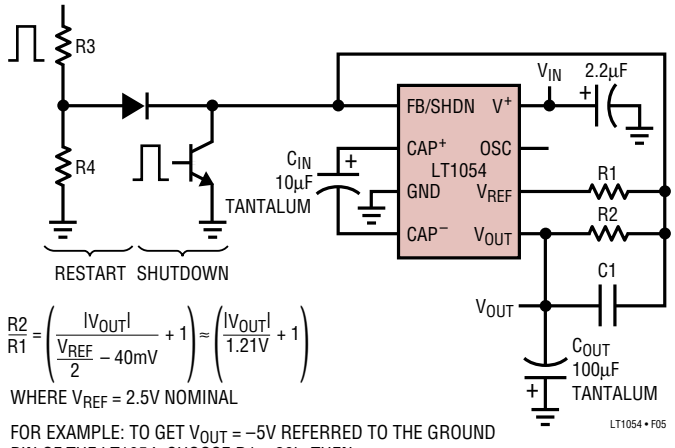
Note that losses also rise as frequency increases. This is caused by internal switching losses which occur due to some finite charge being lost on each switching cycle. This charge loss per-unit-cycle, when multiplied by the switching frequency, becomes a current loss. At high frequency this loss becomes significant and voltage losses again rise.

The oscillator of the LT1054 is designed to run in the frequency band where voltage losses are at a minimum.

### Regulation

The error amplifier of the LT1054 servos the drive to the PNP switch to control the voltage across the input capacitor ($C_{IN}$) which in turn will determine the output voltage. Using the reference and error amplifier of the LT1054, an external resistive divider is all that is needed to set the regulated output voltage. Figure 5 shows the basic regulator configuration and the formula for calculating the appropriate resistor values. R1 should be chosen to be

## APPLICATIONS INFORMATION




$$\frac{R2}{R1} = \left(\frac{|V_{OUT}|}{\frac{V_{REF}}{2} - 40mV} + 1\right) \approx \left(\frac{|V_{OUT}|}{1.21V} + 1\right)$$

WHERE $V_{REF}$ = 2.5V NOMINAL

FOR EXAMPLE: TO GET $V_{OUT}$ = –5V REFERRED TO THE GROUND PIN OF THE LT1054, CHOOSE R1 = 20k, THEN

$$R2 = 20k\left(\frac{|-5V|}{\frac{2.5V}{2} - 40mV} + 1\right) = 102.6k^*$$

*CHOOSE THE CLOSEST 1% VALUE

**Figure 5**

20k or greater because the reference output current is limited to ≈ 100µA. R2 should be chosen to be in the range of 100k to 300k. For optimum results the ratio of $C_{IN}/C_{OUT}$ is recommended to be 1/10. C1, required for good load regulation at light load currents, should be 0.002µF for all output voltages.

A new die layout was required to fit into the physical dimensions of the S8 package. Although the new die of the LT1054CS8 will meet all the specifications of the existing LT1054 data sheet, subtle differences in the layout of the new die require consideration in some application circuits. In regulating mode circuits using the 1054CS8 the nominal values of the capacitors, $C_{IN}$ and $C_{OUT}$, must be approximately equal for proper operation at elevated junction temperatures. This is different from the earlier part. Mismatches within normal production tolerances for the capacitors are acceptable. Making the nominal capacitor values equal will ensure proper operation at elevated junction temperatures at the cost of a small degradation in the transient response of regulator circuits. For unregulated circuits the values of $C_{IN}$ and $C_{OUT}$ are normally equal for all packages. For S8 applications assistance in unusual applications circuits, please consult the factory.

It can be seen from the circuit block diagram that the maximum regulated output voltage is limited by the supply voltage. For the basic configuration, $|V_{OUT}|$ referred to the ground pin of the LT1054 must be less than the total of the supply voltage minus the voltage loss due to the switches. The voltage loss versus output current due to the switches can be found in Typical Performance Characteristics. Other configurations such as the negative doubler can provide higher output voltages at reduced output currents (see Typical Applications).

### Capacitor Selection

For unregulated circuits the nominal values of $C_{IN}$ and $C_{OUT}$ should be equal. For regulated circuits see the section on Regulation. While the exact values of $C_{IN}$ and $C_{OUT}$ are noncritical, good quality, low ESR capacitors such as solid tantalum are necessary to minimize voltage losses at high currents. For $C_{IN}$ the effect of the ESR of the capacitor will be multiplied by four due to the fact that switch currents are approximately two times higher than output current and losses will occur on both the charge and discharge cycle. This means that using a capacitor with 1Ω of ESR for $C_{IN}$ will have the same effect as increasing the output impedance of the LT1054 by 4Ω. This represents a significant increase in the voltage losses. For $C_{OUT}$ the affect of ESR is less dramatic. $C_{OUT}$ is alternately charged and discharged at a current approximately equal to the output current and the ESR of the capacitor will cause a step function to occur in the output ripple at the switch transitions. This step function will degrade the output regulation for changes in output load current and should be avoided. Realizing that large value tantalum capacitors can be expensive, a technique that can be used is to parallel a smaller tantalum capacitor with a large aluminum electrolytic capacitor to gain both low ESR and reasonable cost. Where physical size is a concern some of the newer chip type surface mount tantalum capacitors can be used. These capacitors are normally rated at working voltages in the 10V to 20V range and exhibit very low ESR (in the range of 0.1Ω).

### Output Ripple

The peak-to-peak output ripple is determined by the value of the output capacitor and the output current. Peak-to-peak output ripple may be approximated by the formula:

$$dV = \frac{I_{OUT}}{2fC_{OUT}}$$

## APPLICATIONS INFORMATION

where dV = peak-to-peak ripple and f = oscillator frequency.

For output capacitors with significant ESR a second term must be added to account for the voltage step at the switch transitions. This step is approximately equal to:

$(2I_{OUT})(\text{ESR of } C_{OUT})$

### Power Dissipation

The power dissipation of any LT1054 circuit must be limited such that the junction temperature of the device does not exceed the maximum junction temperature ratings. The total power dissipation must be calculated from two components, the power loss due to voltage drops in the switches and the power loss due to drive current losses. The total power dissipated by the LT1054 can be calculated from:

$$P \approx (V_{IN} - |V_{OUT}|)(I_{OUT}) + (V_{IN})(I_{OUT})(0.2)$$

where both $V_{IN}$ and $V_{OUT}$ are referred to the ground pin (Pin 3) of the LT1054. For LT1054 regulator circuits, the power dissipation will be equivalent to that of a linear regulator. Due to the limited power handling capability of the LT1054 packages, the user will have to limit output current requirements or take steps to dissipate some power external to the LT1054 for large input/output differentials. This can be accomplished by placing a resistor in series with $C_{IN}$ as shown in Figure 6. A portion of the input voltage will then be dropped across this resistor without affecting the output regulation. Because switch current is approximately 2.2 times the output current and the resistor will cause a voltage drop when $C_{IN}$ is both charging and discharging, the resistor should be chosen as:

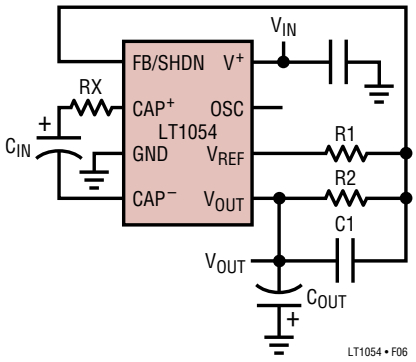



**Figure 6**

$$R_X = V_X/(4.4\ I_{OUT})$$

where

$$V_X \approx V_{IN} - [(\text{LT1054 Voltage Loss})(1.3) + |V_{OUT}|]$$

and $I_{OUT}$ = maximum required output current. The factor of 1.3 will allow some operating margin for the LT1054.

For example: assume a 12V to –5V converter at 100mA output current. First calculate the power dissipation without an external resistor:

$P = (12V - |-5V|)(100mA) + (12V)(100mA)(0.2)$
$P = 700mW + 240mW = 940mW$

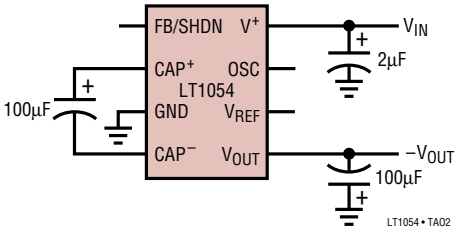
At $\theta_{JA}$ of 130°C/W for a commercial plastic device this would cause a junction temperature rise of 122°C so that the device would exceed the maximum junction temperature at an ambient temperature of 25°C. Now calculate the power dissipation with an external resistor ($R_X$). First find how much voltage can be dropped across $R_X$. The maximum voltage loss of the LT1054 in the standard regulator configuration at 100mA output current is 1.6V, so

$V_X = 12V - [(1.6V)(1.3) + |-5V|] = 4.9V$ and
$R_X = 4.9V/(4.4)(100mA) = 11\Omega$

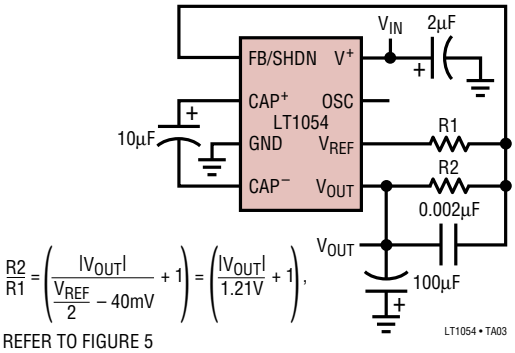
This resistor will reduce the power dissipated by the LT1054 by (4.9V)(100mA) = 490mW. The total power dissipated by the LT1054 would then be (940mW – 490mW) = 450mW. The junction temperature rise would now be only 58°C. Although commercial devices are guaranteed to be functional up to a junction temperature of 125°C, the specifications are only guaranteed up to a junction temperature of 100°C, so ideally you should limit the junction temperature to 100°C. For the above example this would mean limiting the ambient temperature to 42°C. Other steps can be taken to allow higher ambient temperatures. The thermal resistance numbers for the LT1054 packages represent worst case numbers with no heat sinking and still air. Small clip-on type heat sinks can be used to lower the thermal resistance of the LT1054 package. In some systems there may be some available airflow which will help to lower the thermal resistance. Wide PC board traces from the LT1054 leads can also help to remove heat from the device. This is especially true for plastic packages.

# TYPICAL APPLICATIONS

### Basic Voltage Inverter



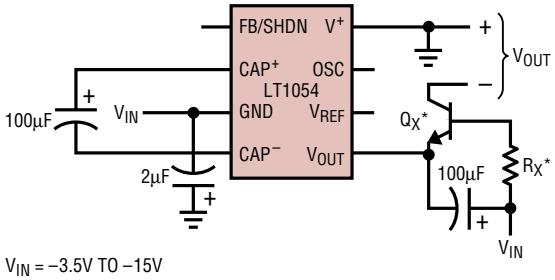

### Basic Voltage Inverter/Regulator




$$\frac{R2}{R1} = \left(\frac{|V_{OUT}|}{\frac{V_{REF}}{2} - 40mV} + 1\right) = \left(\frac{|V_{OUT}|}{1.21V} + 1\right),$$

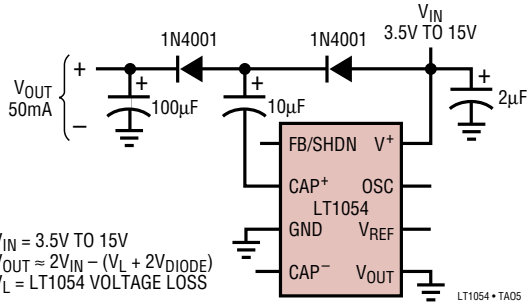
REFER TO FIGURE 5

### Negative Voltage Doubler



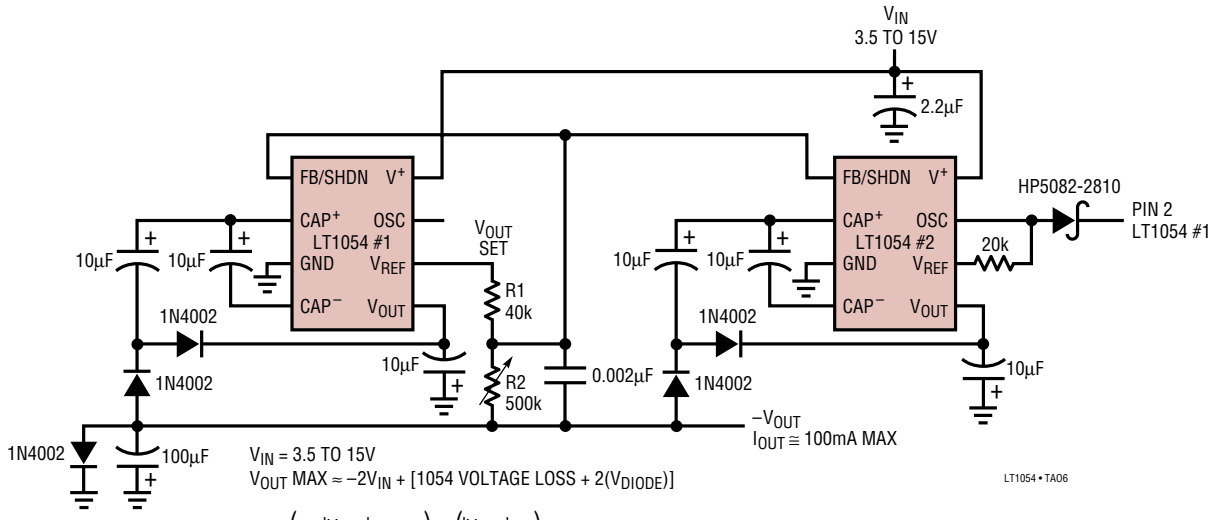

$V_{IN}$ = –3.5V TO –15V
$V_{OUT} = 2V_{IN}$ + (LT1054 VOLTAGE LOSS) + ($Q_X$ SATURATION VOLTAGE)
*SEE FIGURE 3

### Positive Doubler




$V_{IN}$ = 3.5V TO 15V
$V_{OUT} \approx 2V_{IN} - (V_L + 2V_{DIODE})$
$V_L$ = LT1054 VOLTAGE LOSS

### 100mA Regulating Negative Doubler

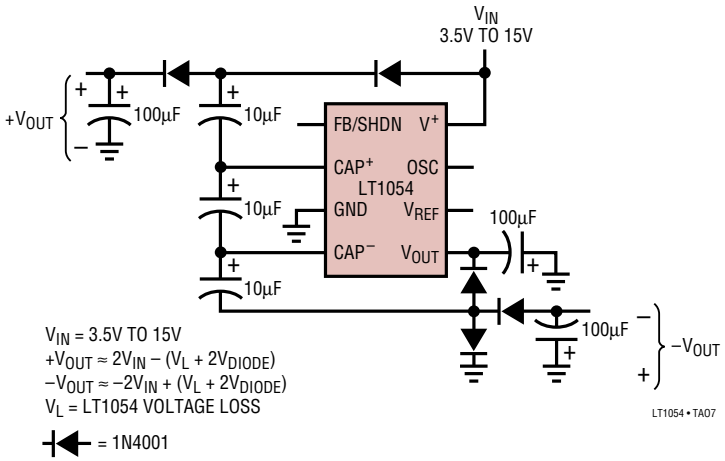



$V_{IN}$ = 3.5 TO 15V
$V_{OUT}$ MAX ≈ –2$V_{IN}$ + [1054 VOLTAGE LOSS + 2($V_{DIODE}$)]

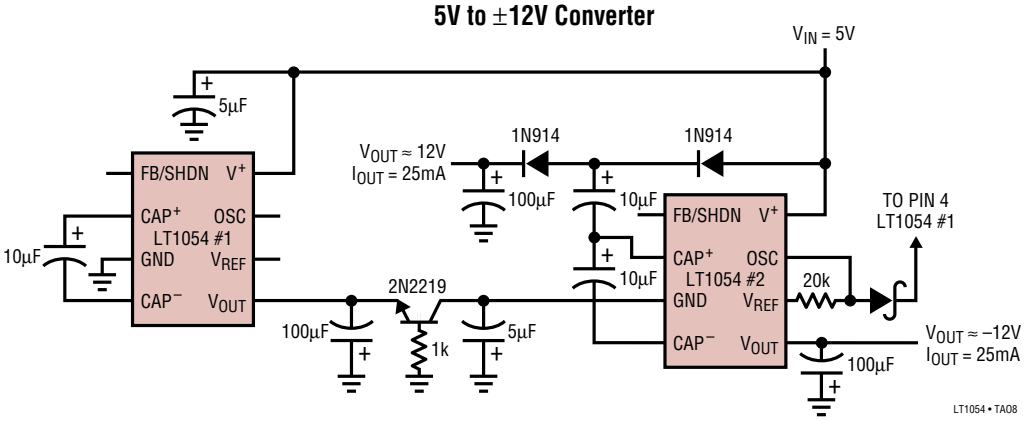
$$\frac{R2}{R1} = \left(\frac{|V_{OUT}|}{\frac{V_{REF}}{2} - 40mV} + 1\right) = \left(\frac{|V_{OUT}|}{1.21V} + 1\right), \text{ REFER TO FIGURE 5}$$

## TYPICAL APPLICATIONS

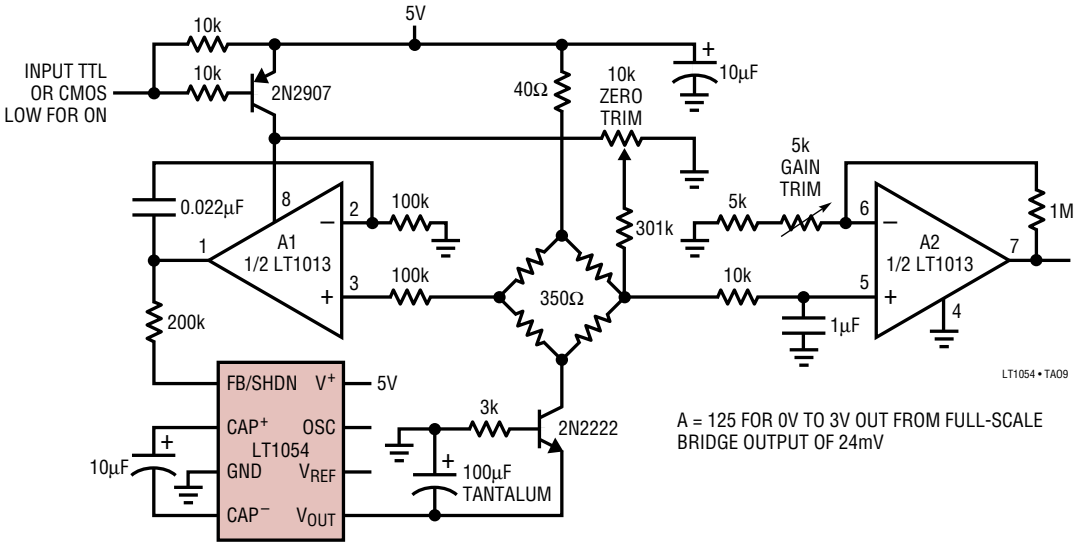
### Bipolar Supply Doubler




### 5V to ±12V Converter

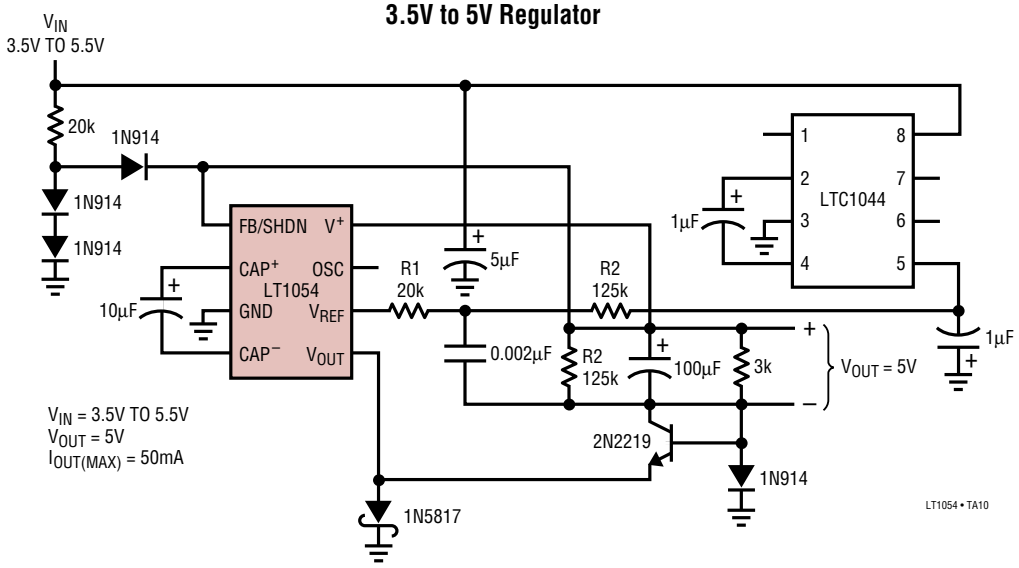



### Strain Gauge Bridge Signal Conditioner

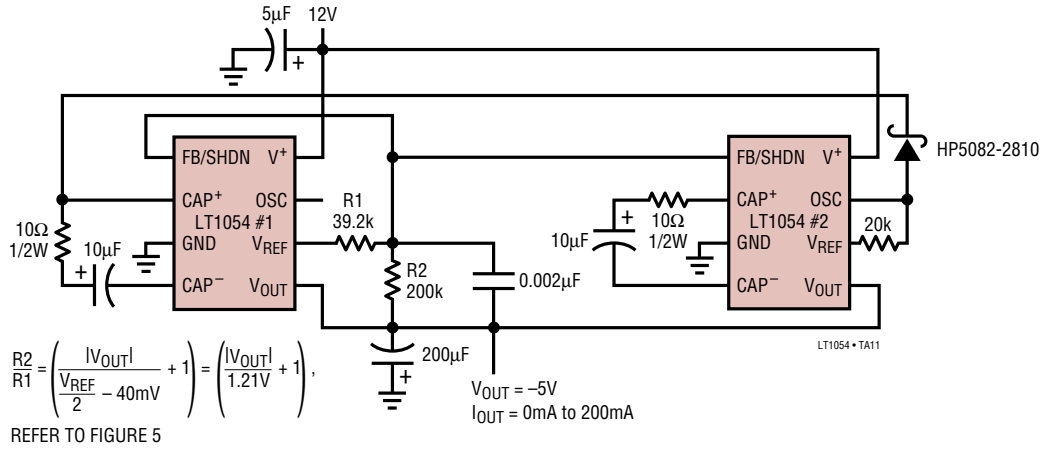


## TYPICAL APPLICATIONS

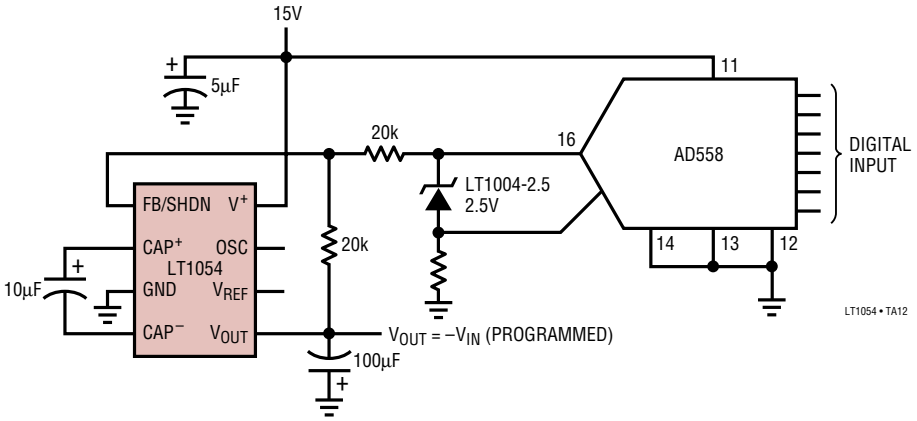
### 3.5V to 5V Regulator




### Regulating 200mA, 12V to –5V Converter



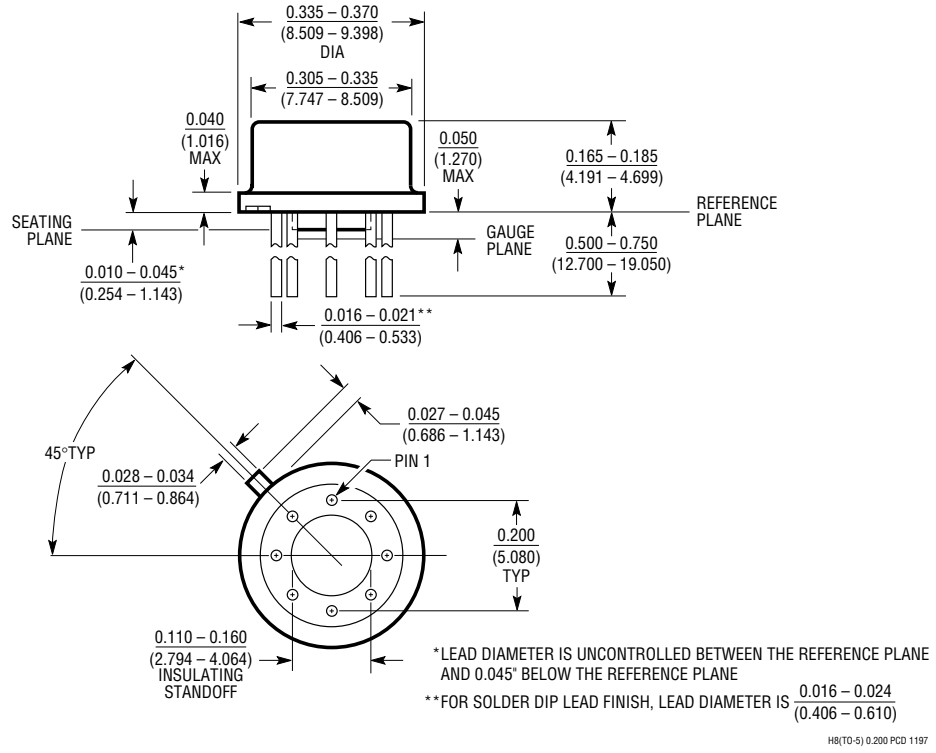

### Digitally Programmable Negative Supply



## PACKAGE DESCRIPTION

**Dimensions in inches (millimeters) unless otherwise noted.**

### H Package
### 8-Lead TO-5 Metal Can (0.200 PCD)
(LTC DWG # 05-08-1320)

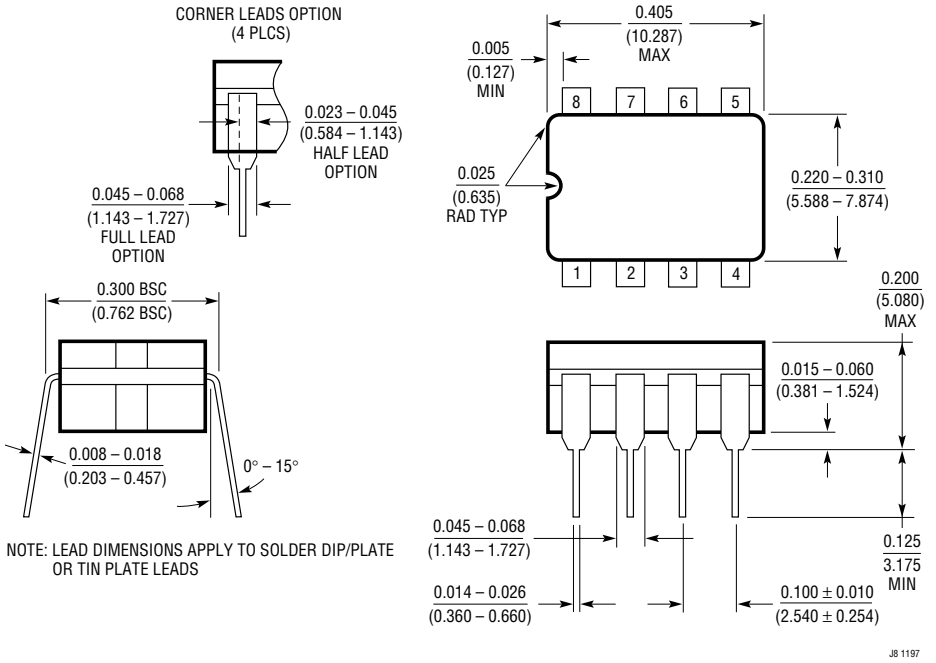



*LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND 0.045" BELOW THE REFERENCE PLANE

**FOR SOLDER DIP LEAD FINISH, LEAD DIAMETER IS 0.016 – 0.024 (0.406 – 0.610)

H8(TO-5) 0.200 PCD 1197

### J8 Package
### 8-Lead CERDIP (Narrow 0.300, Hermetic)
(LTC DWG # 05-08-1110)



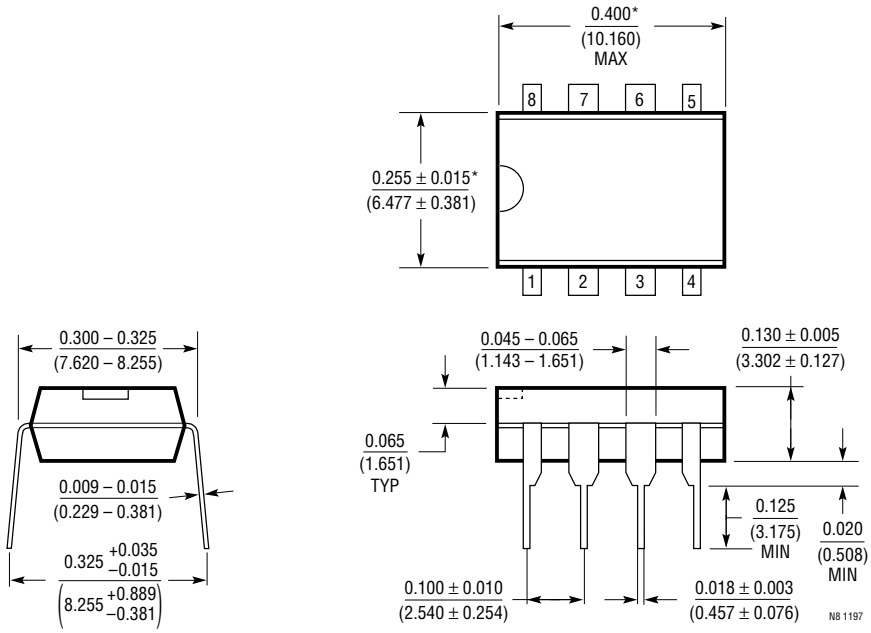

NOTE: LEAD DIMENSIONS APPLY TO SOLDER DIP/PLATE OR TIN PLATE LEADS

J8 1197

## PACKAGE DESCRIPTION

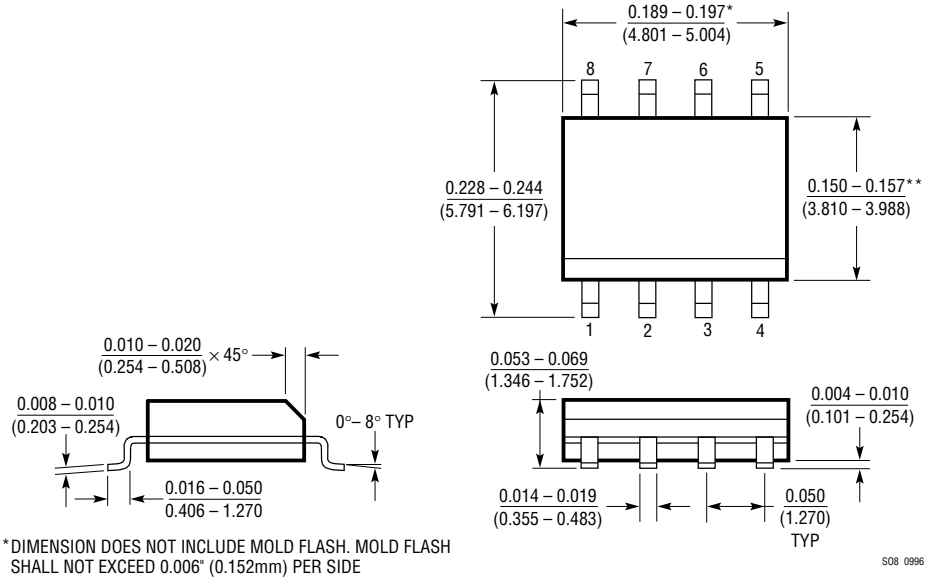
**Dimensions in inches (millimeters) unless otherwise noted.**

### N8 Package
### 8-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)




*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

### S8 Package
### 8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



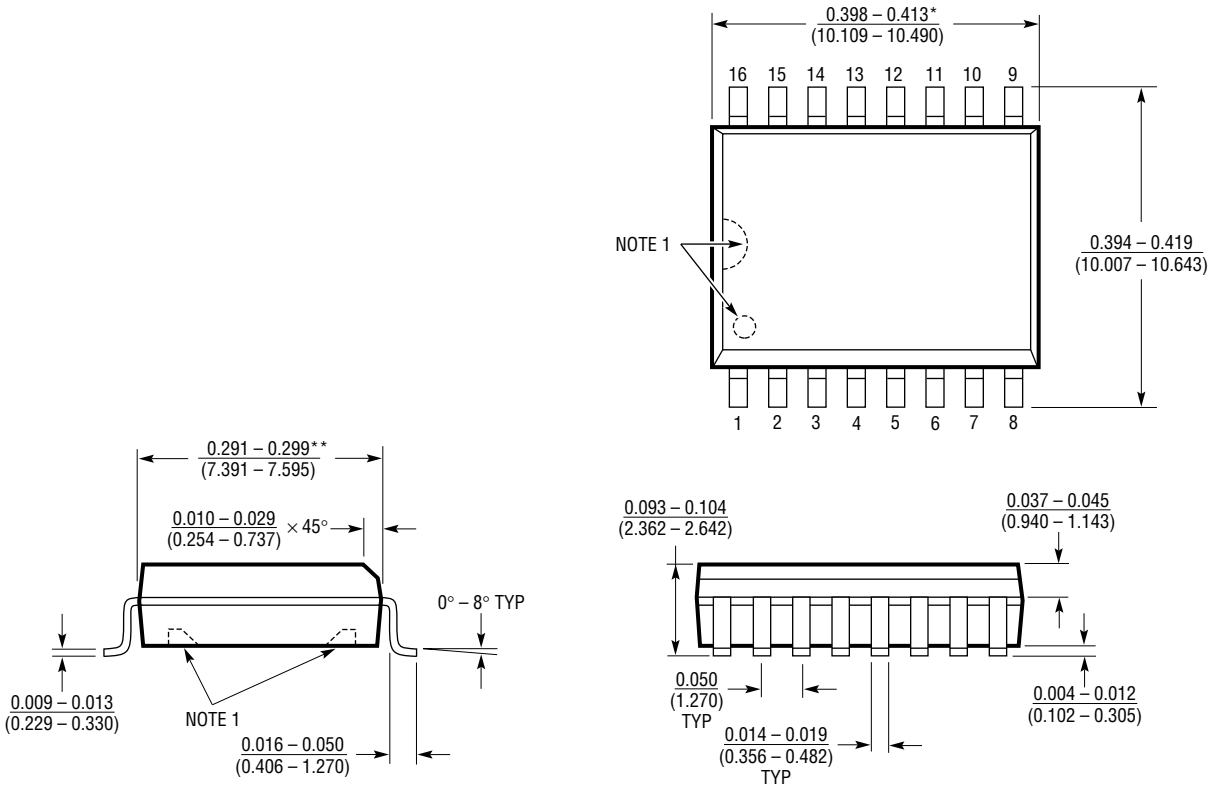

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

## PACKAGE DESCRIPTION

**Dimensions in inches (millimeters) unless otherwise noted.**

**SW Package**
**16-Lead Plastic Small Outline (Wide 0.300)**
(LTC DWG # 05-08-1620)




NOTE:
1. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS

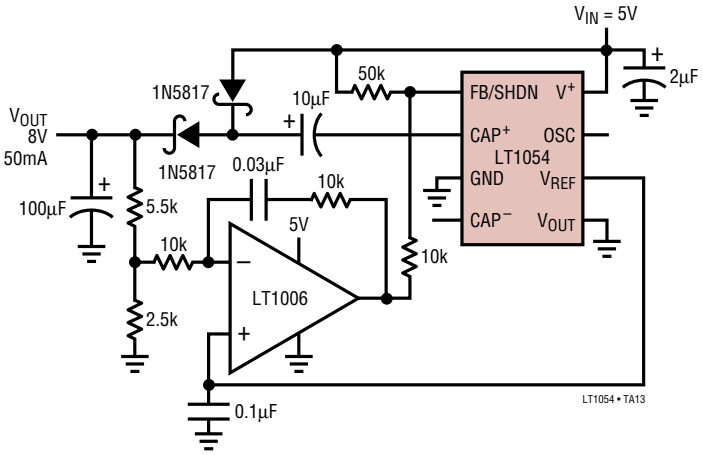
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

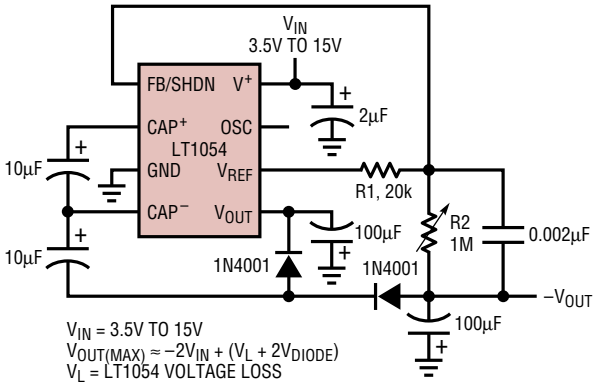
S16 (WIDE) 0396

# TYPICAL APPLICATIONS

### Positive Doubler with Regulation




### Negative Doubler with Regulator




THE TYPICAL APPLICATIONS CIRCUITS WERE VERIFIED USING THE STANDARD LT1054. FOR S8 APPLICATIONS ASSISTANCE IN ANY OF THE UNUSUAL APPLICATIONS CIRCUITS PLEASE CONSULT THE FACTORY

# RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LTC1144 | Switched-Capacitor Voltage Converter | Wide Input Voltage Range, 2V to 18V |
| LTC1514/LTC1515 | Step-Up/Step-Down Switched Capacitor DC/DC Converters | Regulated 5V Doublers |
| LT1611 | Micropower Inverting DC/DC Converter | 150mA Output |
| LT1614 | Micropower Inverting DC/DC Converter | 250mA Output |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