PCI 9656RDK–LITE

- PCI r2.2 compliant PCI form factor

- The PCI 9656 I/O Accelerator

– Supports 64-bit, 66MHz PCI bus operation

– Supports 32-bit, 66MHz generic Local Bus operation

- CPLD Local Bus memory controller and 128KB SRAM

- PLX Option Module (POM) expansion connector

- 32 surface mount footprints for processors, DSPs, ASICs, FPGAs, memory, I/O devices

- 30x25 0.1" through hole grid space for through hole devices

Complete Design Documentation

- OrCAD schematics

- Bill of Materials (BOM)

- OrCAD layout source with Gerber output files

- CPLD Memory controller Verilog source code

- All hardware manuals in PDF format

Complete Windows Host Software Development Environment

- Windows 98/Me/NT/2000 device drivers with source code

- PCI 9656 Windows Host API and object code library

- PLXMon Windows GUI debug tool for monitoring, debugging, configuration, and code download

- Power Management Event D_{3COLD} wake-up event emulation

Rapid Development Kit For PCI 9656 Generic Local Bus Designs

An Invaluable Development Aid

The PLX PCI 9656RDK–LITE (RDK–LITE) delivers a flexible development platform for designs using the PCI 9656 with generic 32-bit local bus devices. The RDK–LITE is shipped pre-configured for de-multiplexed generic address/data bus operation, but is very easily reconfigured for multiplexed address/data bus applications. The RDK–LITE provides 32 suftace-mount footprints for hardware designers to easily add processors, DSPs, ASICs, FPGAs, memory, and I/O devices to test, simulate, and debug their designs without fabricating their own boards, which can save considerable time in the development process and shorten time to market. The RDK–LITE also includes the PLX Software Development Kite Lite Edition (SDK–LITE) CD, which provides a complete Microsoft Windows® software development environment. The PCI 9656RDK–LITE's software, hardware registers, and footprints are backward-compatible with the PCI 9054RDK–LITE, simplifying the move from existing 32-bit, 33MHz PCI 9054 generic local-bus designs into 64-bit, 66MHz PCI 9656 based products.
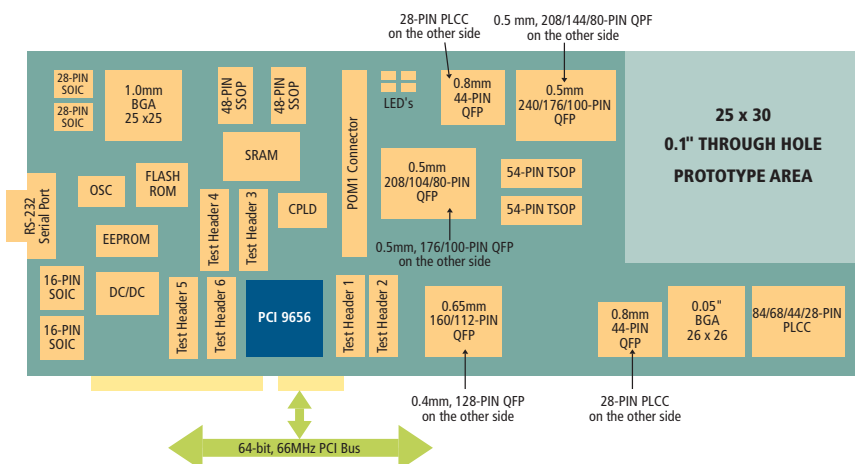
A Complete Package

The hardware reference board serves as both a hardware and software development platform for PCI 9656 based designs. This board is configured for de-multiplexed address and data bus operation (C Mode), but it is user configurable for multiplexed address and data bus operation (J Mode). Its local bus memory controller and SRAM enable immediate Direct Slave and DMA code development and testing. Its large and flexible prototyping area enables the easy extension of the test and debug features of the RDK to include your value added logic.

The Hardware Development Kit LITE (HDK–LITE) CD-ROM includes complete documentation of the reference board hardware design, making its components easily reusable in your designs. This documentation includes the board schematics, the board layout source and output files, Bill of Materials (BOM), the Verilog source code for the CPLD memory controller and manuals in PDF fromat.

The SDK–LITE is a CD-ROM which provides a complete set of Windows host side software and tools, including host-side Windows 98/Me/NT/2000 drivers for the reference board, PCI 9656 specific APIs and object code libraries, and the PLXMon Windows GUI debug tool. The APIs are backward compatible with the PCI 9054, enabling the easy migration of PCI 9054 software to the PCI 9656.

PCI 9656RDK-LITE Block Diagram

PCI 9656RDK-LITE Board

Function	Description
PCI Bus Interface	PLX PCI 9656 I/O Accelerator
PCI Bus Speed	64-bit, 66 MHz Max
Local Bus Speed	32-bit, 66 MHz Max with C or J mode
PME D3$_{cold}$ wake up emulation button	Emulate Power Management wake up event
32K x 32 synchronous SRAM with CPLD memory controller	Demonstrating the infinite bursting capability of the PCI 9656 for both C and J modes
BGA Footprints	0.050" 26x26, 1.0 mm 25x25
QFP/PLCC Footprints	0.65mm 160/112-pin with 0.4mm 128-pin on soldering side 0.5mm 240/176/100-pin with 0.5mm 208/144/80-pin on soldering side 0.5mm 208/144/80-pin with 0.5mm 176/100-pin on soldering side Two (2) 0.5 mm 44-pin with 28-pin PLCC on soldering side 32-pin PLCC 28/44/68/84-pin PLCC
SDRAM Footprint	Two (2) 54-pin supporting up to 64 Mbytes SDRAM
EEPROM Socket	Supports boot-up FLASH memory
RS232 DP-9 Serial Port	Used for debugging or code downloading
RJ 40 and USB Connector Footprints	Supports Ethernet or USB port
Termination Adapter Footprints	Six (6) 2 x 10-pin
0.1" Through Hole Grid Space	For through hole devices

PCI 9656HDK-LITE CD-ROM

Contents	Description
PCI 9656HDK-LITE CD-ROM	A CD-ROM containing all hardware design information: OrCAD schematics, OrCAD layout source and Gerber output files, Bill of Materials (BOM), glue logic code, hardware manuals in PDF format

PLX SDK-LITE CD-ROM

Contents	Description
PCI 9656 host side API and object code libraries	Simplifies the programming of complex hardware control with simple, powerful API calls. The reusable components enable easy creation of device drivers for customer environments and provide for easy porting to future PLX PCI devices
Windows 98/Me/NT/2000 drivers	PCI 9656 Windows reference drivers
PLXMon™	Enables easy monitoring, debugging, and configuring of PLX's PCI devices and other PCI/local bus devices. Supports downloading of sample boot FLASH code onto RDK or customer design and allows debugging via serial and/or Ethernet ports
Comprehensive Manuals (PDF)	Shortens learning curve and development cycle

Product Ordering Information

Part Number	Description
PCI 9656-AA66BI	PCI 9656 I/O Accelerator Chip (PBGA)
CompactPCI 9656RDK-860	CompactPCI Rapid Development Kit with PLX PCI 9656 I/O Accelerator Chip and Motorola MPC860 PowerQUICC
PCI 9656RDK-LITE	PCI 9656 flexible Rapid Development Kit
SDK-LITE	Windows host side software development kit for PLX I/O Accelerators and Processor
SDK-PRO	Windows host and local sides software development kit, plus RTOS and source code for PLX I/O Accelerators and Processor

Please visit the PLX Web site at http://www.plxtech.com or contact PLX sales at 408-774-9060 for pricing and samples.

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