Integrated 802.11 b/g WLAN Module

FEATURES

- IEEE 802.11 b/g compliant.
- Typical WLAN Transmit Power:
  - +19.0 dBm, 11 Mbps, CCK (b)
  - +15 dBm, 54 Mbps, OFDM (g)
- Typical WLAN Sensitivity:
  - - 85 dBm, 8% PER,11 Mbps
  - -70 dBm, 10% PER, 54 Mbps
- Miniature footprint: 14 mm x 21 mm
- Low height profile: 2.3 mm
- Operating Voltage: 2.9V to 3.6V
- Operating temperature: -40 to +85^{o} C
- Embedded network stack
- Wireless Security WEP, WPA Personal, WPA2 Personal
- Terminal for PCB/Chip antenna feeds
- Compact design based on Texas Instruments CC3000 transceiver
- SPI host interface
- Simple integration with microcontrollers and microprocessors
- Worldwide acceptance: FCC (USA), IC (Canada), and ETSI (Europe)
- RoHS compliant
- Streamlined development with LSR design services

APPLICATIONS

- HVAC Control, Smart Energy
- Sensor Networks
- Medical
- Home Automation
- Home Monitoring

DESCRIPTION

The TiWi-SL is a high performance 2.4 GHz WLAN module that contains an IP networking stack in a pre-certified footprint.

The module includes the necessary PHY, MAC, and network layers to support WLAN applications through a simple SPI connection to host microcontrollers or other embedded processors.

Need to get to market quickly? Not an expert in 802.11. Need a custom antenna? Would you like to own the design? Would you like a custom design? Not quite sure what you need? Do you need help with your host board? LS Research Design Services will be happy to develop custom hardware or software, or assist with integrating the design. Contact us at sales@lsr.com or call us at 262-375-4400.

ORDERING INFORMATION

Order Number	Description
450-0067	TiWi-SL Module
450-0089	TiWi-SL EM Board with Chip Antenna

Table 1 Orderable TiWi-SL Part Numbers

MODULE ACCESSORIES

	Order Number	Description
	**001-0001**	2.4 GHz Dipole Antenna with Reverse Polarity SMA Connector
	**080-0001**	U.FL to Reverse Polarity SMA Bulkhead Cable 105mm

Table 2 Module Accessories

APPLICABLE DOCUMENTS

- TiWi-SL EM Board User Guide (330-0086)
- TiWi-SL Antenna Design Guide (330-0092)

BLOCK DIAGRAM

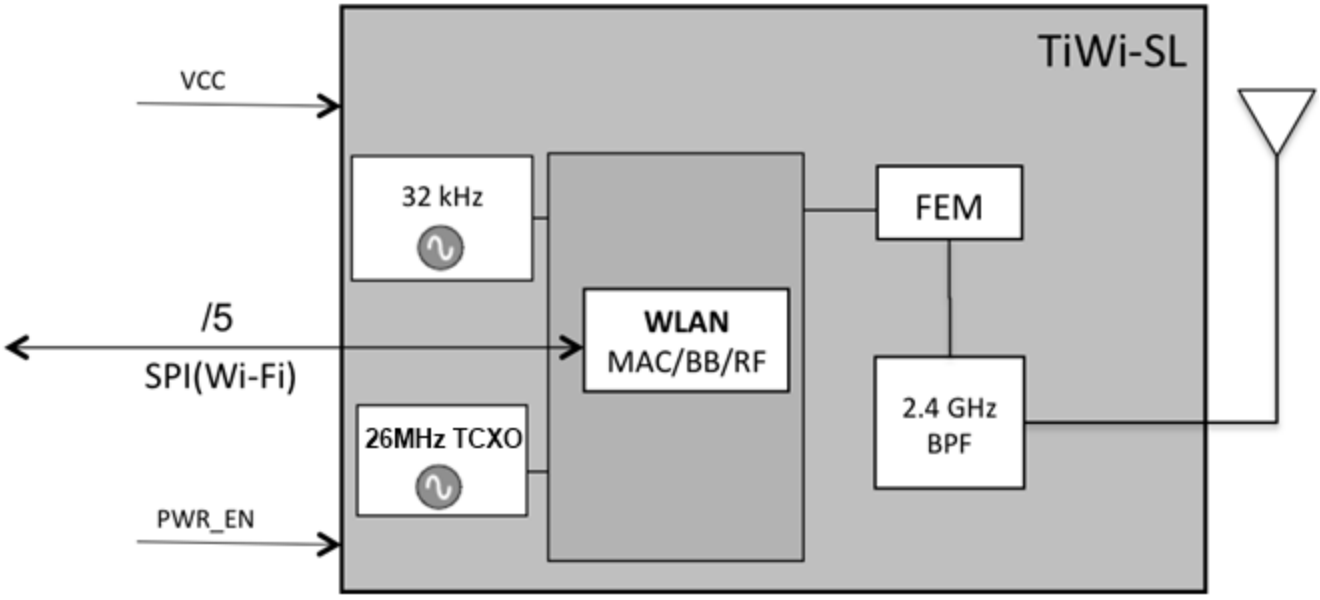

Figure 1 TiWi-SL Module Block Diagram – Top Level

FUNCTIONAL BLOCK FEATURES

WLAN Features

- IEEE802.11b/g compliant WLAN MAC Baseband Processor and RF transceiver
- IEEE Std 802.11d,i PICS compliant
- Supports serial debug interface
- Supports Serial Peripheral Interface (SPI) Host Interface
- **Media Access Controller (MAC)**
  - Embedded ARM™ Central Processing Unit (CPU)
  - Hardware-Based Encryption/Decryption Using 64-, 128-Bit WEP, TKIP or AES Keys,
  - Supports requirements for Wireless Fidelity (Wi-Fi) Protected Access (WPA and WPA2.0) and IEEE
  - Std 802.11i [Includes Hardware-Accelerated Advanced-Encryption Standard (AES)]
- Baseband Processor
- **2.4GHz Radio**
  - Digital Radio Processor (DRP) implementation
  - Internal LNA
  - Supports : IEEE Std 802.11b, 802.11g, 802.11b/g

Network Stack Supported Protocols

- **Transport layer:**
  - TCP
  - UDP
- **Network layer:**
  - IPv4
  - Ping
  - DHCP
  - DNS Client
- **Link layer:**
  - ARP

Wireless Security System Features

- **Supported modes:**
  - Open (no security)
  - WEP
  - WPA-personal
  - WPA2-personal
- **Supported encryption types:**
  - WEP
  - TKIP
  - AES
  - Open

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TIWI-SL MODULE FOOTPRINT AND PIN DEFINITIONS

To apply the TiWi-SL module, it is important to use the module pins in your application as they are designated below, and in the corresponding pin definition table found on pages 8 and 9. Not all the pins on the TiWi-SL module may be used, as some are reserved.

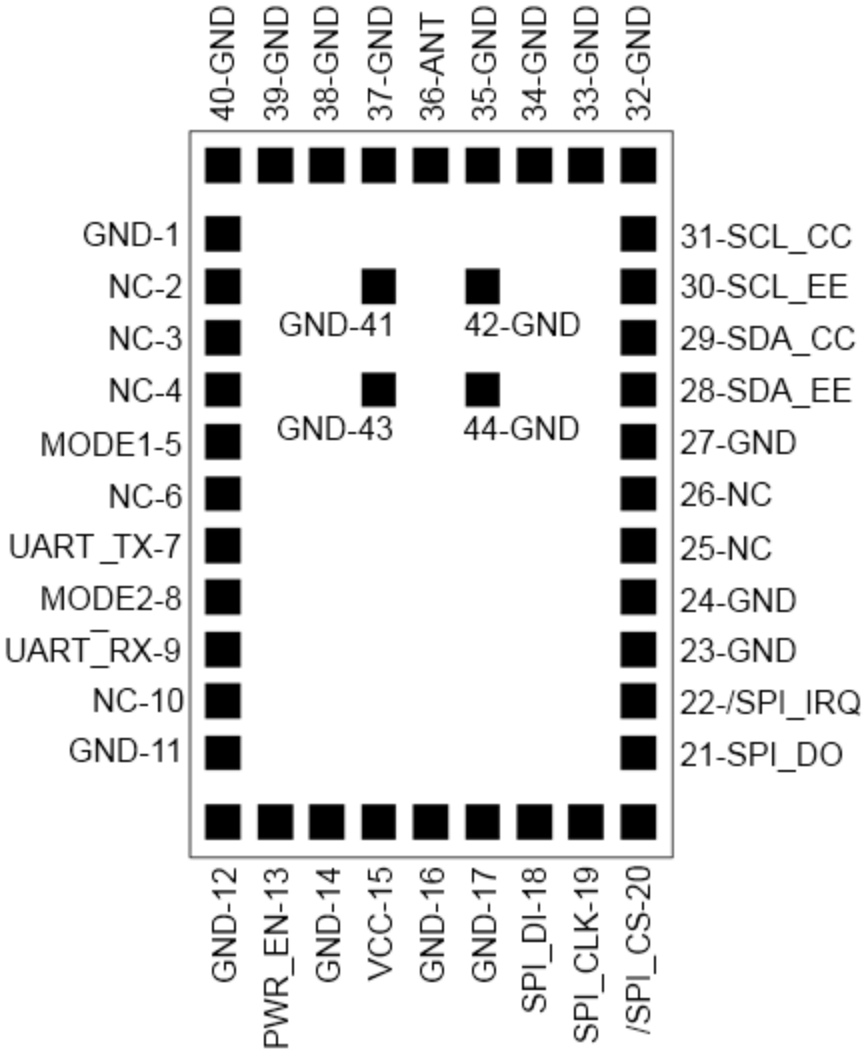


Figure 2 TiWi-SL Pinout

PIN DESCRIPTIONS

Module Pin	Name	I/O Type	Buffer Type	Logic Level	Description
1	GND	GND	-	-	GROUND
2	NC	-	-	-	NO CONNECT (DO NOT CONNECT)
3	NC	-	-	-	NO CONNECT (DO NOT CONNECT)
4	NC	-	-	-	NO CONNECT (DO NOT CONNECT)
5	MODE1	DI	-	-	MODE1 (SHORT TO MODE2 FOR NORMAL USE, SHORT TO GROUND FOR TEST USE)
6	NC	-	-	-	NO CONNECT (DO NOT CONNECT)
7	UART_TX (1)	DO	-	1.8 VDC	TEST UART TX (1.8V LOGIC)
8	MODE2	DI	-	-	MODE2 (SHORT TO MODE1 FOR NORMAL USE, LEAVE OPEN FOR TEST USE)
9	UART_RX (1)	DI	-	1.8 VDC	TEST UART RX (1.8V LOGIC)
10	NC	-	-	-	NO CONNECT (DO NOT CONNECT)
11	GND	GND	-	-	GROUND
12	GND	GND	-	-	GROUND
13	PWR_EN	DI	-	-	MODULE POWER ENABLE (1.8-VCC)
14	GND	GND	-	-	GROUND
15	VCC	PI	-	-	POWER TO MODULE (2.9-3.6 VDC)
16	GND	GND	-	-	GROUND
17	GND	GND	-	-	GROUND
18	SPI_DI	DI	-	3.3 VDC	HOST INTERFACE SPI DATA IN
19	SPI_CLK	DI	-	3.3 VDC	HOST INTERFACE SPI CLOCK
20	/SPI_CS	DI	-	3.3 VDC	HOST INTERFACE SPI CHIP SELECT (ACTIVE LOW)
21	SPI_DO	DO	10mA	3.3 VDC	HOST INTERFACE SPI DATA OUT
22	/SPI_IRQ	DO	10mA	3.3 VDC	HOST INTERFACE SPI INTERRUPT (ACTIVE LOW)
23	GND	GND	-	-	GROUND
24	GND	GND	-	-	GROUND
25	NC	-	-	-	NO CONNECT (DO NOT CONNECT)
26	NC	-	-	-	NO CONNECT (DO NOT CONNECT)
27	GND	GND	-	-	GROUND

Module Pin	Name	I/O Type	Buffer Type	Logic Level	Description
28	SDA_EE (2)	DIO	-	1.8 VDC	I2C DATA LINE FROM EEPROM (1.8V LOGIC)
29	SDA_CC (2)	DIO	4mA	1.8 VDC	I2C DATA LINE FROM CC3000, PULL-UP ON MODULE (1.8V LOGIC)
30	SCL_EE (3)	DI	-	1.8 VDC	I2C CLOCK LINE FROM EEPROM (1.8V LOGIC)
31	SCL_CC (3)	DO	4mA	1.8 VDC	I2C CLOCK LINE FROM CC3000, PULL-UP ON MODULE (1.8V LOGIC)
32	GND	GND	-	-	GROUND
33	GND	GND	-	-	GROUND
34	GND	GND	-	-	GROUND
35	GND	GND	-	-	GROUND
36	ANT (4)	RF	-	-	ANTENNA, 50 OHMS
37	GND	GND	-	-	GROUND
38	GND	GND	-	-	GROUND
39	GND	GND	-	-	GROUND
40	GND	GND	-	-	GROUND
41	GND	GND	-	-	GROUND
42	GND	GND	-	-	GROUND
43	GND	GND	-	-	GROUND
44	GND	GND	-	-	GROUND

(1) These signals are test UART signals which are 1.8v logic, and they should be left unconnected for normal operation.
(2) The I2C data signals from the CC3000 and EEPROM must be connected together for normal operation.
(3) The I2C clock signals from the CC3000 and EEPROM must be connected together for normal operation.
(4) The antenna terminal presents a DC short circuit to ground.

PI = Power Input
DI = Digital Input
DO = Digital Output
DIO = Bi-directional Digital Port
RF = Bi-directional RF Port
GND=Ground

Table 3 TiWi-SL Module Pin Descriptions

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Min	Max	Unit
Power supply voltage (VCC)	-0.5	+3.8	V
Voltage on digital pins (1)	-0.5	VCC + 0.5	V
Voltage on EEPROM and UART test pins (2)	-0.5	2.1	V
RF input power, antenna port		+10	dBm
Operating temperature	-40	+85	ºC
Storage temperature	-55	+125	ºC

(1) This includes the SPI signals and the PWR_EN signal.
(2) These signals are not intended for general purpose use.

Table 4 Absolute Maximum Ratings

Recommended Operating Conditions

Parameter	Min	Typical	Max	Unit
VCC	2.9	3.3	3.6	V
Voltage on digital pins (1)	0	3.3	VCC	V
Voltage on EEPROM and UART test pins (2)	0		1.8	V
Ambient temperature range (3)	-30	25	75	ºC

(1) Applies to SPI signals.
(2) These signals are not intended for general purpose use.
(3) The device can be reliably operated for 5000 active hours cumulative at $T_{ambient}$ of 85C.

Table 5 Recommended Operating Conditions

General Characteristics

DC Characteristics – UART/EEPROM I/O

Parameter	Test Conditions	Min	Typical	Max	Unit
Logic input low, V_{IL}		0	-	0.63	V
Logic input high, V_{IH}		1.7	-	1.8	V
Logic output low, V_{OL}	8mA	0	-	0.45	V
Logic output high, V_{OH}	8mA	1.35	-	1.8	V

Table 6 DC Characteristics General Purpose I/O

DC Characteristics – General Purpose I/O

Parameter	Test Conditions	Min	Typical	Max	Unit
Logic input low, V_{IL}		0	-	0.8	V
Logic input high, V_{IH}		2.0	-	VCC	V
Logic output low, V_{OL}	12mA	0	-	0.8	V
Logic output high, V_{OH}	12mA	2.3	-	VCC	V

Applies to the SPI signals and the PWR_EN signal.

Table 7 DC Characteristics General Purpose I/O

RF Characteristics

Parameter	Min	Typical	Max	Unit
RF frequency range	2412		2472	MHz
RF data rate	1	802.11 b/g rates supported	54	Mbps

Table 8 RF Characteristics

TCP and UDP Throughput

Traffic Type	Privacy	Throughput (Mbps)
UDP Tx	Open	6.86
UDP Rx	Open	5.54
TCP Tx	Open	3.52
TCP Rx	Open	2.57
UDP Tx	WEP128	6.60
UDP Rx	WEP128	5.53
TCP Tx	WEP128	3.21
TCP Rx	WEP128	2.45
UDP Tx	WPAv1	6.50
UDP Rx	WPAv1	5.50
TCP Tx	WPAv1	3.27
TCP Rx	WPAv1	2.38
UDP Tx	WPAv2	6.84
UDP Rx	WPAv2	5.54
TCP Tx	WPAv2	3.25
TCP Rx	WPAv2	2.48

Table 9 TCP and UDP Throughput

Power Consumption

Parameter	Test Conditions	Min	Typical	Max	Unit
CCK (b) TX Current	2437 MHz, VCC = 3.3V, T_{amb} = +25°C Po = 19 dBm, 1 Mbps CCK L = 1200 bytes, t_{delay} (idle) = 40 uS	-	276	-	mA
CCK (b) TX Current	2437 MHz, VCC = 3.3V, T_{amb} = +25°C Po = 19 dBm, 11 Mbps CCK L = 1200 bytes, t_{delay} (idle) = 40 uS	-	273	-	mA
OFDM (g) TX Current	2437 MHz, VCC = 3.3V, T_{amb} = +25°C Po = 17 dBm, 18 Mbps OFDM L = 1200 bytes, t_{delay} (idle) = 4 uS	-	232	-	mA
OFDM (g) TX Current	2437 MHz, VCC = 3.3V, T_{amb} = +25°C Po = 15 dBm, 54 Mbps OFDM L = 1200 bytes, t_{delay} (idle) = 4 uS	-	194	-	mA
CCK (b) RX Current		-	115	-	mA
OFDM (g) RX Current		-	115	-	mA
Power Down Mode [1]		-	<1	-	uA

[1] Total Current from VCC when PWR_EN is low and VCC is present.

Table 10 WLAN Power Consumption

RF Characteristics

WLAN Transmitter Characteristics
(TA = +25°C, VCC = 3.3 V)

Parameter	Test Conditions	Min	Typ	Max	Unit
1 Mbps DSSS (b) TX Output Power	1 Mbps CCK 802.11(b) Mask Compliance 35% EVM RMS power over TX packet	-	19.3	-	dBm
2 Mbps DSSS (b) TX Output Power	2 Mbps CCK 802.11(b) Mask Compliance 35% EVM RMS power over TX packet	-	19.2	-	dBm
11 Mbps CCK (b) TX Output Power	11 Mbps CCK 802.11(b) Mask Compliance 35% EVM RMS power over TX packet	-	18.9	-	dBm
6 Mbps OFDM (g) TX Output Power	6 Mbps OFDM 802.11(g) Mask Compliance -8 dB EVM RMS power over TX packet	-	17.4	-	dBm
9 Mbps OFDM (g) TX Output Power	9 Mbps OFDM 802.11(g) Mask Compliance -8 dB EVM RMS power over TX packet	-	17.2	-	dBm
18 Mbps OFDM (g) TX Output Power	18 Mbps OFDM 802.11(g) Mask Compliance -13 dB EVM RMS power over TX packet	-	17.3	-	dBm
36 Mbps OFDM (g) TX Output Power	36 Mbps OFDM 802.11(g) Mask Compliance -19 dB EVM RMS power over TX packet	-	15.3	-	dBm
54 Mbps OFDM (g) TX Output Power	54 Mbps OFDM 802.11(g) Mask Compliance -25 dB EVM RMS power over TX packet	-	15.4	-	dBm

Table 11 WLAN Transmitter RF Characteristics

WLAN Transmitter Characteristics
(TA = +85°C, VCC = 3.3 V)

Parameter	Test Conditions	Min	Typ	Max	Unit
1 Mbps DSSS (b) TX Output Power	1 Mbps CCK 802.11(b) Mask Compliance 35% EVM RMS power over TX packet	-	18.6	-	dBm
2 Mbps DSSS (b) TX Output Power	2 Mbps CCK 802.11(b) Mask Compliance 35% EVM RMS power over TX packet	-	18.4	-	dBm
11 Mbps CCK (b) TX Output Power	11 Mbps CCK 802.11(b) Mask Compliance 35% EVM RMS power over TX packet	-	18.2	-	dBm
6 Mbps OFDM (g) TX Output Power	6 Mbps OFDM 802.11(g) Mask Compliance -8 dB EVM RMS power over TX packet	-	16.5	-	dBm
9 Mbps OFDM (g) TX Output Power	9 Mbps OFDM 802.11(g) Mask Compliance -8 dB EVM RMS power over TX packet	-	16.4	-	dBm
18 Mbps OFDM (g) TX Output Power	18 Mbps OFDM 802.11(g) Mask Compliance -13 dB EVM RMS power over TX packet	-	16.5	-	dBm
36 Mbps OFDM (g) TX Output Power	36 Mbps OFDM 802.11(g) Mask Compliance -19 dB EVM RMS power over TX packet	-	14.5	-	dBm
54 Mbps OFDM (g) TX Output Power	54 Mbps OFDM 802.11(g) Mask Compliance -25 dB EVM RMS power over TX packet	-	14.6	-	dBm

Table 12 WLAN Transmitter RF Characteristics

WLAN Transmitter Characteristics
(TA = -40°C, VCC = 3.3 V)

Parameter	Test Conditions	Min	Typ	Max	Unit
1 Mbps DSSS (b) TX Output Power	1 Mbps CCK 802.11(b) Mask Compliance 35% EVM RMS power over TX packet	-	17.4	-	dBm
2 Mbps DSSS (b) TX Output Power	2 Mbps CCK 802.11(b) Mask Compliance 35% EVM RMS power over TX packet	-	17.3	-	dBm
11 Mbps CCK (b) TX Output Power	11 Mbps CCK 802.11(b) Mask Compliance 35% EVM RMS power over TX packet	-	17.0	-	dBm
6 Mbps OFDM (g) TX Output Power	6 Mbps OFDM 802.11(g) Mask Compliance -8 dB EVM RMS power over TX packet	-	16.3	-	dBm
9 Mbps OFDM (g) TX Output Power	9 Mbps OFDM 802.11(g) Mask Compliance -8 dB EVM RMS power over TX packet	-	16.3	-	dBm
18 Mbps OFDM (g) TX Output Power	18 Mbps OFDM 802.11(g) Mask Compliance -13 dB EVM RMS power over TX packet	-	16.3	-	dBm
36 Mbps OFDM (g) TX Output Power	36 Mbps OFDM 802.11(g) Mask Compliance -19 dB EVM RMS power over TX packet	-	14.4	-	dBm
54 Mbps OFDM (g) TX Output Power	54 Mbps OFDM 802.11(g) Mask Compliance -25 dB EVM RMS power over TX packet	-	14.4	-	dBm

Table 13 WLAN Transmitter RF Characteristics

WLAN Receiver Characteristics
(TA = +25°C, VCC = 3.3V) [1]

Parameter	Test Conditions	Min	Typ	Max	Unit
1 Mbps CCK (b) RX Sensitivity	8% PER	-	-91.1	-	dBm
2 Mbps CCK (b) RX Sensitivity	8% PER	-	-85.3	-	dBm
11 Mbps CCK (b) RX Sensitivity	8% PER	-	-84.8	-	dBm
6 Mbps CCK (b) RX Sensitivity	10% PER	-	-87.6	-	dBm
9 Mbps OFDM (g) RX Sensitivity	10% PER	-	-86.1	-	dBm
18 Mbps OFDM (g) RX Sensitivity	10% PER	-	-84.6	-	dBm
36 Mbps OFDM (g) RX Sensitivity	10% PER	-	-84.6	-	dBm
54 Mbps OFDM (g) RX Sensitivity	10% PER	-	-70.3	-	dBm
1 Mbps CCK (b) RX Overload Level	8% PER	-6.3	-	-	dBm
2 Mbps CCK (b) RX Overload Level	8% PER	-6.3	-	-	dBm
11 Mbps CCK (b) RX Overload Level	8% PER	-6.3	-	-	dBm
9 Mbps OFDM (g) RX Overload Level	10% PER	-16.3	-	-	dBm
18 Mbps OFDM (g) RX Overload Level	10% PER	-16.3	-	-	dBm
36 Mbps OFDM (g) RX Overload Level	10% PER	-16.3	-	-	dBm
54 Mbps OFDM (g) RX Overload Level	10% PER	-16.3	-	-	dBm

[1] Up to 2 dB degradation at Channel 13 for 11g modes and up to 2 dB degradation at Channel 14 for 11b/g modes.

Table 14 WLAN Receiver RF Characteristics

WLAN Receiver Characteristics
(TA = +85°C, VCC = 3.3V) [1]

Parameter	Test Conditions	Min	Typ	Max	Unit
1 Mbps CCK (b) RX Sensitivity	8% PER	-	-91.6	-	dBm
2 Mbps CCK (b) RX Sensitivity	8% PER	-	-85.6	-	dBm
11 Mbps CCK (b) RX Sensitivity	8% PER	-	-83.3	-	dBm
6 Mbps CCK (b) RX Sensitivity	10% PER	-	-86.1	-	dBm
9 Mbps OFDM (g) RX Sensitivity	10% PER	-	-85.8	-	dBm
18 Mbps OFDM (g) RX Sensitivity	10% PER	-	-83.6	-	dBm
36 Mbps OFDM (g) RX Sensitivity	10% PER	-	-75.1	-	dBm
54 Mbps OFDM (g) RX Sensitivity	10% PER	-	-69.3	-	dBm
1 Mbps CCK (b) RX Overload Level	8% PER	-6.3	-	-	dBm
2 Mbps CCK (b) RX Overload Level	8% PER	-6.3	-	-	dBm
11 Mbps CCK (b) RX Overload Level	8% PER	-6.3	-	-	dBm
9 Mbps OFDM (g) RX Overload Level	10% PER	-16.3	-	-	dBm
18 Mbps OFDM (g) RX Overload Level	10% PER	-16.3	-	-	dBm
36 Mbps OFDM (g) RX Overload Level	10% PER	-16.3	-	-	dBm
54 Mbps OFDM (g) RX Overload Level	10% PER	-16.3	-	-	dBm

[1] Up to 2 dB degradation at Channel 13 for 11g modes and up to 2 dB degradation at Channel 14 for 11b/g modes.

Table 15 WLAN Receiver RF Characteristics

WLAN Receiver Characteristics
(TA = -40°C, VCC = 3.3V) [1]

Parameter	Test Conditions	Min	Typ	Max	Unit
1 Mbps CCK (b) RX Sensitivity	8% PER	-	-93.1	-	dBm
2 Mbps CCK (b) RX Sensitivity	8% PER	-	-85.3	-	dBm
11 Mbps CCK (b) RX Sensitivity	8% PER	-	-85.8	-	dBm
6 Mbps CCK (b) RX Sensitivity	10% PER	-	-88.1	-	dBm
9 Mbps OFDM (g) RX Sensitivity	10% PER	-	-86.8	-	dBm
18 Mbps OFDM (g) RX Sensitivity	10% PER	-	-84.8	-	dBm
36 Mbps OFDM (g) RX Sensitivity	10% PER	-	-76.1	-	dBm
54 Mbps OFDM (g) RX Sensitivity	10% PER	-	-71.6	-	dBm
1 Mbps CCK (b) RX Overload Level	8% PER	-6.3	-	-	dBm
2 Mbps CCK (b) RX Overload Level	8% PER	-6.3	-	-	dBm
11 Mbps CCK (b) RX Overload Level	8% PER	-6.3	-	-	dBm
9 Mbps OFDM (g) RX Overload Level	10% PER	-16.3	-	-	dBm
18 Mbps OFDM (g) RX Overload Level	10% PER	-16.3	-	-	dBm
36 Mbps OFDM (g) RX Overload Level	10% PER	-16.3	-	-	dBm
54 Mbps OFDM (g) RX Overload Level	10% PER	-16.3	-	-	dBm

[1] Up to 2 dB degradation at Channel 13 for 11g modes and up to 2 dB degradation at Channel 14 for 11b/g modes.

Table 16 WLAN Receiver RF Characteristics

DEVICE POWER-UP AND ENABLE

Normal operation mode requirements:

1. The MODE1 and MODE2 signals need to be shorted together.

The following sequence describes the device power-up from shutdown.

Normal operation power-up requirements:

1. Apply power to the module through the VCC input.
2. Wait for the module to power-up and stabilize (t1).
3. Enable the module through the PWR_EN input.
4. Wait for the module to start-up and be ready (t2).

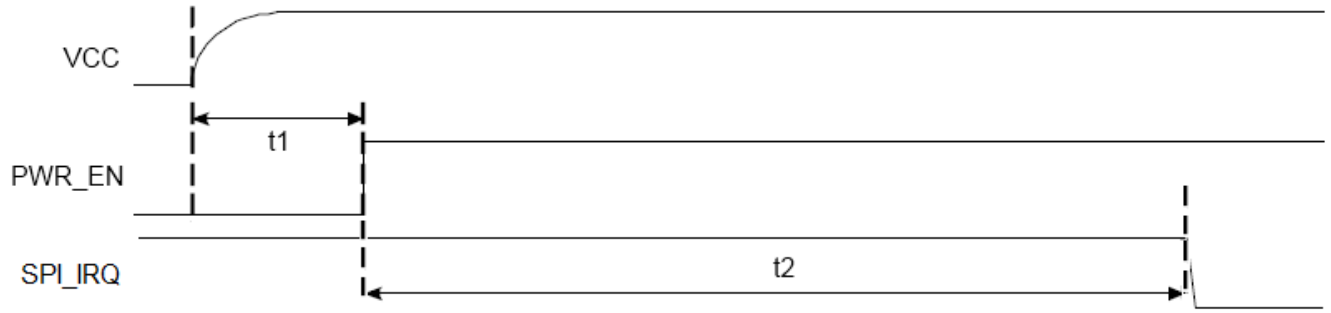


Figure 3 Device Power-Up Timing

Timing Parameter	Symbol	Max	Unit
VCC to PWR_EN	t1	1000	ms
PWR_EN to SPI_IRQ	t2	60	ms

Table 17 Device Power-Up Timing

DEVICE POWER-DOWN

Normal operation power-down requirements:

1. Disable the module through the PWR_EN input.
2. Remove power to the module through the VCC input.

SPI HOST CONTROLLER INTERFACE

The main interface to the TiWi-SL Module is a Serial Peripheral Interface (SPI).

This section describes the SPI Host Controller interface (HCI).

Overview

The SPI interface provides high-speed data transfer capability with low power consumption for mobile electronic devices. The SPI bus was designed to operate on a point-to-multipoint basis by providing a separate, active-low chip select (CS) per device.

Supported SPI Features

SPI supports the following features:

- Point-to-multipoint
- Supported clock rate = 0-26MHz
- The device interface is always an SPI Slave, host is always an SPI Master

SPI Interface Description

In order to facilitate a broad implementation, the protocol is half duplex and does not require simultaneous operation of data OUT (DO) and data IN (DI). All TI communication devices are slaves in this protocol, and all transactions are initiated by the host, as the SPI Master. The clock rate for each one of the connected devices may be different and configured per device.

Figure 4 illustrates the SPI interface signals; Table 18 describes the SPI interface signals.

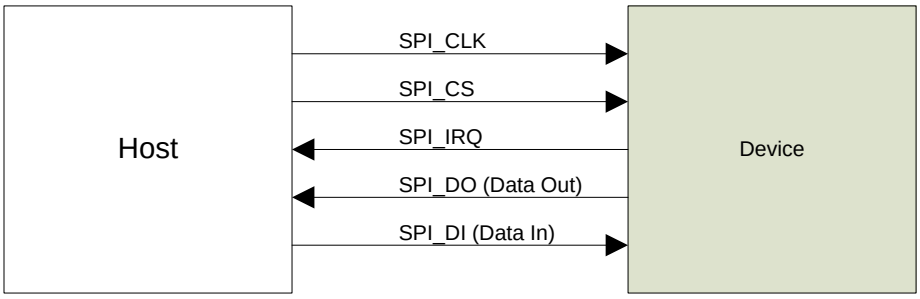


Figure 4 SPI Interface Signals

Port Name	Input/Output	Description
SPI_CLK	Input	Clock (0 MHz to 26MHz) from host to device
SPI_DI	Input	Data from host to device
SPI_CS	Input	CS signal from host to device
SPI_IRQ	Output	Interrupt from device to host
SPI_DO	Output	Data from device to host

Table 18 SPI Interface Signals Description

/CS and Bus Sharing Operation

The /CS line selects a specific device on the shared SPI bus. /CS is asserted at the beginning of an SPI transaction and de-asserted when the transaction completes; /CS must not be de-asserted during the transaction.

Bus sharing by multiple devices is implemented by asserting one /CS signal at a time and performing transactions with a specific device. Device multiplexing is performed on a transaction basis rather than on a byte or word basis.

SPI Transactions

NOTE:

The first command to be sent to the device requires special consideration. Refer to Section First Write Transaction for more details.

Write/Read Transactions

16-Bit Alignment

All data sent or received over the SPI interface are 16-bit aligned.

Write Operation: Host to Device Data Transfer

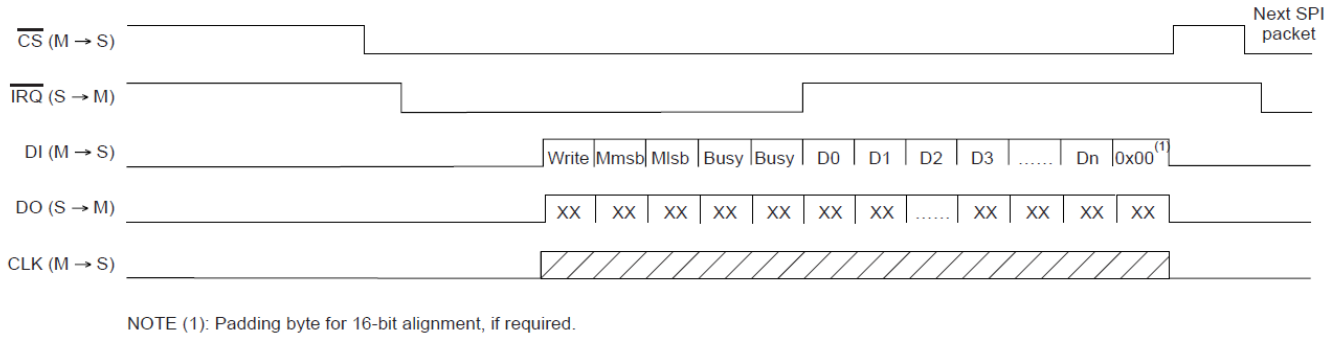


Figure 5 SPI Write Transaction

The host must assert /CS (that is, drive the signal to low) to indicate that it is about to write to the device. Consequently, the device will assert the /IRQ line when it is ready to receive the data and after completing its wake-up sequence. The host will wait for the /IRQ line to be asserted and then will start driving the data on the DI line. Data on the DI line consist of a 5-byte header followed by the data payload.

The first byte of the header is the WRITE opcode, followed by two bytes that indicate the size of the payload length (including the alignment byte). Two BUSY bytes will then follow to conclude the header. Directly following the last byte of the header will be the data payload.

When the device detects the HCI packet header, it de-asserts its /IRQ line during the packet data. When the host completes the SPI transaction, it must de-assert its /CS line.

SPI Header:

Write = Opcode for write is 0x01
MMSB, MLSB = 16-bit data payload length (including alignment byte)
Busy = Busy byte (0x00)

SPI Payload (equal to the HCI command + padding byte):

D(0) … D(n), 0x00 (depending on the number of bytes in SPI payload)
XX = Should be ignored by master

In order for the total SPI packet (that is, the SPI transaction) to be 16-bit aligned, the HCI command must be padded with an additional 0x00 byte if the HCI packet is even size. Refer to Table 19 for more information.

SPI Header	SPI Payload	Padding Byte
5 bytes	Odd	None
5 bytes	Even	0x00

Table 19 SPI Read/Write Transaction: 16-bit Alignment

The write transaction is performed according to the following parameters:

- A complete HCI packet must be included within every SPI transaction.
- Pausing and resuming the SPI clock: the host may stop driving the SPI CLK during the SPI packet. During this time, /CS will remain asserted. Upon resuming the SPI CLK the Host will *not* send the header again and will simply continue driving the data from the point it was previously stopped.
- The number of bytes for each SPI transaction is always even.
- The padding byte is added at the end of the HCI packet, but is not reflected in the HCI header length parameter (H4 packet length ignores this byte).
- The device ignores the additional byte.

First Write Transaction

The first write transaction to occur after release of the PWR_EN pin has a slightly different timing than the one shown in Figure 5. The normal SPI host write sequence is /CS low (host → device), followed by /IRQ low (device → host), indicating that the device is ready to accept data. However, after power-up, the sequence is slightly different, as Figure 6 illustrates.

After the release of the PWR_EN pin (indicated by (A) in Figure 6 below), the /IRQ line will assert (that is, go from high to low), as indicated by (B). The Host must wait for /IRQ to be low before asserting /CS, as noted by (C). The Host must then wait for at least 50 µs from the assertion of /CS (that is, 50 µs after /CS goes low) before sending the SPI packet.

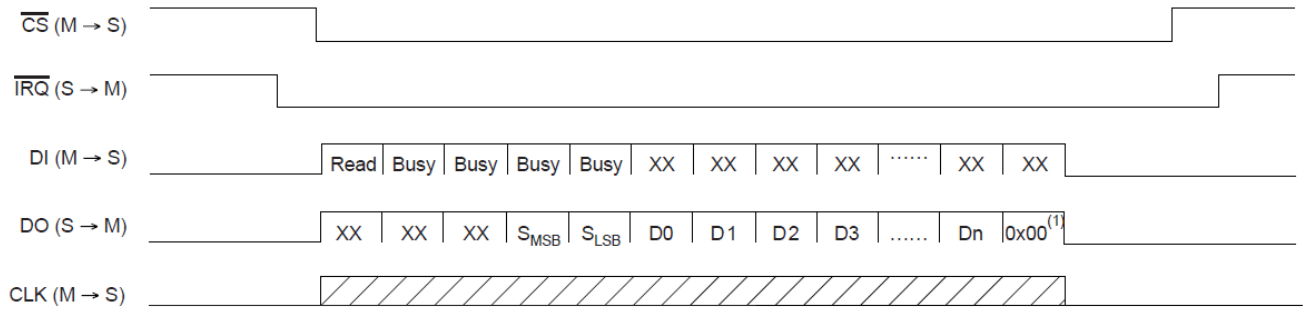
(A): See Fig3 for device power-up timing

(B) In addition, during this command the device performs its internal processing to switch to the required SPI mode. This processing requires an additional small amount of time. Therefore, for the first command only, a short delay is required after the first four bytes and before the following bytes. This delay must also be greater than 50 µs.

Figure 6 Write First Transaction

Read Operation: to Host Data Transfer

Figure 7 shows the SPI read transaction timing.



(1) Padding byte for 16-bit alignment, if required.

Figure 7 SPI Read Transaction

SPI Header:

Read = Opcode for write is 0x03
SMSB, SLSB = 16-bit data payload length (including alignment byte)
Busy = Busy byte (0x00)

SPI Payload (equal to the HCI command + padding byte):

D(0) … D(n), 0x00 (depending on the number of bytes in SPI payload)

In order for the total SPI packet (that is, the SPI transaction) to be 16-bit aligned, the HCI event sent from the device is padded with an additional 0x00 byte (if required). The device signals to the host its desire to transfer data by asserting the /IRQ line. The host asserts /CS and drives the following 3 bytes to DI line: READ opcode followed by two BUSY bytes. The device will then drive the data on the DO line. The first two bytes will indicate the payload length, and immediately after that, the data payload bytes will follow. Upon completing the read transaction, the host must de-assert /CS. The WLAN device then de-asserts its /IRQ line immediately as a response (within ≤ 250 ns).

NOTE

The host interrupt input should be set to trigger on high to low edge.

The read transaction is performed according to the following parameters:

- A single SPI read transaction includes a full HCI packet.
- The number of bytes for each SPI transaction will always be even.
- The padded byte is added at the end of the HCI packet, but is not reflected in the HCI header length parameter.
- The host should read a full SPI packet (including the alignment byte) according to the SPI packet length (SMSB and SLSB).
- **The host must ignore the additional byte according to the HCI packet length.**

Refer to Section “SPI Timing Information” for the SPI read and write timing diagrams.

Clock Polarity

Data is sampled on the falling edge of the clock as shown in Figure 9.

Shared SPI Bus Mode

This section describes the solution for a system in which the SPI host controller interfaces with other SPI-compatible devices.

The topology includes one SPI master and an SPI bus shared by several slaves. The bus topology has a single master (Host) and multiple slaves. The following lines are common to all SPI devices in the system:

- CLK
- Data IN
- Data OUT - when this line is shared between the different devices, it must be set to go to a 3-state output when /CS is de-asserted

Figure 8 illustrates the shared SPI bus architecture, depicting three devices as examples.

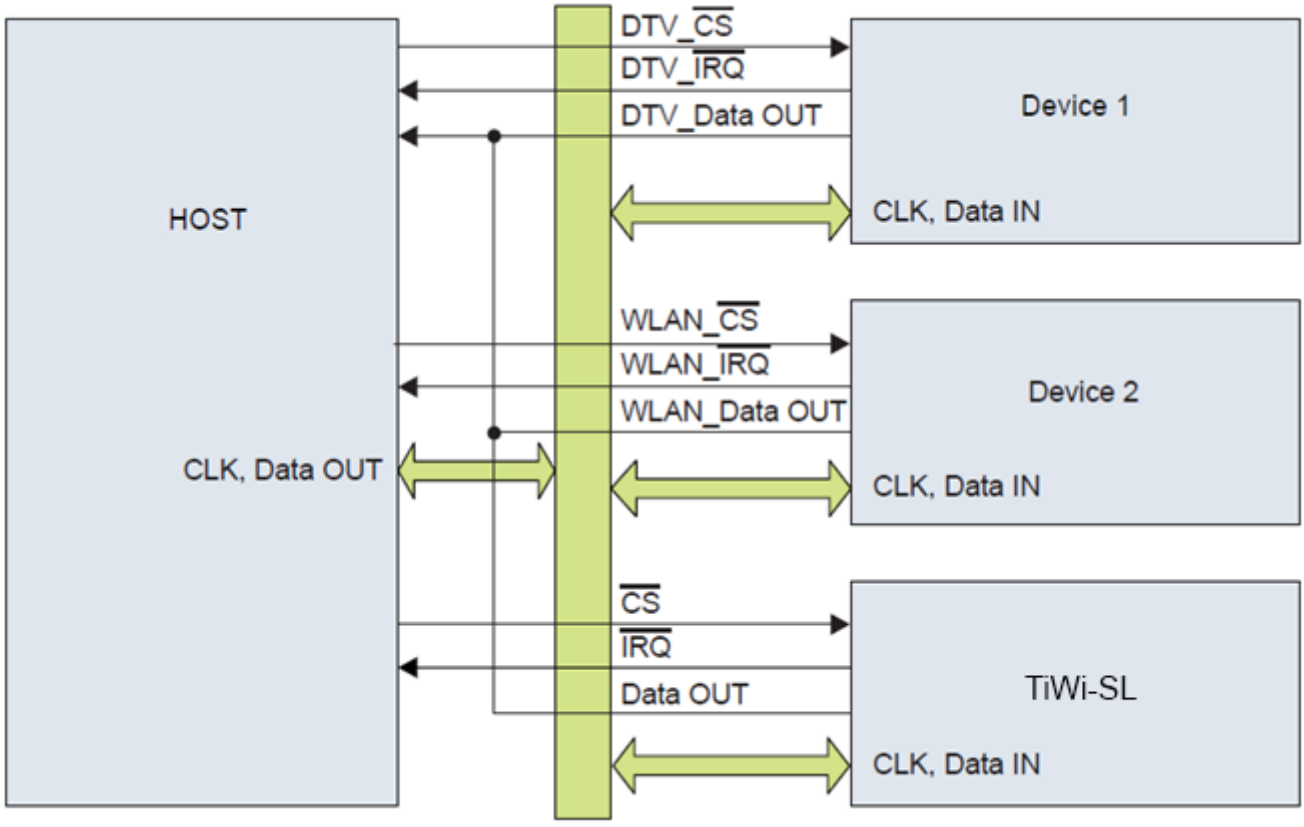


Figure 8 Shared SPI Bus Topology

SPI Timing Information

Figure 9 through Figure 11 show the SPI write and read timing sequences, respectively. Figure 11 is an expanded view of the first byte timing sequence for the SPI read header shown in Figure 10. Table 20 defines the SPI read/write timing parameters.

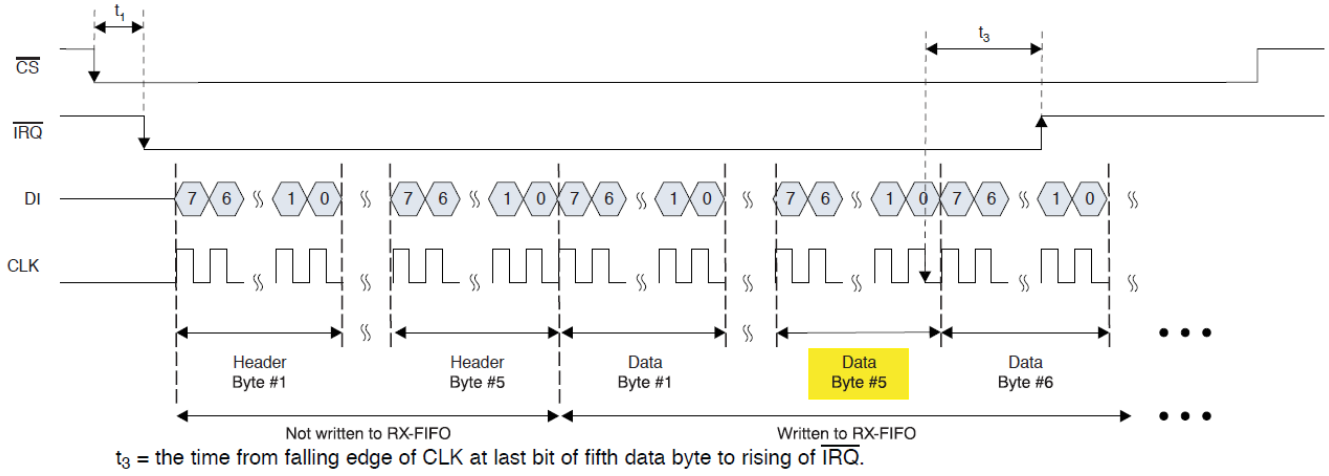


Figure 9 SPI Write Timing

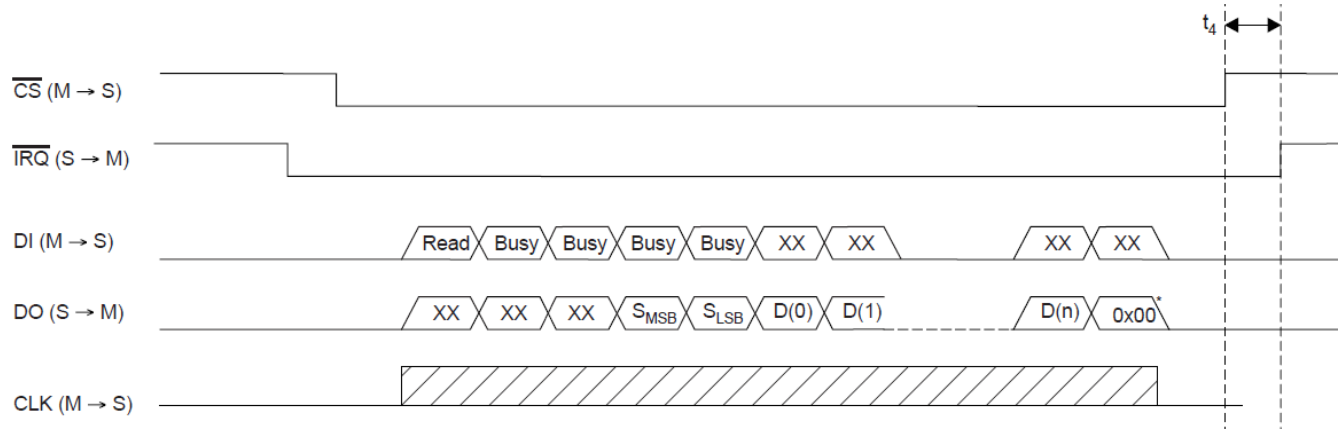


Figure 10 SPI Read Transaction

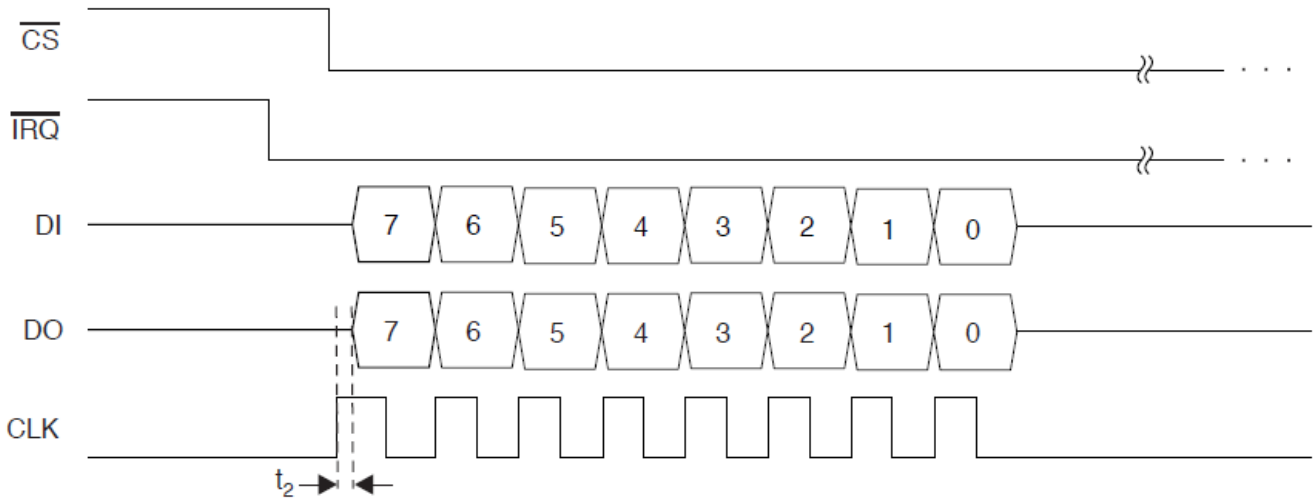


Figure 11 SPI Read Header: First Byte Timing

Time	Min	Typ	Max	Unit
t_1	83		375	ns
t_2	2.9		9.52	ns
t_3	666		2125	ns
t_4	83		375	ns

Table 20 SPI Read/Write Timing

SPI Clock Switching Characteristics

This interface supports single block reads and writes.

Parameter			Min	Max	Unit
f_{clock}	Clock frequency, CLK	$C_L \leq 15pF$	0	48	ns
DC	Low/high duty cycle	$C_L \leq 15pF$	40	60	ns
t_{TLH}	Rise time, CLK	$C_L \leq 15pF$		4.3	ns
t_{THL}	Fall time, CLK	$C_L \leq 15pF$		3.5	ns
t_{ISU}	Setup time, input valid before CLK↑	$C_L \leq 15pF$	3.5		ns
t_{IH}	Hold time, input valid after CLK↑	$C_L \leq 15pF$	5		ns
t_{ODLY}	Setup time, input valid before CLK↑	$C_L \leq 15pF$	4	15	ns
$t_{setupSPI\_CSx}$	CSn Delay time, CLK↑ to output invalid	$C_L \leq 15pF$	5.5		ns

Over recommended operating conditions (See Figure 12)

Table 21 SPI Clock Switching Characteristics

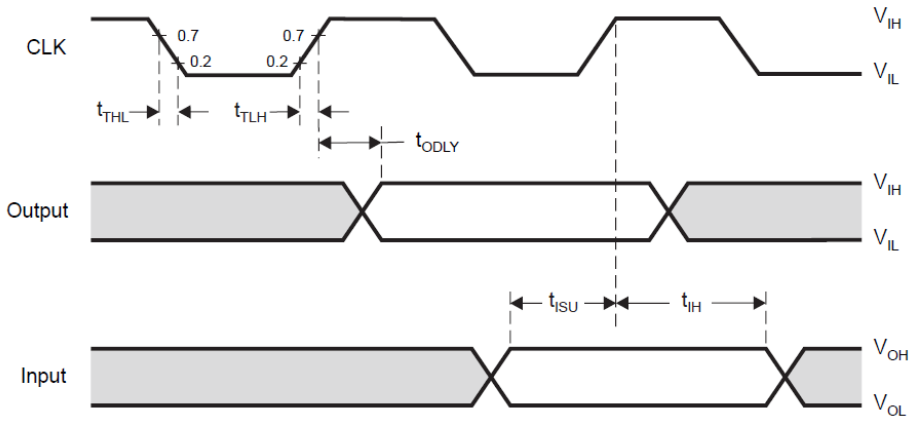
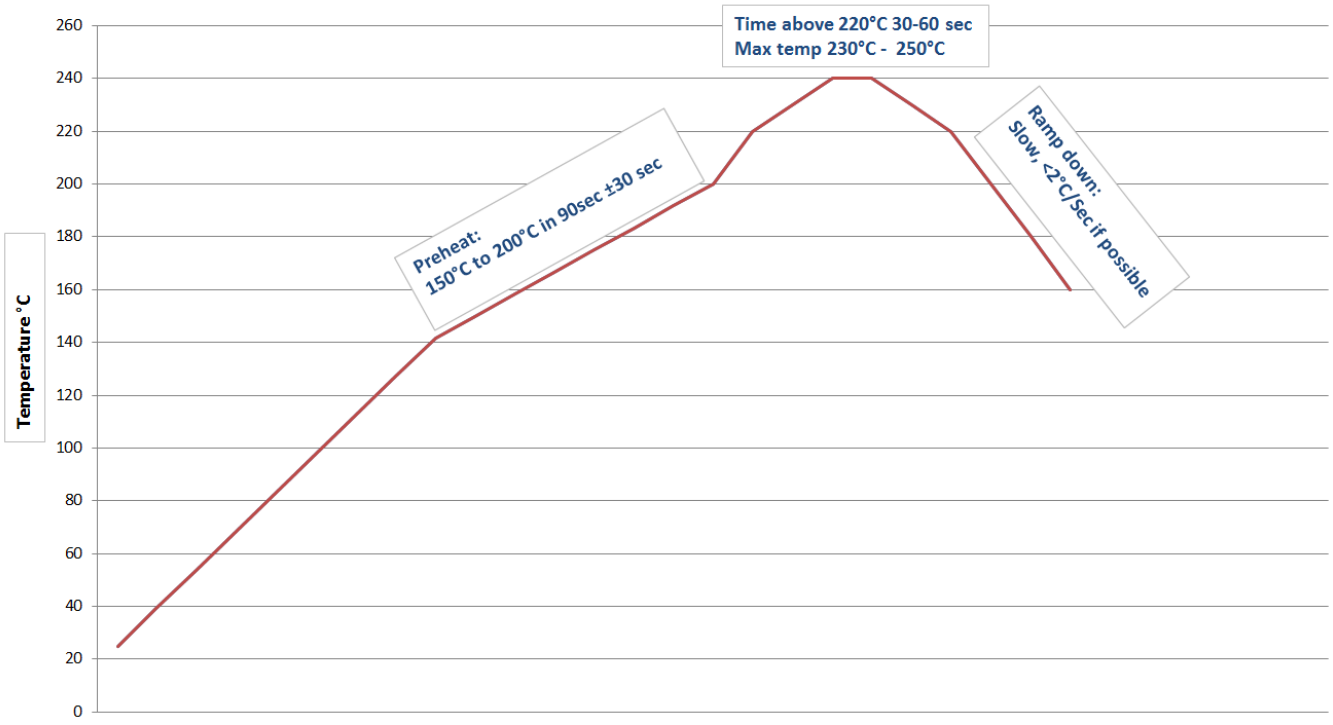


Figure 12 SPI Interface Clock Timing

SOLDERING RECOMMENDATIONS

Recommended Reflow Profile for Lead Free Solder



Note: The quality of solder joints on the surface mount pads where they contact the host board should meet the appropriate IPC Specification. See IPC-A-610-D Acceptability of Electronic Assemblies, section 8.2.1 "Bottom Only Terminations."

CLEANING

In general, cleaning the populated modules is strongly discouraged. Residuals under the module cannot be easily removed with any cleaning process.

- Cleaning with water can lead to capillary effects where water is absorbed into the gap between the host board and the module. The combination of soldering flux residuals and encapsulated water could lead to short circuits between neighboring pads. Water could also damage any stickers or labels.
- Cleaning with alcohol or a similar organic solvent will likely flood soldering flux residuals into the RF shield, which is not accessible for post-washing inspection. The solvent could also damage any stickers or labels.
- Ultrasonic cleaning could damage the module permanently.

OPTICAL INSPECTION

After soldering the Module to the host board, consider optical inspection to check the following:

- Proper alignment and centering of the module over the pads.
- Proper solder joints on all pads.
- Excessive solder or contacts to neighboring pads, or vias.

REWORK

The TiWi-SL module can be unsoldered from the host board. Use of a hot air rework tool and hot plate for pre-heating from underneath is recommended. Avoid overheating.

Never attempt a rework on the module itself, e.g. replacing individual components. Such actions will terminate warranty coverage.

SHIPPING, HANDLING, AND STORAGE

Shipping

Bulk orders of the TiWi-SL modules are delivered in trays of 50.

Handling

The TiWi-SL modules contain a highly sensitive electronic circuitry. Handling without proper ESD protection may destroy or damage the module permanently. ESD protection may destroy or damage the module permanently.

Moisture Sensitivity Level (MSL)

MSL 4, per J-STD-020

Devices not stored in a sealed bag with desiccant pack should be baked.

After opening devices that will be subjected to reflow must be mounted within 72 hours of factory conditions (<30°C and 60% RH) or stored at <10% RH.

Bake devices for 48 hours at 125°C.

Storage

Storage/shelf life in sealed bags is 12 months at <40°C and <90% relative humidity.

Repeating Reflow Soldering

Only a single reflow soldering process is encouraged for host boards.

AGENCY CERTIFICATIONS

FCC ID: TFB-TIWISL01, 15.247

IC ID: 5969A-TIWISL01, RSS 210

ETSI: The European Telecommunications Standards Institute. It produces the radio and communication standards for Europe. Our testing is to the ETSI standards EN 300 328 and EN 301 489, which are the portions of the relevant directives needed for a radio to obtain a CE mark.

AGENCY STATEMENTS

Federal Communication Commission Interference Statement

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

FCC CAUTION: Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

Industry Canada Statements

Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that permitted for successful communication.

This device has been designed to operate with the antenna(s) listed below, and having a maximum gain of 4.3 dBi (LSR Dipole) and 1.3dBi (Johanson Chip). Antennas not included in this list or having a gain greater than 4.3 dBi and 1.3dBi are strictly prohibited for use with this device. The required antenna impedance is 50 ohms.

List of all Antennas Acceptable for use with the Transmitter

1) LS Research 001-0001 center-fed dipole antenna and LS Research 080-0001 U.FL to Reverse Polarity SMA connector cable.
2) Johanson 2450AT43B100 chip antenna.

L'opération est soumise aux deux conditions suivantes: (1) cet appareil ne peut pas provoquer d'interférences et (2) cet appareil doit accepter toute interférence, y compris les interférences qui peuvent causer un mauvais fonctionnement de l'appareil.

Pour réduire le risque d'interférence aux autres utilisateurs, le type d'antenne et son gain doiventêtre choisis de manière que la puissance isotrope rayonnée équivalente (PIRE) ne dépasse pascelle permise pour une communication réussie.

Cet appareil a été conçu pour fonctionner avec l'antenne (s) ci-dessous, et ayant un gain maximum de 4,3 dBi (LSR dipôle) et1.3dBi (Chip Johanson). Antennes pas inclus danscette liste ou d'avoir un gain supérieur à 4,3 dBi et-1.3dBi sont strictement interdites pour l'utilisation avec cet appareil. L'impédance d'antenne requise est de 50 ohms.

Liste de toutes les antennes acceptables pour une utilisation avec l'émetteur

1) LS Research 001-0001 alimenté par le centre antenne dipôle et LS Research 080-0001 U.FL d'inversion de polarité du câble connecteur SMA.
2) Antenne Johanson puce 2450AT43B100.

OEM RESPONSIBILITIES TO COMPLY WITH FCC AND INDUSTRY CANADA REGULATIONS

The TiWi-SL Module has been certified for integration into products only by OEM integrators under the following conditions:

This device is granted for use in Mobile only configurations in which the antennas used for this transmitter must be installed to provide a separation distance of at least 20cm from all person and not be co-located with any other transmitters except in accordance with FCC and Industry Canada multi-transmitter product procedures.

As long as the two conditions above are met, further transmitter testing will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

IMPORTANT NOTE: In the event that these conditions cannot be met (for certain configurations or co-location with another transmitter), then the FCC and Industry Canada authorizations are no longer considered valid and the FCC ID and IC Certification Number cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC and Industry Canada authorization.

Le module de TiWi-SL a été certifié pour l'intégration dans des produits uniquement par des intégrateurs OEM dans les conditions suivantes:

Ce dispositif est accordé pour une utilisation dans des configurations mobiles seul dans lequel les antennes utilisées pour cet émetteur doit être installé pour fournir une distance de séparation d'au moins 20cm de toute personne et ne pas être colocalisés avec les autres émetteurs, sauf en conformité avec la FCC et de l'Industrie Canada, multi-émetteur procédures produit.

Tant que les deux conditions précitées sont réunies, les tests de transmetteurs supplémentaires ne seront pas tenus. Toutefois, l'intégrateur OEM est toujours responsable de tester leur produit final pour toutes les exigences de conformité supplémentaires requis avec ce module installé (par exemple, les émissions appareil numérique, les exigences de périphériques PC, etc.)

NOTE IMPORTANTE: Dans le cas où ces conditions ne peuvent être satisfaites (pour certaines configurations ou de co-implantation avec un autre émetteur), puis la FCC et Industrie autorisations Canada ne sont plus considérés comme valides et l'ID de la FCC et IC numéro de certification ne peut pas être utilisé sur la produit final. Dans ces circonstances, l'intégrateur OEM sera chargé de réévaluer le produit final (y compris l'émetteur) et l'obtention d'un distincte de la FCC et Industrie Canada l'autorisation.

OEM LABELING REQUIREMENTS FOR END-PRODUCT

The TiWi-SL module is labeled with its own FCC ID and IC Certification Number. The FCC ID and IC certification numbers are not visible when the module is installed inside another device, as such the end device into which the module is installed must display a label referring to the enclosed module. The final end product must be labeled in a visible area with the following:

"**Contains Transmitter Module FCC ID: TFB-TIWISL01"**

"**Contains Transmitter Module IC: 5969A-TIWISL01"**

or

"**Contains FCC ID: TFB-TIWISL01"**

"**Contains IC: 5969A-TIWISL01"**

The OEM of the TiWi-SL Module must only use the approved antenna(s) listed above, which have been certified with this module.

Le module de TiWi-SL est étiqueté avec son propre ID de la FCC et IC numéro de certification. L'ID de la FCC et IC numéros de certification ne sont pas visibles lorsque le module est installé à l'intérieur d'un autre appareil, comme par exemple le terminal dans lequel le module est installé doit afficher une etiquette faisant référence au module ci-joint. Le produit final doit être étiqueté dans un endroit visible par le suivant:

"Contient Module émetteur FCC ID: TFB-TIWISL01"
"Contient Module émetteur IC: 5969A-TIWISL01"

ou

"Contient FCC ID: TFB-TIWISL01"
"Contient IC: 5969A-TIWISL01"

Les OEM du module TiWi-SL ne doit utiliser l'antenne approuvée (s) ci-dessus, qui ont été certifiés avec ce module.

OEM END PRODUCT USER MANUAL STATEMENTS

The OEM integrator should not to provide information to the end user regarding how to install or remove this RF module or change RF related parameters in the user manual of the end product.

The user manual for the end product must include the following information in a prominent location:

This device is granted for use in Mobile only configurations in which the antennas used for this transmitter must be installed to provide a separation distance of at least 20cm from all person and not be co-located with any other transmitters except in accordance with FCC and Industry Canada multi-transmitter product procedures.

Other user manual statements may apply.

L'intégrateur OEM ne devraient pas fournir des informations à l'utilisateur final sur la façon d'installer ou de supprimer ce module RF ou modifier les paramètres liés RF dans le manuel utilisateur du produit final.

Le manuel d'utilisation pour le produit final doit comporter les informations suivantes dans unendroit bien en vue:

Ce dispositif est accordé pour une utilisation dans des configurations mobiles seule dans laquelle les antennes utilisées pour cet émetteur doit être installé pour fournir une distance de séparation d'au moins 20cm de toute personne et ne pas être co-localisés avec les autres émetteurs, sauf en conformité avec FCC et Industrie Canada, multi-émetteur procédures produit.

Autres déclarations manuel de l'utilisateur peuvent s'appliquer.

MECHANICAL DATA

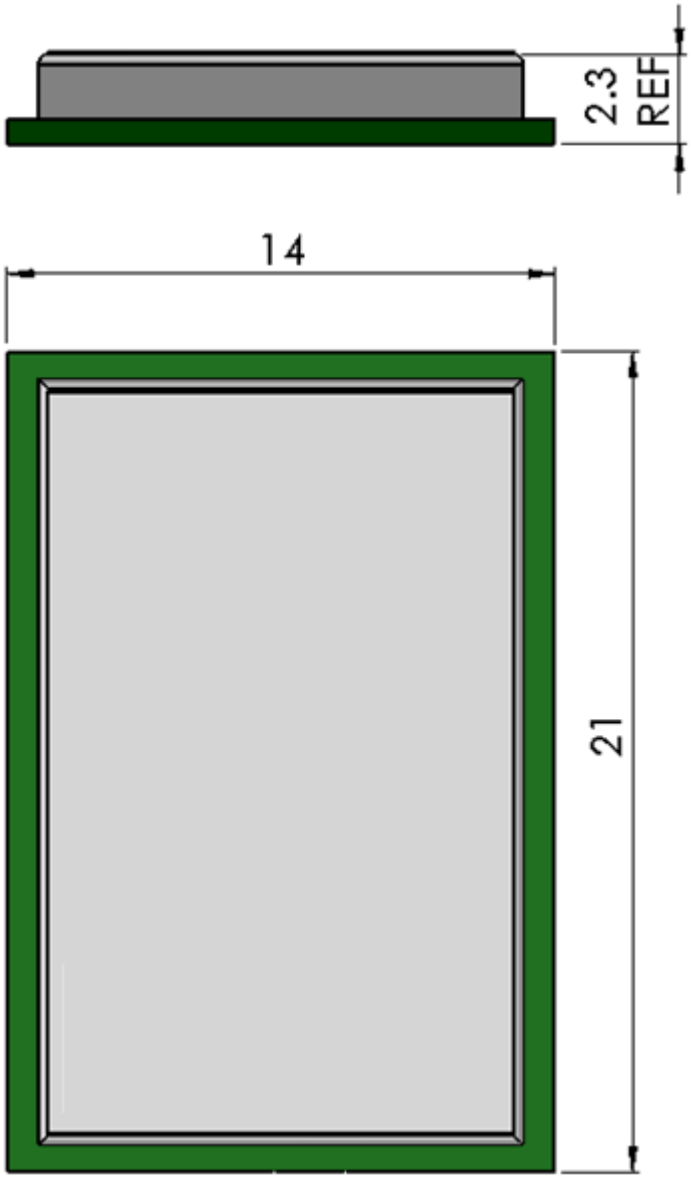


Figure 13 Module Mechanical Dimensions (Maximum Module Height = 2.4 mm)

PCB FOOTPRINT

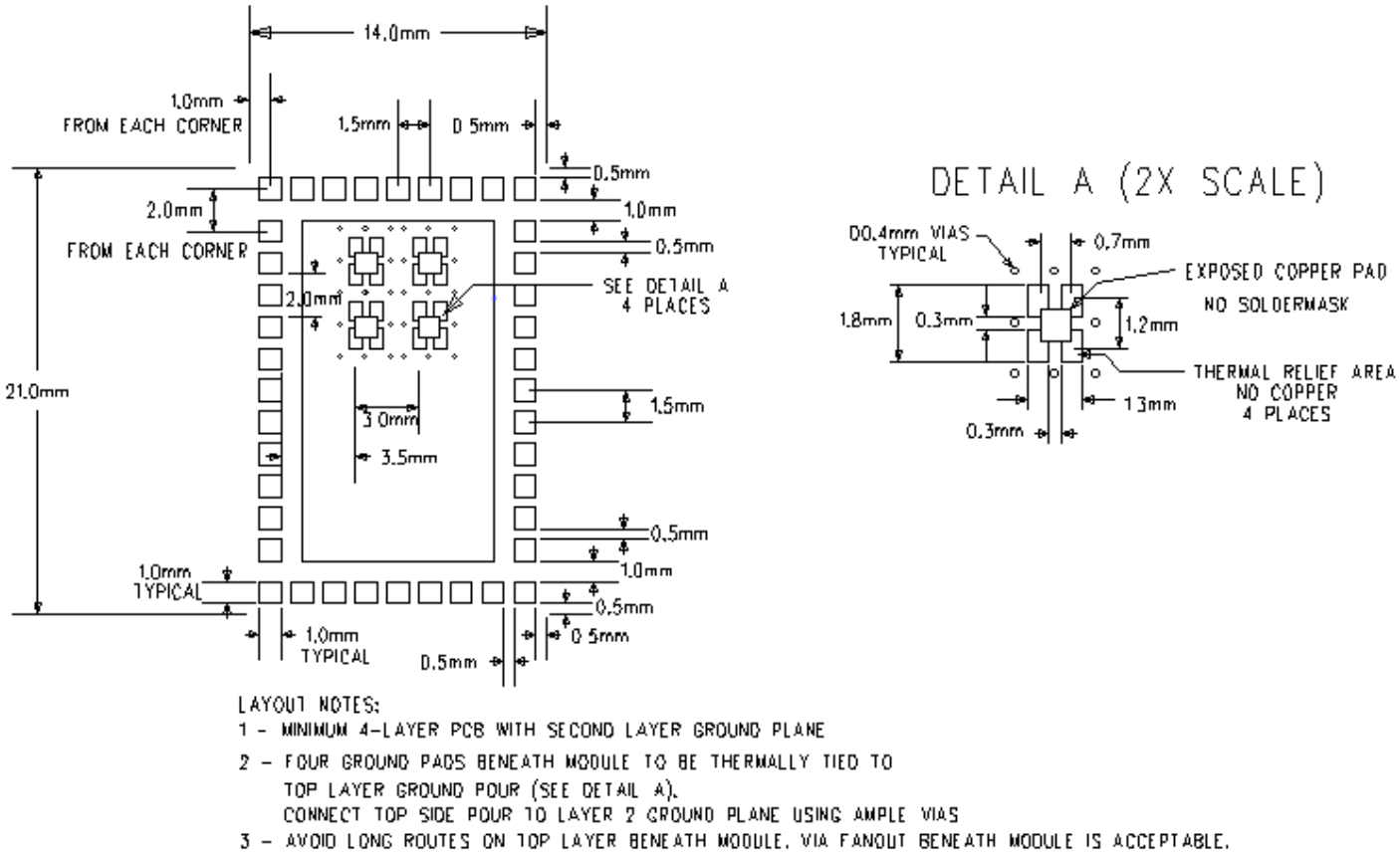


Figure 14 TiWi-SL Footprint

REFERENCE SCHEMATIC

The following reference schematic shows the recommend connections in an application circuit.

It is recommended that access to pins 7 and 9 (test UART transmit and receive respectively) and a ground be made available in the application circuit design. These signals can be used for low level RF testing and may be needed for end product test or compliance testing. Access to these signals could be as simple as test pads that could be soldered to, or with through holes to which a connector could be installed.

For circuit requirements regarding the pre-certified antenna options that work with the TiWi-SL module, refer to the TiWi-SL Antenna Design Guide.

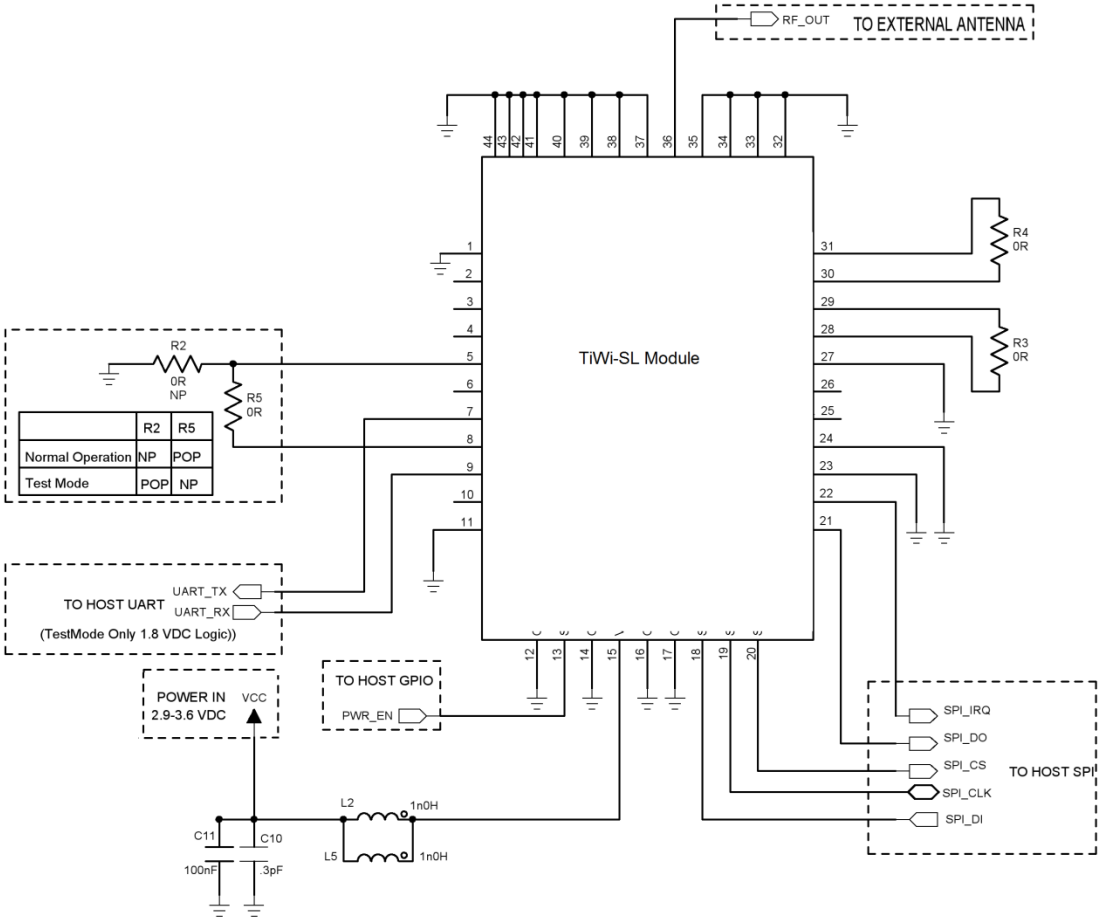
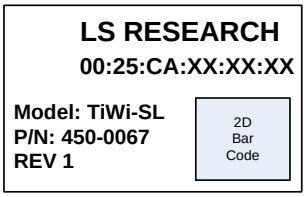


Figure 13 TiWi-SL Reference Schematic

DEVICE MARKINGS

Rev 1 Devices

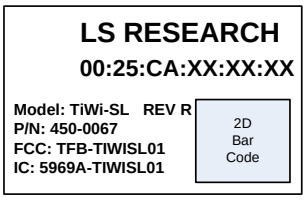
CC3000: CC3000BYFVR
Front End: TQM679002A



02:25:CA:XX:XX:XX = MAC ID
2D Barcode Format is Data Matrix Standard
XX:XX:XX = unique portion of MAC ID that changes for each module

Rev 2 and Rev 3 Devices

CC3000: CC3000BYFVR
Front End: TQM679002A



R = Revision 2 or 3
02:25:CA:XX:XX:XX = MAC ID
2D Barcode Format is Data Matrix Standard
XX:XX:XX = unique portion of MAC ID that changes for each module

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