19-4117; Rev 1; 4/09

EVALUATION KIT AVAILABLE

# Hi-Speed USB-to-SD Card Readers with Bypass



## General Description

The MAX14500–MAX14503 USB-to-SD™ card readers provide a means for portable devices that support full-speed USB communication (12Mbps) with one or two SD card slots, upgrading the USB SD card reader function to USB Hi-Speed (480Mbps) operation. The MAX14500–MAX14503 have two modes of operation: Pass Thru and Card Reader. In pass thru, the SD and USB signals pass through the MAX14500–MAX14503 without modification, appearing like the device is not present. The host microprocessor firmware does not need modification, as there is no change from the host microprocessor's perspective. In Card Reader mode, the MAX14500–MAX14503 implement a Hi-Speed USB card reader that operates independently of the host microprocessor. All the capabilities of the full-speed USB port and SD card slot are preserved with the additional feature that allows a faster way for a PC to read or write to the SD card. The MAX14500–MAX14503 support SD high capacity SDHC cards. The 40-pin TQFN version supports one SD card, while the 56-bump WLP version supports two SD cards.

The MAX14500–MAX14503 feature advanced power-saving modes to reduce power consumption in portable applications. The low-power Sleep modes allow the ability to disable internal circuit blocks, providing power-saving operating modes. The default clock input for each part number is specified in the ordering information. The MAX14500–MAX14503 feature the option to change the default values using the I²C interface.

The MAX14500–MAX14503 are available in 5mm x 5mm, 40-pin TQFN, and 3.23mm x 3.5mm, 56-bump WLP packages. These devices operate over a wide supply voltage range and are specified over the -40°C to +85°C extended temperature range.

## Applications

Cell Phones

PDAs

MP3 Players

Digital Still Cameras

GPS

## Features

- ♦ **USB 2.0 Hi-Speed and Full-Speed Compliant**
- ♦ **SDHC Card Support**
- ♦ **Internal Hi-Speed USB SD Card Reader Eases Host µP Overhead**
- ♦ **On-Chip Termination and Pullup Resistors**
- ♦ **Internal SD Switches Allow For Multiplexing Two SD Cards on a Single-Microprocessor SD Port**
- ♦ **Accommodates Clock Input Frequencies 26MHz, 19.2MHz, 13MHz, and 12MHz**
- ♦ **Internal Clock Squarer for Low-Amplitude TCXO Signals**
- ♦ **No Power-Supply Sequencing Required**
- ♦ **Compatible with +1.8V to +3.3V I/O Host Microprocessor**
- ♦ **Simple Control Mode Requires Only a Single GPIO**
- ♦ **I²C Control Provides Multiple Configuration Options**
- ♦ **I²C Control Required for Two SD Cards**
- ♦ **On-Chip Power-On Reset/Brown-Out Reset**

## Ordering Information/ Selector Guide

| PART | INPUT FREQUENCY (MHz) | SD CARDS | PIN-PACKAGE |
|---|---|---|---|
| **MAX14500**ETL+* | 12 | 1 | 40 TQFN-EP** |
| MAX14500AEWN+* | 12 | 2 | 56 WLP |
| **MAX14501**ETL+* | 13 | 1 | 40 TQFN-EP** |
| MAX14501AEWN+* | 13 | 2 | 56 WLP |
| **MAX14502**AETL+ | 19.2 | 1 | 40 TQFN-EP** |
| MAX14502AEWN+* | 19.2 | 2 | 56 WLP |
| **MAX14503**ETL+* | 26 | 1 | 40 TQFN-EP** |
| MAX14503AEWN+* | 26 | 2 | 56 WLP |

***Note:*** *All devices are specified over the -40°C to +85°C operating temperature range.*
*+Denotes a lead(Pb)-free/RoHS-compliant package.*
**Future product—contact factory for availability.*
***EP = Exposed pad.*

*SD is a trademark of the SD Card Association.*

# Hi-Speed USB-to-SD Card Readers with Bypass

## ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)

$V_{CC}$ .....-0.3V to +4V
$V_{SD}$ .....-0.3V to +4V
$V_{IO}$ .....-0.3V to +4V
$V_{TM}$ .....-0.3V to +4V
KVBUS.....-0.3V to +4V
CLDO.....-0.3V to +2V
CDAT1_[3:0], HDAT1_[3:0], CCMD1, HCMD1, CCLK1, HCLK1, CCRD_PRST, HCRD_PRST, CDAT2_[3:0], HDAT2_[3:0], CCMD2, HCMD2, CCLK2, HCLK2 .....-0.3V to ($V_{SD}$ + 0.3V)
$\overline{BUSY}$, $\overline{BERR}$/INT, MODE, SCL, SDA, I2C_SEL, ADD, $\overline{RST}$.....-0.3V to ($V_{IO}$ + 0.3V)
CD+, CD-, HD+, HD-, RREF, FREF .....-0.3V to ($V_{TM}$ + 0.3V)
Continuous Power Dissipation ($T_A$ = +70°C)
40-Pin TQFN (derate 35.7mW/°C above +70°C) .....2857mW
Junction-to-Case Thermal Resistance ($\theta_{JC}$) (Note 1)
40-Pin TQFN .....1.7°C/W
Junction-to-Ambient Thermal Resistance ($\theta_{JA}$) (Note 1)
40-Pin TQFN .....28°C/W
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10s) .....+300°C

**Note 1:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

($V_{CC}$ = +2.4V to +3.6V, $V_{SD}$ = +2.4V to +3.6V, $V_{IO}$ = +1.5V to +3.6V, $V_{TM}$ = +2.91V to +3.4V, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{CC}$ = +3.3V, $V_{IO}$ = +2.5V, $V_{SD}$ = +2.5V, $V_{TM}$ = +3.3V, $T_A$ = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **DC CHARACTERISTICS** | | | | | | |
| $V_{CC}$ Supply Voltage | $V_{CC}$ | Pass thru | 2.1 | | 3.6 | V |
| | | Card reader active, $f_{CCLK\_} \le 26MHz$ | 2.1 | | 3.6 | |
| | | Card reader active, $f_{CCLK\_} > 26MHz$ | 2.4 | | 3.6 | |
| $V_{SD}$ Supply Voltage | $V_{SD}$ | Pass thru | 2.0 | | 3.6 | V |
| | | Card reader active, $f_{CCLK\_} \le 26MHz$ | 2.0 | | 3.6 | |
| | | Card reader active, $f_{CCLK\_} > 26MHz$ | 2.4 | | 3.6 | |
| Logic Interface Supply Voltage | $V_{IO}$ | | 1.5 | | 3.6 | V |
| USB Supply Voltage | $V_{TM}$ | | 2.91 | | 3.4 | V |
| Digital Core LDO Regulator Output Voltage | $V_{CLDO}$ | $C_{CLDO}$ = 1.0µF | | 1.8 | | V |
| $V_{CC}$ Supply Current | $I_{CC}$ | Pass thru | | 5 | 15 | µA |
| | | Card reader active | | 35 | 50 | mA |
| $V_{SD}$ Supply Current | $I_{SD}$ | Pass thru | | 17 | 40 | µA |
| | | Card reader active | | 3 | | mA |
| $V_{IO}$ Supply Current | $I_{IO}$ | Pass thru | | 2 | 10 | µA |
| | | Card reader active | | 0.2 | | mA |
| $V_{TM}$ Supply Current | $I_{TM}$ | Pass thru | | 13 | 50 | µA |
| | | Card reader active | | 25 | | mA |
| $V_{SD}$ Comparator Threshold | $V_{SDCT}$ | | 1.0 | 1.5 | 1.9 | V |
| $V_{TM}$ Comparator Threshold | $V_{TMCT}$ | | 2.0 | 2.5 | 2.9 | V |
| MODE, I2C_SEL, ADD, $\overline{RST}$ Input-Voltage Low | $V_{IL}$ | | | | 0.4 | V |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = +2.4V to +3.6V, $V_{SD}$ = +2.4V to +3.6V, $V_{IO}$ = +1.5V to +3.6V, $V_{TM}$ = +2.91V to +3.4V, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{CC}$ = +3.3V, $V_{IO}$ = +2.5V, $V_{SD}$ = +2.5V, $V_{TM}$ = +3.3V, $T_A$ = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| MODE, I2C_SEL, ADD, $\overline{RST}$ Input-Voltage High | $V_{IH}$ | | 2/3 x $V_{IO}$ | | | V |
| $\overline{BUSY}$, $\overline{BERR}$/INT Output-Voltage Low | $V_{OL}$ | $I_{LOAD}$ = 1mA | | | 0.4 | V |
| $\overline{BUSY}$, $\overline{BERR}$/INT Output-Voltage High | $V_{OH}$ | $I_{LOAD}$ = -1mA | $V_{IO}$ - 0.4 | | | V |
| I2C_SEL, ADD, $\overline{RST}$ Input Leakage Current | $I_{IL}$ | | -1 | | +1 | µA |
| MODE Input Resistance to GND | $R_{MODE}$ | | 150 | 300 | 500 | kΩ |
| FREF Full-Swing Input-Voltage High | $V_{IH}$ | | 1.3 | | | V |
| FREF Full-Swing Input-Voltage Low | $V_{IL}$ | | | | 0.4 | V |
| FREF Low-Amplitude Input-Voltage Low | $V_{IL}$ | | 200 | | | mV |
| FREF Input Leakage Current | $I_{ILF}$ | Full-Swing mode | -10 | | +10 | µA |
| FREF Input Resistance | | Low-Amplitude input mode | | 1 | | MΩ |
| KVBUS Comparator Threshold | $V_{TH}$ | | 1.0 | 1.25 | 1.5 | V |
| KVBUS Comparator Hysteresis | $V_{HYS}$ | | | 20 | | mV |
| KVBUS Comparator Input Impedance | $R_{IN}$ | | 10 | | | MΩ |
| SDA/SCL Input Low Voltage | $V_{IL\_I2C}$ | | | | 0.3 x $V_{IO}$ | V |
| SDA/SCL Input High Voltage | $V_{IH\_I2C}$ | | 0.7 x $V_{IO}$ | | | V |
| SDA Output Logic-Low | $V_{OL\_I2C}$ | $V_{IO}$ > +2V, 3mA sink current | 0 | | 0.4 | V |
| | | $V_{IO}$ ≤ +2V, 3mA sink current | 0 | | 0.2 x $V_{IO}$ | |
| SDA/SCL Input Leakage Current | $I_{IN\_I2C}$ | | -10 | | +10 | µA |
| **SD CARD INTERFACE** | | | | | | |
| On-Resistance | $R_{ON}$ | $V_{TEST}$ = 0 or $V_{SD}$, $I_{TEST}$ = 10mA (Note 3) | | 10 | | Ω |
| Off-Leakage Current | $I_{ILSD}$ | $V_{TEST}$ = 0 or $V_{SD}$ (Note 3) | -1 | | +1 | µA |
| Off-Capacitance | $C_{SD\_OFF}$ | (Note 4) | | 5 | | pF |
| On-Capacitance | $C_{SD\_ON}$ | (Note 5) | | 10 | | pF |
| Pullup Resistance | $R_{PU}$ | CCMD1, CCMD2, CDAT1_[3:0], CDAT2_[3:0] | 50 | 75 | 100 | kΩ |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -100µA | 0.75 x $V_{SD}$ | | | V |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 100µA | | | 0.125 x $V_{SD}$ | V |

# Hi-Speed USB-to-SD Card Readers with Bypass

## ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = +2.4V to +3.6V, $V_{SD}$ = +2.4V to +3.6V, $V_{IO}$ = +1.5V to +3.6V, $V_{TM}$ = +2.91V to +3.4V, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{CC}$ = +3.3V, $V_{IO}$ = +2.5V, $V_{SD}$ = +2.5V, $V_{TM}$ = +3.3V, $T_A$ = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Input High Voltage | $V_{IH}$ | $V_{SD}$ < 2.4V | 0.8 x $V_{SD}$ | | | V |
| | | $V_{SD}$ ≥ 2.4V | 0.625 x $V_{SD}$ | | | |
| Input Low Voltage | $V_{IL}$ | $V_{SD}$ < 2.4V | | | 0.2 x $V_{SD}$ | V |
| | | $V_{SD}$ ≥ 2.4V | | | 0.25 x $V_{SD}$ | |
| **USB INTERFACE** | | | | | | |
| On-Resistance | $R_{ON}$ | $V_{CD\_}$ = 0 or $V_{TM}$, switch closed | | 5 | | Ω |
| On-Resistance Flatness | $R_{ONFLAT}$ | $V_{CD\_}$ = 0 to 3.3V, $V_{TM}$ = +3.3V | | 2 | | Ω |
| On-Capacitance | $C_{ON\_USB}$ | Switch closed, measured from CD+ and CD- | | 12 | | pF |
| Off-Capacitance | $C_{OFF\_USB}$ | Switch open, measured from CD+, CD-, HD+, HD- | | 6 | | pF |
| **AC CHARACTERISTICS (Note 6)** | | | | | | |
| **SD CARD CLOCK TIMING (CCLK_), DEFAULT SPEED (Figure 5a)** | | | | | | |
| Clock Low Time | $t_{WL}$ | $C_L$ = 10pF | 19 | | | ns |
| Clock High Time | $t_{WH}$ | $C_L$ = 10pF | 19 | | | ns |
| Clock Rise Time | $t_{TLH}$ | $C_L$ = 10pF | | | 10 | ns |
| Clock Fall Time | $t_{THL}$ | $C_L$ = 10pF | | | 10 | ns |
| **SD CARD CLOCK TIMING (CCLK_), HI-SPEED (Figure 5b)** | | | | | | |
| Clock Low Time | $t_{WL}$ | $C_L$ = 40pF | 7 | | | ns |
| Clock High Time | $t_{WH}$ | $C_L$ = 40pF | 7 | | | ns |
| Clock Rise Time | $t_{TLH}$ | $C_L$ = 40pF | | | 3 | ns |
| Clock Fall Time | $t_{THL}$ | $C_L$ = 40pF | | | 3 | ns |
| **SD CARD COMMAND TIMING (CCMD1, CCMD2) (Figure 5b)** | | | | | | |
| Input Setup Time | $t_{ISU}$ | | 5 | | | ns |
| Input Hold Time | $t_{IH}$ | | 2 | | | ns |
| Output Delay Time During Data Transfer Mode | $t_{ODLY}$ | | | | 14 | ns |
| Output Hold Time | $t_{OH}$ | | 2.5 | | | ns |
| **I²C CHARACTERISTICS** | | | | | | |
| SCL Clock Frequency | $f_{SCL}$ | | | | 400 | kHz |
| SDA, SCL Capacitance | $C_{IO\_I2C}$ | | | 5 | | pF |
| SDA Output Fall Time | $t_{OF\_I2C}$ | | | | 250 | ns |
| Hold Time After Repeated START | $t_{HD,STA}$ | | 0.6 | | | µs |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = +2.4V to +3.6V, $V_{SD}$ = +2.4V to +3.6V, $V_{IO}$ = +1.5V to +3.6V, $V_{TM}$ = +2.91V to +3.4V, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{CC}$ = +3.3V, $V_{IO}$ = +2.5V, $V_{SD}$ = +2.5V, $V_{TM}$ = +3.3V, $T_A$ = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Clock Low Period | $t_{LOW\_I2C}$ | | 1.3 | | | µs |
| Clock High Period | $t_{HIGH\_I2C}$ | | 0.6 | | | µs |
| Setup Time for Repeated START | $t_{SU,STA}$ | | 0.6 | | | µs |
| Hold Time for Data | $t_{HD,DAT}$ | | | 0 | 0.9 | µs |
| Setup Time for Data | $t_{SU,DAT}$ | | 100 | | | ns |
| SDA/SCL Input Fall Time | $t_{F\_I2C}$ | | | | 300 | ns |
| SDA/SCL Rise Time | $t_{R\_I2C}$ | | | | 300 | ns |
| Setup Time for STOP | $t_{SU,STO}$ | | 0.6 | | | µs |
| Bus Free Time Between STOP and START | $t_{BUF}$ | | 1.3 | | | µs |

## USB HI-SPEED SOURCE ELECTRICAL CHARACTERISTICS

($V_{CC}$ = +2.4V to +3.6V, $V_{SD}$ = +2.4V to +3.6V, $V_{IO}$ = +1.5V to +3.6V, $V_{TM}$ = +2.91V to +3.4V, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{CC}$ = +3.3V, $V_{IO}$ = +2.5V, $V_{SD}$ = +2.5V, $V_{TM}$ = +3.3V, $T_A$ = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **DC CHARACTERISTICS** | | | | | | |
| Hi-Speed Squelch Detection Threshold (Diff Signal Amplitude) | $V_{HSSQ}$ | (Note 6) | 100 | | 150 | mV |
| Hi-Speed Differential Input Signaling Levels | $V_{IL}$ | Specified by Hi-Speed receive eye diagram | | | | |
| Hi-Speed Data Signaling Common-Mode Voltage Range | SCM | (Note 6) | -50 | | +500 | mV |
| Hi-Speed Idle Level | $V_{HSOI}$ | | -10 | | +10 | mV |
| Hi-Speed Data Signaling High | $V_{HSOH}$ | | 360 | | 440 | mV |
| Hi-Speed Data Signaling Low | $V_{HSOL}$ | | -10 | | +10 | mV |
| Chirp J Level (Differential Voltage) | $V_{CHIRPJ}$ | | 700 | | 1100 | mV |
| Chirp K Level (Differential Voltage) | $V_{CHIRPK}$ | | -900 | | -500 | mV |
| Termination Voltage (Hi-Speed) | $V_{HSTERM}$ | | -10 | | +10 | mV |
| **AC CHARACTERISTICS** | | | | | | |
| Rise Time | $t_{HSR}$ | (Note 6) | 500 | | | ps |
| Fall Time | $t_{HSF}$ | (Note 6) | 500 | | | ps |
| Driver Waveform Requirements | | Specified by Hi-Speed transmit eye diagram | See the *Typical Operating Characteristics* section | | | |
| Driver-Output Resistance | $Z_{HSDRV}$ | | 40.5 | | 49.5 | Ω |
| Source Jitter Total (Including Frequency Tolerance) | | Specified by Hi-Speed transmit eye diagram | See the *Typical Operating Characteristics* section | | | |

# Hi-Speed USB-to-SD Card Readers with Bypass

## USB FULL-SPEED SOURCE ELECTRICAL CHARACTERISTICS

($V_{CC}$ = +2.4V to +3.6V, $V_{SD}$ = +2.4V to +3.6V, $V_{IO}$ = +1.5V to +3.6V, $V_{TM}$ = +2.91V to +3.4V, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{CC}$ = +3.3V, $V_{IO}$ = +2.5V, $V_{SD}$ = +2.5V, $V_{TM}$ = +3.3V, $T_A$ = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **DC CHARACTERISTICS** | | | | | | |
| SE Receiver Input High | $V_{IH}$ | | 2.0 | | | V |
| SE Receiver Input Low | $V_{IL}$ | | | | 0.8 | V |
| Differential Common-Mode Voltage | $V_{CM}$ | | 0.8 | | 2.0 | V |
| Receiver Differential Input Sensitivity | $V_{DI}$ | | 0.2 | | | V |
| Transmitter High | $V_{OH}$ | $R_L$ = 15kΩ connected to GND | 2.8 | | 3.6 | V |
| Transmitter Low | $V_{OL}$ | $R_L$ = 1.5kΩ connected to 3.3V | 0 | | 0.3 | V |
| Transmitter Output Signal Crossover Voltage | $V_{CRS}$ | (Note 6) | 1.3 | | 2.0 | V |
| Bus Pullup Resistor on Upstream Facing Port (Idle Bus) | $R_{PUI}$ | | 0.900 | 1.25 | 1.575 | kΩ |
| Bus Pullup Resistor on Upstream Facing Port (Upstream Port Receiving) | $R_{PUA}$ | | 1.425 | 2.5 | 3.090 | kΩ |
| Input Impedance | $Z_{INP}$ | | 300 | | | kΩ |
| Termination Voltage for Upstream Facing Port Pullup ($R_{PU}$) | $V_{TERM}$ | | | $V_{TM}$ | | V |
| **AC CHARACTERISTICS** | | | | | | |
| Rise Time | $t_{FR}$ | | 4 | | 20 | ns |
| Fall Time | $t_{FF}$ | | 4 | | 20 | ns |
| Differential Rise and Fall Time Matching | $t_{FRFM}$ | (Note 6) | 90 | | 111.11 | % |
| Full-Speed Data Rate | $t_{FDRATHS}$ | | 11.994 | | 12.030 | Mbps |

**Note 2:** All parameters are tested at $T_A$ = +25°C. Specifications over temperature are guaranteed by design.

**Note 3:** On-resistance is measured by applying voltage and current on the SD card interface (CCLK1, CCMD1, CDAT1_[3:0], CCLK2, CCMD2, CDAT2_[3:0]).

**Note 4:** Off-capacitance measured with SD switch open (CCLK1, HCLK1, CCMD1, HCMD1, CDAT1_[3:0], HDAT1_[3:0], CCLK2, HCLK2, CCMD2, HCMD2, CDAT2_[3:0], HDAT2_[3:0]).

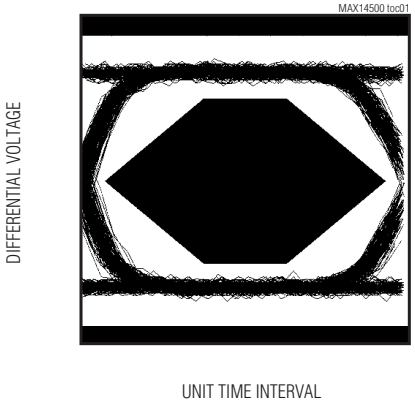
**Note 5:** On-capacitance measured on SD card side (CCLK1, CCMD1, CDAT1_[3:0], CCLK2, CCMD2, CDAT2_[3:0]).

**Note 6:** Specifications guaranteed by design.

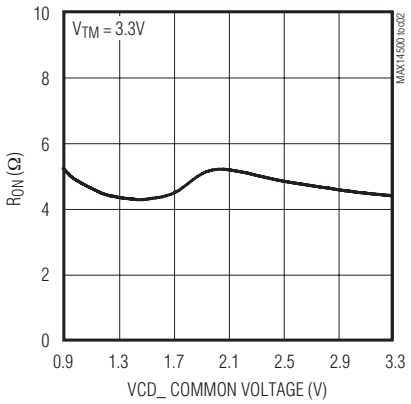
## Typical Operating Characteristics

($V_{CC}$ = +3.3V, $V_{IO}$ = +2.5V, $V_{SD}$ = +2.5V, $V_{TM}$ = +3.3V, $T_A$ = +25°C, unless otherwise noted.)

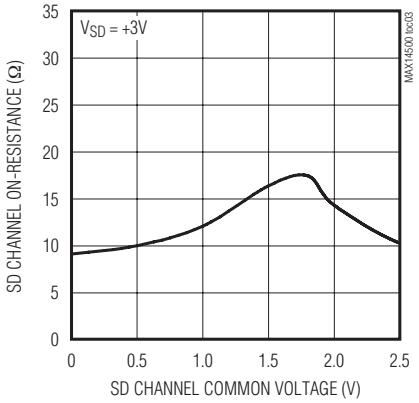
**HI-SPEED EYE DIAGRAM FOR CARD READER MODE**



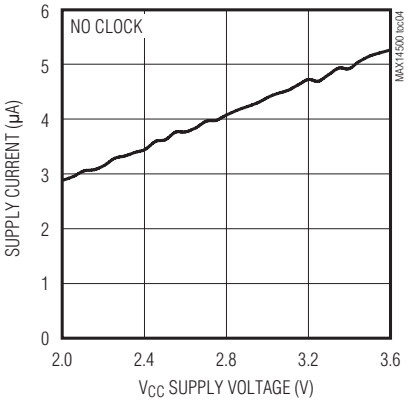

**USB ON-RESISTANCE vs. USB COMMON VOLTAGE (VCD_)**



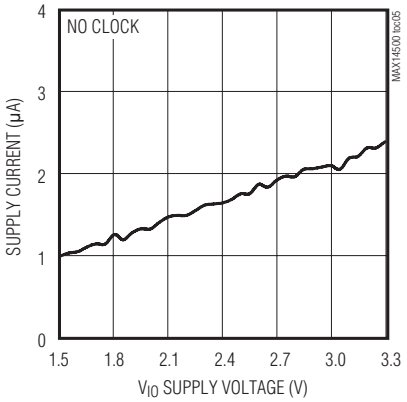

**SD CHANNEL ON-RESISTANCE vs. SD CHANNEL COMMON VOLTAGE**



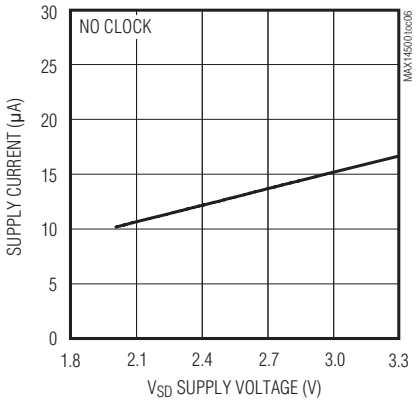

**PASS THRU $V_{CC}$ SUPPLY CURRENT vs. SUPPLY VOLTAGE**




**PASS THRU $V_{IO}$ SUPPLY CURRENT vs. SUPPLY VOLTAGE**




**PASS THRU $V_{SD}$ SUPPLY CURRENT vs. SUPPLY VOLTAGE**

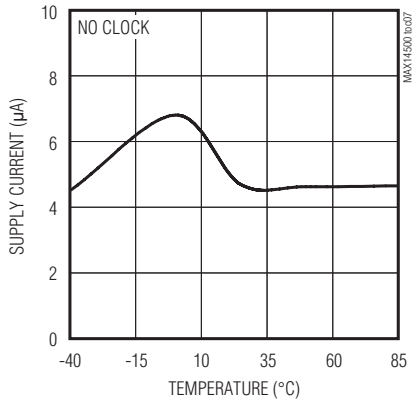


# Hi-Speed USB-to-SD Card Readers with Bypass

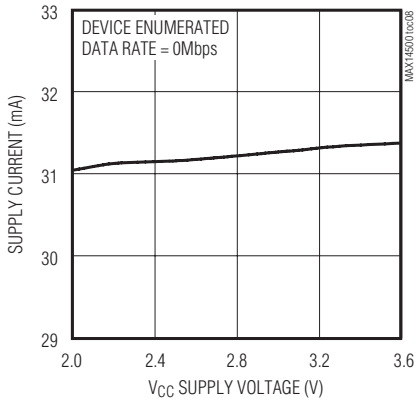
## Typical Operating Characteristics (continued)

($V_{CC}$ = +3.3V, $V_{IO}$ = +2.5V, $V_{SD}$ = +2.5V, $V_{TM}$ = +3.3V, $T_A$ = +25°C, unless otherwise noted.)

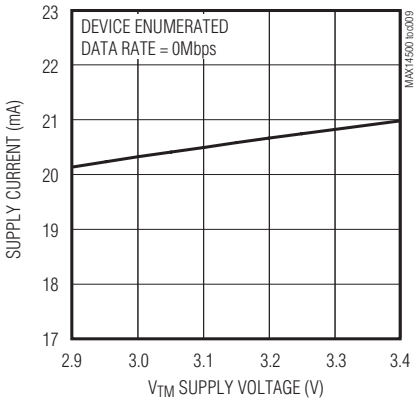
**PASS THRU $V_{CC}$ SUPPLY CURRENT vs. TEMPERATURE**



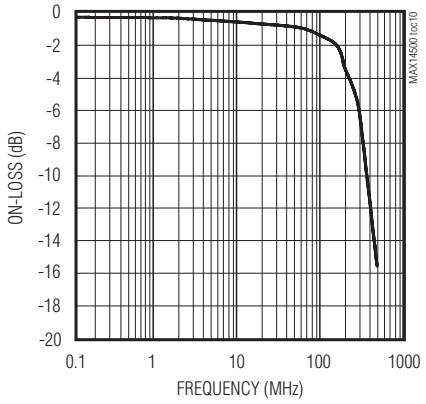

**CARD READER $V_{CC}$ SUPPLY CURRENT vs. SUPPLY VOLTAGE**



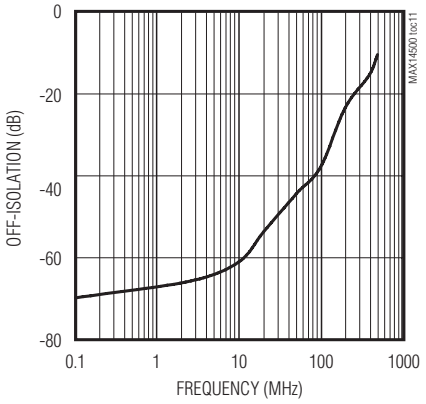

**CARD READER $V_{TM}$ SUPPLY CURRENT vs. SUPPLY VOLTAGE**




**PASS THRU USB CHANNEL FREQUENCY RESPONSE**




**PASS THRU SD CHANNEL OFF-ISOLATION**



## Pin Description

| PIN | | NAME | FUNCTION |
|---|---|---|---|
| TQFN | WLP | | |
| **INPUTS/OUTPUTS** | | | |
| 1 | C4 | I2C_SEL | I²C Select Input. I2C_SEL must be connected to $V_{IO}$ or GND at power-up. Drive I2C_SEL low to disable I²C control and drive I2C_SEL high to enable I²C control. |
| 2 | A2 | SCL | I²C Serial-Clock Input. SCL is +3.6V tolerant and the high threshold is set by $V_{IO}$. If the I²C interface is not used, connect SCL to GND. |
| 3 | B4 | SDA | I²C Serial-Data I/O. SDA is +3.6V tolerant and the high threshold is set by $V_{IO}$. If the I²C interface is not used, connect SDA to GND. |
| 4 | A3 | ADD | I²C Address Selection Input. Connect ADD to $V_{IO}$ or GND to select between two I²C slave addresses: (GND = 1110 000Xb and $V_{IO}$ = 1110 001Xb). |
| 6 | B6 | $\overline{BERR}$/INT | Card Reader Error/Interrupt Output. $\overline{BERR}$/INT becomes $\overline{BERR}$ for simple control and INT for I²C control. $\overline{BERR}$/INT goes low to indicate an error in Card Reader mode during simple control and asserts for enabled interrupts during I²C control. |
| 7 | A7 | $\overline{BUSY}$ | Busy Output. $\overline{BUSY}$ asserts low to indicate device is in Card Reader mode. |
| 8 | C6 | MODE | Card Reader/Pass Thru Mode Select Input. MODE is only active during simple control. Drive MODE low to enable Pass Thru mode and drive MODE high to enable Card Reader mode. For I²C control, MODE must be connected to GND. |
| 9 | B7 | $\overline{RST}$ | Reset Input. Drive $\overline{RST}$ low to reset the internal registers to default values and put all outputs in high impedance. Connect $\overline{RST}$ to $V_{IO}$ for normal operation. |
| 25 | E6 | FREF | Frequency Input. FREF is the clock input (12MHz/13MHz/19.2MHz/26MHz) for the internal logic and USB PHY. FREF can accept a square-wave or sine-wave clock. An internal clock squaring circuit can be enabled or disabled through I²C. In simple control, the internal clock squarer is enabled by default. |
| 27 | F5 | RREF | Reference Resistor. Connect a Bias Resistor 6.19kΩ ±1% from RREF to GND. |
| **USB INTERFACE** | | | |
| 22 | G7 | CD+ | USB Analog Switch/Hi-Speed USB Transceiver. CD+ connects to D+ on the USB connector. |
| 21 | F7 | CD- | USB Analog Switch/Hi-Speed USB Transceiver. CD- connects to D- on the USB connector. |
| 20 | G8 | HD+ | USB Analog Switch. HD+ connects to D+ on the host side. |
| 19 | F8 | HD- | USB Analog Switch. HD- connects to D- on the host side. |
| 28 | E5 | KVBUS | USB Bus Power-Supply Detection Input. Connect a resistor-divider between USB VBUS, KVBUS, and GND. |
| **SD CARD INTERFACE** | | | |
| 13 | C8 | CDAT1_0 | SD Card 1 Data Bus Analog Switch/Card Reader Interface. CDAT1_0 connects to DAT0 on the SD card. |
| 12 | B8 | CDAT1_1 | SD Data Card 1 Bus Analog Switch/Card Reader Interface. CDAT1_1 connects to DAT1 on the SD card. |
| 11 | C7 | CDAT1_2 | SD Data Card 1 Bus Analog Switch/Card Reader Interface. CDAT1_2 connects to DAT2 on the SD card. |

# Hi-Speed USB-to-SD Card Readers with Bypass

## Pin Description (continued)

| PIN | | NAME | FUNCTION |
|---|---|---|---|
| TQFN | WLP | | |
| 10 | A8 | CDAT1_3 | SD Card 1 Data Bus Analog Switch/Card Reader Interface. CDAT1_3 connects to DAT3 on the SD card. |
| 34 | E2 | CCMD1 | SD Card 1 Command Analog Switch/Card Reader Interface. CCMD1 connects to CMD on the SD card. |
| 32 | E3 | CCLK1 | SD Card 1 Clock Analog Switch/Card Reader Interface. CCLK1 connects to CLK on the SD card. |
| 33 | F1 | CCRD_PRST | SD Card 1 Analog Switch for Card Present Detection. CCRD_PRST is the card detection line to the SD socket. When in Pass Thru mode, CCRD_PRST is connected to HCRD_PRST. |
| 17 | D7 | HDAT1_0 | SD Card 1 Data Bus Analog Switch. HDAT1_0 connects to DAT0 on the SD port of the host µP. |
| 16 | D8 | HDAT1_1 | SD Card 1 Data Bus Analog Switch. HDAT1_1 connects to DAT1 on the SD port of the host µP. |
| 15 | D6 | HDAT1_2 | SD Card 1 Data Bus Analog Switch. HDAT1_2 connects to DAT2 on the SD port of the host µP. |
| 14 | D5 | HDAT1_3 | SD Card 1 Data Bus Analog Switch. HDAT1_3 connects to DAT3 on the SD port of the host µP. |
| 31 | G1 | HCMD1 | SD Card 1 Command Analog Switch. HCMD1 connects to CMD on the SD port of the host µP. |
| 29 | G2 | HCLK1 | SD Card 1 Clock Analog Switch. HCLK1 connects to CLK on the SD port of the host µP. |
| 30 | F2 | HCRD_PRST | SD Card 1 Analog Switch for Card Present Detection. HCRD_PRST is connected to CCRD_PRST in Pass Thru mode. |
| — | D2 | CDAT2_0 | SD Card 2 Data Bus Analog Switch/Card Reader Interface. CDAT2_0 connects to DAT0 on the SD card. |
| — | D1 | CDAT2_1 | SD Card 2 Data Bus Analog Switch/Card Reader Interface. CDAT2_1 connects to DAT1 on the SD card. |
| — | B5 | CDAT2_2 | SD Card 2 Data Bus Analog Switch/Card Reader Interface. CDAT2_2 connects to DAT2 on the SD card. |
| — | A5 | CDAT2_3 | SD Card 2 Data Bus Analog Switch/Card Reader Interface. CDAT2_3 connects to DAT3 on the SD card. |
| — | F4 | CCMD2 | SD Card 2 Command Analog Switch/Card Reader Interface. CCMD2 connects to CMD on the SD card. |
| — | F3 | CCLK2 | SD Card 2 Clock Analog Switch/Card Reader Interface. CCLK2 connects to CLK on the SD card. |
| — | D3 | HDAT2_0 | SD Card 2 Data Bus Analog Switch. HDAT2_0 connects to DAT0 on the SD port of the host µP. |
| — | E1 | HDAT2_1 | SD Card 2 Data Bus Analog Switch. HDAT2_1 connects to DAT1 on the SD port of the host µP. |

## Pin Description (continued)

| PIN | | NAME | FUNCTION |
|---|---|---|---|
| TQFN | WLP | | |
| — | C5 | HDAT2_2 | SD Card 2 Data Bus Analog Switch. HDAT2_2 connects to DAT2 on the SD port of the host µP. |
| — | A4 | HDAT2_3 | SD Card 2 Data Bus Analog Switch. HDAT2_3 connects to DAT3 on the SD port of the host µP. |
| — | G4 | HCMD2 | SD Card 2 Command Analog Switch. HCMD2 connects to CMD on the SD port of the host µP. |
| — | G3 | HCLK2 | SD Card 2 Clock Analog Switch. HCLK2 connects to CLK on the SD port of the host µP. |
| **POWER SUPPLY** | | | |
| 5 | A6 | $V_{IO}$ | I/O Logic-Level Translator Voltage. Bypass $V_{IO}$ to GND with a 0.1µF ceramic capacitor. $V_{IO}$ powers the logic inputs/outputs and $I^2C$ block. |
| 23 | F6 | $V_{TM}$ | USB Analog Switch and Transceiver Power Supply. Bypass $V_{TM}$ to GND with a 0.1µF ceramic capacitor. |
| 38 | B1, B2 | CLDO | Bypass Capacitor for Internal +1.8V LDO. Connect a 1µF ceramic capacitor (X7R, X5R, or better) from CLDO to GND. CLDO must not be used to power external circuitry. |
| 39 | B3, C3 | $V_{CC}$ | Digital Supply Voltage. Bypass $V_{CC}$ to GND with a 1µF ceramic capacitor (X7R, X5R, or better). |
| 40 | A1 | $V_{SD}$ | SD Card Voltage. Bypass $V_{SD}$ to GND with a 1µF ceramic capacitor (X7R, X5R, or better). |
| 18, 24, 26, 37 | C1, C2, E7, E8, G5, G6 | GND | Ground |
| **NO CONNECTION** | | | |
| 35, 36 | D4, E4 | N.C. | No Connection. Connect N.C. to GND. |
| **EXPOSED PAD** | | | |
| — | — | EP | Exposed Pad. Connect EP to GND. Do not use EP as the sole GND connection. |

# Hi-Speed USB-to-SD Card Readers with Bypass

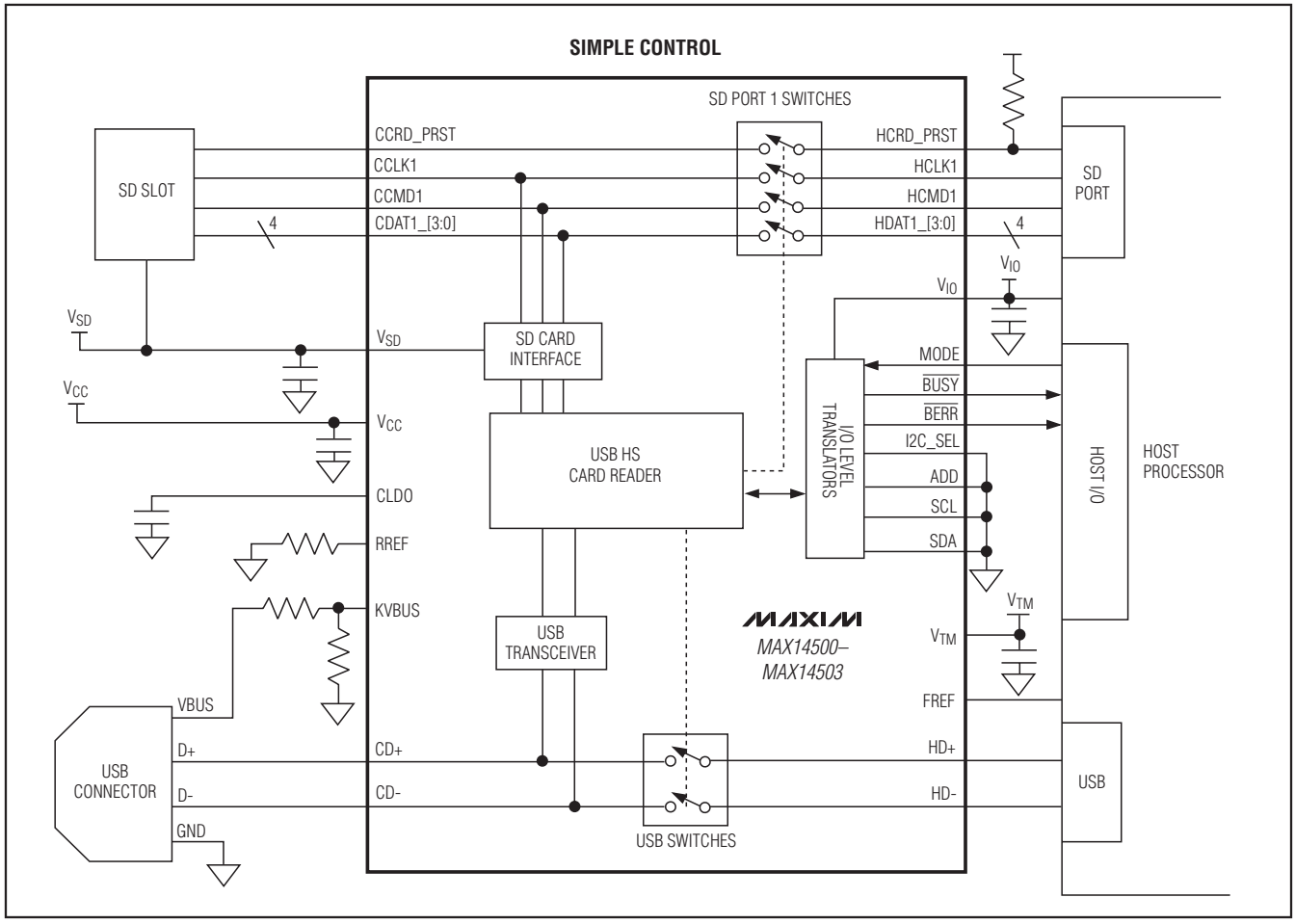



*Figure 1. Typical Application Circuit for Simple Control Mode with One SD Card*

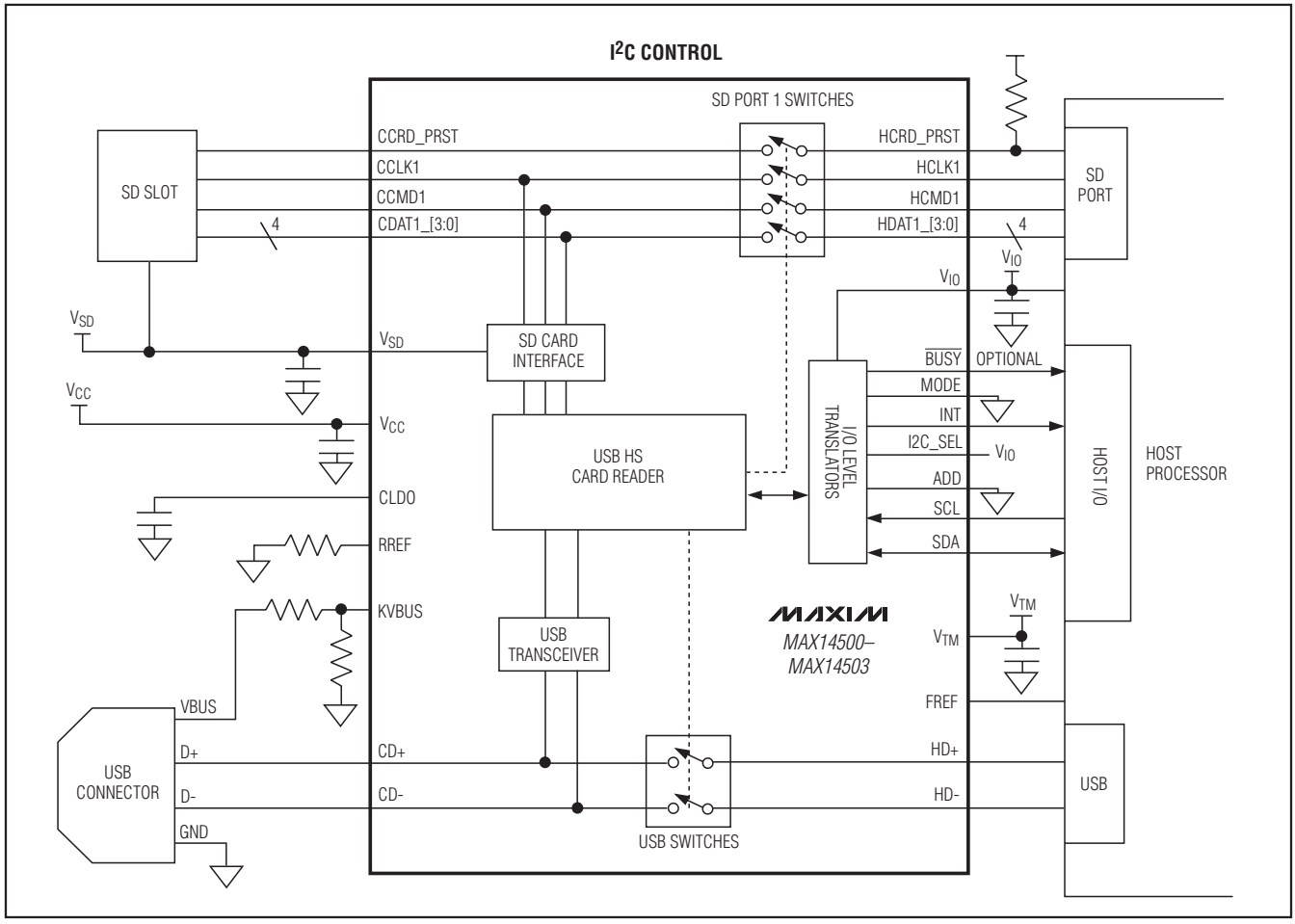



*Figure 2. Typical Application Circuit for I²C Control Mode with One SD Card*

# Hi-Speed USB-to-SD Card Readers with Bypass

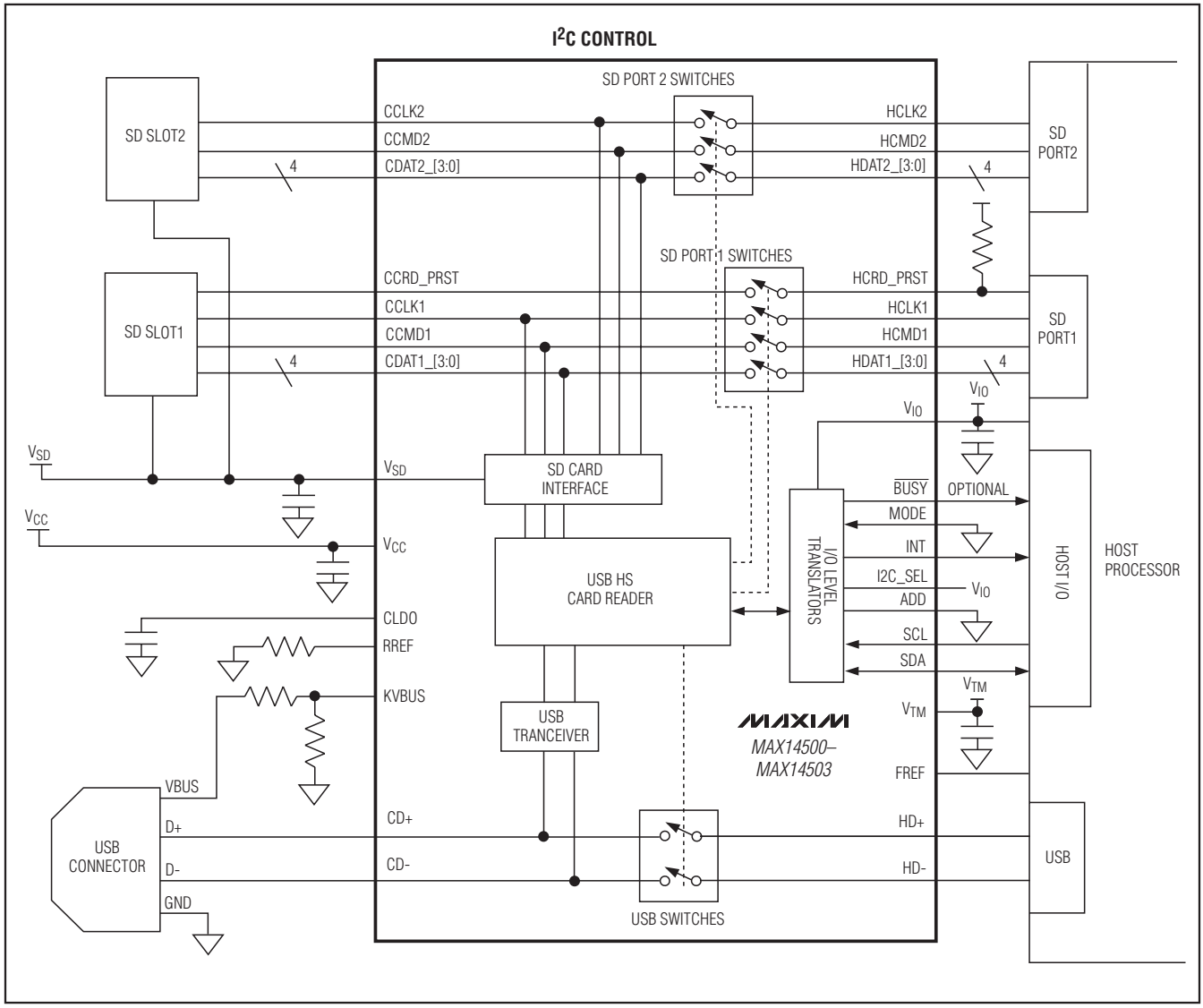



*Figure 3. Typical Application Circuit for I²C Control Mode with Two SD Cards*

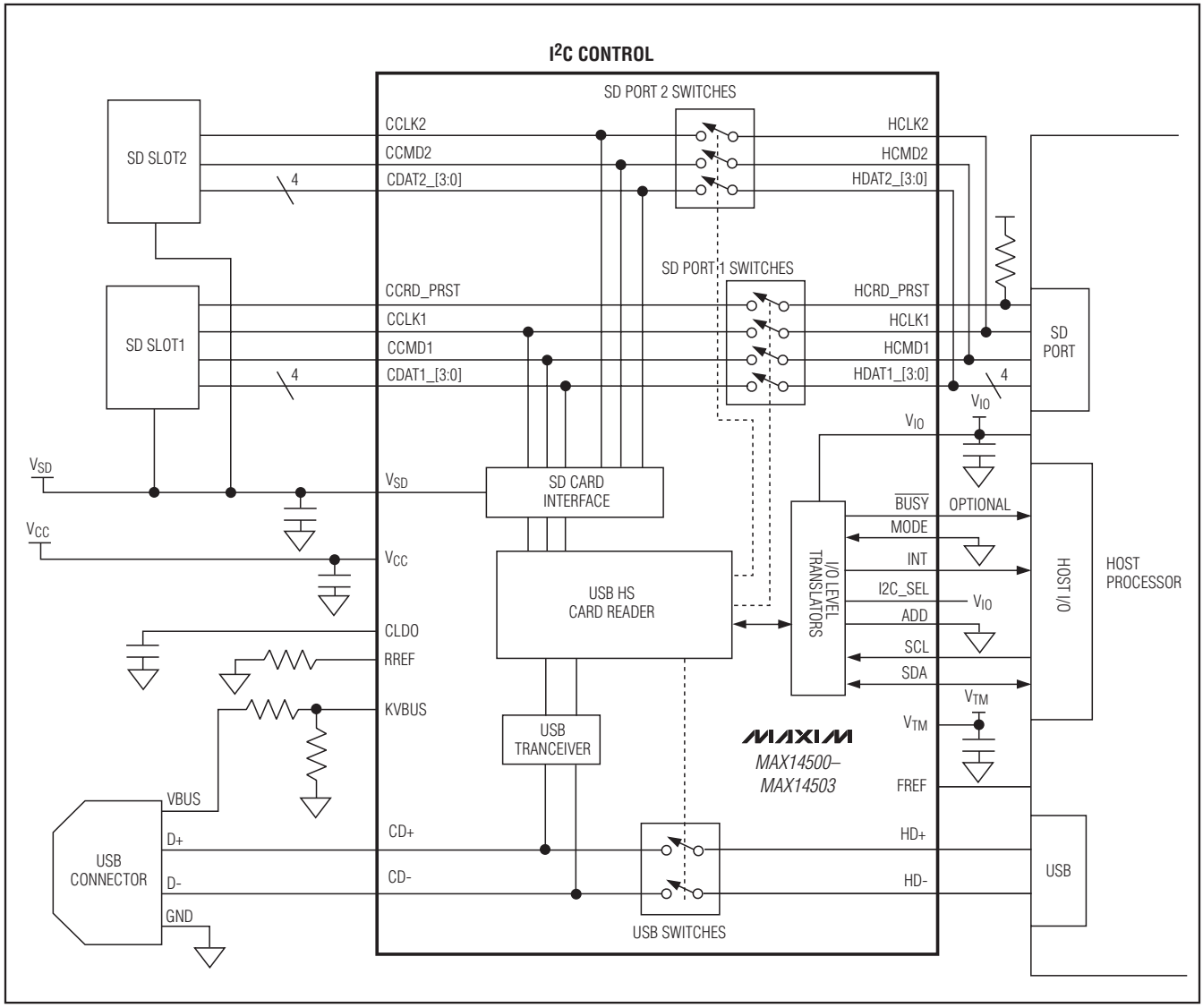



*Figure 4. Typical Application Circuit for I²C Control Mode with One SD Port and Two SD Cards*

## Timing Diagrams

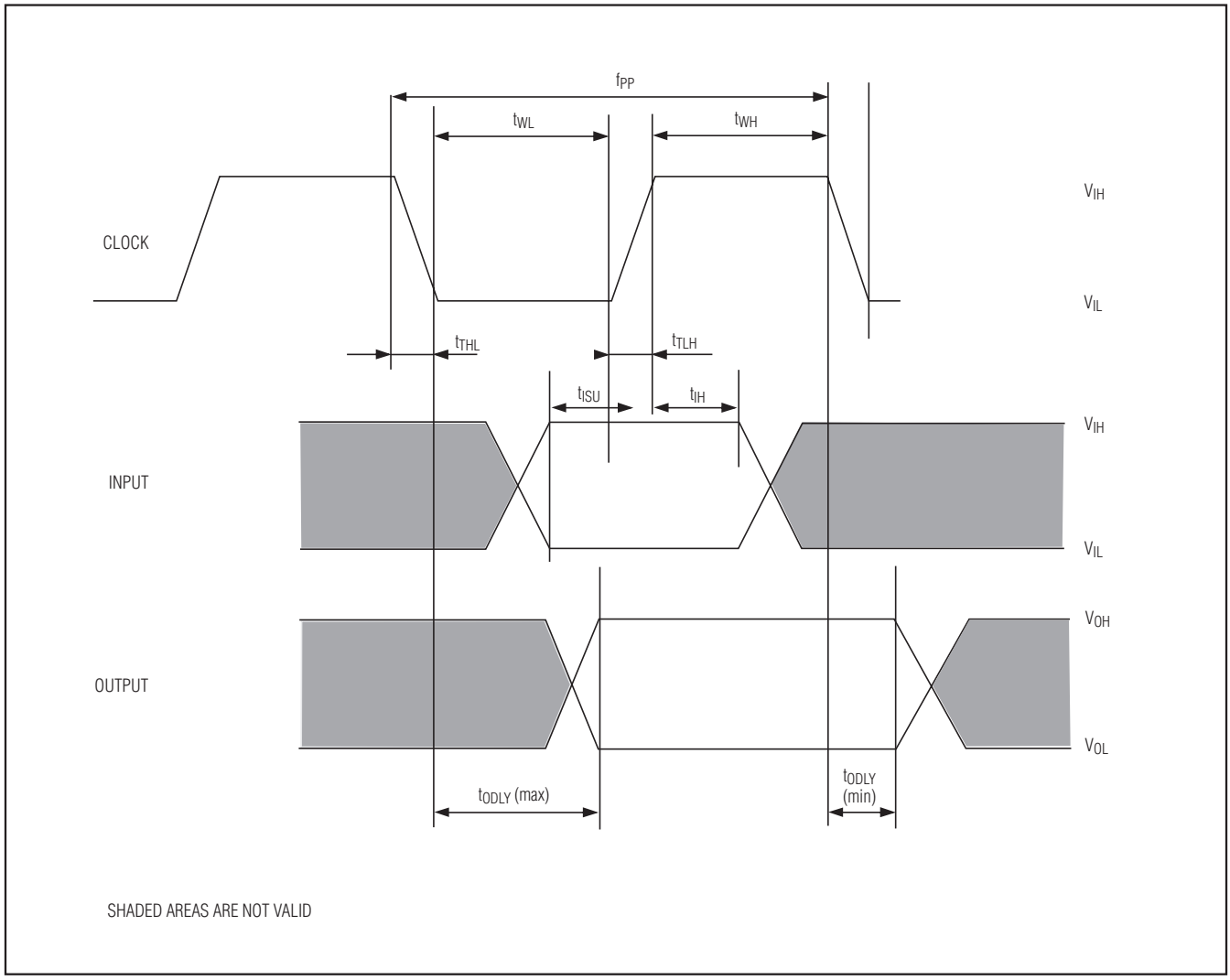



*Figure 5a. SD Card Default Timing Diagram*

## Timing Diagrams (continued)

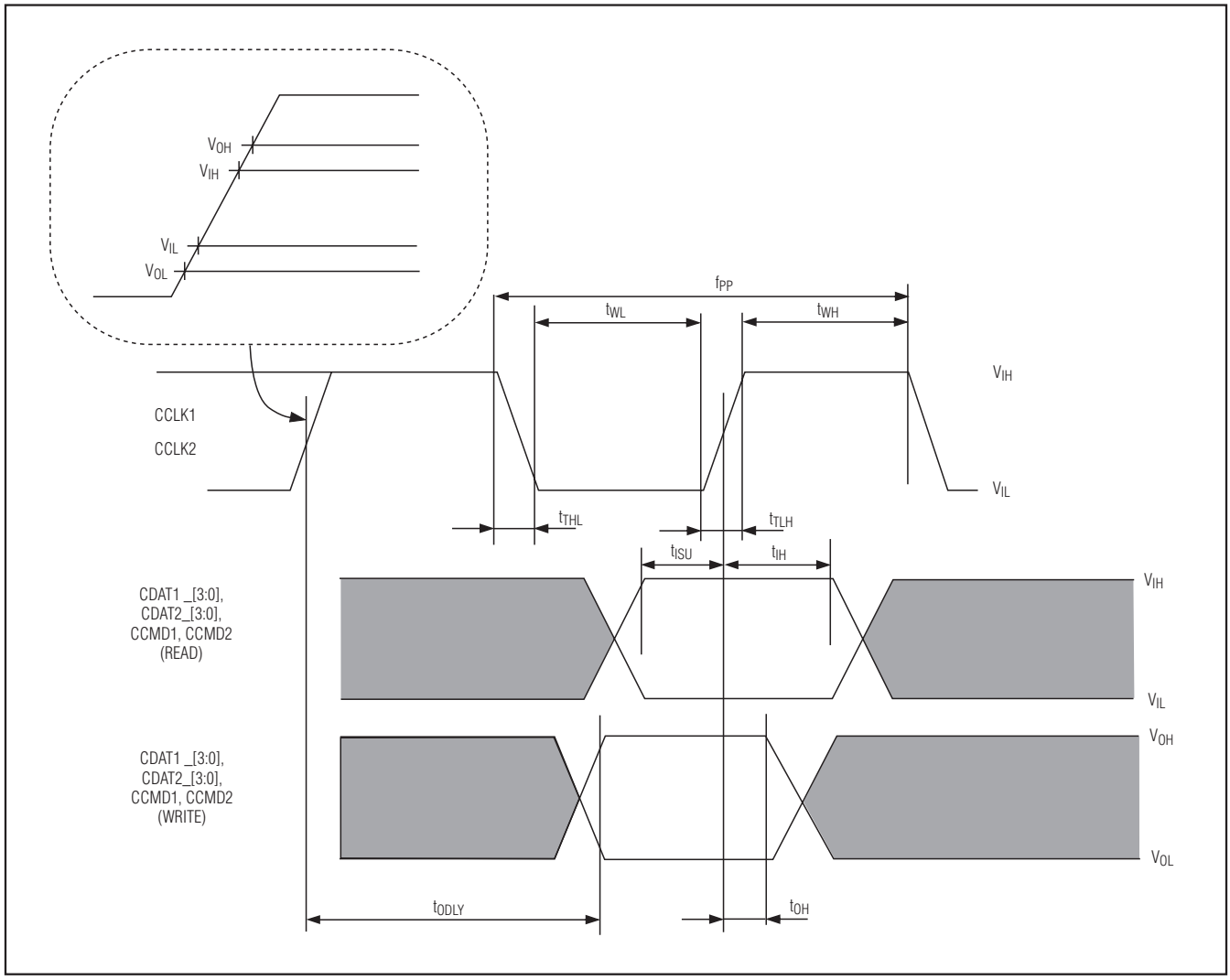



*Figure 5b. SD Card Hi-Speed Timing Diagram*

# Hi-Speed USB-to-SD Card Readers with Bypass

## Timing Diagrams (continued)

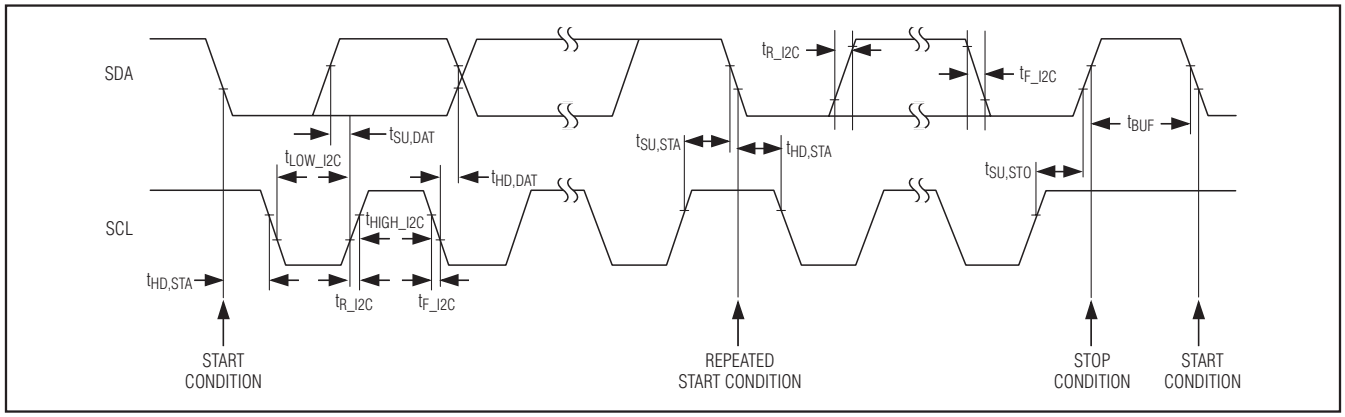



*Figure 6. I²C Timing Diagram*

## Detailed Description

The MAX14500–MAX14503 can be added to devices that have an SD card slot and a USB full-speed port (12Mbps) to provide a Hi-Speed USB path to an SD card bypassing the host microprocessor (µP), allowing for faster SD card transfers (Figures 1–4). Without the MAX14500–MAX14503, a host µP with a full-speed USB port moves data between an SD card and a host PC at 12Mbps when transferring data from an SD card through USB. The host µP has additional overhead because it has to accept data from the SD cards, process the data by putting it in USB format, and then transfer the data through the USB port. The MAX14500–MAX14503 create an alternate path from the SD card to USB, providing USB Hi-Speed capability. By bypassing the host µP using the MAX14500–MAX14503, SD card read and write operations are not limited by host µP overhead and USB full-speed data rates.

The MAX14500–MAX14503 operate in Pass Thru and Card Reader mode. In Pass Thru mode, the MAX14500–MAX14503 are transparent to the host µP. All read and write operations pass from the host µP SD port to the SD card without modification. All of the features of the original device are intact and there is no need to change firmware in the host µP. In Card Reader mode, the SD card is connected to the PC with the internal USB Hi-Speed card reader, bypassing the host µP.

The MAX14500–MAX14503 can be controlled in two ways. The simple control method uses a single output from a µP or ASIC to select Pass Thru or Card Reader mode. Only one SD card can be used as a Hi-Speed USB card reader in simple control. I²C control allows more configuration options and provides status information along with error conditions and additional interrupts. Two SD cards can be connected and each set of SD port switches can be controlled independently (two SD port version under I²C control). The state of I2C_SEL must not change after $V_{IO}$ is applied.

With I²C control, the I²C bus is used to read and write to internal registers for configuration, error checking, control, and status reporting. The control and configuration registers have various functions including wakeup, SD card selection, interrupt enable, and SD switch settings. The status registers give the status of errors, SD card detection, power supplies, and interrupts. Putting the MAX14500–MAX14503 to sleep puts the device into Pass Thru mode. The state of SD port switches for card 1 and card 2 can be changed while in Pass Thru. Some I²C commands are executed upon waking up or entering Card Reader mode. For register settings that involve Card Reader mode, (when in Sleep mode), programming the I²C registers changes the values, but the actions do not execute until the internal logic wakes up or Card Reader mode is entered. The register map indicates when register bit changes take effect.

## Table 1. Power-Up Default Mini Register Map for Configuration Registers

| REGISTER NAME | REGISTER ADDRESS (hex) | POWER-UP VALUE (hex) | POWER-UP DEFAULT SETTINGS |
|---|---|---|---|
| Control Register (CONTROL) | 0x00 | 0x18 | SD2SW = 1, SD switch 2 is closed<br>SD1SW = 1, SD switch 1 is closed<br>MODE[1:0] = 00, Card Reader mode is not active<br>WAKEUP = 0, shutdown |
| Configuration Register 1 (CONFIG1) | 0x01 | 0x00 | SD2ONEBIT = 0, SD2 bus in 4-bit data mode<br>SD1ONEBIT = 0, SD1 bus in 4-bit data mode<br>INTPULSE = 0, INT stays asserted until status register is read<br>INTACTHI = 0, INT asserts active low |
| Configuration Register 2 (CONFIG2) | 0x02 | 0x00 | CLKSOURCE = 00000, default clock input<br>FORCEFS = 0, USB Hi-Speed |
| Configuration Register 3 (CONFIG3) | 0x03 | 0x00 | SD2MAXCLK = 0000, default clock (base SD clock)<br>SD1MAXCLK = 0000, default clock (base SD clock) |
| Interrupt Enable Register 1 (IE1) | 0x04 | 0x00 | USBFS = 0, disable INT for full-speed status change<br>USBSR = 0, disable INT for suspend/resume status change<br>VTM = 0, disable INT for $V_{TM}$ status change<br>VSD = 0, disable INT for $V_{SD}$ status change<br>KVBUS = 0, disable INT for VBUS status change<br>BSY = 0, disable INT for $\overline{BUSY}$ status change<br>SDSTAT = 0, disable INT for SD card status change |
| Interrupt Enable Register 2 (IE2) | 0x05 | 0x00 | FWUPD = 0, disable INT for firmware update status change |
| USB Vendor ID High Byte (USBVIDH) | 0x06 | 0x00 | If VID = 0x0000, 0x06BA is used during USB enumeration, VID high byte = 0x06 |
| USB Vendor ID Low Byte (USBVIDL) | 0x07 | 0x00 | If VID = 0x0000, 0x06BA is used during USB enumeration, VID low byte = 0xBA |
| USB Product ID High Byte (USBPIDH) | 0x08 | 0x00 | If PID = 0x0000, 0x38A4 is used during USB enumeration, PID high byte = 0x38 |
| USB Product ID Low Byte (USBPIDL) | 0x09 | 0x00 | If PID = 0x0000, 0x38A4 is used during USB enumeration. PID low byte = 0xA4 |

# Hi-Speed USB-to-SD Card Readers with Bypass

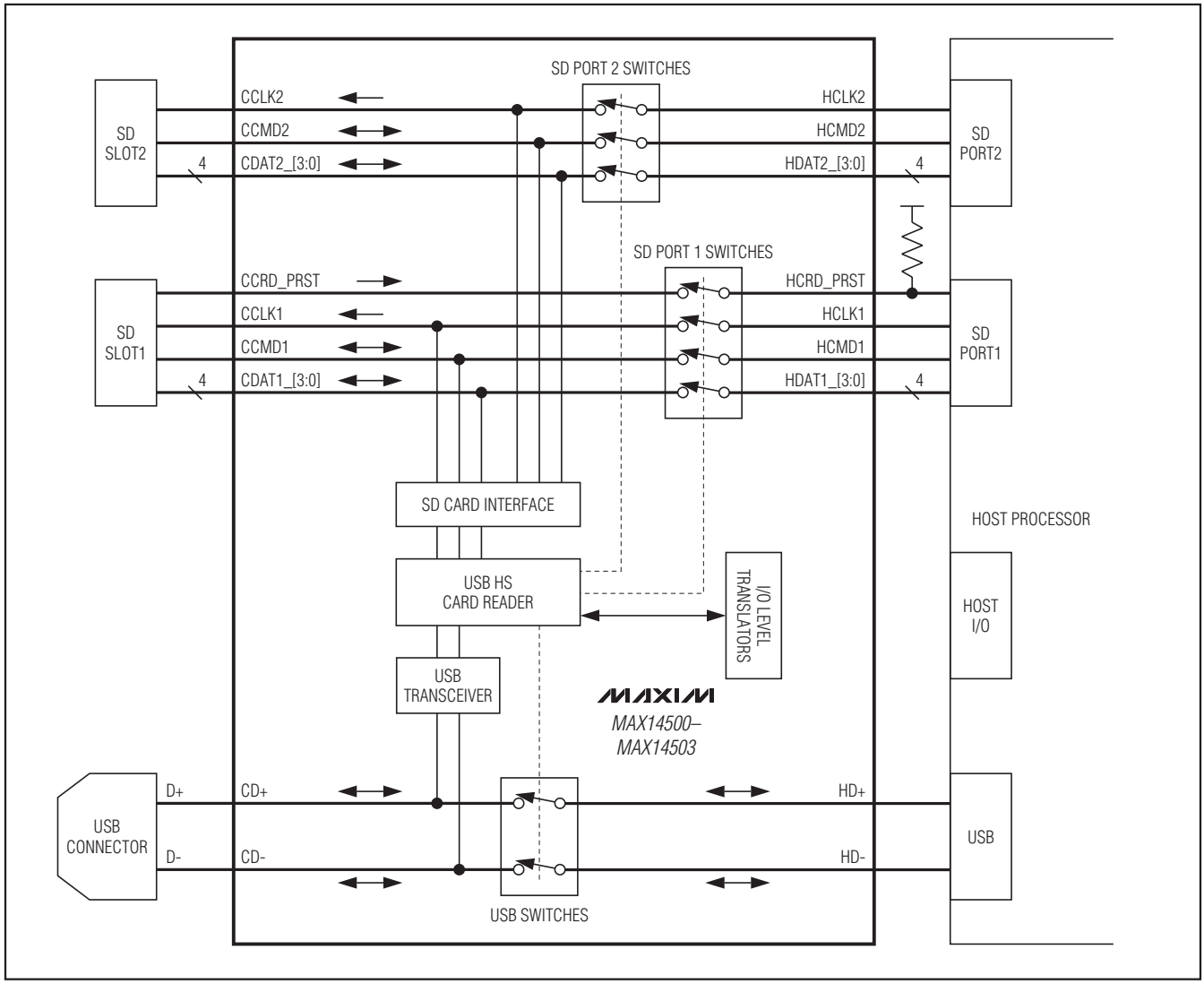



*Figure 7. Default Startup (Pass Thru Mode)*

### Default Power-Up (Pass Thru Mode)

In the default Pass Thru mode, the MAX14500–MAX14503 are transparent and the existing host functions (access to SD cards and USB) are preserved (Figure 7). The host µP reads and writes data to the SD card from the SD port, and can communicate to a PC through its existing full-speed USB port. All of the features of the original chipset are intact. The MAX14500–MAX14503 sleep when in Pass Thru mode (WAKEUP = 0), when the MODE input is low, or when the MODE bits [2:1] in control register (0x00) are set to Card Reader mode, not active. In Sleep mode, the internal microcontroller is turned off and current consumption is minimized. The settings for SD port switches for card 1 and card 2 are controlled by SD port switch bits [4:3] in the control register.

### Card Reader Mode

In Card Reader mode, the PC communicates with the SD card through USB with an internal Hi-Speed SD card reader, bypassing the host µP. Figure 8 shows card reader mode with SD card 1 connected to the PC with the internal card reader. The 40-pin TQFN can connect to a single SD card in Card Reader mode. With the 56-bump WLP operating under I²C control, either SD card can be selected for Card Reader mode.

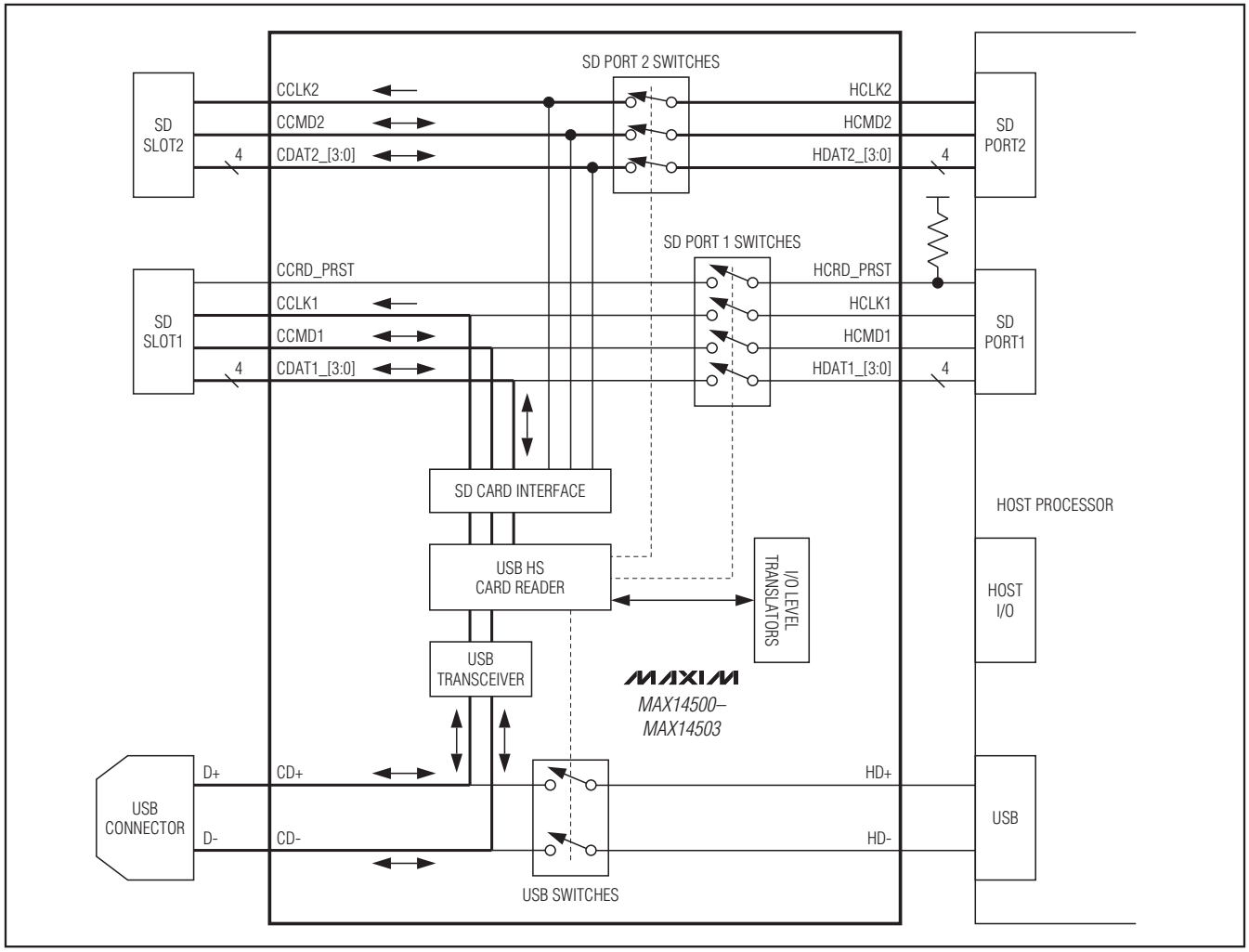



*Figure 8. Card Reader Mode. The USB port is connected to SD card 1. In the 2 port version, a second SD card (SD slot 2) can be independently connected and disconnected to the host µP.*

When the card reader is initiated in the control register, the internal USB switch disconnects from the host µP USB port and connects to the internal USB Hi-Speed SD card reader unit. When the MAX14500–MAX14503 disconnect from the host to implement a stand-alone high-speed card reader, it simulates a disconnect on the host USB and SD ports to maintain data coherence. The SD connections are restored to the host µP by closing the analog switch connecting CCRD_PRST to HCRD_PRST.

Certain registers execute actions when entering Card Reader mode. These actions are only valid for Card Reader mode. Writing to these registers in Sleep mode, or when awake, updates the registers, but the action is carried out when Card Reader mode is activated for one of the SD cards (see the *Register Map* section).

When Card Reader mode is initially entered, the internal microcontroller enumerates with the PC to establish a high-speed USB mass storage device. No actions by the host µP are required for enumeration other than entering Card Reader mode. Once the USB-SD card connection is established, PC to SD card data transfer begins and various interrupts monitor the status the of Card Reader mode if enabled. The BSY flag is represented externally by the $\overline{BUSY}$ output and can be read serially through $I^2C$. The $\overline{BUSY}$ output is always active. If the host µP requests Sleep mode in the middle of the data transfer, the MAX14500–MAX14503 do not complete the transfer, exit Card Reader mode, reconnect USB switches, and

# Hi-Speed USB-to-SD Card Readers with Bypass

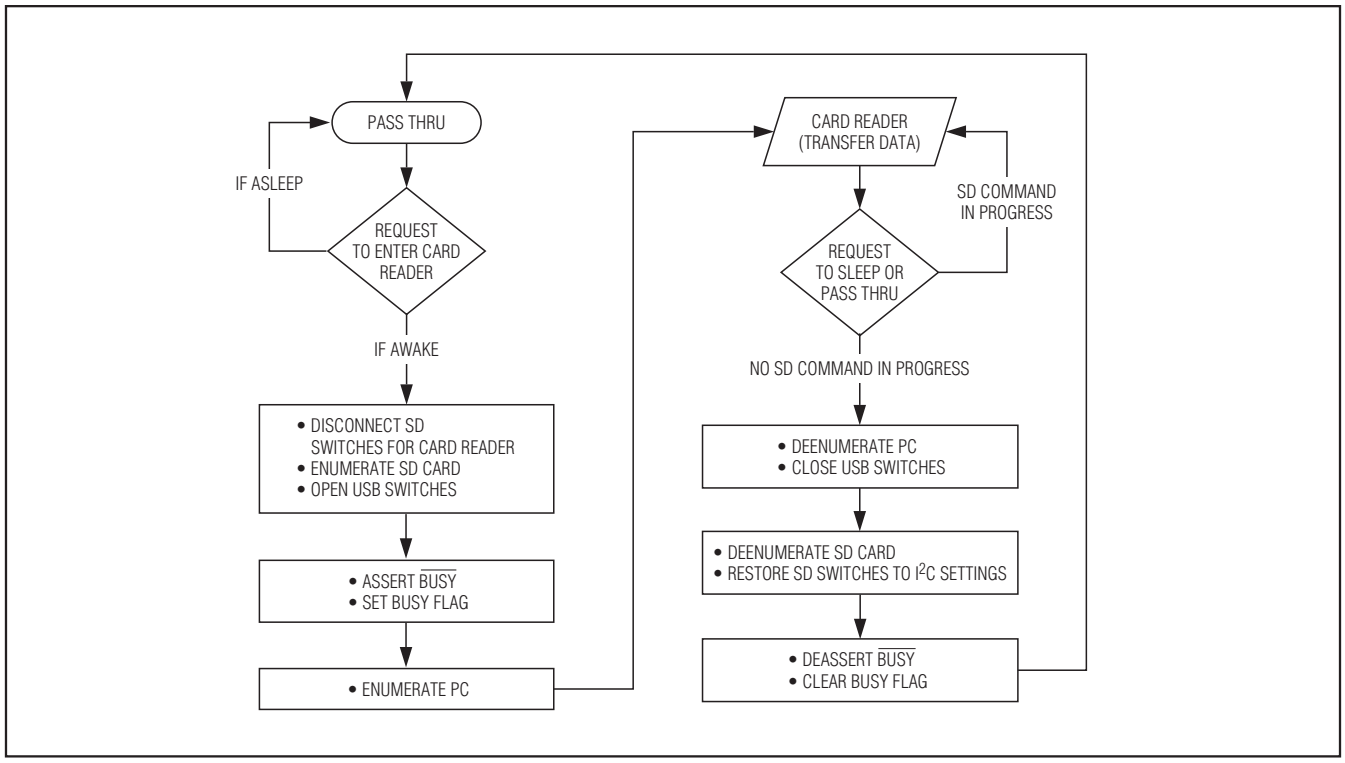



*Figure 9. Card Reader Flow Chart*

go to sleep. Because the $\overline{BUSY}$ output (BSY bit in I²C) indicates Card Reader mode, the host µP may monitor this output after commanding a mode change to determine when the change takes place (Figure 9). If the host requests the other SD card to enter Card Reader mode, the busy flag deasserts and reasserts to let the host know that the change took place.

### Simple Control (I2C_SEL = Low)

The MAX14500–MAX14503 feature a very simple control scheme for entering Card Reader mode that requires a single logic (GPIO) from the host µP. The simple control may only be used with the single SD port versions. When I2C_SEL is connected low at startup, the MODE input controls whether the device is in Pass Thru or Card Reader mode. Driving MODE low enables Pass Thru mode (Figure 10), and the host µP has a direct connection to the SD card and USB connector through internal analog switches. Driving MODE high enables Card Reader mode between SD card 1 and the PC through the USB connector (Figure 11). $\overline{BERR}$/INT functions as the bridge error output $\overline{BERR}$ that asserts for card reader errors. Interrupts are not enabled, the clock source is set to the default as defined by the part number, and the $\overline{BERR}$ and $\overline{BUSY}$ outputs are active. Upon MODE transitioning high, SD card 1 connects to the USB connector in Card Reader mode and $\overline{BUSY}$ asserts low. The $\overline{BUSY}$ output indicates that the device is in Card Reader mode. $\overline{BUSY}$ may be important to the host µP, as the time to complete enumeration/de-enumeration may take a long time (> 100ms).

### I²C Control (I2C_SEL = High)

The MAX14500–MAX14503 feature I²C control that allows access to internal registers for complete control over configuration, SD port analog switches, interrupts, clock configuration, advanced power-on states, and error status. I²C control uses I²C to serially program the MAX14500–MAX14503 to be in Card Reader or Pass Thru mode, and allows either SD card to be connected in Card Reader mode. While a SD card is connected in Card Reader mode, the other SD port analog switches can be independently controlled serially through I²C. Using the I²C bus to put the device to sleep minimizes the supply current while maintaining control over the SD port switches.

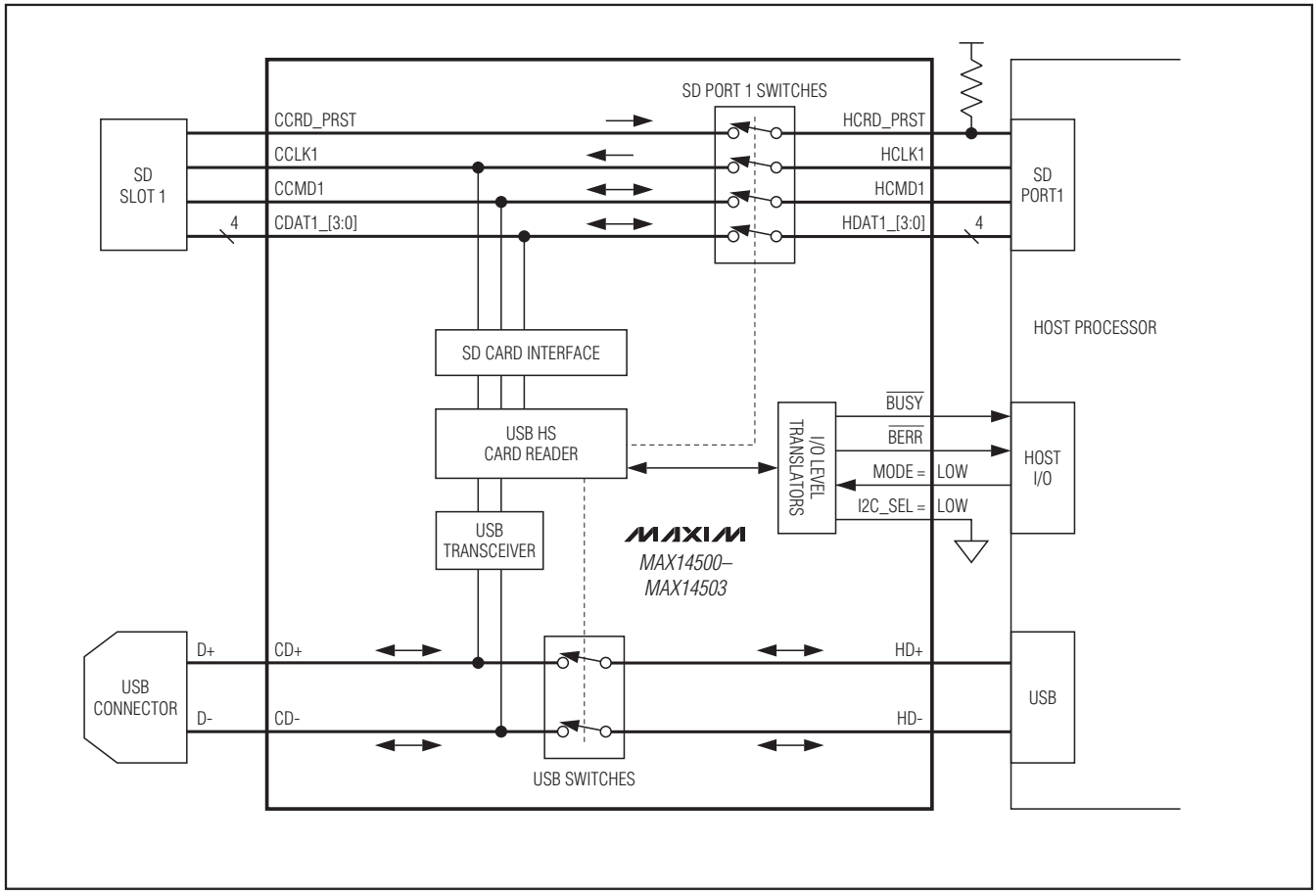



*Figure 10. I2C_SEL Connected Low to Enable Simple Control and MODE = 0 to Enable Pass Thru*

### Control Register (0x00)

The control register controls the settings of SD port analog switches, Card Reader mode, and sleep (Table 2.) The state of the SD port analog switches can be changed when the device is in Sleep mode or in Card Reader mode, and actions are executed immediately. If SD card 1 is connected to the PC through USB in Card Reader mode, the state of the SD port 1 switches are ignored, but the SD port 2 switches can still be controlled through the Control register. Likewise, if SD card 2 is connected to the USB connector in Card Reader mode, the state of the SD port 2 switches are ignored, but the SD port 1 switches can still be controlled through the Control register. Changing the card reader bits in Sleep mode does not cause the device to enter Card Reader mode. Under this condition, the MAX14500–MAX14503 enter Card Reader mode upon waking up.

### Configuration Registers

The MAX14500–MAX14503 have three configuration registers (CONFIG1 = 0x01, CONFIG2 = 0x02, CONFIG3 = 0x03). The configuration registers control the SD bus bit data mode, interrupt polarity, interrupt clearance, clock configuration, SD clock, and USB speed for Card Reader mode. The default settings are shown in the *Register Map* section.

### Interrupts (INT)

All interrupts are masked in the default reset state. There are two interrupt enable registers (IE1 = 0x04, IE2 = 0x05) and two interrupt request registers (IRQ1 = 0x10, IRQ2 = 0x11). The $\overline{BERR}$/INT output functions as the bridge error output $\overline{BERR}$ in simple control and functions as an interrupt INT in I²C control. The polarity of INT and how INT is asserted can be programmed in CONFIG1. The INT output asserts for enabled interrupts and errors in Card Reader mode. The polarity of INT can be active-high or active-low, and INT can be pro-

# Hi-Speed USB-to-SD Card Readers with Bypass

## Table 2. Control Register (0x00)

| BIT | DESCRIPTION | VALUE | FUNCTION | DEFAULT |
|---|---|---|---|---|
| [7:5] | **RESERVED** | 000 | Set these bits to 0. | 000 |
| 4 | **SD PORT 2 ANALOG SWITCHES**<br>SD Port 2 is a set of six analog switches connecting the SD port to the SD card. This set contains: clock (CCLK2), command (CCMD2), and four data lines (CDAT2_[3:0]). The card-present line is not available for this port. This setting is ignored when Card Reader mode is enabled for this port. | 0 | Analog switches are open, disconnecting the SD port from the SD card. | 1 |
| | | 1 | Analog switches are closed, connecting the SD port to the SD card. | |
| 3 | **SD PORT 1 ANALOG SWITCHES**<br>SD Port 1 is a set of seven analog switches connecting the SD port to the SD card. This set contains: card-present (CCRD_PRST), clock (CCLK1), command (CCMD1), and four data lines (CDAT1_[3:0]). The difference between Port 1 and Port 2 is the card-present line. This setting is ignored when Card Reader mode is enabled for this port. | 0 | Analog switches are open, disconnecting the SD port from the SD card. | 1 |
| | | 1 | Analog switches are closed, connecting the SD port to the SD card. | |
| [2:1] | **CARD READER MODE**<br>Changing these bits in Sleep mode does not execute the action until the host µP wakes up the MAX14500–MAX14503. | 00, 11 | Card Reader mode not active. | 00 |
| | | 01 | Card Reader mode active: Connects to SD card 1. | |
| | | 10 | Card Reader mode active: Connects to SD card 2. | |
| 0 | **WAKEUP**<br>In Sleep mode, the MAX14500–MAX14503 are in Pass Thru mode. SD port switches are controlled by their respective bits. Entering Sleep mode reduces the supply current by turning off the internal logic. Request to shut down may be delayed due to USB and de-enumeration. | 0 | Request internal logic to shut down. | 0 |
| | | 1 | Wake up internal logic. | |

grammed to stay asserted until the status register is read, or stay asserted for 10ms. If INT is programmed to stay asserted, a read to the status register is required to clear INT. INT can be programmed to be active-high or active-low when I2C_SEL is high ($I^2C$ control). INT is high impedance in Sleep mode (WAKEUP = 0), regardless of the INT polarity programmed in the $I^2C$ registers. Use a pullup or pulldown resistor for the desired inactive INT polarity state during Sleep mode.

### *Interrupt Masking*

All interrupts are masked at power-up. While masked interrupts do not assert the INT output, they do register as changes in the interrupt request registers (IRQ1 and IRQ2). The status register (STATUS1 = 0x12) indicates the current state of the interrupt bits. If interrupts are masked, polling IRQ1 and IRQ2 indicate the fields with changes, and STATUS1 gives the current state. Reading the IRQ registers resets the interrupt request bits. If polling is used to read the device status, it is required to read both the status register and the interrupt request registers to check for state changes.

### *USB Interrupts*

When enabled, the INT output asserts an interrupt for changes in the USB connection and if the operating system suspends the USB connection. VBUS is detected at the KVBUS input and changes in VBUS voltage can assert an interrupt when enabled.

### *Power-Supply Interrupts*

The MAX14500–MAX14503 feature many advanced power-saving modes. $V_{CC}$, $V_{SD}$, and $V_{TM}$ do not need to be applied for $I^2C$ communication. Changes in $V_{SD}$ and $V_{TM}$ can assert an interrupt when enabled to indicate different power-saving modes (see the *Power-Supply Modes* section).

### *Busy Interrupt*

When enabled, changes in the BSY bit can assert an interrupt (see the *Busy Indication (BSY)* section).

### *SD Status Interrupt*

When enabled, the SDSTAT bit asserts an interrupt for card detection and removal upon entering Card Reader mode for the SD card socket configured as the card reader. The SDSTAT bit is not active during Pass Thru mode and does not change states in the IRQ registers upon card insertion and removal during Pass Thru mode.

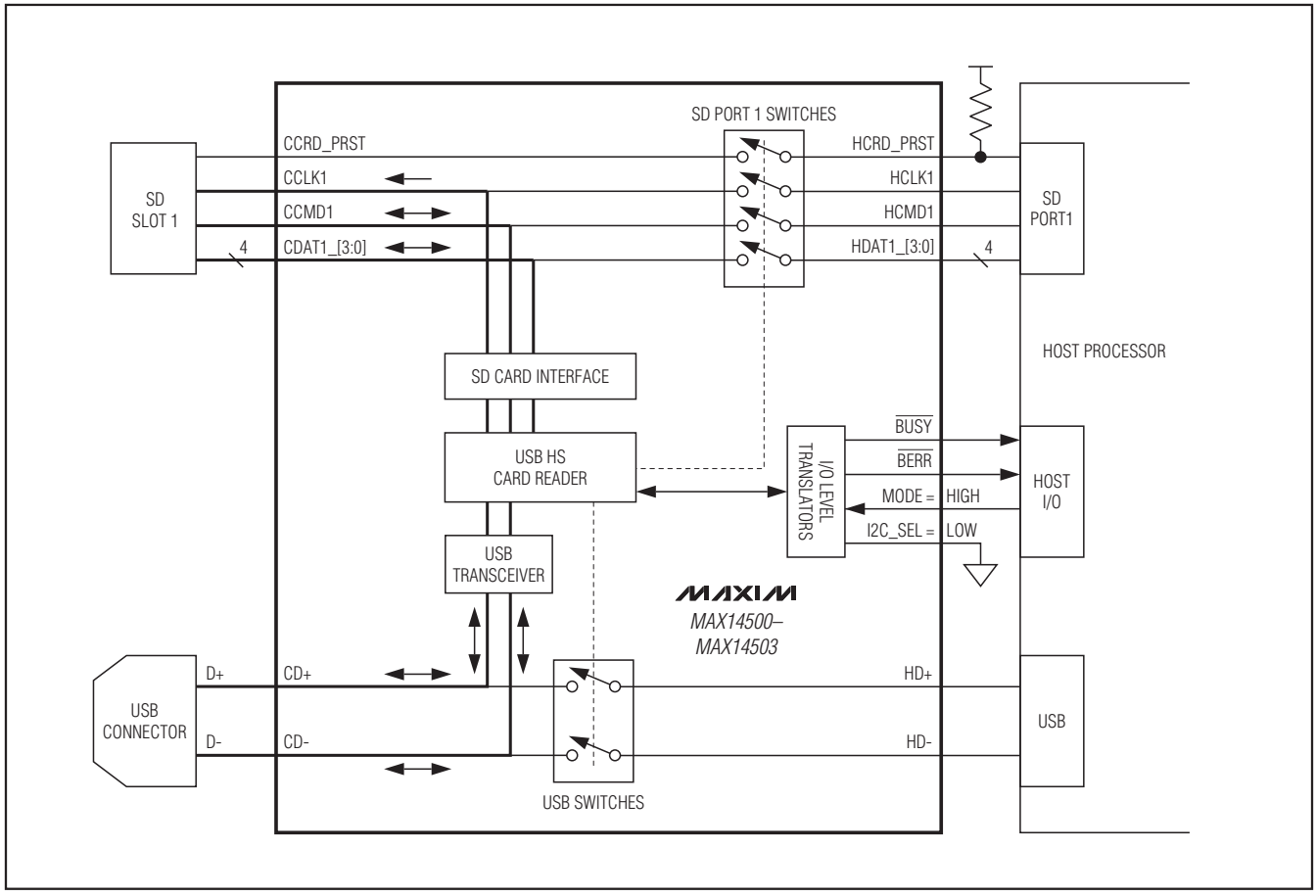



*Figure 11. I2C_SEL is connected low to enable simple control and MODE = 1 to enable Card Reader mode for SD card 1.*

### Error Checking

In simple control, the $\overline{BERR}$/INT output functions as $\overline{BERR}$ and indicates if an error occurs during Card Reader mode. If $\overline{BERR}$ asserts low to indicate an error, the MAX14500–MAX14503 stay in Card Reader mode. If the error clears, data transfer begins. $\overline{BERR}$ asserts if KVBUS, $V_{TM}$, or $V_{SD}$ are not present. It is recommended that MODE be pulled low when $\overline{BERR}$ indicates an error to return the MAX14500–MAX14503 to Pass Thru mode for the host µP to clear the error.

In I²C control, $\overline{BERR}$/INT functions as an interrupt output (INT) and asserts for errors encountered in Card Reader mode when interrupts are not masked. To find the source of the interrupt, read the interrupt request registers and status register.

### Busy Indication (BSY)

The $\overline{BUSY}$ output is used in simple control and I²C control to indicate when Card Reader mode is active. In simple control, transitioning MODE high to low requests the internal microcontroller to enable Pass Thru mode. $\overline{BUSY}$ asserts low while in Card Reader mode and deasserts high in Pass Thru mode.

The BSY bit in STATUS1 (0x12) behaves similarly with I²C control. The $\overline{BUSY}$ output is represented by the BSY bit. Requests to put the device to sleep or bypass (Pass Thru mode) while in Card Reader mode can be verified by checking the state of the $\overline{BUSY}$ signal or BSY bit. The $\overline{BUSY}$ output indicates the status of the BUSY flag in STATUS1. The BSY bit is 1 when the $\overline{BUSY}$ output asserts low. When enabled, changes in the busy flag cause an interrupt. In I²C control, either the BSY bit or the $\overline{BUSY}$ output give the status of the busy state.

# Hi-Speed USB-to-SD Card Readers with Bypass

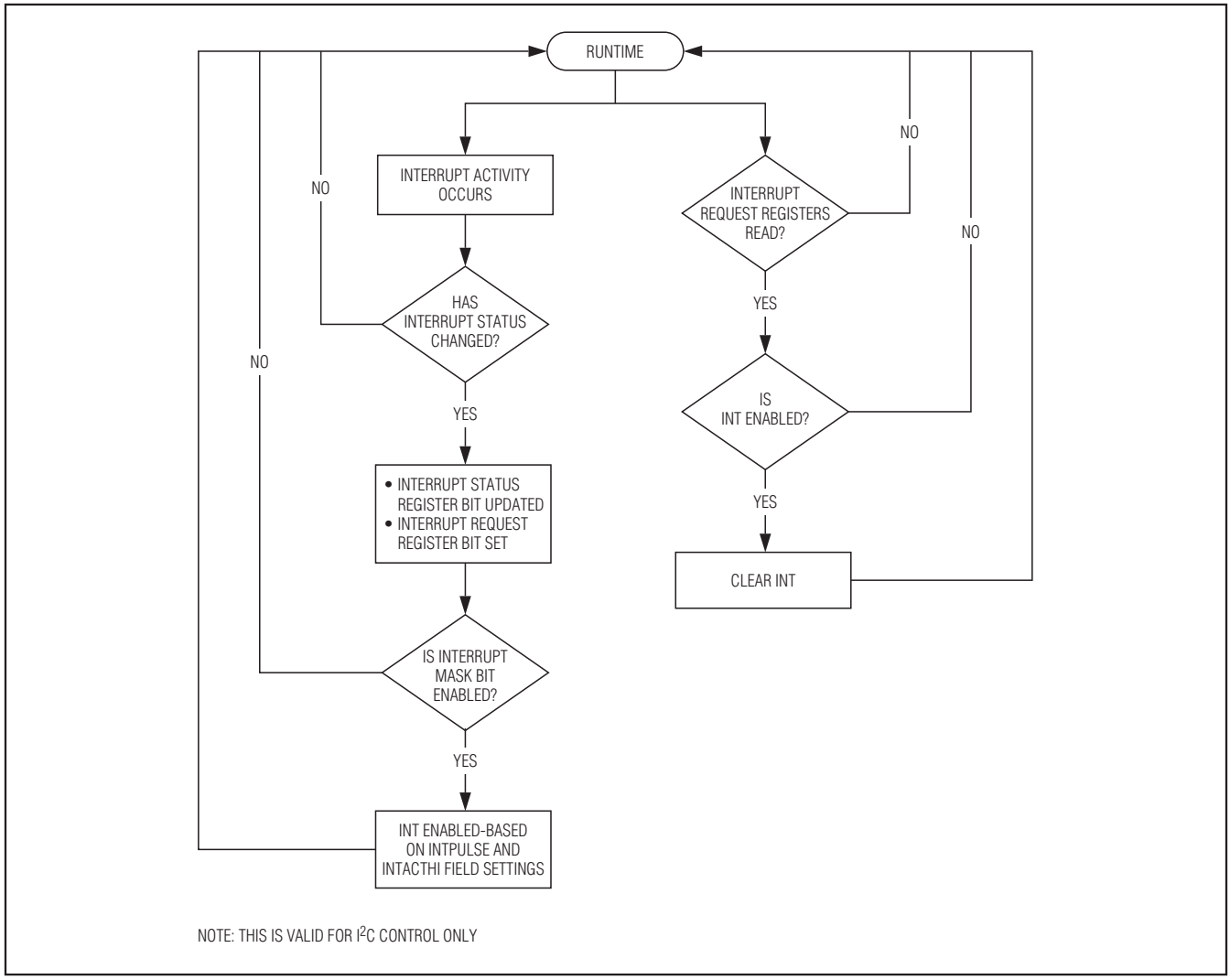



*Figure 12. Typical Interrupt Servicing Flowchart*

### Reset ($\overline{RST}$)

Drive $\overline{RST}$ low to reset all the registers to the default value and minimize the supply current.

### Sleep

The MAX14500–MAX14503 can be put to sleep by programming the WAKEUP bit to 0 in the control register with I²C control, or by driving the MODE input low in simple control. This turns off the internal microcontroller to minimize current. Reads and writes to the I²C are still functional, and registers can be updated with new values. Most register actions do not take effect until the internal microcontroller wakes up or when Card Reader mode is enabled. The SD port analog switches can change states while the internal microcontroller is in Sleep mode. The *Register Map* section shows which registers are enabled in Sleep mode, at power-up, and upon entering Card Reader mode.

### Clock Configuration

The MAX14500–MAX14503 come preprogrammed to accept a 12MHz, 13MHz, 19.2MHz, or 26MHz default clock input with the clock squarer enabled for low-amplitude TCXO signals (see the *Ordering Information/Selector Guide*). This clock is used for the USB and SD subsystems and is not required for operation of the I²C interface. This allows the clock frequency to be changed in the system. The PLL subsystem con-

sists of two blocks: a clock squarer input (enabled by default), which accepts low-signal amplitude TCXO signals (down to 200mV), and a PLL with fixed dividers. The PLL sub system can be configured using the I²C interface. The complete list of PLL subsystem combinations are listed in Table 3.

## Table 3. Clock Source Bit Values

| CLKSOURCE | SOURCE (MHz) | NOTES |
|---|---|---|
| 00000b | See *Ordering Information/ Selector Guide* | Default low-amplitude clock |
| 00001b | 19.2 | Rail-to-rail square wave |
| 00010b | 19.2 | Low-amplitude sine wave |
| 00101b | 13.0 | Rail-to-rail square wave |
| 00110b | 13.0 | Low-amplitude sine wave |
| 01001b | 12.0 | Rail-to-rail square wave |
| 01010b | 12.0 | Low-amplitude sine wave |
| 01101b | 26.0 | Rail-to-rail square wave |
| 01110b | 26.0 | Low-amplitude sine wave |

### I²C Serial Interface

#### Serial Addressing

The MAX14500–MAX14503 operate as I²C slave devices that send and receive data through an I²C-compatible 2-wire interface. The interface uses a serial-data line (SDA) and a serial-clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). A master initiates all data transfers to and from the MAX14500–MAX14503, and generates the SCL clock that synchronizes the data transfer. The SDA line operates as both an input and an open-drain output requiring a pullup resistor on SDA. The SCL line operates only as an input. A pullup resistor is required on SCL if there are multiple masters on the 2-wire interface, or if the master in a single-master system has an open-drain SCL output. Each transmission consists of a START (S) condition by a master, followed by the MAX14500–MAX14503's 7-bit slave address, plus a R/$\overline{W}$ bit, a register address byte, one or more data bytes, and finally a STOP (P) condition.

#### START and STOP Conditions

Both SCL and SDA remain high when the interface is idle. A master signals the beginning of a transmission with a START condition by transitioning SDA from high to low while SCL is high (Figure 13). When the master has finished communicating with the slave, it issues a STOP condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

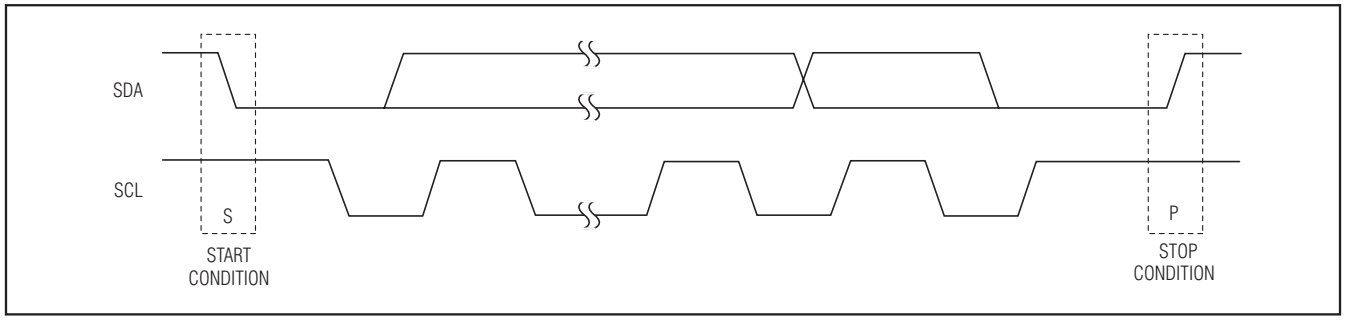



*Figure 13. START and STOP Conditions*

# Hi-Speed USB-to-SD Card Readers with Bypass

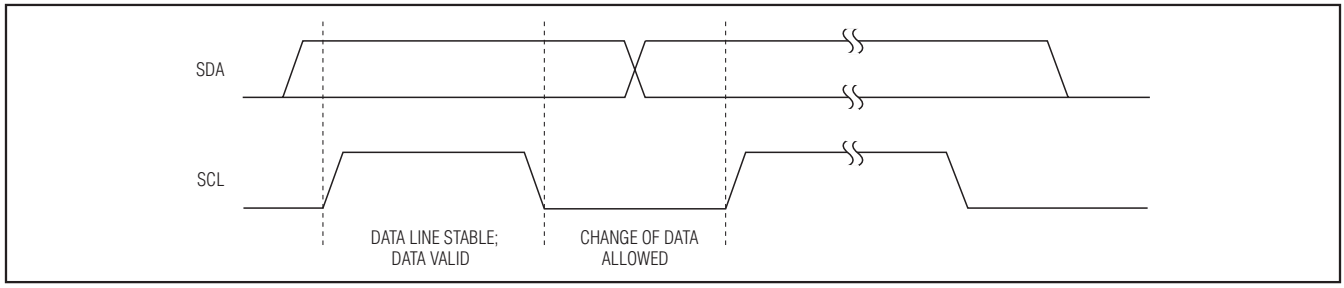



*Figure 14. Bit Transfer*

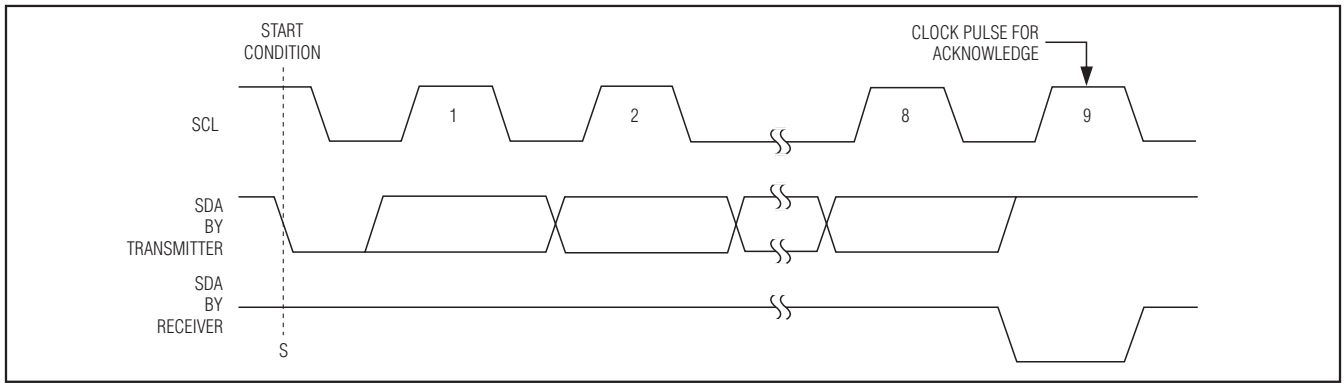



*Figure 15. Acknowledge*

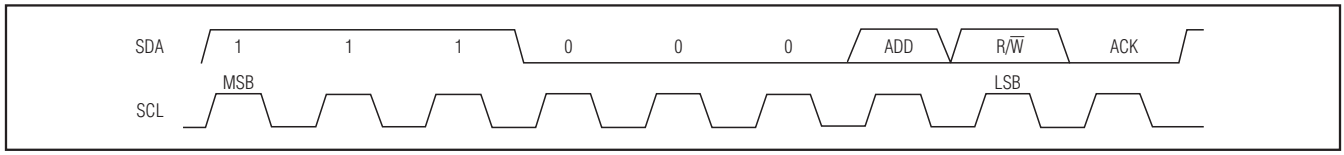



*Figure 16. Slave Address*

### Bit Transfer

One data bit is transferred during each clock pulse (Figure 14). The data on SDA must remain stable while SCL is high.

### Acknowledge

The acknowledge bit is a clocked 9th bit (Figure 15), which the recipient uses to handshake receipt of each byte of data. Each byte transferred effectively requires nine bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse. The SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the MAX14500–MAX14503, the MAX14500–MAX14503 generate the acknowledge bit because the MAX14500–MAX14503 are the recipients. When the MAX14500–MAX14503 are transmitting to the master, the master generates the acknowledge bit because the master is the recipient.

### Slave Addresses

The MAX14500–MAX14503 have a 7-bit long slave address. The bit following the 7-bit slave address is the R/$\overline{W}$ bit, which is low for a write command and high for a read command. The address bit ADD is externally driven high or low by the ADD input to select between two slave addresses to avoid conflict with other I²C addresses (Figure 16). Table 4 shows the binary values for reads and writes.

## Table 4. Slave Addresses

| ADD | FUNCTION | DEVICE ADDRESS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| High | Read | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| High | Write | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 |
| GND | Read | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| GND | Write | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

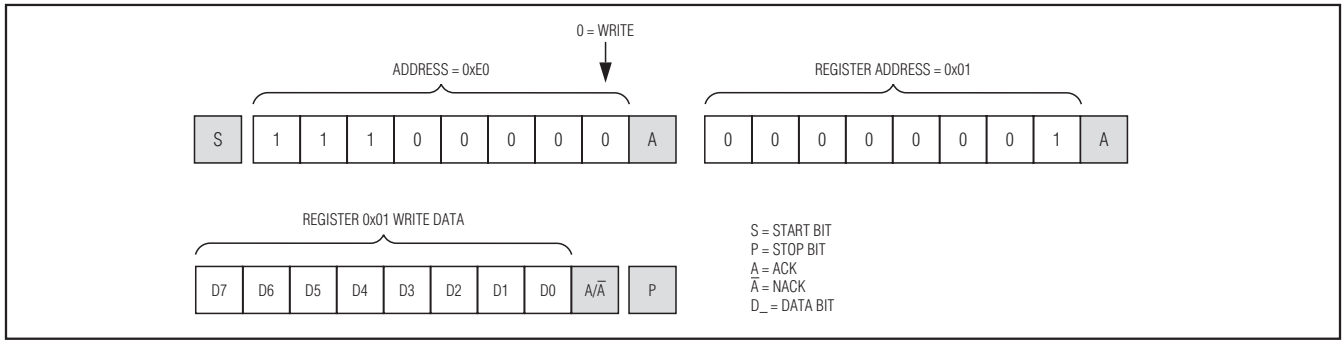



*Figure 17. Format for I²C Write. In this example the register 0x01 is written.*

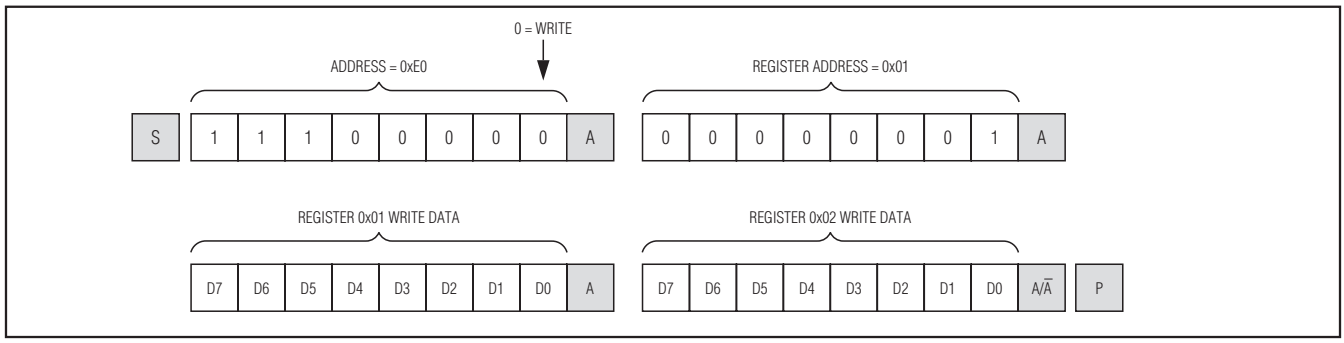



*Figure 18. Format for Writing to Multiple Registers. In this example, registers 0x01 and 0x02 are written in sequence.*

### Format for Writing

A write to the MAX14500–MAX14503 comprises the transmission of the slave address with the R/$\overline{W}$ bit set to zero, followed by at least 1 byte of information. The first byte of information is the register address or command byte. The register address determines which register of the MAX14500–MAX14503 is to be written by the next byte if received. If a STOP condition is detected after the register address is received, then the MAX14500–MAX14503 take no further action beyond storing the register address (Figure 17).

Any bytes received after the register address are data bytes. The first data byte goes into the register selected by the register address and subsequent data bytes go into subsequent registers (Figure 18). If multiple data bytes are transmitted before a STOP condition, these bytes are stored in subsequent registers because the register address autoincrements.

### Format for Reading

The MAX14500–MAX14503 are read using the internally stored register address as an address pointer, the same way the stored register address is used as an address pointer for a write. The pointer autoincrements after each data byte is read using the same rules used for a write. Thus, a read is initiated by first configuring the register address by performing a write (Figure 19). The master can now read consecutive bytes from the MAX14500–MAX14503, with the first data byte being read from the register addressed pointed by the previously written register address (Figure 20). Once the master sends a NACK, the MAX14500–MAX14503 stop sending valid data.

## Applications Information

### SD Ports

The MAX14500–MAX14503 support one or two SD cards or SD interface NAND flash memory.

### SD Ports Configuration

There are three operational configurations:

- 40-pin TQFN version, containing one host port and one SD card (Figures 1, 2)
- 56-bump WLP version, containing two SD host ports and two SD cards. There are two SD hosts and two SD memory cards. Use this mode if the host has two SD ports (Figure 3).

# Hi-Speed USB-to-SD Card Readers with Bypass

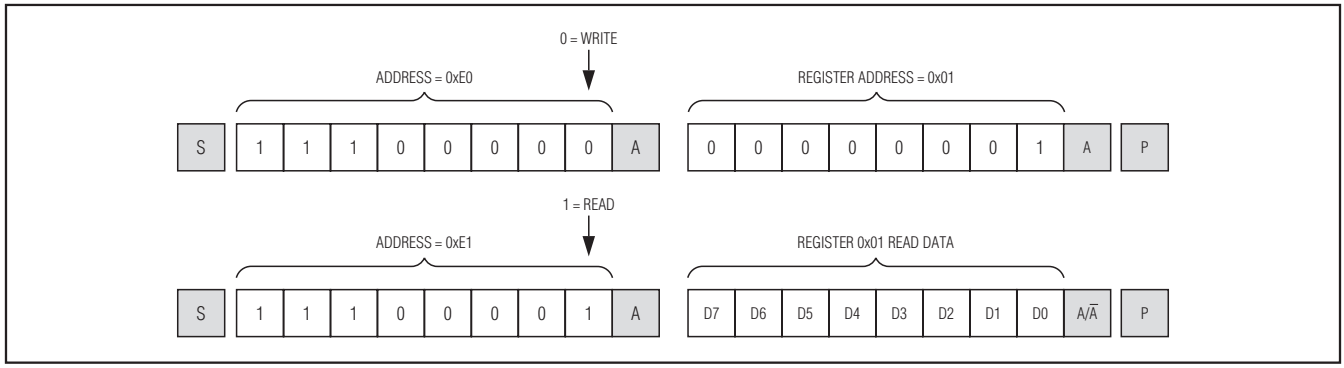



*Figure 19. Format for Reading*

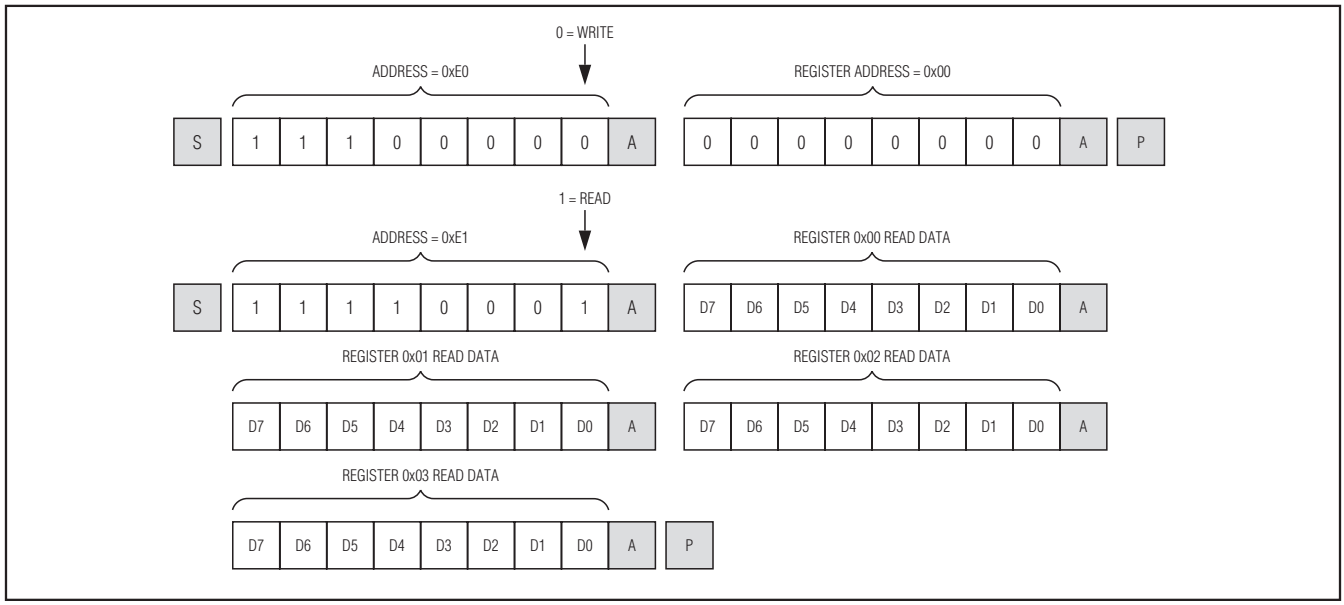



*Figure 20. Format for Reading Multiple Registers*

- 56-bump WLP version, containing one port and two SD cards. The host SD ports 1 and 2 are connected together at the host. This configuration allows two SD cards connected to one host, but only one SD card is connected to the host at a time. The host uses the MAX14500–MAX14503's internal SD port switches to multiplex between the cards. This configuration can also be used to limit the bus capacitive loading of having two cards connected at the same time to the bus (Figure 4).

### *SD Card Clock Frequency*

The SD card clock frequency is the lower of the maximum the card can support as read from the SD card and base SD clock (base SD clock is determined from values shown in Table 5). The MAX14500–MAX14503 internally read the max frequency directly from the SD card. In I²C control, the maximum clock frequency is programmable to values lower than the maximum allowed by the SD card, helping with issues such as excessive bus capacitance causing data errors.

## Table 5. Maximum SD Card Clock Frequency

| INPUT FREQUENCY (MHz) | BASE SD CLOCK (MHz) |
|---|---|
| 12 | 48 |
| 13 | 52 |
| 19.2 | 48 |
| 26 | 52 |

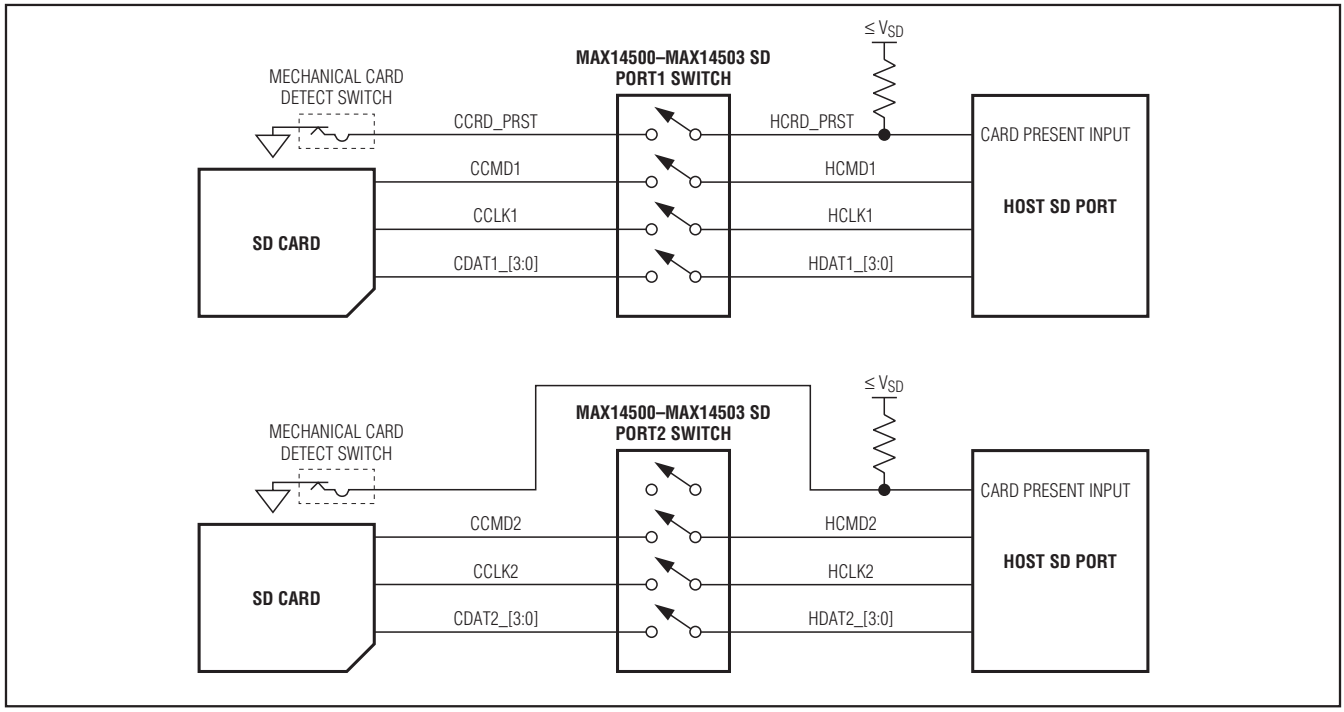



*Figure 21. Host Card Detection Schemes*

### SD Port Switches

The SD port analog switches change states immediately whether the MAX14500–MAX14503 are in Sleep mode (WAKEUP = 0) or awake. If the internal USB Hi-Speed SD card reader is in operation, the SD card switches for the selected path are opened automatically. Any writes to the SD port switch bits for that path are ignored. The SD port analog switches for the path not being used for the card reader are controllable by the host µP, and any writes to these bits affect state changes immediately.

### Card Detection

The MAX14500–MAX14503 provide an analog switch to pass the card present signal on SD card slot 1. This allows the host µP to continue using the SD slot card present switch (see Figure 21). The internal analog switch can be bypassed if an alternate algorithm is used to detect card data change. The second SD card path does not provide this analog switch so if this path is used for another SD card socket, an alternate card-detection mechanism for the host µP may be needed. If the second SD card path is used for an SD interface NAND chip, no card detection is required.

The MAX14500–MAX14503 do not use the SD card slot switch to detect insertion and removals. Instead, a protocol-based detection mechanism is used that polls for the presence or absence of an SD card. This allows both path 1 and path 2 to support an SD card slot with removable SD cards without a connection between the MAX14500–MAX14503 and the SD socket card present switch. The pullup voltage for the card slot detection may be any voltage equal to or less than $V_{SD}$.

### Enumeration

The MAX14500–MAX14503 enumerate to the USB mass storage class and appear as a USB mass storage device on most operating systems.

### USB Hi-Speed vs. Full-Speed

The MAX14500–MAX14503 support USB Hi-Speed and full-speed operation. The MAX14500–MAX14503 operate at 480Mbps when plugged into a Hi-Speed USB host, and at 12Mbps when plugged into a full-speed host.

### USB VID/PID

Using $I^2C$, the MAX14500–MAX14503 have dedicated $I^2C$ registers for vendor identification (VID) and product identification (PID). The programmed 16-bit default values are shown in the *Register Map* section. The factory default values can be replaced with your company's VID and PID.

# Hi-Speed USB-to-SD Card Readers with Bypass

### Power-Supply Modes

The MAX14500–MAX14503 have four power-supply inputs (Table 6). Bypass $V_{CC}$, $V_{IO}$, $V_{SD}$, and $V_{TM}$ with high-frequency, surface-mount ceramic capacitors as close as possible to the supply pins.

## Table 6. Power-Supply Inputs

| SUPPLY | FUNCTION | RANGE (V) |
|---|---|---|
| $V_{TM}$ | USB transceiver and USB switch power | +2.91 to +3.4 |
| $V_{CC}$ | Digital core 1.8V LDO | +2.1 to +3.6 |
| $V_{SD}$ | SD card level translator and SD switches | +2.0 to +3.6 |
| $V_{IO}$ | Host microprocessor level translator | +1.5 to +3.6 |

Power-supply inputs:

1) $V_{TM}$ USB Transceiver Power. This supply powers the USB analog switches, PLL subsystem, and the USB 2.0 transceiver. This regulator can be internal to a power-management IC, or it can be discrete and is recommended to be powered from USB VBUS. This supply must be present when the MAX14500–MAX14503 are used in Card Reader mode to pass USB signals in Pass Thru mode.
2) $V_{CC}$ Digital Logic Power. This supply powers the digital logic/internal microcontroller/flash memory. There is an internal +1.8V LDO (CLDO) with shutdown controlled by the state of the MODE input and internal logic.
3) $V_{SD}$ SD Card Power. This supply powers the SD card level translator and SD card switches. $V_{SD}$ needs to be present to pass SD signals in Pass Thru mode.
4) $V_{IO}$ Host Interface Power. This supply powers the digital I/O and $I^2C$ interface.

Power modes:

1) Idle. Only $V_{IO}$ is required to be present. $I^2C$ registers can be updated, but no operation is possible.
2) Pass Thru Mode. $V_{IO}$ needs to be present so the voltage level at MODE can be detected. To allow USB pass thru, the $V_{TM}$ supply needs to be present. To allow SD pass thru, $V_{SD}$ supply needs to be present. Each supply is independent from the others and no power-supply sequencing is required.
3) Card Reader Mode. All supplies are needed. When the card reader is actively transferring data, this mode draws the most current, mainly from $V_{CC}$ and $V_{TM}$.

### Layout Considerations

The MAX14500–MAX14503 support Hi-Speed USB and requires careful PCB layout. Use controlled-impedance matched traces of equal lengths to the USB connector with no discontinuities and a minimum number of feedthroughs. All SD traces (CLK, CMD, DAT_) should be of equal lengths and as short as possible.

### Choosing Pullup Resistors

$I^2C$ requires pullup resistors to provide a logic-high level to data and clock lines. There are tradeoffs between power dissipation and speed, and a compromise must be made in choosing pullup resistor values. Every device connected to the bus introduces some capacitance, even when the device is not in operation. $I^2C$ specifies 300ns rise time to go from low to high (30% to 70%) for fast mode, which is defined for data rates up to 400kbps. To meet the rise time requirement, choose pullup resistors so the rise time ($t_R$) is less than 300ns where $t_R \approx 0.85 \times R_{PULLUP} \times C_{BUS}$. If the transition time becomes too slow, the setup and hold times may not be met and waveforms may not be recognized.

## Register Map

| FIELD NAME | READ WRITE | BITS | RESET | DESCRIPTION | VALID WHEN |
|---|---|---|---|---|---|
| **CONTROL: Control Register (0x00)** | | | | | |
| RFU | R/W | [7:5] | 000 | Reserved for future use | — |
| SD2SW | R/W | 4 | 1 | Setting of SD port 2 switches:<br>0 = open<br>1 = closed | Powered |
| SD1SW | R/W | 3 | 1 | Setting of SD port 1 switches:<br>0 = open<br>1 = closed | Powered |
| MODE | R/W | [2:1] | 00 | Activates PC USB Hi-Speed SD card reader:<br>00 = not active<br>01 = card reader active for SD port 1<br>10 = card reader active for SD port 2<br>11 = not active | WAKEUP = 1 |
| WAKEUP | R/W | 0 | 0 | Wakes the internal µC:<br>0 = requests µC to shut down<br>1 = wakes µC | Powered |
| **CONFIG1: Configuration Register 1 (0x01)** | | | | | |
| SD2ONEBIT | R/W | 7 | 0 | Force the SD port 2 bus to 1 bit mode:<br>0 = SD bus 4-bit data mode<br>1 = SD bus 1-bit data mode | Enter Card Reader mode |
| SD1ONEBIT | R/W | 6 | 0 | Force the SD port 1 bus to 1 bit mode:<br>0 = SD bus 4-bit data mode<br>1 = SD bus 1-bit data mode | Enter Card Reader mode |
| INTPULSE | R/W | 5 | 0 | INT assertion method:<br>0 = INT stays asserted until STATUS register is read<br>1 = INT asserts for 10ms pulse | WAKEUP = 1 |
| INTACTHI | R/W | 4 | 0 | INT pin active level:<br>0 = active-low<br>1 = active-high | WAKEUP = 1 |
| RFU | R/W | [3:0] | 0000 | Reserved for future use | — |
| **CONFIG2: Configuration Register 2 (0x02)** | | | | | |
| RFU | R/W | 7 | 0 | Reserved for future use | — |
| CLKSOURCE | R/W | [6:2] | 00000 | Sets the configuration for the clock input:<br>00000 = default<br>00001 = 19.2MHz rail-to-rail square wave<br>00010 = 19.2MHz low-amplitude AC-coupled sine wave<br>00101 = 13MHz rail-to-rail square wave<br>00110 = 13MHz low-amplitude AC-coupled sine wave<br>01001 = 12MHz rail-to-rail square wave<br>01010 = 12MHz low-amplitude AC-coupled sine wave<br>01101 = 26MHz rail-to-rail square wave<br>01110 = 26MHz low-amplitude AC-coupled sine wave<br>All other values = default | Enter Card Reader mode |

## Register Map (continued)

| FIELD NAME | READ WRITE | BITS | RESET | DESCRIPTION | VALID WHEN |
|---|---|---|---|---|---|
| FORCEFS | R/W | 1 | 0 | Sets the maximum USB speed:<br>0 = Hi-Speed<br>1 = full speed | Enter Card Reader mode |
| RFU | R/W | 0 | 0 | Reserved for future use | — |
| **CONFIG3: Configuration Register 3 (0x03)** | | | | | |
| SD2MAXCLK | R/W | [7:4] | 0000 | Limits the max clock for SD card 2. The SD clock will be the minimum of either this register or the SD card max speed register.<br>0111 = base SD clock/64<br>0110 = base SD clock/32<br>0101 = base SD clock/16<br>0100 = base SD clock/8<br>0011 = base SD clock/4<br>0010 = base SD clock/2<br>0001 = base SD clock<br>0000 = default (base SD clock) | Enter Card Reader mode |
| SD1MAXCLK | R/W | [3:0] | 0000 | Limits the max clock for SD card 1. The SD clock will be the minimum of either this register or the SD card max speed register.<br>0111 = base SD clock/64<br>0110 = base SD clock/32<br>0101 = base SD clock/16<br>0100 = base SD clock/8<br>0011 = base SD clock/4<br>0010 = base SD clock/2<br>0001 = base SD clock<br>0000 = default (base SD clock) | Enter Card Reader mode |
| **IE1: Interrupt Enable Register 1 (0x04)** | | | | | |
| RFU | R/W | 7 | 0 | Reserved for future use | — |
| USBFS | R/W | 6 | 0 | Full-speed status change:<br>0 = disable contribution to INT<br>1 = enable contribution to INT | Powered |
| USBSR | R/W | 5 | 0 | USB suspend-resume status change:<br>0 = disable contribution to INT<br>1 = enable contribution to INT | Powered |
| VTM | R/W | 4 | 0 | $V_{TM}$ voltage-detector change:<br>0 = disable contribution to INT<br>1 = enable contribution to INT | Powered |
| VSD | R/W | 3 | 0 | $V_{SD}$ voltage-detector change:<br>0 = disable contribution to INT<br>1 = enable contribution to INT | Powered |
| KVBUS | R/W | 2 | 0 | VBUS voltage-detector change:<br>0 = disable contribution to INT<br>1 = enable contribution to INT | Powered |

## Register Map (continued)

| FIELD NAME | READ WRITE | BITS | RESET | DESCRIPTION | VALID WHEN |
|---|---|---|---|---|---|
| BUSY | R/W | 1 | 0 | $\overline{\text{BUSY}}$ state change:<br>0 = disable contribution to INT<br>1 = enable contribution to INT | Powered |
| SDSTAT | R/W | 0 | 0 | SD card status change:<br>0 = disable contribution to INT<br>1 = enable contribution to INT<br>**Note:** Reflects currently selected card in Card Reader mode | Powered |
| **IE2: Interrupt Enable Register 2 (0x05)** | | | | | |
| FWUPD | R/W | 7 | 0 | Firmware update status change:<br>0 = disable contribution to INT<br>1 = enable contribution to INT | Powered |
| RFU | R/W | [6:0] | 0000000 | Reserved for future use | — |
| **USBVIDH: USB Vendor ID High Byte (0x06)** | | | | | |
| VID 1 | R/W | [7:0] | 0x00 | Bits 15–8 of USB vendor ID reported during card reader enumeration. If this register is written, the written value is used for USB enumeration, otherwise a default VID of 0x06BA (Maxim Integrated Products) is used. | Enter Card Reader mode |
| **USBVIDL: USB Vendor ID Low Byte (0x07)** | | | | | |
| VID 2 | R/W | [7:0] | 0x00 | Bits 7–0 of USB vendor ID reported during card reader enumeration. If this register is written, the written value is used for USB enumeration, otherwise a default VID of 0x06BA (Maxim Integrated Products) is used. | Enter Card Reader mode |
| **USBPIDH: USB Product ID High Byte (0x08)** | | | | | |
| PID 1 | R/W | [7:0] | 0x00 | Bits 15–8 of USB product ID reported during card reader enumeration. If this register is written, the written value is used for USB enumeration, otherwise a default PID of 0x38A4 is used. | Enter Card Reader mode |
| **USBPIDL: USB Product ID Low Byte (0x09)** | | | | | |
| PID 2 | R/W | [7:0] | 0x00 | Bits 7–0 of USB product ID reported during card reader enumeration. If this register is written, the written value is used for USB enumeration, otherwise if zero, a default PID of 0x38A4 is used. | Enter Card Reader mode |
| **Test Register (0x0A)** | | | | | |
| Test Register | R/W | — | 0x00 | Do not write to this register | — |
| **Test Register (0x0B)** | | | | | |
| Test Register | R/W | — | 0x00 | Do not write to this register | — |
| **Test Register (0x0C)** | | | | | |
| Test Register | R/W | — | 0x00 | Do not write to this register | — |
| **Test Register (0x0D)** | | | | | |
| Test Register | R/W | — | 0x00 | Do not write to this register | — |

# Hi-Speed USB-to-SD Card Readers with Bypass

## Register Map (continued)

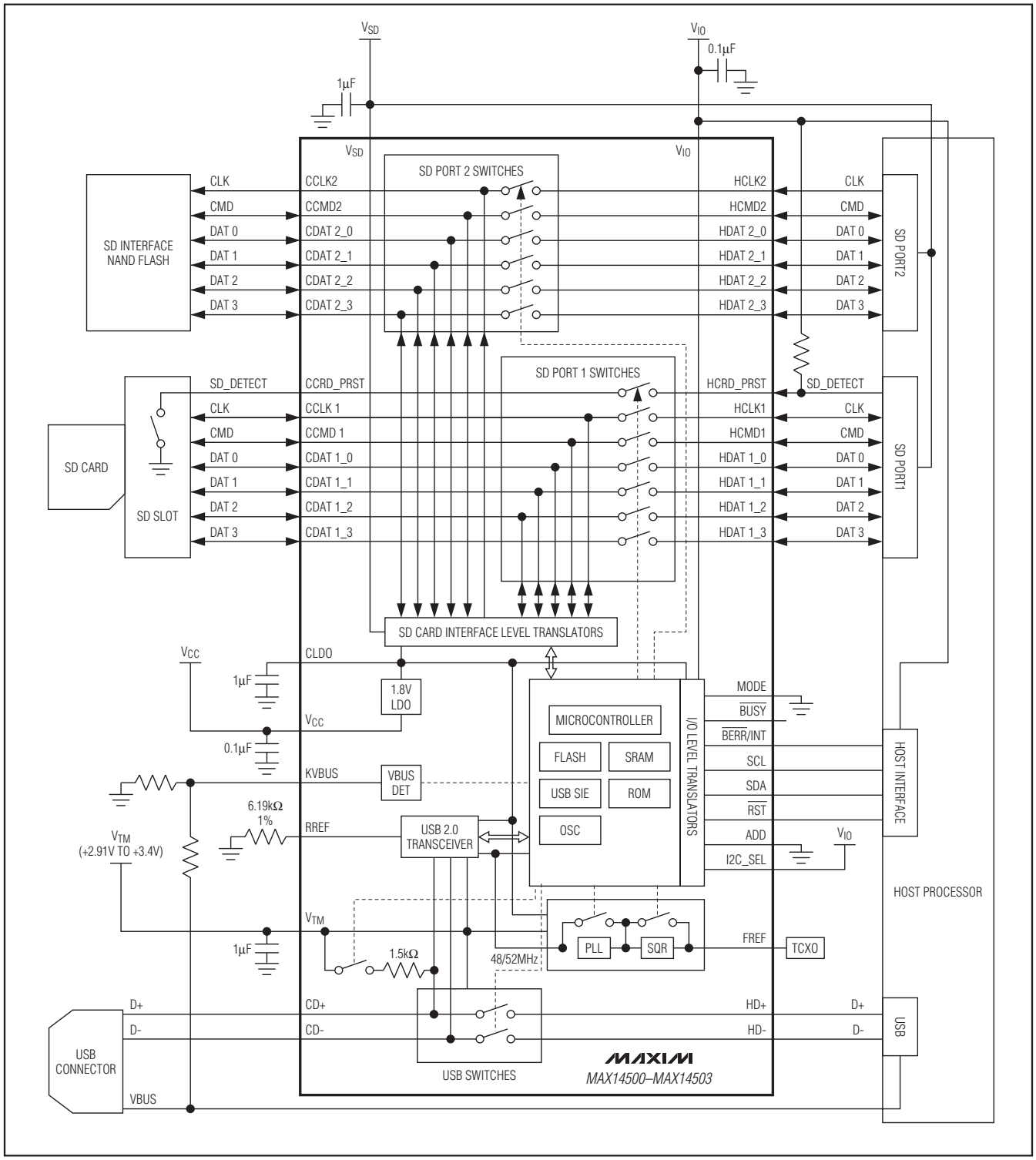
| FIELD NAME | READ WRITE | BITS | RESET | DESCRIPTION | VALID WHEN |
|---|---|---|---|---|---|
| **Test Register (0x0E)** | | | | | |
| Test Register | R/W | — | 0x00 | Do not write to this register | — |
| **FWP: Firmware Portal (0x0F)** | | | | | |
| Firmware Portal | R/W | [7:0] | 0x00 | Contact factory. Do not write to this register. | — |
| **IRQ1: Interrupt Request Register 1 (0x10)** | | | | | |
| RFU | R | 7 | | Reserved for future use | — |
| USBFS | R | 6 | | 0 = no change in USB full-speed mode status<br>1 = change in USB full-speed mode status | Enter Card Reader mode |
| USBSR | R | 5 | | 0 = no change in USB suspend/resume status<br>1 = change in USB suspend/resume status | Enter Card Reader mode |
| VTM | R | 4 | | 0 = no change in $V_{TM}$ detector status<br>1 = change in $V_{TM}$ detector status | WAKEUP = 1 |
| VSD | R | 3 | | 0 = no change in $V_{SD}$ detector status<br>1 = change in $V_{SD}$ detector status | WAKEUP = 1 |
| VBUS | R | 2 | | 0 = no change in VBUS detector status<br>1 = change in VBUS detector status | WAKEUP = 1 |
| BSY | R | 1 | | 0 = no change in $\overline{BUSY}$ status<br>1 = change in $\overline{BUSY}$ status | WAKEUP = 1 |
| SDSTAT | R | 0 | | 0 = no change in SD card present status<br>1 = change in SD card present status | Enter Card Reader mode |
| **IRQ2: Interrupt Request Register 2 (0x11)** | | | | | |
| Firmware Update | R | 7 | | Contact factory | Code download |
| RFU | R | [6:0] | | Reserved for future use | — |
| **STATUS1: Status Register 1 (0x12)** | | | | | |
| RFU | R | 7 | | Reserved for future use | — |
| USBFS | R | 6 | | 0 = no connection or Hi-Speed connection<br>1 = full-speed connection | Enter Card Reader mode |
| USBSR | R | 5 | | 0 = USB resume<br>1 = USB suspend | Enter Card Reader mode |
| VTM | R | 4 | | 0 = no voltage<br>1 = $V_{TM}$ supply present | WAKEUP = 1 |
| VSD | R | 3 | | 0 = no voltage<br>1 = $V_{SD}$ supply present | WAKEUP = 1 |
| VBUS | R | 2 | | 0 = no voltage<br>1 = VBUS supply present | WAKEUP = 1 |
| BSY | R | 1 | | 0 = not busy<br>1 = busy | WAKEUP = 1 |

## Register Map (continued)

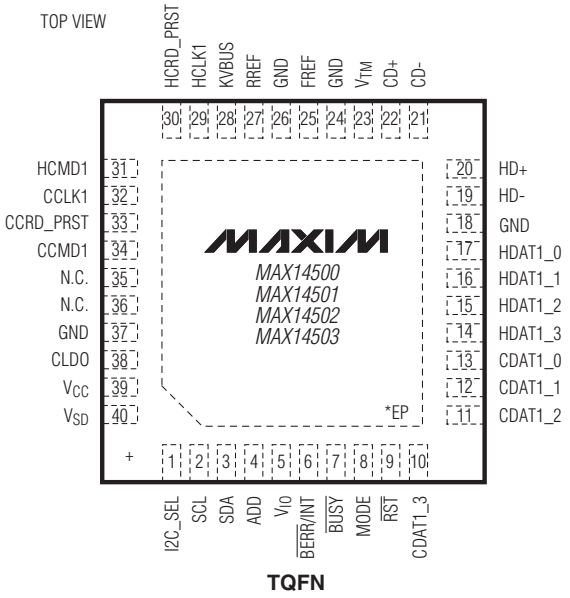
| FIELD NAME | READ WRITE | BITS | RESET | DESCRIPTION | VALID WHEN |
|---|---|---|---|---|---|
| SDSTAT | R | 0 | | The insert/removal status is only valid for the card currently set to Card Reader mode (Reg 0x00 bits 1-2)<br>0 = no card<br>1 = card present | Enter Card Reader mode |
| **STATUS2: Status Register 2 (0x13)** | | | | | |
| RFU | R | [7:0] | | Reserved for future use | — |
| **FWUGRRH: Firmware Upgrade Response Data High Byte (0x14)** | | | | | |
| High Byte of Response Data | R | [7:0] | | Contact factory | Code download |
| **FWUPGRL: Firmware Upgrade Response Data Low Byte (0x15)** | | | | | |
| Low Byte of Response Data | R | [7:0] | | Contact factory | Code download |
| **RFU Register (0x16)** | | | | | |
| RFU | R | [7:0] | | Reserved for future use | — |
| **RFU Register (0x17)** | | | | | |
| RFU | R | [7:0] | | Reserved for future use | — |
| **RFU Register (0x18)** | | | | | |
| RFU | R | [7:0] | | Reserved for future use | — |
| **RFU Register (0x19)** | | | | | |
| RFU | R | [7:0] | | Reserved for future use | — |
| **RFU Register (0x1A)** | | | | | |
| RFU | R | [7:0] | | Reserved for future use | — |
| **Firmware Incremental Revision (0x1B)** | | | | | |
| Firmware Incremental Revision | R | [7:0] | | Firmware incremental revision | WAKEUP = 1 |
| **Firmware Minor Revision (0x1C)** | | | | | |
| Firmware Minor Revision | R | [7:0] | | Firmware minor revision | WAKEUP = 1 |
| **Firmware Major Revision (0x1D)** | | | | | |
| Firmware Major Revision | R | [7:0] | | Firmware major revision | WAKEUP = 1 |
| **Chip Revision (0x1E)** | | | | | |
| Chip Revision | R | [7:0] | | Chip revision | WAKEUP = 1 |
| **Package Type (0x1F)** | | | | | |
| Package Type | R | [7:0] | | 0x00 = 40-lead TQFN<br>0x05 = 56-bump WLP<br>0xFF = unknown | WAKEUP = 1 |

# Hi-Speed USB-to-SD Card Readers with Bypass

## Functional Diagram



## Pin Configurations



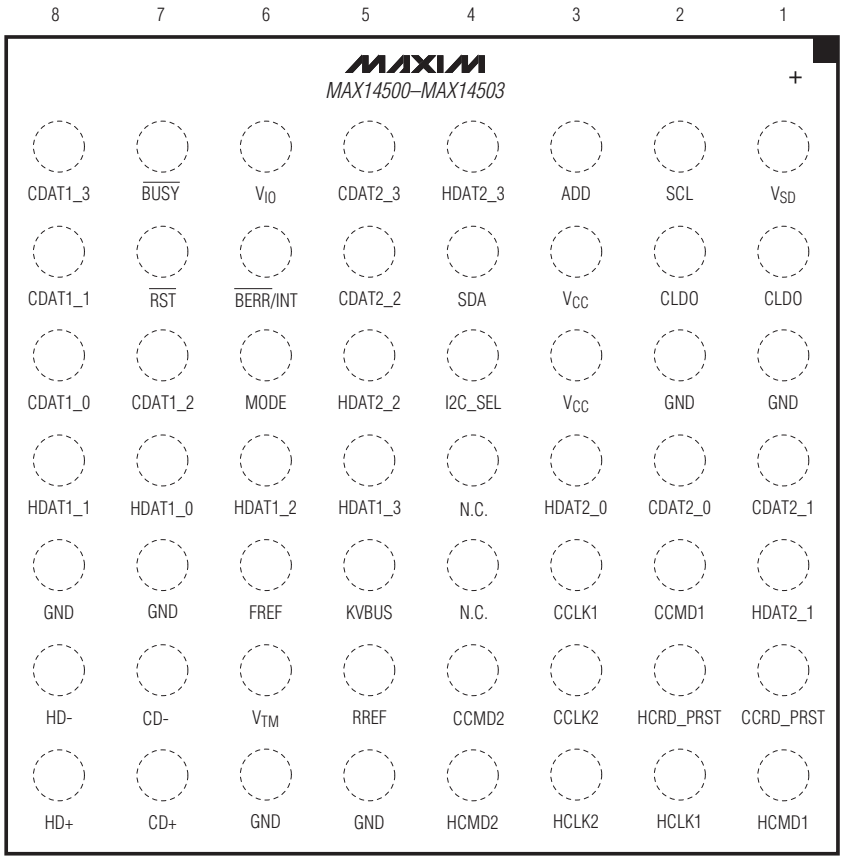

**TQFN**

*CONNECT EXPOSED PAD TO GND.

# Hi-Speed USB-to-SD Card Readers with Bypass

## Pin Configurations (continued)

TOP VIEW
(BUMPS ON BOTTOM)




**WLP**

## Chip Information

PROCESS: CMOS

## Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | DOCUMENT NO. |
|---|---|---|
| 40 TQFN-EP | T4055-1 | **21-0140** |
| 56 WLP | W563B3+1 | **21-0090** |

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 4/08 | Initial release | — |
| 1 | 4/09 | Fixed data sheet to reflect new rev material including *EC table*, *Pin Description*, *Applications Information*, *Functional Diagram*, and *Pin Configurations* | 1–41 |