Teridian Smart Grid Solutions

# 71M6521DE/DH/FE Energy Meter ICs

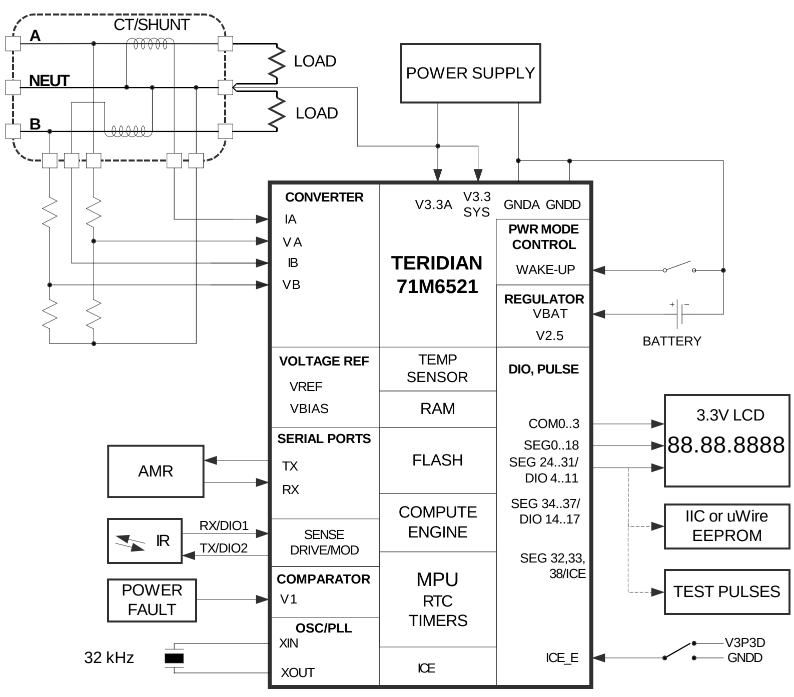
DATA SHEET

## GENERAL DESCRIPTION

The Teridian™ 71M6521DE/DH/FE energy meter ICs are highly integrated systems-on-a-chip (SoCs) with an MPU core, RTC, flash, and LCD driver. The Single Converter Technology® with a 22-bit delta-sigma ADC, four analog inputs, digital temperature compensation, precision voltage reference, battery voltage monitor, and 32-bit computation engine (CE) supports a wide range of residential metering applications with very few low-cost external components. A 32kHz crystal time base for the entire system and internal battery-backup support for RAM and RTC further reduce system cost. The ICs support 2-wire, 3-wire, and 4-wire single-phase and dual-phase residential metering along with tamper-detection mechanisms.

Maximum design flexibility is provided by multiple UARTs, $I^2C$, MICROWIRE®, up to 18 DIO pins, and in-system programmable flash memory, which can be updated with data or application code in operation.

A complete array of ICE and development tools, programming libraries, and reference designs enable rapid development and certification of TOU, AMR, and prepay meters that comply with worldwide electricity metering standards.

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*MICROWIRE is a registered trademark of National Semiconductor Corp.*

## FEATURES

- Up to 0.1% Wh Accuracy Over 2000:1 Current Range
- Exceeds IEC 62053/ANSI C 12.20 Standards
- Voltage Reference < 40 ppm/°C (< 20ppm/°C for 71M6521DH)
- Four Sensor Inputs—$V_{DD}$ Referenced
- Low-Jitter Wh and VARh Pulse Test Outputs (10kHz max)
- Pulse Count for Pulse Outputs
- Four-Quadrant Metering
- Tamper Detection
  - Neutral Current with CT or Shunt
- Line Frequency Count for RTC
- Digital Temperature Compensation
- Sag Detection for Phase A and B
- Independent 32-Bit Compute Engine
- 46-64Hz Line Frequency Range with Same Calibration
- Phase Compensation (±7°)
- Battery backup for RTC and battery monitor
- Three Battery Modes with Wake-Up on Pushbutton or Timer:
  - Brownout Mode (48µA)
  - LCD Mode (5.7µA)
  - Sleep Mode (2.9µA)
- Energy Display on Main Power Failure
- Wake-Up with Pushbutton
- 22-Bit Delta-Sigma ADC
- 8-Bit MPU (80515), 1 Clock Cycle per Instruction with Integrated ICE for MPU Debug
- RTC with Temperature Compensation
- Auto-Calibration
- Hardware Watchdog Timer, Power-Fail Monitor
- LCD Driver (Up to 152 Pixels)
- Up to 18 General-Purpose I/O Pins
- 32kHz Time Base
- 16KB (6521DE/DH) or 32KB (6521FE) Flash with Security
- 2KB MPU XRAM
- Two UARTs for IR and AMR
- Digital I/O Pins Compatible with 5V Inputs
- 64-Pin LQFP or 68-Pin QFN Package
- Lead(Pb)-Free Packages

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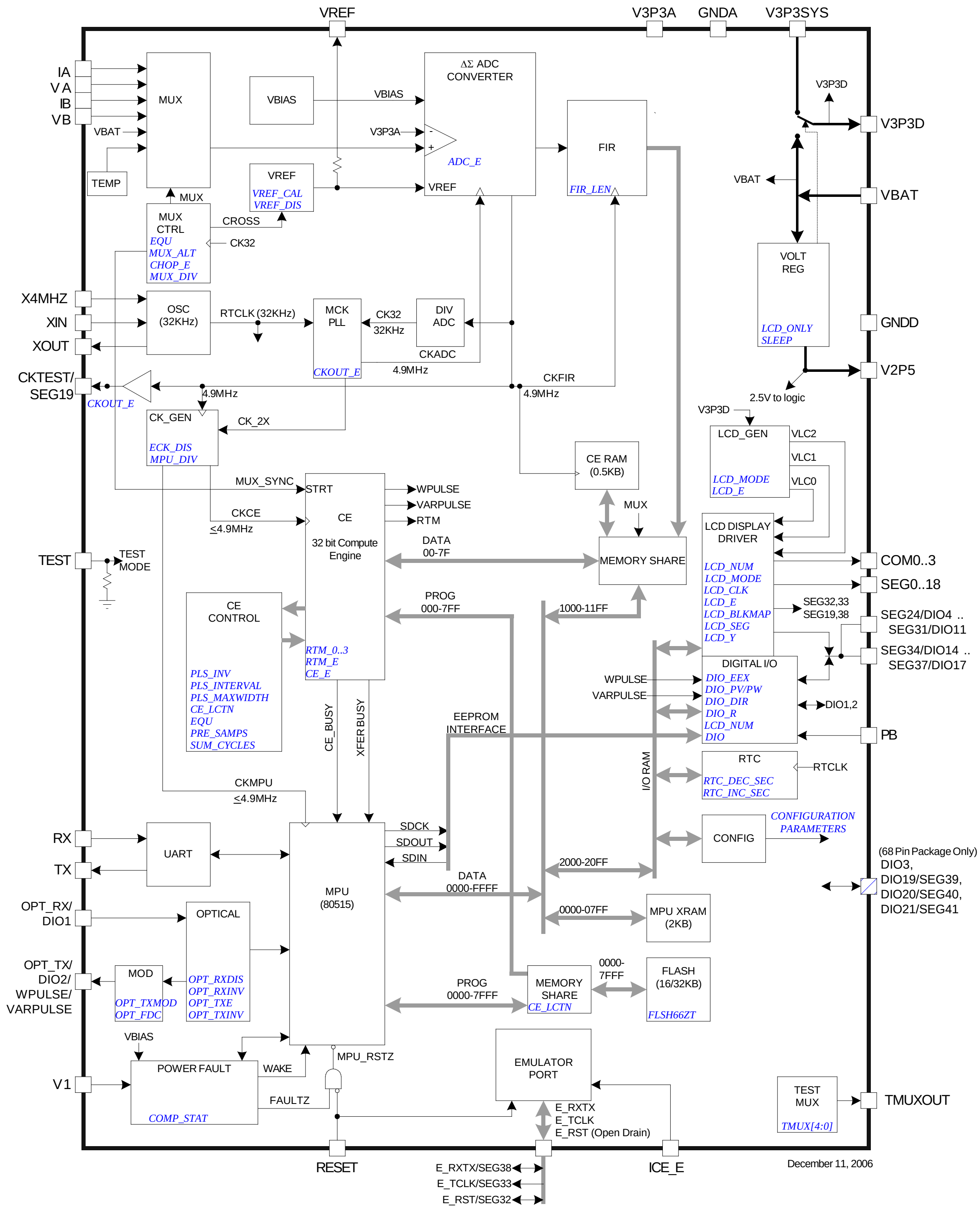



**Figure 1: IC Functional Block Diagram**

# HARDWARE DESCRIPTION

## Hardware Overview

The Teridian 71M6521DE/DH/FE single-chip energy meter integrates all primary functional blocks required to implement a solid-state electricity meter. Included on chip are an analog front end (AFE), an independent digital computation engine (CE), an 8051-compatible microprocessor (MPU) which executes one instruction per clock cycle (80515), a voltage reference, a temperature sensor, LCD drivers, RAM, flash memory, a real time clock (RTC), and a variety of I/O pins. Various current sensor technologies are supported including Current Transformers (CT), and Resistive Shunts.

In a typical application, the 32-bit compute engine (CE) of the 71M6521DE/DH/FE sequentially processes the samples from the voltage inputs on pins IA, VA, IB, VB and performs calculations to measure active energy (Wh), reactive energy (VARh), $A^2$h, and $V^2$h for four-quadrant metering. These measurements are then accessed by the MPU, processed further and output using the peripheral devices available to the MPU.

In addition to advanced measurement functions, the real time clock function allows the 71M6521DE/DH/FE to record time of use (TOU) metering information for multi-rate applications and to time-stamp tamper events. Measurements can be displayed on 3.3V LCD commonly used in low temperature environments. Flexible mapping of LCD display segments will facilitate integration of existing custom LCD. Design trade-off between number of LCD segments vs. DIO pins can be implemented in software to accommodate various requirements.

In addition to the temperature-trimmed ultra-precision voltage reference, the on-chip digital temperature compensation mechanism includes a temperature sensor and associated controls for correction of unwanted temperature effects on measurement and RTC accuracy, e.g. to meet the requirements of ANSI and IEC standards. Temperature dependent external components such as crystal oscillator, current transformers (CTs), and their corresponding signal conditioning circuits can be characterized and their correction factors can be programmed to produce electricity meters with exceptional accuracy over the industrial temperature range.

The 71M6521DH is trimmed at +85°C in addition to the trim at room temperature, which provides a set of individualized trim fuse values that enable temperature compensation with accuracy better than ±20 PPM/°C.

One of the two internal UARTs is adapted to support an Infrared LED with internal drive and sense configuration, and can also function as a standard UART. The optical output can be modulated at 38 kHz. This flexibility makes it possible to implement AMR meters with an IR interface. A block diagram of the IC is shown in Figure 1. A detailed description of various functional blocks follows.

## Analog Front End (AFE)

The AFE of the 71M6521DE/DH/FE is composed of an input multiplexer, a delta-sigma A/D converter and a voltage reference.

### Input Multiplexer

The input multiplexer supports up to four input signals that are applied to pins IA, VA, IB and VB of the device. Additionally, using the alternate mux selection, it has the ability to select temperature and the battery voltage. The multiplexer can be operated in two modes:

- During a normal multiplexer cycle, the signals from the IA, IB, VA, and VB pins are selected.
- During the alternate multiplexer cycle, the temperature signal (TEMP) and the battery monitor are selected, along with the signal sources shown in Table 1. To prevent unnecessary drainage on the battery, the battery monitor is enabled only with the *BME* bit (0x2020[6]) in the I/O RAM.

The alternate mux cycles are usually performed infrequently (e.g. every second) by the MPU. In order to prevent disruption of the voltage tracking PLL and voltage allpass networks, VA is not replaced in the ALT mux selections. Table 1 details the regular and alternative MUX sequences. Missing samples due to an ALT multiplexer sequence are filled in by the CE.

| | Regular MUX Sequence | | | | ALT MUX Sequence | | | |
|---|---|---|---|---|---|---|---|---|
| | Mux State | | | | Mux State | | | |
| *EQU* | **0** | **1** | **2** | **3** | **0** | **1** | **2** | **3** |
| 0, 1, 2 | IA | VA | IB | VB | TEMP | VA | VBAT | VB |

**Table 1: Inputs Selected in Regular and Alternate Multiplexer Cycles**

In a typical application, IA and IB are connected to current transformers that sense the current on each phase of the line voltage. VA and VB are typically connected to voltage sensors through resistor dividers.

The multiplexer control circuit handles the setting of the multiplexer. The function of the control circuit is governed by the I/O RAM registers *MUX_ALT, MUX_DIV* and *EQU*. *MUX_DIV* controls the number of samples per cycle. It can request 2, 3, or 4 multiplexer states per cycle. Multiplexer states above 4 are reserved and must not be used. The multiplexer always starts at the beginning of its list and proceeds until *MUX_DIV* states have been converted.

The *MUX_ALT* bit requests an alternative multiplexer frame. The bit may be asserted on any MPU cycle and may be subsequently de-asserted on any cycle including the next one. A rising edge on *MUX_ALT* will cause the multiplexer control circuit to wait until the next multiplexer cycle and implement a single alternate cycle.

The multiplexer control circuit also controls the FIR filter initiation and the chopping of the ADC reference voltage, VREF. The multiplexer control circuit is clocked by CK32, the 32768Hz clock from the PLL block, and launches with each new pass of the CE program.

## A/D Converter (ADC)

A single delta-sigma A/D converter digitizes the voltage and current inputs to the 71M6521DE/DH/FE. The resolution of the ADC is programmable using the *FIR_LEN* register as shown in the I/O RAM section. ADC resolution can be selected to be 21 bits (*FIR_LEN*=0), or 22 bits (*FIR_LEN*=1). Conversion time is two cycles of CK32 with *FIR_LEN* = 0 and three cycles with *FIR_LEN* = 1.

**In order to provide the maximum resolution, the ADC should be operated with *FIR_LEN* = 1. Accuracy and timing specifications in this data sheet are based on *FIR_LEN* = 1.**

Initiation of each ADC conversion is controlled by the multiplexer control circuit as described previously. At the end of each ADC conversion, the FIR filter output data is stored into the CE DRAM location determined by the multiplexer selection.

## FIR Filter

The finite impulse response filter is an integral part of the ADC and it is optimized for use with the multiplexer. The purpose of the FIR filter is to decimate the ADC output to the desired resolution. At the end of each ADC conversion, the output data is stored into the fixed CE DRAM location determined by the multiplexer selection. FIR data is stored LSB justified, but shifted left by nine bits.

## Voltage References

The device includes an on-chip precision bandgap voltage reference that incorporates auto-zero techniques. The reference is trimmed to minimize errors caused by component mismatch and drift. The result is a voltage output with a predictable temperature coefficient.

The amplifier within the reference is chopper stabilized, i.e. the polarity can be switched by the MPU using the I/O RAM register *CHOP_E* (0x2002[5:4]). The two bits in the *CHOP_E* register enable the MPU to operate the chopper circuit in regular or inverted operation, or in "toggling" mode. When the chopper circuit is toggled in between multiplexer cycles, DC offsets on the measured signals will automatically be averaged out.

The general topology of a chopped amplifier is given in Figure 2.

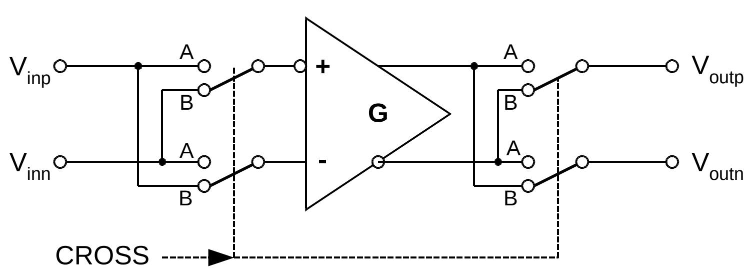



**Figure 2: General Topology of a Chopped Amplifier**

It is assumed that an offset voltage Voff appears at the positive amplifier input. With all switches, as controlled by CROSS in the “A” position, the output voltage is:

Voutp – Voutn = G (Vinp + Voff – Vinn) = G (Vinp – Vinn) + G Voff

With all switches set to the “B” position by applying the inverted CROSS signal, the output voltage is:

Voutn – Voutp = G (Vinn – Vinp + Voff) = G (Vinn – Vinp) + G Voff, or

Voutp – Voutn = G (Vinp – Vinn) - G Voff

Thus, when CROSS is toggled, e.g. after each multiplexer cycle, the offset will alternately appear on the output as positive and negative, which results in the offset effectively being eliminated, regardless of its polarity or magnitude.

When CROSS is high, the hookup of the amplifier input devices is reversed. This preserves the overall polarity of that amplifier gain; it inverts its input offset. By alternately reversing the connection, the amplifier’s offset is averaged to zero. This removes the most significant long-term drift mechanism in the voltage reference. The *CHOP_E* bits control the behavior of CROSS. The CROSS signal will reverse the amplifier connection in the voltage reference in order to negate the effects of its offset. On the first CK32 rising edge after the last mux state of its sequence, the mux will wait one additional CK32 cycle before beginning a new frame. At the beginning of this cycle, the value of CROSS will be updated according to the *CHOP_E* bits. The extra CK32 cycle allows time for the chopped VREF to settle. During this cycle, MUXSYNC is held high. The leading edge of muxsync initiates a pass through the CE program sequence. The beginning of the sequence is the serial readout of the 4 RTM words.

*CHOP_E* has 3 states: positive, reverse, and chop. In the ‘positive’ state, CROSS is held low. In the ‘reverse’ state, CROSS is held high. In the ‘chop’ state, CROSS is toggled near the end of each Mux Frame, as described above. It is desirable that CROSS take on alternate values at the beginning of each Mux cycle. For this reason, if ‘chop’ state is selected, CROSS will not toggle at the end of the last Mux cycle in a SUM cycle.

The internal bias voltage VBIAS (typically 1.6 V) is used by the ADC when measuring the temperature and battery monitor signals.

## Temperature Sensor

The 71M6521DE/DH/FE includes an on-chip temperature sensor implemented as a bandgap reference. It is used to determine the die temperature The MPU may request an alternate multiplexer cycle containing the temperature sensor output by asserting *MUX_ALT*.

The primary use of the temperature data is to determine the magnitude of compensation required to offset the thermal drift in the system (see section titled “Temperature Compensation”).

## Battery Monitor

The battery voltage is measured by the ADC during alternative multiplexer frames if the *BME* (Battery Measure Enable) bit in the I/O RAM is set. While *BME* is set, an on-chip 45kΩ load resistor is applied to the battery, and a scaled fraction of the battery voltage is applied to the ADC input. After each alternative MUX frame, the result of the ADC conversion is available at CE DRAM address 07. *BME* is ignored and assumed zero when system power is not available (V1 < VBIAS). See the Battery Monitor section of the Electrical Specifications for details regarding the ADC LSB size and the conversion accuracy.

## Functional Description

The AFE functions as a data acquisition system, controlled by the MPU. The main signals (IA, VA, IB, VB) are sampled and the ADC counts obtained are stored in CE DRAM where they can be accessed by the CE and, if necessary, by the MPU. Alternate multiplexer cycles are initiated less frequently by the MPU to gather access to the slow temperature and battery signals.

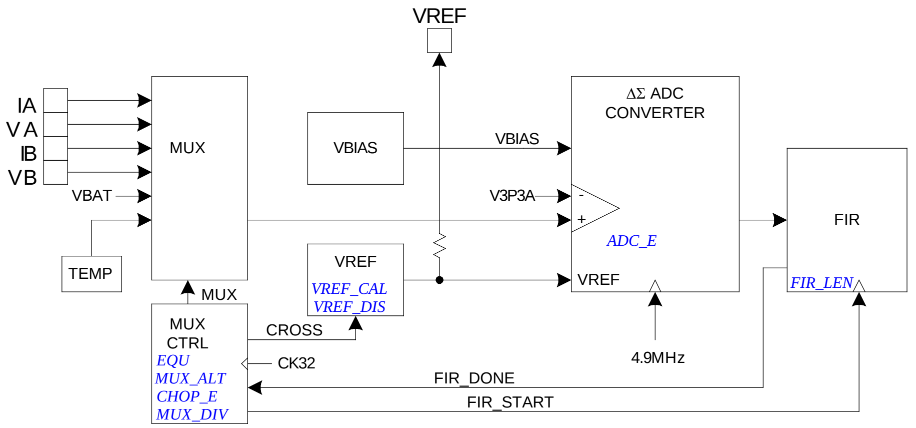



**Figure 3: AFE Block Diagram**

# Digital Computation Engine (CE)

The CE, a dedicated 32-bit signal processor, performs the precision computations necessary to accurately measure energy. The CE calculations and processes include:

- Multiplication of each current sample with its associated voltage sample to obtain the energy per sample (when multiplied with the constant sample time).
- Frequency-insensitive delay cancellation on all six channels (to compensate for the delay between samples caused by the multiplexing scheme).
- 90° phase shifter (for VAR calculations).
- Pulse generation.
- Monitoring of the input signal frequency (for frequency and phase information).
- Monitoring of the input signal amplitude (for sag detection).
- Scaling of the processed samples based on calibration coefficients.

The CE program resides in flash memory. Common access to flash memory by CE and MPU is controlled by a memory share circuit. Each CE instruction word is two bytes long. Allocated flash space for the CE program cannot exceed 1024 words (2KB). The CE program counter begins a pass through the CE code each time multiplexer state 0 begins. The code pass ends when a HALT instruction is executed. For proper operation, the code pass must be completed before the multiplexer cycle ends (see System Timing Summary in the Functional Description Section).

The CE program must begin on a 1Kbyte boundary of the flash address. The I/O RAM register *CE_LCTN[4:0]* defines which 1KB boundary contains the CE code. Thus, the first CE instruction is located at 1024**CE_LCTN[4:0]*.

The CE DRAM can be accessed by the FIR filter block, the RTM circuit, the CE, and the MPU. Assigned time slots are reserved for FIR, RTM, and MPU, respectively, to prevent bus contention for CE DRAM data access. Holding registers are used to convert 8-bit wide MPU data to/from 32-bit wide CE DRAM data, and wait states are inserted as needed, depending on the frequency of CKMPU.

The CE DRAM contains 128 32-bit words. The MPU can read and write the CE DRAM as the primary means of data communication between the two processors.

Table 2 shows the CE DRAM addresses allocated to analog inputs from the AFE.

| ADDRESS (HEX) | NAME | DESCRIPTION |
|---|---|---|
| 00 | IA | Phase A current |
| 01 | VA | Phase A voltage |
| 02 | IB | Phase B current |
| 03 | VB | Phase B voltage |
| 04 | - | Not used |
| 05 | - | Not used |
| 06 | TEMP | Temperature |
| 07 | VBAT | Battery Voltage |

**Table 2: CE DRAM Locations for ADC Results**

The CE of the 71M6521DE/DH/FE is aided by support hardware that facilitates implementation of equations, pulse counters, and accumulators. This support hardware is controlled through I/O RAM locations *EQU* (equation assist), *DIO_PV* and *DIO_PW* (pulse count assist), and *PRE_SAMPS* and *SUM_CYCLES* (accumulation assist). *PRE_SAMPS* and *SUM_CYCLES* support a dual level accumulation scheme where the first accumulator accumulates results from *PRE_SAMPS* samples and the second accumulator accumulates up to *SUM_CYCLES* of the first accumulator results. The integration time for each energy output is *PRE_SAMPS* * *SUM_CYCLES*/2520.6 (with *MUX_DIV* = 1). CE hardware issues the XFER_BUSY interrupt when the accumulation is complete.

## Meter Equations

Compute Engine (CE) firmware and hardware for residential meter configurations implement the equations listed in Table 3. The register *EQU* (located in the I/O RAM) specifies the equation to be used based on the number of phases used for metering.

| *EQU* | Description | Watt & VAR Formula | |
|---|---|---|---|
| | | Element 0 | Element 1 |
| 0 | 1 element, 2W 1$\phi$ with neutral current sense and tamper detection (VA connected to VB) | VA IA | VA IB |
| 1 | 1 element, 3W 1$\phi$ | VA(IA-IB)/2 | N/A |
| 2 | 2 element, 4W 2$\phi$ | VA IA | VB IB |

**Table 3: Meter Equations.**

## Real-Time Monitor

The CE contains a Real-Time Monitor (RTM), which can be programmed through the UART to monitor four selectable CE DRAM locations at full sample rate. The four monitored locations are serially output to the TMUXOUT pin via the digital output multiplexer at the beginning of each CE code pass. The RTM can be enabled and disabled with *RTM_EN*. The RTM output is clocked by CKTEST. Each RTM word is clocked out in 35 cycles and contains a leading flag bit. See the Functional Description section for the RTM output format. RTM is low when not in use.

## Pulse Generator

The chip contains two pulse generators that create low-jitter pulses at a rate set by either CE or MPU. The function is distinguished by *EXT_PULSE* (a CE input variable in CE DRAM):

- If *EXT_PULSE* = 1, *APULSEW***WRATE* and *APULSER***WRATE* control the pulse rate (external pulse generation)
- If *EXT_PULSE* is 0, *APULSEW* is replaced with *WSUM_X* and *APULSER* is replaced with *VARSUM_X* (internal pulse generation).

The I/O RAM bits *DIO_PV* and *DIO_PW,* as described in the Digital I/O section, can be programmed to route WPULSE to the output pin DIO6 and VARPULSE to the output pin DIO7. Pulses can also be output on OPT_TX (see *OPT_TXE[1:0]* for details).

During each CE code pass, the hardware stores exported sign bits in an 8-bit FIFO and outputs them at a specified interval. This permits the CE code to calculate all of the pulse generator outputs at the beginning of its code pass and to rely on hardware to spread them over the MUX frame. The FIFO is reset at the beginning of each MUX frame. *PLS_INTERVAL* controls the delay to the first pulse update and the interval between subsequent updates. Its LSB is four CK_FIR cycles, or 4 * 203ns. If *PLS_INTERVAL* is zero, the FIFO is deactivated and the pulse outputs are updated immediately. Thus, NINTERVAL is *4*PLS_INTERVAL.*

For use with the supplied standard Teridian CE code, *PLS_INTERVAL* is set to a fixed value of 81. *PLS_INTERVAL* is specified so that all of the pulse updates are output <u>before</u> the MUX frame completes.

On-chip hardware provides a maximum pulse width feature: *PLS_MAXWIDTH[7:0]* selects a maximum negative pulse width to be 'Nmax' updates per multiplexer cycle according to the formula: Nmax = (2**PLS_MAXWIDTH*+1). If *PLS_MAXWIDTH* = 255, no width checking is performed.

Given that *PLS_INTERVAL* = 81, the maximum pulse width is determined by:

Maximum Pulse Width = (2 * *PLS_MAXWIDTH* +1) * 81*4*203ns = 65.9µs + *PLS_MAXWIDTH* * 131.5µs

If the pulse period corresponding to the pulse rate exceeds the desired pulse width, a square wave with 50% duty-cycle is generated.

The CE pulse output polarity is programmable to be either positive or negative. Pulse polarity may be inverted with *PLS_INV*. When this bit is set, the pulses are active high, rather than the more usual active low.

## CE Functional Overview

The ADC processes one sample per channel per multiplexer cycle. Figure 4 shows the timing of the samples taken during one multiplexer cycle.

The number of samples processed during one accumulation cycle is controlled by the I/O RAM registers *PRE_SAMPS* (0x2001[7:6]) and *SUM_CYCLES* (0x2001[5:0]). The integration time for each energy output is

*PRE_SAMPS* * *SUM_CYCLES* / 2520.6, where 2520.6 is the sample rate [Hz]

For example, *PRE_SAMPS* = 42 and *SUM_CYCLES* = 50 will establish 2100 samples per accumulation cycle. *PRE_SAMPS* = 100 and *SUM_CYCLES* = 21 will result in the exact same accumulation cycle of 2100 samples or 833ms. After an accumulation cycle is completed, the XFER_BUSY interrupt signals to the MPU that accumulated data are available.

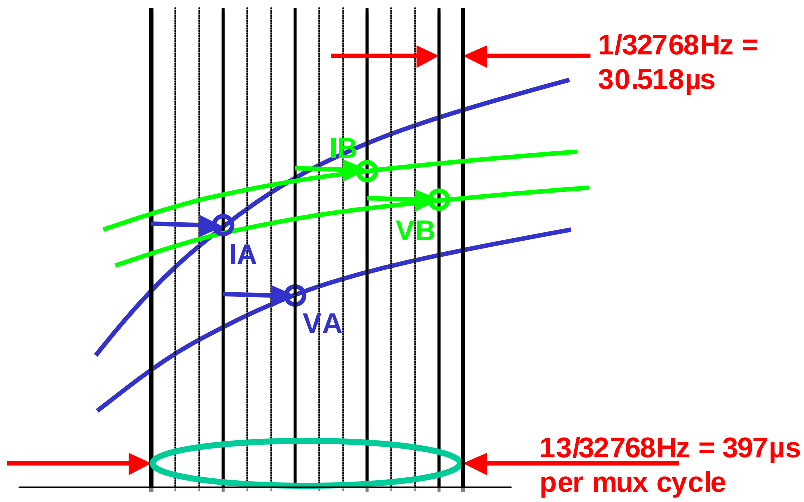



**Figure 4: Samples from Multiplexer Cycle**

The end of each multiplexer cycle is signaled to the MPU by the CE_BUSY interrupt. At the end of each multiplexer cycle, status information, such as sag data and the digitized input signal, is available to the MPU.

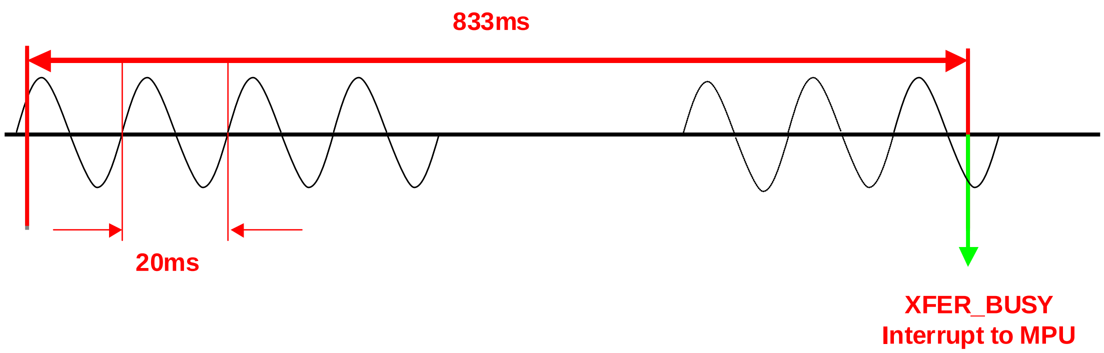



**Figure 5: Accumulation Interval**

Figure 5 shows the accumulation interval resulting from *PRE_SAMPS* = 42 and *SUM_CYCLES* = 50, consisting of 2100 samples of 397µs each, followed by the XFER_BUSY interrupt. The sampling in this example is applied to a 50Hz signal.

There is no correlation between the line signal frequency and the choice of *PRE_SAMPS* or *SUM_CYCLES* (even though when *SUM_CYCLES* = 42 one set of *SUM_CYCLES* happens to sample a period of 16.6ms). Furthermore, sampling does not have to start when the line voltage crosses the zero line, and the length of the accumulation interval need not be an integer multiple of the signal cycles.

It is important to note that the length of the accumulation interval, as determined by $N_{ACC}$, the product of *SUM_CYCLES* and *PRE_SAMPS,* is not an exact multiple of 1000ms. For example, if *SUM_CYCLES* = 60, and *PRE_SAMPS* = 00 (42), the resulting accumulation interval is:

$$\tau = \frac{N_{ACC}}{f_S} = \frac{60 \cdot 42}{\frac{32768 Hz}{13}} = \frac{2520}{2520.62 Hz} = 999.75 ms$$

This means that accurate time measurements should be based on the RTC, not the accumulation interval.

## 80515 MPU Core

The 71M6521DE/DH/FE includes an 80515 MPU (8-bit, 8051-compatible) that processes most instructions in one clock cycle. Using a 5 MHz clock results in a processing throughput of 5 MIPS. The 80515 architecture eliminates redundant bus states and implements parallel execution of fetch and execution phases. Normally a machine cycle is aligned with a memory fetch, therefore, most of the 1-byte instructions are performed in a single cycle. This leads to an 8x performance (in average) improvement (in terms of MIPS) over the Intel 8051 device running at the same clock frequency.

Actual processor clocking speed can be adjusted to the total processing demand of the application (metering calculations, AMR management, memory management, LCD driver management and I/O management) using the I/O RAM register *MPU_DIV[2:0]*.

Typical measurement and metering functions based on the results provided by the internal 32-bit compute engine (CE) are available for the MPU as part of the Teridian standard library. A standard ANSI "C" 80515-application programming interface library is available to help reduce design cycle.

## Memory Organization

The 80515 MPU core incorporates the Harvard architecture with separate code and data spaces.

Memory organization in the 80515 is similar to that of the industry standard 8051. There are three memory areas: Program memory (flash), external data memory (XRAM), physically consisting of XRAM, CE DRAM, and I/O RAM, and internal data memory (Internal RAM). Table 4 shows the memory map.

| Address (hex) | Memory Technology | Memory Type | Typical Usage | Wait States (at 5MHz) | Memory Size (bytes) |
|---|---|---|---|---|---|
| 0000-7FFF<br>0000-3FFF<br>0000-1FFF | Flash Memory | Non-volatile | MPU Program and non-volatile data | 0 | 32K<br>16K<br>8K |
| on 1K boundary | Flash Memory | Non-volatile | CE program | 0 | 2K |
| 0000-07FF | Static RAM | Volatile | MPU data XRAM, | 0 | 2K |
| 1000-11FF | Static RAM | Volatile | CE data | 6 | 512 |
| 2000-20FF | Static RAM | Volatile | Configuration RAM<br>I/O RAM | 0 | 256 |

**Table 4: Memory Map**

**Internal and External Data Memory:** Both internal and external data memory are physically located on the 71M6521DE/DH/FE IC. "External" data memory is only external to the 80515 MPU core.

**Program Memory:** The 80515 can theoretically address up to 64KB of program memory space from 0x0000 to 0xFFFF. Program memory is read when the MPU fetches instructions or performs a MOVC operation.

After reset, the MPU starts program execution from location 0x0000. The lower part of the program memory includes reset and interrupt vectors. The interrupt vectors are spaced at 8-byte intervals, starting from 0x0003.

**External Data Memory:** While the 80515 is capable of addressing up to 64KB of external data memory (0x0000 to 0xFFFF), **only the memory ranges shown in Table 4: Memory Map**

**contain physical memory.** The 80515 writes into external data memory when the MPU executes a MOVX @Ri,A or MOVX @DPTR,A instruction. The MPU reads external data memory by executing a MOVX A,@Ri or MOVX A,@DPTR instruction (SFR USR2 provides the upper 8 bytes for the MOVX A,@Ri instruction).

**Clock Stretching:** MOVX instructions can access fast or slow external RAM and external peripherals. The three low order bits of the *CKCON* register define the stretch memory cycles. Setting all the *CKCON* stretch bits to one allows access to very slow external RAM or external peripherals.

Table 5 shows how the signals of the External Memory Interface change when stretch values are set from 0 to 7. The widths of the signals are counted in MPU clock cycles. The post-reset state of the CKCON register, which is in bold in the table, performs the MOVX instructions with a stretch value equal to 1.

| *CKCON* register | | | Stretch Value | Read signals width | | Write signal width | |
|---|---|---|---|---|---|---|---|
| *CKCON.2* | *CKCON.1* | *CKCON.0* | | memaddr | memrd | memaddr | memwr |
| 0 | 0 | 0 | 0 | 1 | 1 | 2 | 1 |
| **0** | **0** | **1** | **1** | **2** | **2** | **3** | **1** |
| 0 | 1 | 0 | 2 | 3 | 3 | 4 | 2 |
| 0 | 1 | 1 | 3 | 4 | 4 | 5 | 3 |
| 1 | 0 | 0 | 4 | 5 | 5 | 6 | 4 |
| 1 | 0 | 1 | 5 | 6 | 6 | 7 | 5 |
| 1 | 1 | 0 | 6 | 7 | 7 | 8 | 6 |
| 1 | 1 | 1 | 7 | 8 | 8 | 9 | 7 |

**Table 5: Stretch Memory Cycle Width**

There are two types of instructions, differing in whether they provide an eight-bit or sixteen-bit indirect address to the external data RAM.

In the first type (MOVX A,@Ri), the contents of R0 or R1, in the current register bank, provide the eight lower-ordered bits of address. The eight high-ordered bits of address are specified with the *USR2* SFR. This method allows the user paged access (256 pages of 256 bytes each) to all ranges of the external data RAM. In the second type of MOVX instruction (MOVX A,@DPTR), the data pointer generates a sixteen-bit address. This form is faster and more efficient when accessing very large data arrays (up to 64 Kbytes), since no additional instructions are needed to set up the eight high ordered bits of address.

It is possible to mix the two MOVX types. This provides the user with four separate data pointers, two with direct access and two with paged access to the entire 64KB of external memory range.

**Dual Data Pointer:** The Dual Data Pointer accelerates the block moves of data. The standard *DPTR* is a 16-bit register that is used to address external memory or peripherals. In the 80515 core, the standard data pointer is called DPTR, the second data pointer is called *DPTR1*. The data pointer select bit chooses the active pointer. The data pointer select bit is located at the LSB of the *DPS* register (*DPS.0*). *DPTR* is selected when *DPS.0* = 0 and *DPTR1* is selected when *DPS.0* = 1.

The user switches between pointers by toggling the LSB of the DPS register. All data pointer-related instructions use the currently selected data pointer for any activity.

**The second data pointer may not be supported by certain compilers.**

**Internal Data Memory:** The Internal data memory provides 256 bytes (0x00 to 0xFF) of data memory. The internal data memory address is always 1 byte wide and can be accessed by either direct or indirect addressing. The Special Function Registers occupy the upper 128 bytes**. This SFR area is available only by direct addressing. Indirect addressing accesses the upper 128 bytes of Internal RAM.**

**Internal Data Memory:** The lower 128 bytes contain working registers and bit-addressable memory. The lower 32 bytes form four banks of eight registers (R0-R7). Two bits on the program memory status word (PSW) select which bank is in use. The next 16 bytes form a block of bit-addressable memory space at bit addressees 0x00-0x7F. All of the bytes in the lower 128 bytes are accessible through direct or indirect addressing. Table 6 shows the internal data memory map.

| Address | Direct addressing | Indirect addressing |
|---|---|---|
| 0xFF | Special Function Registers (SFRs) | **RAM** |
| 0x80 | | |
| 0x7F | Byte-addressable area | |
| 0x30 | | |
| 0x2F | Bit-addressable area | |
| 0x20 | | |
| 0x1F | **Register banks R0…R7** | |
| 0x00 | | |

**Table 6: Internal Data Memory Map**

## Special Function Registers (SFRs)

A map of the Special Function Registers is shown in Table 7.

| Hex\Bin | Bit-address-able | Byte-addressable | | | | | | | Bin/Hex |
|---|---|---|---|---|---|---|---|---|---|
| | X000 | X001 | X010 | X011 | X100 | X101 | X110 | X111 | |
| F8 | ***INTBITS*** | | | | | | | | FF |
| F0 | *B* | | | | | | | | F7 |
| E8 | ***WDI*** | | | | | | | | EF |
| E0 | *A* | | | | | | | | E7 |
| D8 | *WDCON* | | | | | | | | DF |
| D0 | *PSW* | | | | | | | | D7 |
| C8 | *T2CON* | | | | | | | | CF |
| C0 | *IRCON* | | | | | | | | C7 |
| B8 | *IEN1* | *IP1* | *S0RELH* | *S1RELH* | | | | *USR2* | BF |
| B0 | | | ***FLSHCTL*** | | | | | ***PGADR*** | B7 |
| A8 | *IEN0* | *IP0* | *S0RELL* | | | | | | AF |
| A0 | ***P2*** | ***DIR2*** | ***DIR0*** | | | | | | A7 |
| 98 | *S0CON* | *S0BUF* | *IEN2* | *S1CON* | *S1BUF* | *S1RELL* | ***EEDATA*** | ***EECTRL*** | 9F |
| 90 | ***P1*** | ***DIR1*** | *DPS* | | ***ERASE*** | | | | 97 |
| 88 | *TCON* | *TMOD* | *TL0* | *TL1* | *TH0* | *TH1* | *CKCON* | | 8F |
| 80 | ***P0*** | *SP* | *DPL* | *DPH* | *DPL1* | *DPH1* | *WDTREL* | *PCON* | 87 |

**Table 7: Special Function Registers Locations**

Only a few addresses are occupied, the others are not implemented. SFRs specific to the 652X are shown in **bold** print. Any read access to unimplemented addresses will return undefined data, while any write access will have no effect. The registers at 0x80, 0x88, 0x90, etc., are bit-addressable, all others are byte-addressable.

## Special Function Registers (Generic 80515 SFRs)

Table 8 shows the location of the SFRs and the value they assume at reset or power-up.

| Name | Location | Reset value | Description |
|---|---|---|---|
| *P0* | 0x80 | 0xFF | Port 0 |
| *SP* | 0x81 | 0x07 | Stack Pointer |
| *DPL* | 0x82 | 0x00 | Data Pointer Low 0 |
| *DPH* | 0x83 | 0x00 | Data Pointer High 0 |
| *DPL1* | 0x84 | 0x00 | Data Pointer Low 1 |
| *DPH1* | 0x85 | 0x00 | Data Pointer High 1 |
| *WDTREL* | 0x86 | 0x00 | Watchdog Timer Reload register |
| *PCON* | 0x87 | 0x00 | UART Speed Control |
| *TCON* | 0x88 | 0x00 | Timer/Counter Control |
| *TMOD* | 0x89 | 0x00 | Timer Mode Control |
| *TL0* | 0x8A | 0x00 | Timer 0, low byte |
| *TL1* | 0x8B | 0x00 | Timer 1, high byte |
| *TH0* | 0x8C | 0x00 | Timer 0, low byte |
| *TH1* | 0x8D | 0x00 | Timer 1, high byte |
| *CKCON* | 0x8E | 0x01 | Clock Control (Stretch=1) |
| *P1* | 0x90 | 0xFF | Port 1 |
| *DPS* | 0x92 | 0x00 | Data Pointer select Register |
| *S0CON* | 0x98 | 0x00 | Serial Port 0, Control Register |
| *S0BUF* | 0x99 | 0x00 | Serial Port 0, Data Buffer |
| *IEN2* | 0x9A | 0x00 | Interrupt Enable Register 2 |
| *S1CON* | 0x9B | 0x00 | Serial Port 1, Control Register |
| *S1BUF* | 0x9C | 0x00 | Serial Port 1, Data Buffer |
| *S1RELL* | 0x9D | 0x00 | Serial Port 1, Reload Register, low byte |
| *P2* | 0xA0 | 0x00 | Port 2 |
| *IEN0* | 0xA8 | 0x00 | Interrupt Enable Register 0 |
| *IP0* | 0xA9 | 0x00 | Interrupt Priority Register 0 |
| *S0RELL* | 0xAA | 0xD9 | Serial Port 0, Reload Register, low byte |
| *IEN1* | 0xB8 | 0x00 | Interrupt Enable Register 1 |
| *IP1* | 0xB9 | 0x00 | Interrupt Priority Register 1 |
| *S0RELH* | 0xBA | 0x03 | Serial Port 0, Reload Register, high byte |
| *S1RELH* | 0xBB | 0x03 | Serial Port 1, Reload Register, high byte |
| *USR2* | 0xBF | 0x00 | User 2 Port, high address byte for MOVX@Ri |
| *IRCON* | 0xC0 | 0x00 | Interrupt Request Control Register |
| *T2CON* | 0xC8 | 0x00 | Polarity for INT2 and INT3 |
| *PSW* | 0xD0 | 0x00 | Program Status Word |
| *WDCON* | 0xD8 | 0x00 | Baud Rate Control Register (only WDCON.7 bit used) |
| *A* | 0xE0 | 0x00 | Accumulator |
| *B* | 0xF0 | 0x00 | B Register |

**Table 8: Special Function Registers Reset Values**

Accumulator (***ACC, A***): ***ACC* is the accumulator register. Most instructions use the accumulator to hold the operand. The mnemonics for accumulator-specific instructions refer to accumulator as "*A*", not *ACC*.**

***B* Register:** The *B* register is used during multiply and divide instructions. It can also be used as a scratch-pad register to hold temporary data.

Program Status Word (*PSW*):

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| *CV* | *AC* | *F0* | *RS1* | *RS* | *OV* | - | *P* |

**Table 9: *PSW* Register Flags**

<table>
<tr><th>Bit</th><th>Symbol</th><th>Function</th></tr>
<tr><td>PSW.7</td><td>CV</td><td>Carry flag</td></tr>
<tr><td>PSW.6</td><td>AC</td><td>Auxiliary Carry flag for BCD operations</td></tr>
<tr><td>PSW.5</td><td>F0</td><td>General purpose Flag 0 available for user.<br>F0 is not to be confused with the F0 flag in the CE STATUS register.</td></tr>
<tr><td>PSW.4</td><td>RS1</td><td rowspan="2">Register bank select control bits. The contents of RS1 and RS0 select the working register bank:
<table>
<tr><th>RS1/RS0</th><th>Bank selected</th><th>Location</th></tr>
<tr><td>00</td><td>Bank 0</td><td>(0x00 – 0x07)</td></tr>
<tr><td>01</td><td>Bank 1</td><td>(0x08 – 0x0F)</td></tr>
<tr><td>10</td><td>Bank 2</td><td>(0x10 – 0x17)</td></tr>
<tr><td>11</td><td>Bank 3</td><td>(0x18 – 0x1F)</td></tr>
</table></td></tr>
<tr><td>PSW.3</td><td>RS0</td></tr>
<tr><td>PSW.2</td><td>OV</td><td>Overflow flag</td></tr>
<tr><td>PSW.1</td><td>-</td><td>User defined flag</td></tr>
<tr><td>PSW.0</td><td>P</td><td>Parity flag, affected by hardware to indicate odd / even number of "one" bits in the Accumulator, i.e. even parity.</td></tr>
</table>

**Table 10: *PSW* Bit Functions**

**Stack Pointer (*SP*):** The stack pointer is a 1-byte register initialized to 0x07 after reset. This register is incremented before PUSH and CALL instructions, causing the stack to begin at location 0x08.

**Data Pointer:** The data pointer (*DPTR*) is 2 bytes wide. The lower part is *DPL*, and the highest is *DPH*. It can be loaded as two registers (e.g. MOV DPL,#data8). It is generally used to access external code or data space (e.g. MOVC A,@A+DPTR or MOVX A,@DPTR respectively).

**Program Counter:** The program counter (*PC*) is 2 bytes wide initialized to 0x0000 after reset. This register is incremented when fetching operation code or when operating on data from program memory.

**Port Registers:** The I/O ports are controlled by Special Function Registers *P0*, *P1*, and *P2*. The contents of the SFR can be observed on corresponding pins on the chip. Writing a '1' to any of the ports (see Table 11) causes the corresponding pin to be at high level (V3P3), and writing a '0' causes the corresponding pin to be held at low level (GND). The data direction registers *DIR0*, *DIR1*, and *DIR2* define individual pins as input or output pins (see section Digital I/O for details).

| Register | SFR Address | R/W | Description |
|---|---|---|---|
| *P0* | 0x80 | R/W | Register for port 0 read and write operations (pins DIO4…DIO7) |
| *DIR0* | 0xA2 | R/W | Data direction register for port 0. Setting a bit to 1 means that the corresponding pin is an output. |
| *P1* | 0x90 | R/W | Register for port 1 read and write operations (pins DIO8…DIO11, DIO14-DIO15) |
| *DIR1* | 0x91 | R/W | Data direction register for port 1. |
| *P2* | 0xA0 | R/W | Register for port 2 read and write operations (pins DIO16…DIO17, DIO19…DIO21) |
| *DIR2* | 0xA1 | R/W | Data direction register for port 2. |

**Table 11: Port Registers**

All DIO ports on the chip are bi-directional. Each of them consists of a Latch (SFR '*P0*' to '*P2*'), an output driver, and an input buffer, therefore the MPU can output or read data through any of these ports. Even if a DIO pin is configured as an output, the state of the pin can still be read by the MPU, for example when counting pulses issued via DIO pins that are under CE control.

The technique of reading the status of or generating interrupts based on DIO pins configured as outputs, can be used to implement pulse counting.

## Special Function Registers Specific to the 71M6521DE/DH/FE

Table 12 shows the location and description of the 71M6521DE/DH/FE-specific SFRs.

| Register | Alternative Name | SFR Address | R/W | Description |
|---|---|---|---|---|
| *ERASE* | *FLSH_ERASE* | 0x94 | W | This register is used to initiate either the Flash Mass Erase cycle or the Flash Page Erase cycle. Specific patterns are expected for *FLSH_ERASE* in order to initiate the appropriate Erase cycle (default = 0x00).<br>0x55 – Initiate Flash Page Erase cycle. Must be preceded by a write to *FLSH_PGADR* @ SFR 0xB7.<br>0xAA – Initiate Flash Mass Erase cycle. Must be preceded by a write to *FLSH_MEEN* @ SFR 0xB2 and the debug port must be enabled.<br>Any other pattern written to FLSH_ERASE will have no effect. |
| *PGADDR* | *FLSH_PGADR* | 0xB7 | R/W | Flash Page Erase Address register containing the flash memory page address (page 0 thru 127) that will be erased during the Page Erase cycle (default = 0x00).<br>Must be re-written for each new Page Erase cycle. |
| *EEDATA* | | 0x9E | R/W | $I^2C$ EEPROM interface data register |
| *EECTRL* | | 0x9F | R/W | $I^2C$ EEPROM interface control register. If the MPU wishes to write a byte of data to EEPROM, it places the data in *EEDATA* and then writes the 'Transmit' code to *EECTRL*. The write to *EECTRL* initiates the transmit sequence. See the EEPROM Interface section for a description of the command and status bits available for *EECTRL*. |

| | | | | |
|---|---|---|---|---|
| *FLSHCRL* | | 0xB2 | R/W<br><br><br><br><br><br>W<br><br><br><br>R/W<br><br><br><br>R | Bit 0 (*FLSH_PWE*): Program Write Enable:<br>0 – MOVX commands refer to XRAM Space, normal operation (default).<br>1 – MOVX @DPTR,A moves A to Program Space (Flash) @ DPTR.<br>This bit is automatically reset after each byte written to flash. Writes to this bit are inhibited when interrupts are enabled.<br>Bit 1 (*FLSH_MEEN*): Mass Erase Enable:<br>0 – Mass Erase disabled (default).<br>1 – Mass Erase enabled.<br>Must be re-written for each new Mass Erase cycle.<br>Bit 6 (*SECURE*):<br>Enables security provisions that prevent external reading of flash memory and CE program RAM. This bit is reset on chip reset and may only be set. Attempts to write zero are ignored.<br>Bit 7 (*PREBOOT*):<br>Indicates that the preboot sequence is active. |
| *WDI* | | 0xE8 | R/W<br><br><br>R/W<br><br><br>W | **Only byte operations on the whole WDI register should be used when writing**. The byte must have all bits set except the bits that are to be cleared.<br>The multi-purpose register *WDI* contains the following bits:<br>Bit 0 (*IE_XFER*): XFER Interrupt Flag:<br>This flag monitors the XFER_BUSY interrupt. It is set by hardware and must be cleared by the interrupt handler<br>Bit 1 (*IE_RTC*): RTC Interrupt Flag:<br>This flag monitors the RTC_1SEC interrupt. It is set by hardware and must be cleared by the interrupt handler<br>Bit 7 (*WD_RST*): WD Timer Reset:<br>Read: Reads the *PLL_FALL* interrupt flag<br>Write 0: Clears the *PLL_FALL* interrupt flag<br>Write 1: Resets the watch dog timer |
| *INTBITS* | INT0…INT6 | 0xF8 | R | Interrupt inputs. The MPU may read these bits to see the input to external interrupts INT0, INT1, up to INT6. These bits do not have any memory and are primarily intended for debug use |

**Table 12: Special Function Registers**

## Instruction Set

All instructions of the generic 8051 microcontroller are supported. A complete list of the instruction set and of the associated op-codes is contained in the 71M6521 Software User's Guide (SUG).

## UART

The 71M6521DE/DH/FE includes a UART (UART0) that can be programmed to communicate with a variety of AMR modules. A second UART (UART1) is connected to the optical port, as described in the optical port description.

The UARTs are dedicated 2-wire serial interfaces, which can communicate with an external host processor at up to 38,400 bits/s (with MPU clock = 1.2288MHz). The operation of each pin is as follows:

**RX**: Serial input data are applied at this pin. Conforming to RS-232 standard, the bytes are input LSB first.

**TX**: This pin is used to output the serial data. The bytes are output LSB first.

The 71M6521DE/DH/FE has several UART-related registers for the control and buffering of serial data. All UART transfers are programmable for parity enable, parity, 2 stop bits/1 stop bit and XON/XOFF options for variable communication baud rates from 300 to 38400 bps. Table 13 shows how the baud rates are calculated. Table 14 shows the selectable UART operation modes.

| | Using Timer 1 | Using Internal Baud Rate Generator |
|---|---|---|
| **UART 0** | $2^{smod} * f_{CKMPU}/ (384 * (256\text{-}TH1))$ | $2^{smod} * f_{CKMPU}/(64 * (2^{10}\text{-}S0REL))$ |
| **UART 1** | N/A | $f_{CKMPU}/(32 * (2^{10}\text{-}S1REL))$ |

**Note:** *S0REL* and *S1REL* are 10-bit values derived by combining bits from the respective timer reload registers. *SMOD* is the *SMOD* bit in the SFR *PCON*. *TH1* is the high byte of timer 1.

**Table 13: Baud Rate Generation**

| | UART 0 | UART 1 |
|---|---|---|
| **Mode 0** | N/A | Start bit, 8 data bits, parity, stop bit, variable baud rate (internal baud rate generator) |
| **Mode 1** | Start bit, 8 data bits, stop bit, variable baud rate (internal baud rate generator or timer 1) | Start bit, 8 data bits, stop bit, variable baud rate (internal baud rate generator) |
| **Mode 2** | Start bit, 8 data bits, parity, stop bit, fixed baud rate 1/32 or 1/64 of $f_{CKMPU}$ | N/A |
| **Mode 3** | Start bit, 8 data bits, parity, stop bit, variable baud rate (internal baud rate generator or timer 1) | N/A |

**Table 14: UART Modes**

Parity of serial data is available through the P flag of the accumulator. Seven-bit serial modes with parity, such as those used by the FLAG protocol, can be simulated by setting and reading bit 7 of 8-bit output data. Seven-bit serial modes without parity can be simulated by setting bit 7 to a constant 1. 8-bit serial modes with parity can be simulated by setting and reading the 9th bit, using the control bits *TB80* (*S0CON*.3) and *TB81* (*S1CON*.3) in the *S0COn* and *S1CON* SFRs for transmit and *RB81* (*S1CON*.2) for receive operations. *SM20* (*S0CON*.5) and *SM21* (*S1CON*.5) can be used as handshake signals for inter-processor communication in multi-processor systems.

Serial Interface 0 Control Register (*S0CON*).

The function of the UART0 depends on the setting of the Serial Port Control Register *S0CON*.

MSB LSB

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| *SM0* | *SM1* | *SM20* | *REN0* | *TB80* | *RB80* | *TI0* | *RI0* |

**Table 15: The *S0CON* Register**

Serial Interface 1 Control Register (*S1CON*).

The function of the serial port depends on the setting of the Serial Port Control Register *S1CON*.

MSB LSB

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| *SM* | - | *SM21* | *REN1* | *TB81* | *RB81* | *TI1* | *RI1* |

**Table 16: The *S1CON* register**

| Bit | Symbol | Function |
|---|---|---|
| *S0CON.7* | *SM0* | These two bits set the UART0 mode:<br>Mode / Description / *SM0* / *SM1*<br>0 / N/A / 0 / 0<br>1 / 8-bit UART / 0 / 1<br>2 / 9-bit UART / 1 / 0<br>3 / 9-bit UART / 1 / 1 |
| *S0CON.6* | *SM1* | |
| *S0CON.5* | *SM20* | Enables the inter-processor communication feature. |
| *S0CON.4* | *REN0* | If set, enables serial reception. Cleared by software to disable reception. |
| *S0CON.3* | *TB80* | The 9th transmitted data bit in Modes 2 and 3. Set or cleared by the MPU, depending on the function it performs (parity check, multiprocessor communication etc.) |
| *S0CON.2* | *RB80* | In modes 2 and 3 it is the 9th data bit received. In Mode 1, if *SM20* is 0, *RB80* is the stop bit. In mode 0 this bit is not used. Must be cleared by software |
| *S0CON.1* | *TI0* | Transmit interrupt flag, set by hardware after completion of a serial transfer. Must be cleared by software. |
| *S0CON.0* | *RI0* | Receive interrupt flag, set by hardware after completion of a serial reception. Must be cleared by software |

**Table 17: The *S0CON* Bit Functions**

| Bit | Symbol | Function |
|---|---|---|
| *S1CON.7* | *SM* | Sets the baud rate for UART1<br>*SM* / Mode / Description / Baud Rate<br>0 / A / 9-bit UART / variable<br>1 / B / 8-bit UART / variable |
| *S1CON.5* | *SM21* | Enables the inter-processor communication feature. |
| *S1CON.4* | *REN1* | If set, enables serial reception. Cleared by software to disable reception. |
| *S1CON.3* | *TB81* | The 9th transmitted data bit in Mode A. Set or cleared by the MPU, depending on the function it performs (parity check, multiprocessor communication etc.) |
| *S1CON.2* | *RB81* | In Modes A and B, it is the 9th data bit received. In Mode B, if *SM21* is 0, *RB81* is the stop bit. Must be cleared by software |
| *S1CON.1* | *TI1* | Transmit interrupt flag, set by hardware after completion of a serial transfer. Must be cleared by software. |
| *S1CON.0* | *RI1* | Receive interrupt flag, set by hardware after completion of a serial reception. Must be cleared by software |

**Table 18: The *S1CON* Bit Functions**

## Timers and Counters

The 80515 has two 16-bit timer/counter registers: Timer 0 and Timer 1. These registers can be configured for counter or timer operations.

In timer mode, the register is incremented every machine cycle meaning that it counts up after every 12 periods of the MPU clock signal.

In counter mode, the register is incremented when the falling edge is observed at the corresponding input signal T0 or T1 (T0 and T1 are the timer gating inputs derived from certain DIO pins, see the DIO Ports chapter). Since it takes 2 machine cycles to recognize a 1-to-0 event, the maximum input count rate is 1/2 of the oscillator frequency. There are no restrictions on the duty cycle, however to ensure proper recognition of 0 or 1 state, an input should be stable for at least 1 machine cycle.

The timers/counters are controlled by the *TCON* Register

Timer/Counter Control Register (*TCON*)

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| *TF1* | *TR1* | *TF0* | *TR0* | *IE1* | *IT1* | *IE0* | *IT0* |

**Table 19: The *TCON* Register**

| Bit | Symbol | Function |
|---|---|---|
| *TCON.7* | *TF1* | The Timer 1 overflow flag is set by hardware when Timer 1 overflows. This flag can be cleared by software and is automatically cleared when an interrupt is processed. |
| *TCON.6* | *TR1* | Timer 1 Run control bit. If cleared, Timer 1 stops. |
| *TCON.5* | *TF0* | Timer 0 overflow flag set by hardware when Timer 0 overflows. This flag can be cleared by software and is automatically cleared when an interrupt is processed. |
| *TCON.4* | *TR0* | Timer 0 Run control bit. If cleared, Timer 0 stops. |
| *TCON.3* | *IE1* | Interrupt 1 edge flag is set by hardware when the falling edge on external pin int1 is observed. Cleared when an interrupt is processed. |
| *TCON.2* | *IT1* | Interrupt 1 type control bit. Selects either the falling edge or low level on input pin to cause an interrupt. |
| *TCON.1* | *IE0* | Interrupt 0 edge flag is set by hardware when the falling edge on external pin int0 is observed. Cleared when an interrupt is processed. |
| *TCON.0* | *IT0* | Interrupt 0 type control bit. Selects either the falling edge or low level on input pin to cause interrupt. |

**Table 20: The TCON Register Bit Functions**

Four operating modes can be selected for Timer 0 and Timer 1. Two Special Function Registers (*TMOD* and *TCON*) are used to select the appropriate mode.

Timer/Counter Mode Control register (*TMOD*):

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| *GATE* | *C/T* | *M1* | *M0* | *GATE* | *C/T* | *M1* | *M0* |
| **Timer 1** | | | | **Timer 0** | | | |

**Table 21: The *TMOD* Register**

Bits *TR1* (*TCON.6*) and *TR0* (TCON.4) in the *TCON* register (see Table 19 and Table 20) start their associated timers when set.

| Bit | Symbol | Function |
|---|---|---|
| *TMOD.7*<br>*TMOD.3* | *Gate* | If set, enables external gate control (pin int0 or int1 for Counter 0 or 1, respectively). When int0 or int1 is high, and TRX bit is set (see *TCON* register), a counter is incremented every falling edge on t0 or t1 input pin |
| *TMOD.6*<br>*TMOD.2* | *C/T* | Selects Timer or Counter operation. When set to 1, a Counter operation is performed. When cleared to 0, the corresponding register will function as a Timer. |
| *TMOD.5*<br>*TMOD.1* | *M1* | Selects the mode for Timer/Counter 0 or Timer/Counter 1, as shown in *TMOD* description. |
| *TMOD.4*<br>*TMOD.0* | *M0* | Selects the mode for Timer/Counter 0 or Timer/Counter 1, as shown in *TMOD* description. |

**Table 22: *TMOD* Register Bit Description**

| *M1* | *M0* | Mode | Function |
|---|---|---|---|
| 0 | 0 | Mode 0 | 13-bit Counter/Timer with 5 lower bits in the *TL0* or *TL1* register and the remaining 8 bits in the *TH0* or *TH1* register (for Timer 0 and Timer 1, respectively). The 3 high order bits of *TL0* and *TL1* are held at zero. |
| 0 | 1 | Mode 1 | 16-bit Counter/Timer. |
| 1 | 0 | Mode 2 | 8-bit auto-reload Counter/Timer. The reload value is kept in *TH0* or *TH1*, while *TL0* or *TL1* is incremented every machine cycle. When *TL*(x) overflows, a value from *TH*(x) is copied to *TL*(x). |
| 1 | 1 | Mode 3 | If Timer 1 *M1* and *M0* bits are set to '1', Timer 1 stops. If Timer 0 *M1* and *M0* bits are set to '1', Timer 0 acts as two independent 8-bit Timer/Counters. |

**Table 23: Timers/Counters Mode Description**

Note: In Mode 3, *TL0* is affected by *TR0* and gate control bits, and sets the *TF0* flag on overflow, while *TH0* is affected by the *TR1* bit, and the *TF1* flag is set on overflow.

Table 24 specifies the combinations of operation modes allowed for timer 0 and timer 1:

| | Timer 1 | | |
|---|---|---|---|
| | **Mode 0** | **Mode 1** | **Mode 2** |
| **Timer 0 - mode 0** | YES | YES | YES |
| **Timer 0 - mode 1** | YES | YES | YES |
| **Timer 0 - mode 2** | Not allowed | Not allowed | YES |

**Table 24: Timer Modes**

Timer/Counter Mode Control register (*PCON*):

MSB LSB

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| *SMOD* | -- | -- | -- | -- | -- | -- | -- |

**Table 25: The *PCON* Register**

The *SMOD* bit in the *PCON* register doubles the baud rate when set.

| Bit | Symbol | Function |
|---|---|---|
| *PCON.7* | *SMOD* | Baud rate control. |

**Table 26: *PCON* Register Bit Description**

## WD Timer (Software Watchdog Timer)

The software watchdog timer is a 16-bit counter that is incremented once every 24 or 384 clock cycles. After a reset, the watchdog timer is disabled and all registers are set to zero. The watchdog consists of a 16-bit counter (WDT), a reload register (*WDTREL*), prescalers (by 2 and by 16), and control logic. Once the watchdog is started, it cannot be stopped unless the internal reset signal becomes active.

**Note: It is recommended to use the hardware watchdog timer instead of the software watchdog timer.**

**WD Timer Start Procedure:** The WDT is started by setting the *SWDT* flag. When the WDT register enters the state 0x7CFF, an asynchronous WDTS signal will become active. The signal WDTS sets bit 6 in the IP0 register and requests a reset state. WDTS is cleared either by the reset signal or by changing the state of the WDT timer.

**Refreshing the WD Timer:** The watchdog timer must be refreshed regularly to prevent the reset request signal from becoming active. This requirement imposes an obligation on the programmer to issue two instructions. The first instruction sets WDT and the second instruction sets SWDT. The maximum delay allowed between setting *WDT* and *SWDT* is 12 clock cycles. If this period has expired and SWDT has not been set, the WDT is automatically reset, otherwise the watchdog timer is reloaded with the content of the *WDTREL* register and the WDT is automatically reset. Since the WDT requires exact timing, firmware needs to be designed with special care in order to avoid unwanted WDT resets. **It is strongly discouraged to use the software WDT.**

### Special Function Registers for the WD Timer

Interrupt Enable 0 Register (*IEN0*):

MSB LSB

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| *EAL* | *WDT* | *ET2* | *ES0* | *ET1* | *EX1* | *ET0* | *EX0* |

**Table 27: The *IEN0* Register (see also Table 32)**

| Bit | Symbol | Function |
|---|---|---|
| *IEN0.6* | *WDT* | Watchdog timer refresh flag.<br>Set to initiate a refresh of the watchdog timer. Must be set directly before *SWDT* is set to prevent an unintentional refresh of the watchdog timer. *WDT* is reset by hardware 12 clock cycles after it has been set. |

**Table 28: The *IEN0* Bit Functions (see also Table 32)**

Note: The remaining bits in the IEN0 register are not used for watchdog control

Interrupt Enable 1 Register (*IEN1*):

MSB LSB

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| *EXEN2* | *SWDT* | *EX6* | *EX5* | *EX4* | *EX3* | *EX2* | |

**Table 29: The *IEN1* Register (see also Tables 30/31)**

| Bit | Symbol | Function |
|---|---|---|
| *IEN1.6* | *SWDT* | Watchdog timer start/refresh flag.<br>Set to activate/refresh the watchdog timer. When directly set after setting *WDT*, a watchdog timer refresh is performed. Bit *SWDT* is reset by the hardware 12 clock cycles after it has been set. |

**Table 30: The *IEN1* Bit Functions (see also Tables 30/31)**

Note: The remaining bits in the *IEN1* register are not used for watchdog control

**Interrupt Priority 0 Register (*IP0*):**

MSB LSB

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| -- | *WDTS* | *IP0.5* | *IP0.4* | *IP0.3* | *IP0.2* | *IP0.1* | *IP0.0* |

**Table 31: The *IP0* Register (see also Table 45)**

| Bit | Symbol | Function |
|---|---|---|
| *IP0.6* | *WDTS* | Watchdog timer status flag. Set when the watchdog timer was started. Can be read by software. |

**Table 32: The *IP0* bit Functions (see also Table 45)**

Note: The remaining bits in the *IP0* register are not used for watchdog control

Watchdog Timer Reload Register (*WDTREL*):

MSB LSB

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| *7* | *6* | *5* | *4* | *3* | *2* | *1* | *0* |

**Table 33: The *WDTREL* Register**

| Bit | Symbol | Function |
|---|---|---|
| *WDTREL.7* | 7 | Prescaler select bit. When set, the watchdog is clocked through an additional divide-by-16 prescaler |
| *WDTREL.6* to *WDTREL.0* | 6-0 | Seven bit reload value for the high-byte of the watchdog timer. This value is loaded to the WDT when a refresh is triggered by a consecutive setting of bits *WDT* and *SWDT*. |

**Table 34: The *WDTREL* Bit Functions**

The *WDTREL* register can be loaded and read at any time.

## Interrupts

The 80515 provides 11 interrupt sources with four priority levels. Each source has its own request flag(s) located in a special function register (*TCON*, *IRCON*, and *SCON*). Each interrupt requested by the corresponding flag can be individually enabled or disabled by the enable bits in SFRs *IEN0*, *IEN1*, and *IEN2*.

**External interrupts are the interrupts external to the 80515 core, i.e. signals that originate in other parts of the 71M6521DE/DH/FE, for example the CE, DIO, RTC EEPROM interface.**

### Interrupt Overview

When an interrupt occurs, the MPU will vector to the predetermined address as shown in Table 53. Once interrupt service has begun, it can be interrupted only by a higher priority interrupt. The interrupt service is terminated by a return from instruction, "RETI". When an RETI is performed, the MPU will return to the instruction that would have been next when the interrupt occurred.

When the interrupt condition occurs, the MPU will also indicate this by setting a flag bit. This bit is set regardless of whether the interrupt is enabled or disabled. Each interrupt flag is sampled once per machine cycle, then samples are polled by the hardware. If the sample indicates a pending interrupt when the interrupt is enabled, then the interrupt request flag is set.

On the next instruction cycle, the interrupt will be acknowledged by hardware forcing an LCALL to the appropriate vector address, if the following conditions are met:

- No interrupt of equal or higher priority is already in progress.
- An instruction is currently being executed and is not completed.
- The instruction in progress is not RETI or any write access to the registers *IEN0, IEN1, IEN2, IP0* or *IP1*.

Special Function Registers for Interrupts:

Interrupt Enable 0 register (*IE0*)

MSB LSB

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| *EAL* | *WDT* | | *ES0* | *ET1* | *EX1* | *ET0* | *EX0* |

**Table 35: The *IEN0* Register**

| Bit | Symbol | Function |
|---|---|---|
| *IEN0.7* | *EAL* | *EAL*=0 – disable all interrupts |
| *IEN0.6* | *WDT* | Not used for interrupt control |
| *IEN0.5* | - | |
| *IEN0.4* | *ES0* | *ES0*=0 – disable serial channel 0 interrupt |
| *IEN0.3* | *ET1* | *ET1*=0 – disable timer 1 overflow interrupt |
| *IEN0.2* | *EX1* | *EX1*=0 – disable external interrupt 1 |
| *IEN0.1* | *ET0* | *ET0*=0 – disable timer 0 overflow interrupt |
| *IEN0.0* | *EX0* | *EX0*=0 – disable external interrupt 0 |

**Table 36: The *IEN0* Bit Functions**

Interrupt Enable 1 Register (*IEN1*)

MSB LSB

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | *SWDT* | *EX6* | *EX5* | *EX4* | *EX3* | *EX2* | |

**Table 37: The *IEN1* Register**

| Bit | Symbol | Function |
|---|---|---|
| *IEN1.7* | - | |
| *IEN1.6* | *SWDT* | Not used for interrupt control |
| *IEN1.5* | *EX6* | *EX6*=0 – disable external interrupt 6 |
| *IEN1.4* | *EX5* | *EX5*=0 – disable external interrupt 5 |
| *IEN1.3* | *EX4* | *EX4*=0 – disable external interrupt 4 |
| *IEN1.2* | *EX3* | *EX3*=0 – disable external interrupt 3 |
| *IEN1.1* | *EX2* | *EX2*=0 – disable external interrupt 2 |
| *IEN1.0* | - | |

**Table 38: The *IEN1* Bit Functions**

Interrupt Enable 2 register (*IE2*)

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| - | - | - | - | - | - | - | *ES1* |

**Table 39: The *IEN2* Register**

| Bit | Symbol | Function |
|---|---|---|
| *IEN2.0* | *ES1* | *ES1*=0 – disable serial channel 1 interrupt |

**Table 40: The *IEN2* Bit Functions**

Timer/Counter Control register (*TCON*)

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| *TF1* | *TR1* | *TF0* | *TR0* | *IE1* | *IT1* | *IE0* | *IT0* |

**Table 41: The *TCON* Register**

| Bit | Symbol | Function |
|---|---|---|
| *TCON.7* | *TF1* | Timer 1 overflow flag |
| *TCON.6* | *TR1* | Not used for interrupt control |
| *TCON.5* | *TF0* | Timer 0 overflow flag |
| *TCON.4* | *TR0* | Not used for interrupt control |
| *TCON.3* | *IE1* | External interrupt 1 flag |
| *TCON.2* | *IT1* | External interrupt 1 type control bit |
| *TCON.1* | *IE0* | External interrupt 0 flag |
| *TCON.0* | *IT0* | External interrupt 0 type control bit |

**Table 42: The *TCON* Bit Functions**

Timer2/Counter2 Control register (*T2CON*):

| Bit | Symbol | Function |
|---|---|---|
| *T2CON.7* | -- | Not used |
| *T2CON.6* | *I3FR* | Polarity control for INT3: 0 - falling edge, 1 – rising edge |
| *T2CON.5* | *I2FR* | Polarity control for INT3: 0 - falling edge, 1 – rising edge |
| *TCON.4 … T2CON0* | -- | Not used |

**Table 43: The *T2CON* Bit Functions**

Interrupt Request register (*IRCON*)

MSB LSB

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | *EX6* | *IEX5* | *IEX4* | *IEX3* | *IEX2* | |

**Table 44: The *IRCON* Register**

| Bit | Symbol | Function |
|---|---|---|
| *IRCON.7* | - | |
| *IRCON.6* | - | |
| *IRCON.5* | *IEX6* | External interrupt 6 edge flag |
| *IRCON.4* | *IEX5* | External interrupt 5 edge flag |
| *IRCON.3* | *IEX4* | External interrupt 4 edge flag |
| *IRCON.2* | *IEX3* | External interrupt 3 edge flag |
| *IRCON.1* | *IEX2* | External interrupt 2 edge flag |
| *IRCON.0* | - | |

**Table 45: The *IRCON* Bit Functions**

Only *TF0* and *TF1* (timer 0 and timer 1 overflow flag) will be automatically cleared by hardware when the service routine is called (Signals T0ACK and T1ACK – port ISR – active high when the service routine is called).

### External Interrupts

The 71M6521DE/DH/FE MPU allows seven external interrupts. These are connected as shown in Table 46. The direction of interrupts 2 and 3 is programmable in the MPU. Interrupts 2 and 3 should be programmed for falling sensitivity. The generic 8051 MPU literature states that interrupt 4 through 6 are defined as rising edge sensitive. Thus, the hardware signals attached to interrupts 5 and 6 are inverted to achieve the edge polarity shown in Table 46.

| External Interrupt | Connection | Polarity | Flag Reset |
|---|---|---|---|
| 0 | Digital I/O High Priority | see *DIO_Rx* | automatic |
| 1 | Digital I/O Low Priority | see *DIO_Rx* | automatic |
| 2 | FWCOL0, FWCOL1 | falling | automatic |
| 3 | CE_BUSY | falling | automatic |
| 4 | PLL_OK (rising), PLL_OK (falling) | rising | automatic |
| 5 | EEPROM busy | falling | automatic |
| 6 | XFER_BUSY OR RTC_1SEC | falling | manual |

**Table 46: External MPU Interrupts**

FWCOLx interrupts occur when the CE collides with a flash write attempt. See the flash write description for more detail.

SFR (special function register) enable bits must be set to permit any of these interrupts to occur. Likewise, each interrupt has its own flag bit, which is set by the interrupt hardware, and reset by the MPU interrupt handler. Note that XFER_BUSY, RTC_1SEC, FWCOL0, FWCOL1, PLLRISE, PLLFALL, have their own enable and flag bits in addition to the interrupt 6, 4, and 2 enable and flag bits.

IE0 through IEX6 are cleared automatically when the hardware vectors to the interrupt handler. The other flags, *IE_XFER* through *IE_PB*, are cleared by writing a zero to them. Since these bits are in a bit-addressable SFR byte, common practice would be to clear them with a bit operation. This is to be avoided. The hardware implements bit operations as a byte wide read-modify-write hardware macro. If an interrupt occurs after the read, but before the write, its flag will be cleared unintentionally. The proper way to clear the flag bits is to write a byte mask consisting of all ones except for a zero in the location of the bit to be cleared. The flag bits are configured in hardware to ignore ones written to them.

| Interrupt Enable | | Interrupt Flag | | Interrupt Description |
|---|---|---|---|---|
| **NAME** | **LOCATION** | **NAME** | **LOCATION** | |
| *EX0* | SFR A8[[0] | *IE0* | SFR 88[1] | External interrupt 0 |
| *EX1* | SFR A8[2] | *IE1* | SFR 88[3] | External interrupt 1 |
| *EX2* | SFR B8[1] | *IEX2* | SFR C0[1] | External interrupt 2 |
| *EX3* | SFR B8[2] | *IEX3* | SFR C0[2] | External interrupt 3 |
| *EX4* | SFR B8[3] | *IEX4* | SFR C0[3] | External interrupt 4 |
| *EX5* | SFR B8[4] | *IEX5* | SFR C0[4] | External interrupt 5 |
| *EX6* | SFR B8[5] | *IEX6* | SFR C0[5] | External interrupt 6 |
| *EX_XFER* | 2002[0] | *IE_XFER* | SFR E8[0] | XFER_BUSY interrupt (int 6) |
| *EX_RTC* | 2002[1] | *IE_RTC* | SFR E8[1] | RTC_1SEC interrupt (int 6) |
| *EX_FWCOL* | 2007[4] | *IE_FWCOL0* | SFR E8[3] | FWCOL0 interrupt (int 2) |
| | | *IE_FWCOL1* | SFR E8[2] | FWCOL1 interrupt (int 2) |
| *EX_PLL* | 2007[5] | *IE_PLLRISE* | SFRE8[6] | PLL_OK rise interrupt (int 4) |
| | | *IE_PLLFALL* | SFRE8[7] | PLL_OK fall interrupt (int 4) |
| | | *IE_WAKE* | SFRE8[5] | AUTOWAKE flag |
| | | *IE_PB* | SFRE8[4] | PB flag |

**Table 47: Interrupt Enable and Flag Bits**

The *AUTOWAKE* and *PB* flag bits are shown in Table 47 because they behave similarly to interrupt flags, even though they are not actually related to an interrupt. These bits are set by hardware when the MPU wakes from a push button or wake timeout. The bits are reset by writing a zero. Note that the PB flag is set whenever the PB is pushed, even if the part is already awake.

Each interrupt has its own flag bit, which is set by the interrupt hardware and is reset automatically by the MPU interrupt handler (0 through 5). XFER_BUSY and RTC_1SEC, which are OR-ed together, have their own enable and flag bits in addition to the interrupt 6 enable and flag bits (see Table 47), and these interrupts must be cleared by the MPU software.

When servicing the XFER_BUSY and RTC_1SEC interrupts, special care must be taken to avoid lock-up conditions: If, for example, the XFER_BUSY interrupt is serviced, control must not return to the main program without checking the *RTC_1SEC* flag. If this rule is ignored, a RTC_1SEC interrupt appearing during the XFER_BUSY service routine will disable the processing of any XFER_BUSY or RTC_1SEC interrupt, since both interrupts are edge-triggered (see the Software User's Guide SUG652X).

The external interrupts are connected as shown in Table 47. The polarity of interrupts 2 and 3 is programmable in the MPU via the *I3FR* and *I2FR* bits in *T2CON*. Interrupts 2 and 3 should be programmed for falling sensitivity. The generic 8051 MPU literature states that interrupts 4 through 6 are defined as rising edge sensitive. Thus, the hardware signals attached to interrupts 5 and 6 are inverted to achieve the edge polarity shown in Table 47.

SFR (special function register) enable bits must be set to permit any of these interrupts to occur. Likewise, each interrupt has its own flag bit that is set by the interrupt hardware and is reset automatically by the MPU interrupt handler (0 through 5). *XFER_BUSY* and *RTC_1SEC*, which are OR-ed together, have their own enable and flag bits in addition to the interrupt 6 enable and flag bits (see Table 47), and these interrupts must be cleared by the MPU software.

### Interrupt Priority Level Structure

All interrupt sources are combined in groups, as shown in Table 48:

| **Group** | | | |
|---|---|---|---|
| **0** | External interrupt 0 | Serial channel 1 interrupt | |
| **1** | Timer 0 interrupt | - | External interrupt 2 |
| **2** | External interrupt 1 | - | External interrupt 3 |
| **3** | Timer 1 interrupt | - | External interrupt 4 |
| **4** | Serial channel 0 interrupt | - | External interrupt 5 |
| **5** | - | - | External interrupt 6 |

**Table 48: Priority Level Groups**

Each group of interrupt sources can be programmed individually to one of four priority levels by setting or clearing one bit in the special function register IP0 and one in IP1. If requests of the same priority level are received simultaneously, an internal polling sequence as per Table 52 determines which request is serviced first.

An overview of the interrupt structure is given in Figure 6.

IEN enable bits must be set to permit any of these interrupts to occur. Likewise, each interrupt has its own flag bit that is set by the interrupt hardware and is reset automatically by the MPU interrupt handler (0 through 5). XFER_BUSY and RTC_1SEC, which are OR-ed together, have their own enable and flag bits in addition to the interrupt 6 enable and flag bits (see Table 47) and these interrupts must be cleared by the MPU software.

Interrupt Priority 0 Register (*IP0*)

MSB LSB

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| -- | *WDTS* | *IP0.5* | *IP0.4* | *IP0.3* | *IP0.2* | *IP0.1* | *IP0.0* |

**Table 49: The *IP0* Register**

Note: WDTS is not used for interrupt controls

Interrupt Priority 1 Register (*IP1*)

MSB LSB

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| - | - | *IP1.5* | *IP1.4* | *IP1.3* | *IP1.2* | *IP1.1* | *IP1.0* |

**Table 50: The *IP1* Register:**

| *IP1.x* | *IP0.x* | **Priority Level** |
|---|---|---|
| 0 | 0 | Level0 (lowest) |
| 0 | 1 | Level1 |
| 1 | 0 | Level2 |
| 1 | 1 | Level3 (highest) |

**Table 51: Priority Levels**

| | |
|---|---|
| External interrupt 0 | Polling sequence |
| Serial channel 1 interrupt | |
| Timer 0 interrupt | |
| External interrupt 2 | |
| External interrupt 1 | |
| External interrupt 3 | |
| Timer 1 interrupt | |
| External interrupt 4 | |
| Serial channel 0 interrupt | |
| External interrupt 5 | |
| External interrupt 6 | |

**Table 52: Interrupt Polling Sequence**

### Interrupt Sources and Vectors

Table 53 shows the interrupts with their associated flags and vector addresses.

| Interrupt Request Flag | Description | Interrupt Vector Address |
|---|---|---|
| *IE0* | External interrupt 0 | 0x0003 |
| *TF0* | Timer 0 interrupt | 0x000B |
| *IE1* | External interrupt 1 | 0x0013 |
| *TF1* | Timer 1 interrupt | 0x001B |
| *RI0/TI0* | Serial channel 0 interrupt | 0x0023 |
| *RI1/TI1* | Serial channel 1 interrupt | 0x0083 |
| *IEX2* | External interrupt 2 | 0x004B |
| *IEX3* | External interrupt 3 | 0x0053 |
| *IEX4* | External interrupt 4 | 0x005B |
| *IEX5* | External interrupt 5 | 0x0063 |
| *IEX6* | External interrupt 6 | 0x006B |

**Table 53: Interrupt Vectors**

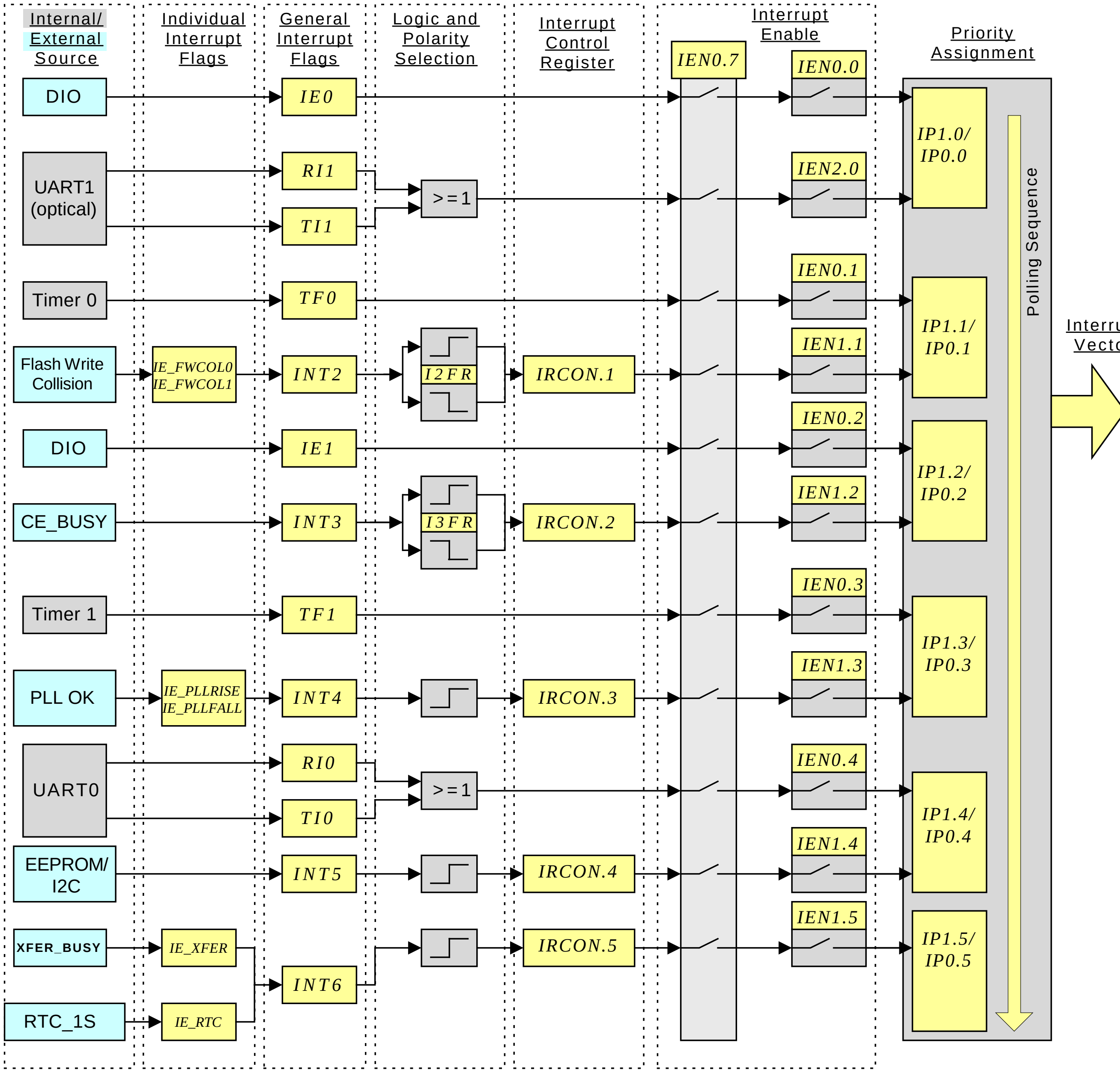



**Figure 6: Interrupt Structure**

# On-Chip Resources

## Oscillator

The 71M6521DE/DH/FE oscillator drives a standard 32.768kHz watch crystal. These crystals are accurate and do not require a high-current oscillator circuit. The 71M6521DE/DH/FE oscillator has been designed specifically to handle these crystals and is compatible with their high impedance and limited power handling capability.

## PLL and Internal Clocks

Timing for the device is derived from the 32.768kHz oscillator output. On-chip timing functions include the MPU master clock, a real time clock (RTC), and the delta-sigma sample clock. In addition, the MPU has two general counter/timers (see MPU section).

The ADC master clock, CKADC, is generated by an on-chip PLL. It multiplies the oscillator output frequency (CK32) by 150.

The CE clock frequency is always CK32 * 150, or 4.9152MHz, where CK32 is the 32kHz clock. The MPU clock frequency is determined by *MPU_DIV* and can be 4.9152MHz $*2^{-MPU\_DIV}$ Hz where *MPU_DIV* varies from 0 to 7 (*MPU_DIV* is 0 on power-up). This makes the MPU clock scalable from 4.9152MHz down to 38.4kHz. The circuit also generates a 2x MPU clock for use by the emulator. This clock is not generated when *ECK_DIS* is asserted by the MPU.

The setting of *MPU_DIV* is maintained when the device transitions to BROWNOUT mode, but the time base in BROWNOUT mode is 28,672Hz.

## Real-Time Clock (RTC)

The RTC is driven directly by the crystal oscillator. It is powered by the net V2P5NV (battery-backed up supply). The RTC consists of a counter chain and output registers. The counter chain consists of seconds, minutes, hours, day of week, day of month, month, and year. The RTC is capable of processing leap years. Each counter has its own output register. Whenever the MPU reads the seconds register, all other output registers are automatically updated. Since the RTC clock is not coherent to the MPU clock, the MPU must read the seconds register until two consecutive reads are the same (requires either 2 or 3 reads). At this point, all RTC output registers will have the correct time. Regardless of the MPU clock speed, RTC reads require one wait state.

RTC time is set by writing to the RTC registers in I/O RAM. Each byte written to RTC must be delayed at least 3 RTC cycles from any previous byte written to RTC. Hardware RTC write protection requires that a write to address 0x201F occur before each RTC write. Writing to address 0x201F opens a hardware 'enable gate' that remains open until an RTC write occurs and then closes. It is not necessary to disable interrupts between the write operation to 0x201F and the RTC write because the 'enable gate' will remain open until the RTC write finally occurs

Two time correction bits, *RTC_DEC_SEC* and *RTC_INC_SEC* are provided to adjust the RTC time. A pulse on one of these bits causes the time to be decremented or incremented by an additional second at the next update of the *RTC_SEC* register. Thus, if the crystal temperature coefficient is known, the MPU firmware can integrate temperature and correct the RTC time as necessary.

## Temperature Sensor

The device includes an on-chip temperature sensor for determining the temperature of the bandgap reference. The MPU may request an alternate multiplexer frame containing the temperature sensor output by asserting *MUX_ALT*. The primary use of the temperature data is to determine the magnitude of compensation required to offset the thermal drift in the system (see section titled "Temperature Compensation").

## Physical Memory

**Flash Memory:** The 71M6521DE/DH/FE includes 16KB (71M6521DE/DH) or 32KB (71M6521FE) of on-chip flash memory. The flash memory primarily contains MPU and CE program code. It also contains images of the CE DRAM, MPU RAM, and I/O RAM. On power-up, before enabling the CE, the MPU copies these images to their respective locations.

Allocated flash space for the CE program cannot exceed 1024 words (2KB). The CE program must begin on a 1KB boundary of the flash address. The *CE_LCTN[4:0]* word defines which 1KB boundary contains the CE code. Thus, the first CE instruction is located at 1024**CE_LCTN[4:0]*. *CE_LCTN* must be defined before the CE is enabled.

The flash memory is segmented into 512 byte individually erasable pages.

The CE engine cannot access its program memory when flash write occurs. Thus, the flash write procedure is to begin a sequence of flash writes when CE_BUSY falls (CE_BUSY interrupt) and to make sure there is sufficient time to complete the sequence before CE_BUSY rises again. The actual time for the flash write operation will depend on the exact number of cycles required by the CE program. Typically (CE program is 512 instructions, mux frame is 13 CK32 cycles), there will be 200µs of flash write time, enough for 4 bytes of flash write. If the CE code is shorter, there will be even more time.

Two interrupts warn of collisions between the MPU firmware and the CE timing. If a flash write is attempted while the CE is busy, the flash write will not execute and the FW_COL0 interrupt will be issued. If a flash write is still in progress when the CE would otherwise begin a code pass, the code pass is skipped, the write is completed, and the FW_COL1 interrupt is issued.

The bit *FLASH66Z* (see I/O RAM table) defines the speed for accessing flash memory. To minimize supply current draw, this bit should be set to 1.

Flash erasure is initiated by writing a specific data pattern to specific SFR registers in the proper sequence. These special pattern/sequence requirements prevent inadvertent erasure of the flash memory.

The mass erase sequence is:

1. Write 1 to the *FLSH_MEEN* bit (SFR address 0xB2[1].
2. Write pattern 0xAA to *FLSH_ERASE* (SFR address 0x94)

The mass erase cycle can only be initiated when the ICE port is enabled.

The page erase sequence is:

1. Write the page address to *FLSH_PGADR* (SFR address 0xB7[7:1]
2. Write pattern 0x55 to *FLSH_ERASE* (SFR address 0x94)

The MPU may write to the flash memory. This is one of the non-volatile storage options available to the user in addition to external EEPROM.

*FLSH_PWE* (flash program write enable) differentiates 80515 data store instructions (MOVX@DPTR,A) between flash and XRAM writes.

Updating individual bytes in flash memory:

The original state of a flash byte is 0xFF (all ones). Once, a value other than 0xFF is written to a flash memory cell, overwriting with a different value usually requires that the cell is erased first. Since cells cannot be erased individually, the page has to be copied to RAM, followed by a page erase. After this, the page can be updated in RAM and then written back to the flash memory.

**MPU RAM:** The 71M6521DE/DH/FE includes 2k-bytes of static RAM memory on-chip (XRAM) plus 256-bytes of internal RAM in the MPU core. The 2K-bytes of static RAM are used for data storage during normal MPU operations.

**CE DRAM**: The CE DRAM is the working data memory of the CE (128 32-bit words). The MPU can read and write the CE DRAM as the primary means of data communication between the two processors.

## Optical Interface

The device includes an interface to implement an IR/optical port. The pin OPT_Tx is designed to directly drive an external LED for transmitting data on an optical link. The pin OPT_RX is designed to sense the input from an external photo detector used as the receiver for the optical link. These two pins are connected to a dedicated UART port (UART1).

The OPT_TX and OPT_RX pins can be inverted with configuration bits *OPT_TXINV* and *OPT_RXINV*, respectively. Additionally, the OPT_TX output may be modulated at 38kHz. Modulation is available when system power is present (i.e. not in BROWNOUT mode). The *OPT_TXMOD* bit enables modulation. Duty cycle is controlled by *OPT_FDC[1:0],* which can select 50%, 25%, 12.5%, and 6.25% duty cycle. 6.25% duty cycle means OPT_TX is low for 6.25% of the period. Figure 7 illustrates the OPT_TX generator.

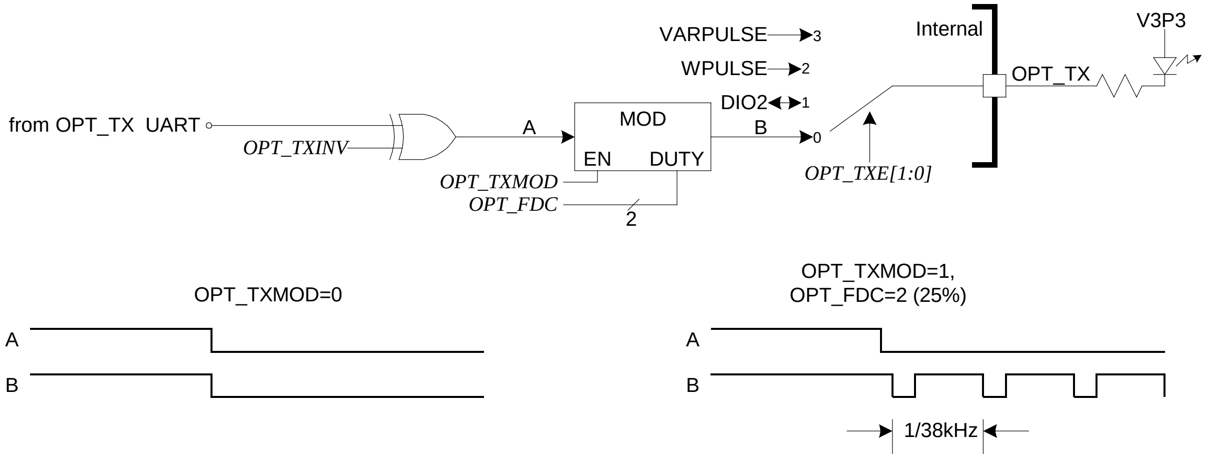



**Figure 7: Optical Interface**

When not needed for the optical UART, the OPT_TX pin can alternatively be configured as DIO2, WPULSE, or VARPULSE. The configuration bits are *OPT_TXE[1:0]*. Likewise, OPT_RX can alternately be configured as DIO_1. Its control is *OPT_RXDIS*.

## Digital I/O

The device includes up to 18 pins (QFN 68 package) or 14 pins (LQFP 64 package) of general purpose digital I/O. These pins are compatible with 5 V inputs (no current-limiting resistors are needed). Some of them are dedicated DIO (DIO3), some are dual-function that can alternatively be used as LCD drivers (DIO4-11, 14-17, 19-21) and some share functions with the optical port (DIO1, DIO2). On reset or power-up, all DIO pins are inputs until they are configured for the desired direction under MPU control. The pins are configured by the DIO registers and by the five bits of the *LCD_NUM* register (located in I/O RAM). Once declared as DIO, each pin can be configured independently as an input or output with the *DIO_DIRn* bits. A 3-bit configuration word, *DIO_Rx*, can be used for certain pins, when configured as DIO, to individually assign an internal resource such as an interrupt or a timer control. Table 54 lists the direction registers and configurability associated with each group of DIO pins. Table 55 shows the configuration for a DIO pin through its associated bit in its *DIO_DIR* register.

Tables showing the relationship between *LCD_NUM* and the available segment/DIO pins can be found in the Applications section and in the I/O RAM Description under *LCD_NUM[4:0]*.

| **DIO** | **PB** | **1** | **2** | **3** | **4** | **5** | **6** | **7** | **8** | **9** | **10** | **11** | **12** | **13** | **14** | **15** |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Pin no. (64 LQFP) | 62 | 57 | 3 | - | 37 | 38 | 39 | 40 | 41 | 42 | 43 | 44 | -- | -- | 20 | 21 |
| Pin no. (68 QFN) | 65 | 60 | 3 | 5 | 39 | 40 | 41 | 42 | 43 | 44 | 45 | 46 | -- | -- | 21 | 22 |
| Data Register | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | -- | -- | 6 | 7 |
| | *DIO0=P0* (SFR 0x80) | | | | | | | | *DIO1=P1* (SFR 0x90) | | | | | | | |
| Direction Register | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | -- | -- | 6 | 7 |
| | *DIO_DIR0* (SFR 0xA2) | | | | | | | | *DIO_DIR1* (SFR 0x91) | | | | | | | |
| Internal Resources Configurable | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y | -- | -- | -- | -- |

| **DIO** | **16** | **17** | **18** | **19** | **20** | **21** | **22** | **23** |
|---|---|---|---|---|---|---|---|---|
| Pin no. (64 LQFP) | 22 | 12 | -- | -- | -- | -- | -- | -- |
| Pin no. (68 QFN) | 23 | 13 | -- | 24 | 47 | 68 | | |
| Data Register | 0 | 1 | -- | 3 | 4 | 5 | -- | -- |
| | *DIO2=P2* (SFR 0xA0) | | | | | | | |
| Direction Register | 0 | 1 | -- | 3 | 4 | 5 | -- | -- |
| | *DIO_DIR2* (SFR 0xA1) | | | | | | | |
| Internal Resources Configurable | N | N | -- | N | N | N | -- | -- |

**Table 54: Data/Direction Registers and Internal Resources for DIO Pin Groups**

| | *DIO_DIR [n]* | |
|---|---|---|
| | **0** | **1** |
| **DIO Pin n Function** | Input | Output |

**Table 55: *DIO_DIR* Control Bit**

Additionally, if DIO6 and DIO7 are declared outputs, they can be configured as dedicated pulse outputs (WPULSE = DIO6, VARPULSE = DIO7) using *DIO_PW* and *DIO_PV* registers. In this case, DIO6 and DIO7 are under CE control. DIO4 and DIO5 can be configured to implement the EEPROM Interface.

The PB pin is a dedicated digital input. If the optical UART is not used, OPT_TX and OPT_RX can be configured as dedicated DIO pins (DIO1, DIO2, see Optical Interface section).

A 3-bit configuration word, I/O RAM register, *DIO_Rx* (0x2009[2:0] through 0x200E[6:4]) can be used for certain pins, when configured as DIO, to individually assign an internal resource such as an interrupt or a timer control (see Table 54 for DIO pins available for this option). This way, DIO pins can be tracked even if they are configured as outputs.

***Tracking DIO pins configured as outputs is useful for pulse counting without external hardware.***

***When driving LEDs, relay coils etc., the DIO pins should <u>sink</u> the current into GNDD (as shown in Figure 8, right), <u>not</u> source it from V3P3D (as shown in Figure 8, left). This is due to the resistance of the internal switch that connects V3P3D to either V3P3SYS or VBAT.***

***When configured as inputs, the dual-function (DIO/SEG) pins should not be pulled above V3P3SYS in MISSION and above VBAT in LCD and BROWNOUT modes. Doing so will distort the LCD waveforms of the other pins. This limitation applies to any pin that can be configured as a LCD driver.***

The control resources selectable for the DIO pins are listed in Table 56. If more than one input is connected to the same resource, the resources are combined using a logical OR.

The PB pin is a dedicated digital input. In addition, if the optical UART is not used, OPT_TX and OPT_RX can be configured as dedicated DIO pins. Thus, in addition to the 16 general-purpose DIO pins (DIO4…DIO11, DIO14…DIO21), there are three additional pins that can be used for digital input and output.

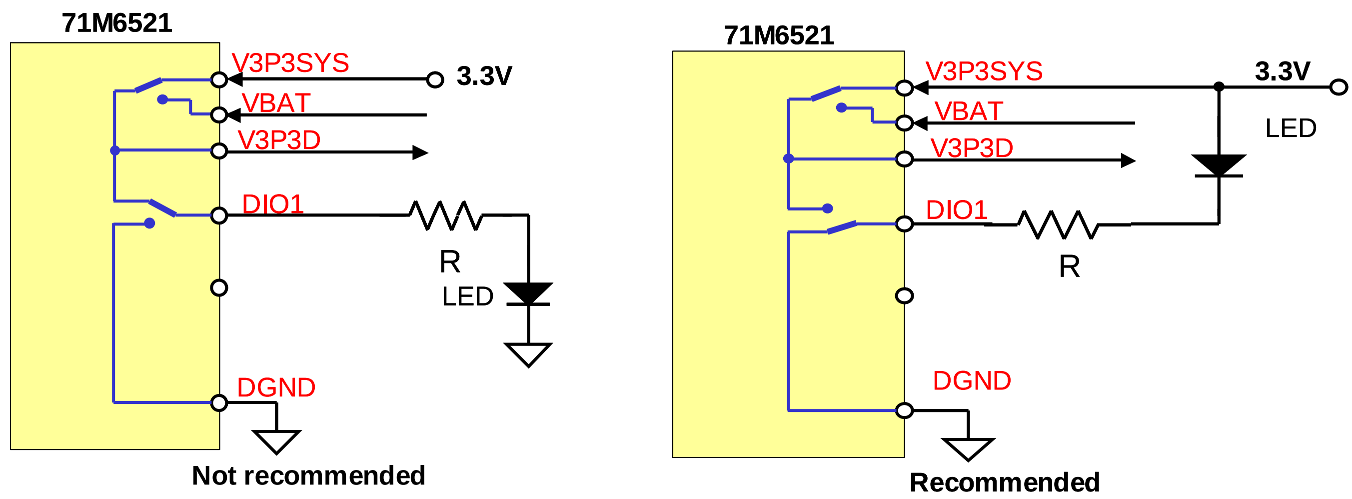



**Figure 8: Connecting an External Load to DIO Pins**

| *DIO_R* Value | Resource Selected for DIO Pin |
|---|---|
| 0 | NONE |
| 1 | Reserved |
| 2 | T0 (counter0 clock) |
| 3 | T1 (counter1 clock) |
| 4 | High priority I/O interrupt (INT0 rising) |
| 5 | Low priority I/O interrupt (INT1 rising) |
| 6 | High priority I/O interrupt (INT0 falling) |
| 7 | Low priority I/O interrupt (INT1 falling) |

**Table 56: Selectable Controls using the *DIO_DIR* Bits**

## LCD Drivers

The device in the 68-pin QFN package contains 20 dedicated LCD segment drivers in addition to the 18 multi-use pins described above. Thus, the device is capable of driving between 80 to 152 pixels of LCD display with 25% duty cycle (or 60 to 114 pixels with 33% duty cycle). At eight pixels per digit, this corresponds to 10 to 19 digits.

The device in the 64-pin LQFP package contains 20 dedicated LCD segment drivers in addition to the 15 multi-use pins described above. Thus, the device is capable of driving between 80 to 140 pixels of LCD display with 25% duty cycle (or 60 to 105 pixels with 33% duty cycle). At eight pixels per digit, this corresponds to 10 to 17 digits.

The LCD drivers are grouped into four commons and up to 38 segment drivers (68-pin package), or 4 commons and 35 segment drivers (64-pin package). The LCD interface is flexible and can drive either digit segments or enunciator symbols.

Segment drivers SEG18 and SEG19 can be configured to blink at either 0.5Hz or 1Hz. The blink rate is controlled by *LCD_Y*. There can be up to four pixels/segments connected to each of these drivers. *LCD_BLKMAP18[3:0]* and *LCD_BLKMAP19[3:0]* identify which pixels, if any, are to blink.

**LCD interface memory is powered by the non-volatile supply. The bits of the LCD memory are preserved in LCD and SLEEP modes, even if their pin is not configured as SEG. In this case, they can be useful as general-purpose nonvolatile storage.**

## Battery Monitor

The battery voltage is measured by the ADC during alternative MUX frames if the *BME* (Battery Measure Enable) bit is set. While *BME* is set, an on-chip 45kΩ load resistor is applied to the battery and a scaled fraction of the battery voltage is applied to the ADC input. After each alternative MUX frame, the result of the ADC conversion is available at CE DRAM address 0x07. *BME* is ignored and assumed zero when system power is not available. See the Battery Monitor section of the Electrical Specification section for details regarding the ADC LSB size and the conversion accuracy.

## EEPROM Interface

The 71M6521DE/DH/FE provides hardware support for either type of EEPROM interface, a two-pin interface and a three-pin interface. The interfaces use the *EECTRL* and *EEDATA* registers for communication.

### Two-Pin EEPROM Interface

The dedicated 2-pin serial interface communicates with external EEPROM devices. The interface is multiplexed onto pins DIO4 (SCK) and DIO5 (SDA) controlled by the *DIO_EEX* bit I/O RAM (see I/O RAM Table). The MPU communicates with the interface through two SFR registers: *EEDATA* and *EECTRL*. If the MPU wishes to write a byte of data to EEPROM, it places the data in *EEDATA* and then writes the 'Transmit' command (CMD = 0011) to *EECTRL*. This initiates the transmit operation. The transmit operation is finished when the *BUSY* bit falls. Interrupt INT5 is also asserted when *BUSY* falls. The MPU can then check the *RX_ACK* bit to see if the EEPROM acknowledged the transmission.

A byte is read by writing the 'Receive' command (CMD = 0001) to *EECTRL* and waiting for the *BUSY* bit to fall. Upon completion, the received data is in *EEDATA*. The serial transmit and receive clock is 78kHz during each transmission, and the clock is held in a high state until the next transmission. The bits in *EECTRL* are shown in Table 57.

The EEPROM interface can also be operated by controlling the DIO4 and DIO5 pins directly ("bit-banging"). **However, controlling DIO4 and DIO5 directly is discouraged, because it may tie up the MPU to the point where it may become too busy to process interrupts**.

<table>
<tr><th>Status Bit</th><th>Name</th><th>Read/ Write</th><th>Reset State</th><th>Polarity</th><th colspan="2">Description</th></tr>
<tr><td>7</td><td>ERROR</td><td>R</td><td>0</td><td>Positive</td><td colspan="2">1 when an illegal command is received.</td></tr>
<tr><td>6</td><td>BUSY</td><td>R</td><td>0</td><td>Positive</td><td colspan="2">1 when serial data bus is busy.</td></tr>
<tr><td>5</td><td>RX_ACK</td><td>R</td><td>1</td><td>Negative</td><td colspan="2">0 indicates that the EEPROM sent an ACK bit.</td></tr>
<tr><td>4</td><td>TX_ACK</td><td>R</td><td>1</td><td>Negative</td><td colspan="2">0 indicates when an ACK bit has been sent to the EEPROM</td></tr>
<tr><td rowspan="8">3-0</td><td rowspan="8">CMD[3:0 ]</td><td rowspan="8">W</td><td rowspan="8">0</td><td rowspan="8">Positive, see CMD Table</td><td>CMD</td><td>Operation</td></tr>
<tr><td>0000</td><td>No-op. Applying the no-op command will stop the I$^2$C clock (SCK, DIO4). Failure to issue the no-op command will keep the SCK signal toggling.</td></tr>
<tr><td>0001</td><td>Receive a byte from EEPROM and send ACK.</td></tr>
<tr><td>0011</td><td>Transmit a byte to EEPROM.</td></tr>
<tr><td>0101</td><td>Issue a 'STOP' sequence.</td></tr>
<tr><td>0110</td><td>Receive the last byte from EEPROM, do not send ACK.</td></tr>
<tr><td>1001</td><td>Issue a 'START' sequence.</td></tr>
<tr><td>Others</td><td>No Operation, set the ERROR bit.</td></tr>
</table>

**Table 57: *EECTRL* Status Bits**

### Three-Wire EEPROM Interface

A 500kHz three-wire interface, using SDATA, SCK, and a DIO pin for CS is available. The interface is selected with *DIO_EEX*=3. The same 2-wire *EECTRL* register is used, except the bits are reconfigured, as shown in Table 58. When *EECTRL* is written, up to 8 bits from *EEDATA* are either written to the EEPROM or read from the EEPROM, depending on the values of the EECTRL bits.

| Control Bit | Name | Read/Write | Description |
|---|---|---|---|
| 7 | *WFR* | W | Wait for Ready. If this bit is set, the trailing edge of *BUSY* will be delayed until a rising edge is seen on the data line. This bit can be used during the last byte of a Write command to cause the INT5 interrupt to occur when the EEPROM has finished its internal write sequence. This bit is ignored if HiZ=0. |
| 6 | *BUSY* | R | Asserted while serial data bus is busy. When the *BUSY* bit falls, an INT5 interrupt occurs. |
| 5 | *HiZ* | W | Indicates that the SD signal is to made high impedance immediately after the last SCK rising edge. |
| 4 | *RD* | W | Indicates that *EEDATA* is to be filled with data from EEPROM. |
| 3-0 | *CNT*[3:0] | W | Specifies the number of clocks to be issued. Allowed values are 0 through 8. If RD=1, CNT bits of data will be read MSB first, and right justified into the low order bits of *EEDATA*. If RD=0, CNT bits will be sent MSB first to EEPROM, shifted out of EEDATA's MSB. If CNT is zero, SDATA will simply obey the HiZ bit. |

**Table 58: *EECTRL* bits for 3-wire interface**

The timing diagrams in Figure 9 through Figure 13 describe the 3-wire EEPROM interface behavior. All commands begin when the *EECTRL* register is written. Transactions start by first raising the DIO pin that is connected to CS. Multiple 8-bit or less commands such as those shown in Figure 9 through Figure 13 are then sent via *EECTRL* and *EEDATA*. When the transaction is finished, CS must be lowered. At the end of a Read transaction, the EEPROM will be driving SDATA, but will transition to HiZ (high impedance) when CS falls. The firmware should then immediately issue a write command with CNT=0 and HiZ=0 to take control of SDATA and force it to a low-Z state.

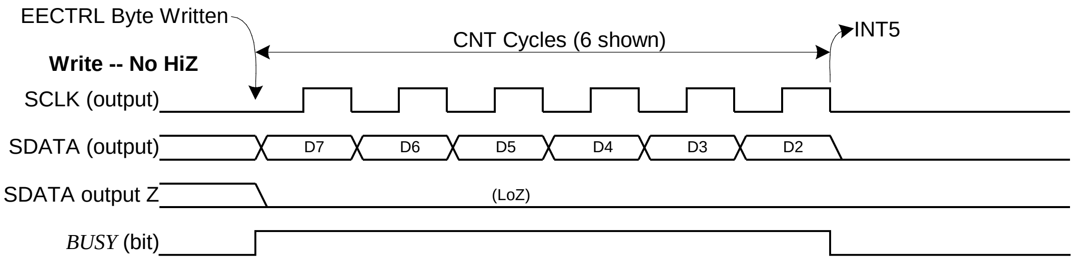



**Figure 9: 3-Wire Interface. Write Command, HiZ=0.**

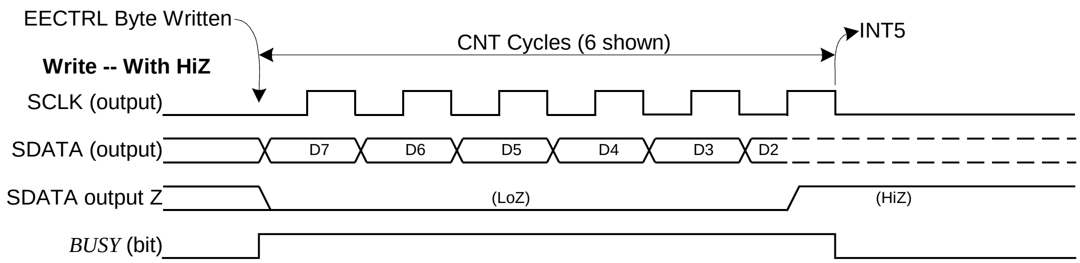



**Figure 10: 3-Wire Interface. Write Command, HiZ=1**

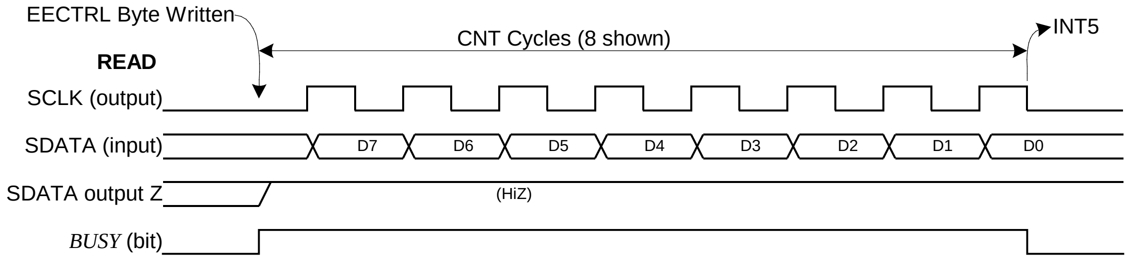



**Figure 11: 3-Wire Interface. Read Command.**

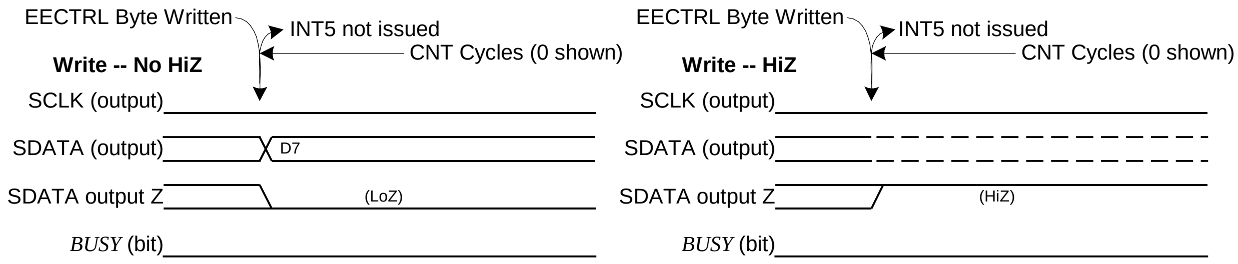



**Figure 12: 3-Wire Interface. Write Command when CNT=0**

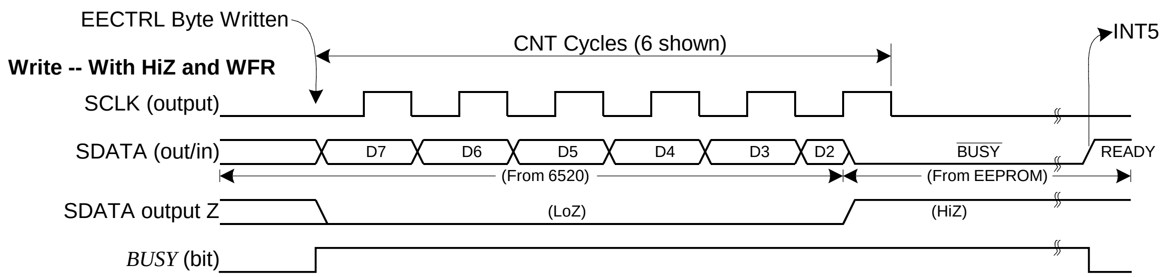
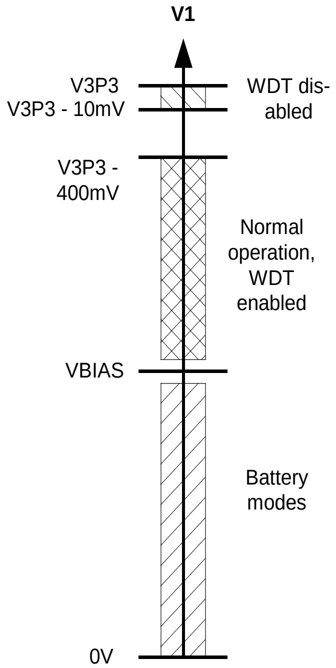



**Figure 13: 3-Wire Interface. Write Command when HiZ=1 and WFR=1.**

## Hardware Watchdog Timer




In addition to the basic watchdog timer included in the 80515 MPU, an independent, robust, fixed-duration, watchdog timer (WDT) is included in the device. It uses the RTC crystal oscillator as its time base and must be refreshed by the MPU firmware at least every 1.5 seconds. When not refreshed on time the WDT overflows, and the part is reset as if the RESET pin were pulled high, except that the I/O RAM bits will be in the same state as after a wake-up from SLEEP or LCD modes (see the I/O RAM description for a list of I/O RAM bit states after RESET and wake-up). 4100 oscillator cycles (or 125ms) after the WDT overflow, the MPU will be launched from program address 0x0000.

A status bit, *WD_OVF*, is set when WDT overflow occurs. This bit is powered by the non-volatile supply and can be read by the MPU to determine if the part is initializing after a WDT overflow event or after a power-up. After it is read, MPU firmware must clear *WD_OVF*. The *WD_OVF* bit is cleared by the RESET pin

There is no internal digital state that deactivates the WDT. For debug purposes, however, the WDT can be disabled by tying the V1 pin to V3P3 (see Figure 39). Of course, this also deactivates V1 power fault detection. Since there is no method in firmware to disable the crystal oscillator or the WDT, it is guaranteed that whatever state the part might find itself in, upon WDT overflow, the part will be reset to a known state.

Asserting ICE_E will also deactivate the WDT. This is the only method that will disable the WDT in BROWNOUT mode.

In normal operation, the WDT is reset by periodically writing a one to the *WDT_RST* bit. The watchdog timer is also reset when the internal signal WAKE=0 (see section on Wake Up Behavior).

**Figure 14: Functions defined by V1**

## Program Security

When enabled, the security feature limits the ICE to global flash erase operations only. All other ICE operations are blocked. This guarantees the security of the user's MPU and CE program code. Security is enabled by MPU code that is executed in a 32 cycle preboot interval before the primary boot sequence begins. Once security is enabled, the only way to disable it is to perform a global erase of the flash, followed by a chip reset.

The first 32 cycles of the MPU boot code are called the preboot phase because during this phase the ICE is inhibited. A read-only status bit, *PREBOOT*, identifies these cycles to the MPU. Upon completion of preboot, the ICE can be enabled and is permitted to take control of the MPU.

*SECURE*, the security enable bit, is reset whenever the chip is reset. Hardware associated with the bit permits only ones to be written to it. Thus, preboot code may set *SECURE* to enable the security feature but may not reset it. Once *SECURE* is set, the preboot code is protected and no external read of program code is possible

Specifically, when *SECURE* is set:

- The ICE is limited to bulk flash erase only.
- Page zero of flash memory, the preferred location for the user's preboot code, may not be page-erased by either MPU or ICE. Page zero may only be erased with global flash erase.
- Writes to page zero, whether by MPU or ICE are inhibited.

**The *SECURE* bit is to be used with caution!** Inadvertently setting this bit will inhibit access to the part via the ICE interface, if no mechanism for actively resetting the part between reset and erase operations is provided (see ICE Interface description).

## Test Ports

**TMUXOUT Pin:** One out of 16 digital or 8 analog signals can be selected to be output on the TMUXOUT pin. The function of the multiplexer is controlled with the I/O RAM register *TMUX* (0x20AA[4:0]), as shown in Table 59.

| ***TMUX*[4:0]** | **Mode** | **Function** |
|---|---|---|
| 0 | Analog | DGND |
| 1 | Analog | Reserved |
| 2 | Analog | DGND |
| 3-5 | Analog | Reserved |
| 6 | Analog | VBIAS |
| 7 | Analog | Not used |
| 8-0x0F | -- | Reserved |
| 0x10 – 0x13 | -- | Not used |
| 0x14 | Digital | RTM (Real time output from CE) |
| 0x15 | Digital | WDTR_EN (Comparator 1 Output AND V1LT3) |
| 0x16 – 0x17 | | Not used |
| 0x18 | Digital | RXD (from Optical interface, w/ optional inversion) |
| 0x19 | Digital | MUX_SYNC |
| 0x1A | Digital | CK_10M (10MHz clock) |
| 0x1B | Digital | CK_MPU (MPU clock) |
| 0x1C | -- | Reserved |
| 0X1D | Digital | RTCLK (output of the oscillator circuit, nominally 32,786Hz) |
| 0X1E | Digital | CE_BUSY (busy interrupt generated by CE, 396µs) |
| 0X1F | Digital | XFER_BUSY (transfer busy interrupt generated by CE, nominally every 999.7ms) |

**Table 59: *TMUX*[4:0] Selections**

# FUNCTIONAL DESCRIPTION

## Theory of Operation

The energy delivered by a power source into a load can be expressed as:

$$E = \int_0^t V(t)I(t)dt$$

Assuming phase angles are constant, the following formulae apply:

- P = Real Energy [Wh] = V * A * cos φ* t
- Q = Reactive Energy [VARh] = V * A * sin φ * t
- S = Apparent Energy [VAh] = $\sqrt{P^2 + Q^2}$

For a practical meter, not only voltage and current amplitudes, but also phase angles and harmonic content may change constantly. Thus, simple RMS measurements are inherently inaccurate. A modern solid-state electricity meter IC such as the Teridian 71M6521DE/DH/FE functions by emulating the integral operation above, i.e. it processes current and voltage samples through an ADC at a constant frequency. As long as the ADC resolution is high enough and the sample frequency is beyond the harmonic range of interest, the current and voltage samples, multiplied with the time period of sampling will yield an accurate quantity for the momentary energy. Summing up the momentary energy quantities over time will result in accumulated energy.

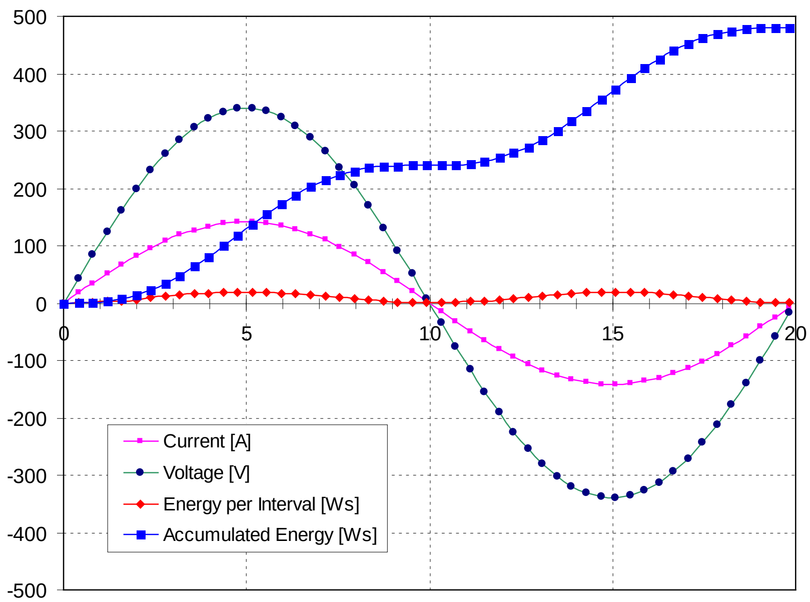



**Figure 15: Voltage. Current, Momentary and Accumulated Energy**

Figure 15 shows the shapes of V(t), I(t), the momentary power and the accumulated power, resulting from 50 samples of the voltage and current signals over a period of 20ms. The application of 240VAC and 100A results in an accumulation of 480Ws (= 0.133Wh) over the 20ms period, as indicated by the Accumulated Power curve.

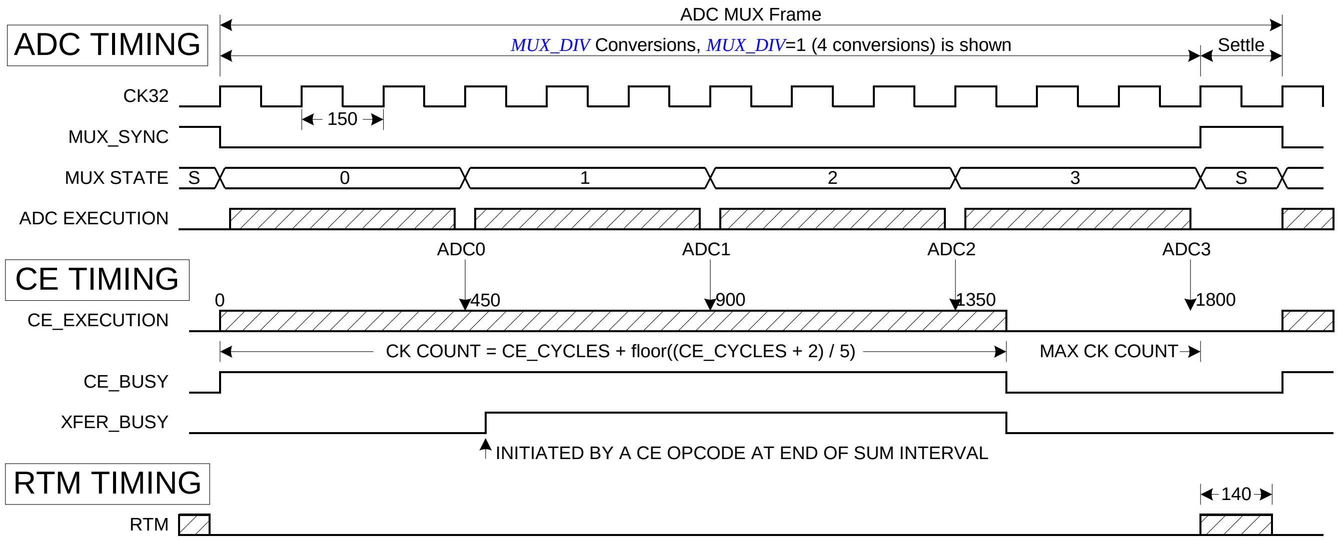
The described sampling method works reliably, even in the presence of dynamic phase shift and harmonic distortion.

## System Timing Summary

Figure 16 summarizes the timing relationships between the input MUX states, the CE_BUSY signal, and the two serial output streams. In this example, *MUX_DIV*=4 and *FIR_LEN*=1 (384). The duration of each MUX frame is 1 + MUX_DIV * 2 if *FIR_LEN*=288, and 1 + *MUX_DIV* * 3 if *FIR_LEN*=384. An ADC conversion will always consume an integer number of CK32 clocks. Followed by the conversions is a single CK32 cycle where the bandgap voltage is allowed to recover from the change in CROSS.

Each CE program pass begins when ADC0 (channel IA) conversion begins. Depending on the length of the CE program, it may continue running until the end of the ADC3 (VB) conversion. CE opcodes are constructed to ensure that all CE code passes consume exactly the same number of cycles. The result of each ADC conversion is inserted into the CE DRAM when the conversion is complete. The CE code is written to tolerate sudden changes in ADC data. The exact CK count when each ADC value is loaded into DRAM is shown in Figure 16.

Figure 16 also shows that the serial RTM data stream begins transmitting at the beginning of state 'S.' RTM, consisting of 140 CK cycles, will always finish before the next code pass starts.




NOTES:
1. ALL DIMENSIONS ARE 5MHZ CK COUNTS.
2. THE PRECISE FREQUENCY OF CK IS 150*CRYSTAL FREQUENCY = 4.9152MHz.
3. XFER_BUSY OCCURS ONCE EVERY (PRESAMPS * SUM_CYCLES) CODE PASSES.

**Figure 16: Timing Relationship between ADC MUX, Compute Engine, and Serial Transfers.**

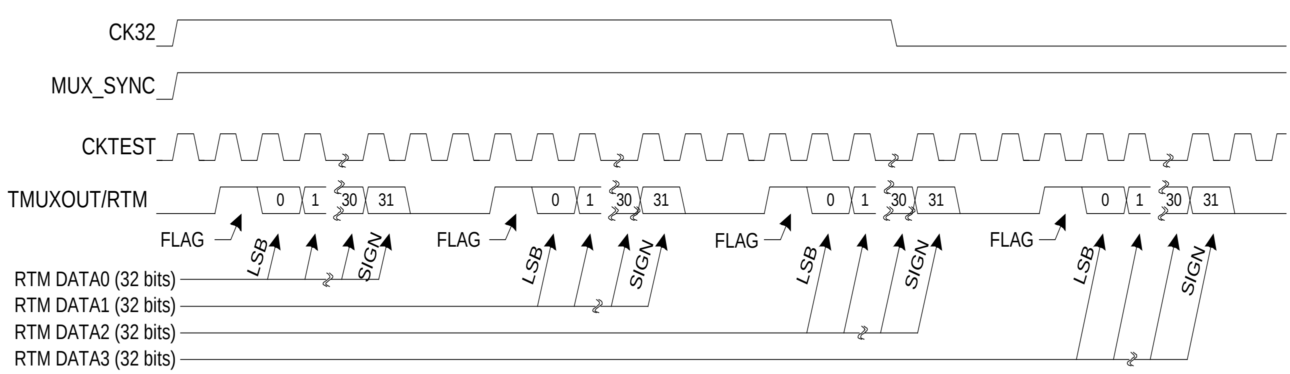



**Figure 17: RTM Output Format**

## Battery Modes

Shortly after system power (V3P3SYS) is applied, the part will be in MISSION mode. MISSION mode means that the part is operating with system power and that the internal PLL is stable. This mode is the normal operation mode where the part is capable of measuring energy.

When system power is <u>not</u> available (i.e. when V1<VBIAS), the 71M6521DE/DH/FE can be in one of three battery modes, i.e. BROWNOUT, LCD, or SLEEP mode. As soon as V1 falls below VBIAS or when the part wakes up under battery power (with sufficient voltage margin), the part will automatically enter BROWNOUT mode (see Wake Up Behavior section). From BROWNOUT mode, the MPU may enter either LCD mode or SLEEP mode by setting either the *LCD_ONLY* or *SLEEP* I/O RAM bits (only one bit can be set at the same time in BROWNOUT mode, since setting one bit will already force the part into SLEEP or LCD mode, disabling the MPU).

Figure 18 shows a state diagram of the various operation modes, with the possible transitions between modes. For information on the timing of mode transitions refer to Figure 22 through Figure 24.

Meters that do not require functionality in the battery modes, e.g. meters that only use the SLEEP mode to maintain the RTC, still need to contain code that brings the chip from BROWNOUT mode to SLEEP mode. Otherwise, the chip remains in BROWNOUT mode, once the system power is missing, and consumes more current than intended.

Similarly, meters equipped with batteries need to contain code that transitions the chip to SLEEP mode as soon as the battery is attached in production. Otherwise, remaining in BROWNOUT mode would add unnecessary drain to the battery.

The transition from MISSION mode to BROWNOUT mode is signaled by the *IE_PLLFALL* interrupt flag (in SFR 0xE8[7]). The transition in the other direction is signaled by the *IE_PLLRISE* interrupt flag (SFR 0xE8[6]), when the PLL becomes stable.

Transitions from both LCD and SLEEP mode back to BROWNOUT mode are initiated by wake-up timer timeout conditions or pushbutton events. When the PB pin is pulled high (pushbutton is pressed), the *IE_PB* interrupt flag (SFR 0xE8[4]) is set, and when the wake-up timer times out, the *IE_WAKE* interrupt flag (SFR 0xE8[5]) is set.

In the absence of system power, if the voltage margin for the LDO regulator providing 2.5 V to the internal circuitry becomes too low to be safe, the part automatically enters sleep mode (BAT_OK false). The battery voltage must stay above 3V to ensure that BAT_OK remains true. Under this condition, the 71M6521DE/DH/FE stays in SLEEP mode, even if the voltage margin for the LDO improves (BAT_OK true).

Table 60 shows the circuit functions available in each operating mode.

| Circuit Function | System Power | Battery Power (Non-volatile Supply) | | |
|---|---|---|---|---|
| | MISSION | BROWNOUT | LCD | SLEEP |
| CE | Yes | -- | -- | -- |
| CE Data RAM | Yes | Yes | -- | -- |
| FIR | Yes | -- | -- | -- |
| Analog circuits:<br>PLL, ADC, VREF, BME etc | Yes | -- | -- | -- |
| MPU clock rate | 4.92MHz<br>(from PLL) | 28.672kHz<br>(7/8 of 32768Hz) | -- | -- |
| *MPU_DIV* | Yes | -- | -- | -- |
| ICE | Yes | Yes | -- | -- |
| DIO Pins | Yes | Yes | -- | -- |
| Watchdog Timer | Yes | Yes | -- | -- |
| LCD | Yes | Yes | Yes | -- |
| EEPROM Interface (2-wire) | Yes | Yes (8kb/s) | -- | -- |
| EEPROM Interface (3-wire) | Yes | Yes (16kb/s) | -- | -- |
| UART | Yes | Yes | -- | -- |
| Optical TX modulation | Yes | -- | -- | -- |
| Flash Read | Yes | Yes | -- | -- |
| Flash Page Erase | Yes | Yes | -- | -- |
| Flash Write | Yes | -- | -- | -- |
| RAM Read and Write | Yes | Yes | -- | -- |
| Wakeup Timer | Yes | Yes | Yes | Yes |
| Oscillator and RTC | Yes | Yes | Yes | Yes |
| DRAM data preservation | Yes | Yes | -- | -- |
| V3P3D voltage output pin | Yes | Yes | -- | -- |

**Table 60: Available Circuit Functions ("—" means "not active)**

## BROWNOUT Mode

In BROWNOUT mode, most non-metering digital functions, as shown in Table 60, are active, including ICE, UART, EEPROM, LCD, and RTC. In BROWNOUT mode, a low bias current regulator will provide 2.5 Volts to V2P5 and V2P5NV. The regulator has an output called BAT_OK to indicate that it has sufficient overhead. When BAT_OK = 0, the part will enter SLEEP mode. From BROWNOUT mode, the MPU can voluntarily enter LCD or SLEEP modes. When system power is restored, the part will automatically transition from any of the battery modes to mission mode, once the PLL has settled.

The MPU will run at crystal clock rate in BROWNOUT. The value of *MPU_DIV* will be remembered (not changed) as the part enters and exits BROWNOUT. *MPU_DIV* will be ignored during BROWNOUT.

While *PLL_OK* = 0, the I/O RAM bits *ADC_E* and *CE_E* are held in zero state disabling both ADC and CE. When *PLL_OK* falls, the CE program counter is cleared immediately and all FIR processing halts. Figure 19 shows the functional blocks active in BROWNOUT mode.

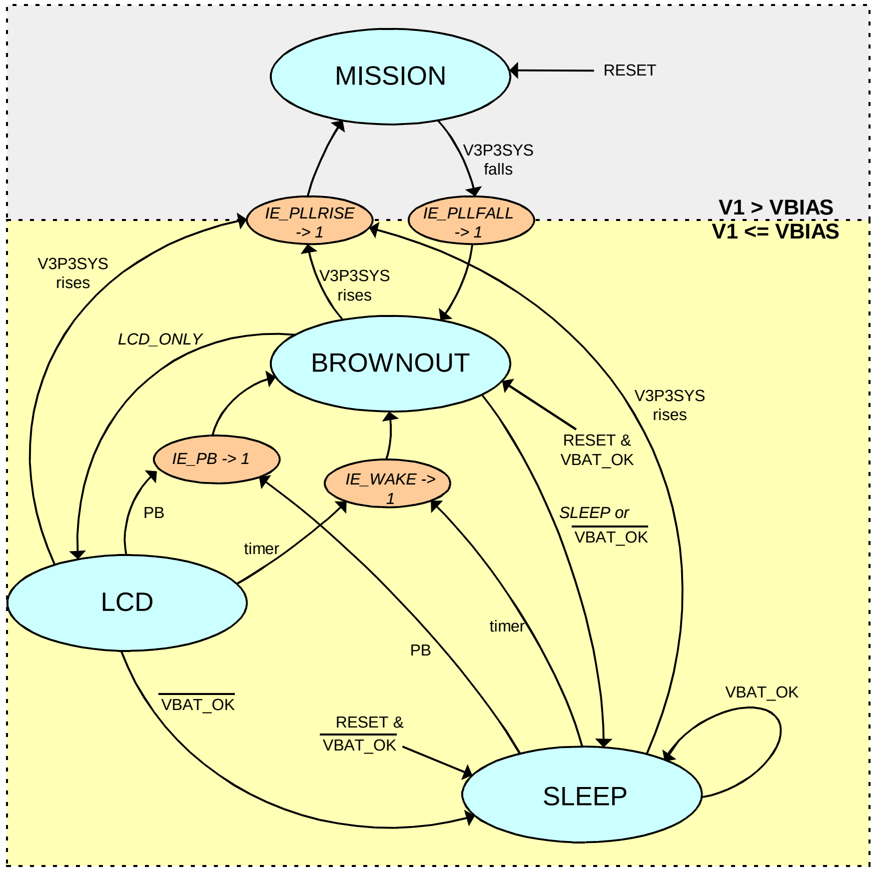



**Figure 18: Operation Modes State Diagram**

## LCD Mode

In LCD mode, the data contained in the *LCD_SEG* registers is displayed, i.e. up to four LCD segments connected to each of the pins SEG18 and SEG19 can be made to blink without the involvement of the MPU, which is disabled in LCD mode.

This mode can be exited only by system power up, a timeout of the wake-up timer, or a push button. Figure 20 shows the functional blocks active in LCD mode.

## SLEEP Mode

In SLEEP mode, the battery current is minimized and only the Oscillator and RTC functions are active. This mode can be exited only by system power-up, a timeout of the wake-up timer, or a push button event. Figure 21 shows the functional blocks active in SLEEP mode.

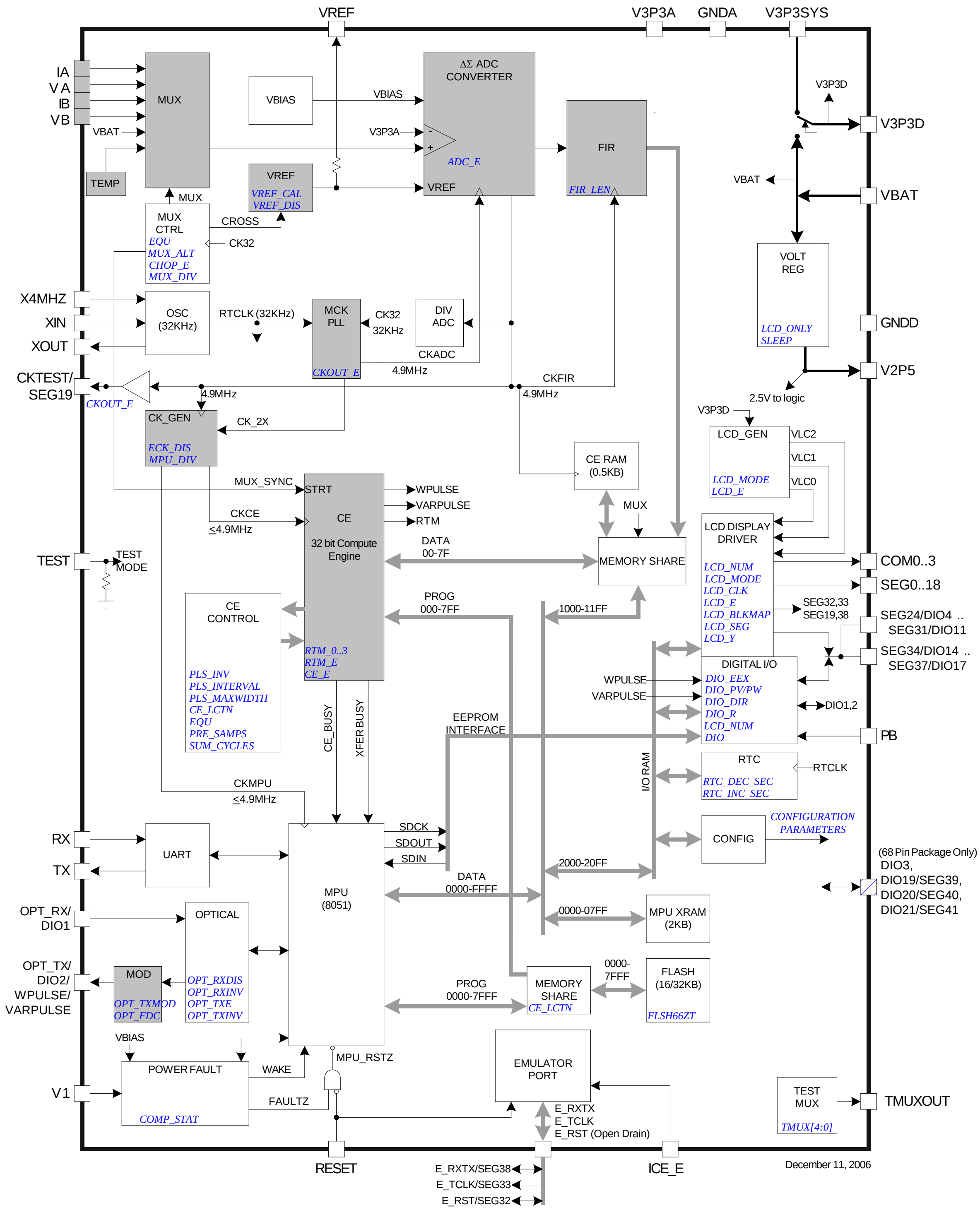



**Figure 19: Functional Blocks in BROWNOUT Mode (inactive blocks grayed out)**

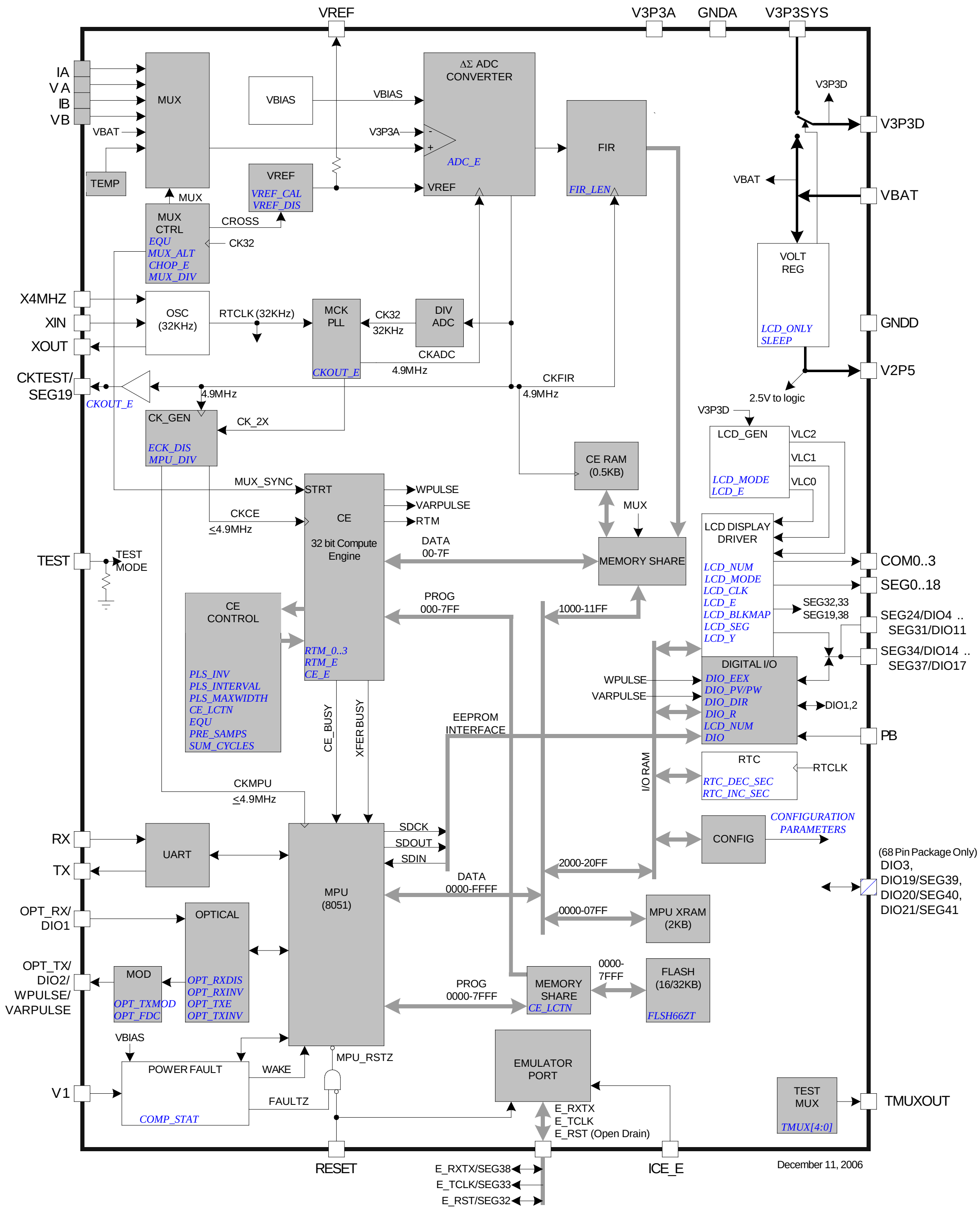



**Figure 20: Functional Blocks in LCD Mode (inactive blocks grayed out)**

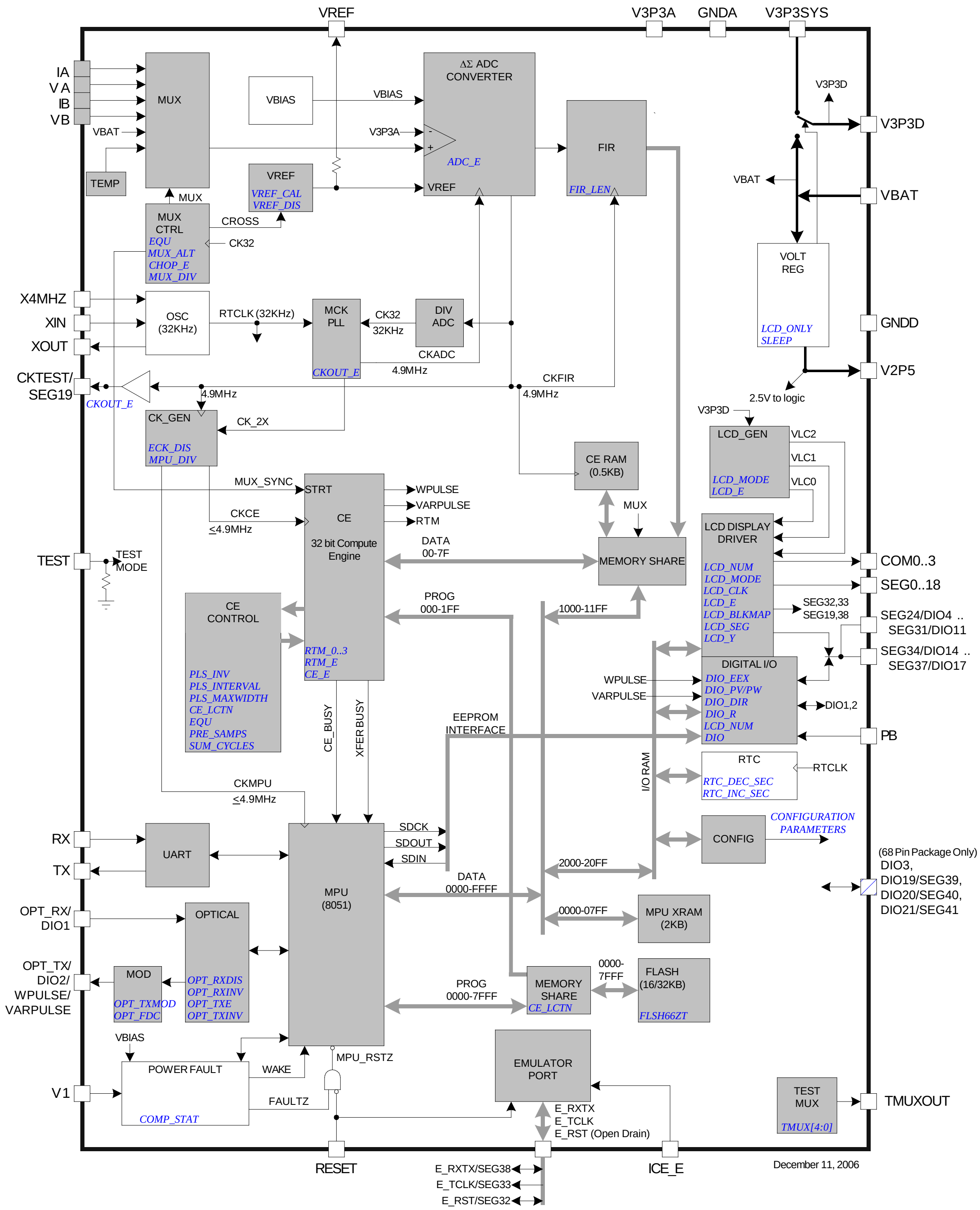



**Figure 21: Functional Blocks in SLEEP Mode (inactive blocks grayed out)**

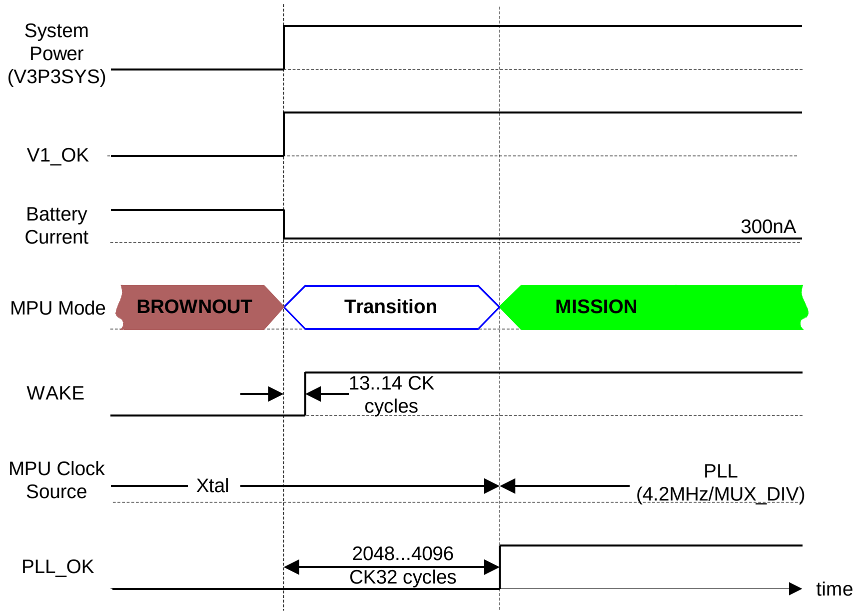



**Figure 22: Transition from BROWNOUT to MISSION Mode when System Power Returns**

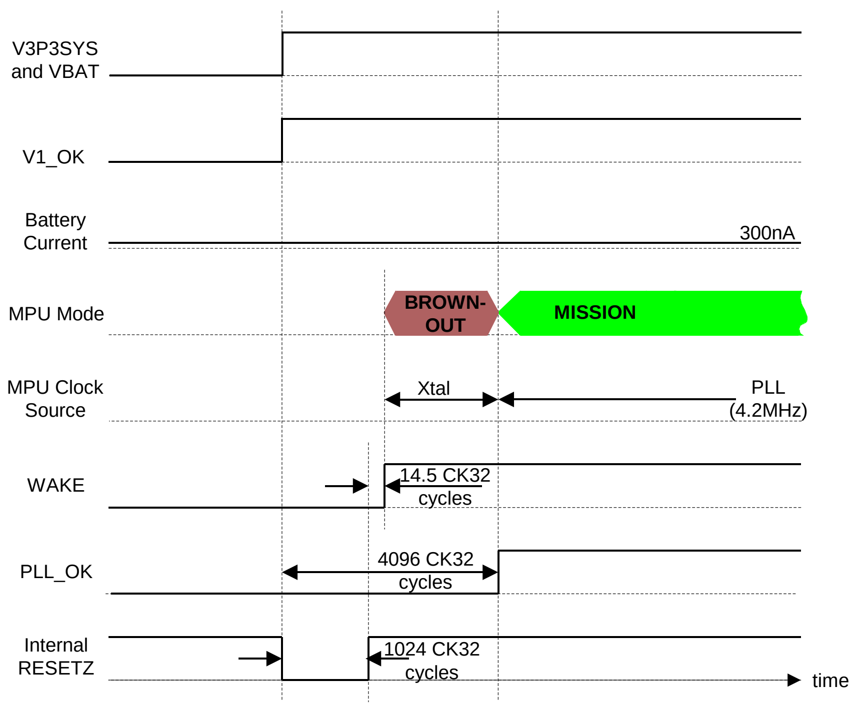



**Figure 23: Power-Up Timing with V3P3SYS and VBAT tied together**

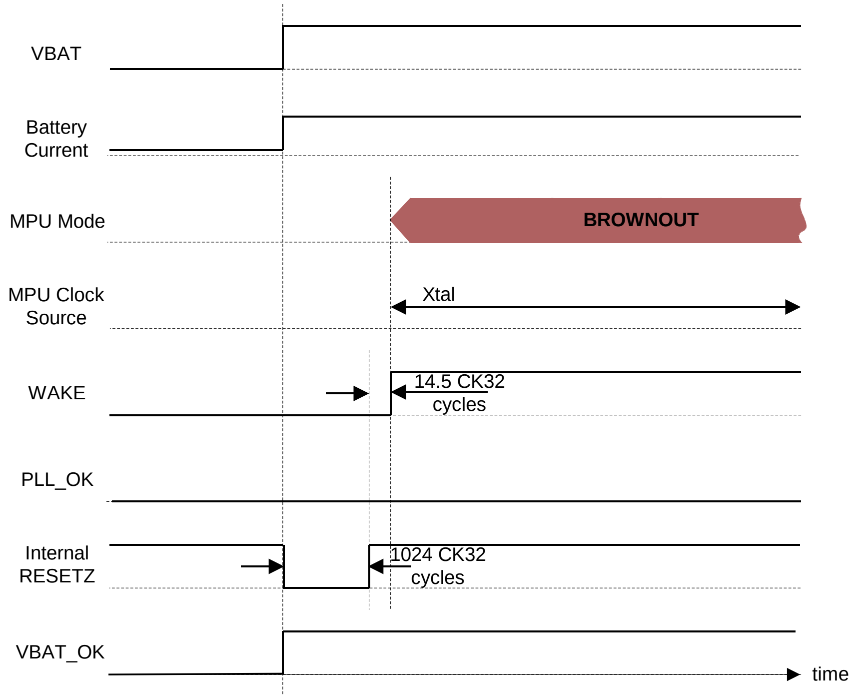



**Figure 24: Power-Up Timing with VBAT only**

## Fault and Reset Behavior

**Reset Mode:** When the RESET pin is pulled high all digital activity stops. The oscillator and RTC module continue to run. Additionally, all I/O RAM bits are set to their default states. As long as V1, the input voltage at the power fault block, is greater than VBIAS, the internal 2.5 V regulator will continue to provide power to the digital section.

Once initiated, the reset mode will persist until the reset timer times out, signified by the internal signal WAKE rising. This will occur in 4100 cycles of the real time clock after RESET goes low, at which time the MPU will begin executing its preboot and boot sequences from address 00. See the security section for more description of preboot and boot.

If system power is not present, the reset timer duration will be 2 cycles of the crystal clock, at which time the MPU will begin executing in BROWNOUT mode, starting at address 00.

**Power Fault Circuit:** The 71M6521DE/DH/FE includes a comparator to monitor system power fault conditions. When the output of the comparator falls (V1<VBIAS), the I/P RAM bits *PLL_OK* is zeroed and the part switches to BROWN-OUT mode if a battery is present. Once, system power returns, the MPU remains in reset and does not start Mission Mode until 4100 oscillator clocks later, when *PLL_OK* rises. If a battery is not present, indicated by BAT_OK=0, WAKE will fall and the part will enter SLEEP mode.

There are several conditions the part could be in as system power returns. If the part is in BROWNOUT mode, it will automatically switch to mission mode when PLL_OK rises. It will receive an interrupt indicating this. No configuration bits will be reset or reconfigured during this transition.

If the part is in LCD or SLEEP mode when system power returns, it will also switch to mission mode when PLL_OK rises. In this case, all configuration bits will be in the reset state due to WAKE having been zero. The RTC clock will not be disturbed, but the MPU RAM must be re-initialized. The hardware watchdog timer will become active when the part enters MISSION mode.

If there is no battery when system power returns, the part will switch to mission mode when PLL_OK rises. All configuration bits will be in reset state, and RTC and MPU RAM data will be unknown and must be initialized by the MPU.

## Wake Up Behavior

As described above, the part will always wake up in mission mode when system power is restored. Additionally, the part will wake up in BROWNOUT mode when PB rises (push button pressed) or when a timeout of the wake-up timer occurs.

## Wake on PB

If the part is in SLEEP or LCD mode, it can be awakened by a rising edge on the PB pin. This pin is normally pulled to GND and can be pulled high by a push button depression. Before the PB signal rises, the MPU is in reset due to the internal signal WAKE being low. When PB rises, WAKE rises and within three crystal cycles, the MPU begins to execute. The MPU can determine whether the PB signal woke it up by checking the *IE_PB* flag.

For debouncing, the PB pin is monitored by a state machine operating from a 32Hz clock. This circuit will reject between 31ms and 62ms of noise. Detection hardware will ignore all transitions after the initial rising edge. This will continue until the MPU clears the *IE_PB* bit.

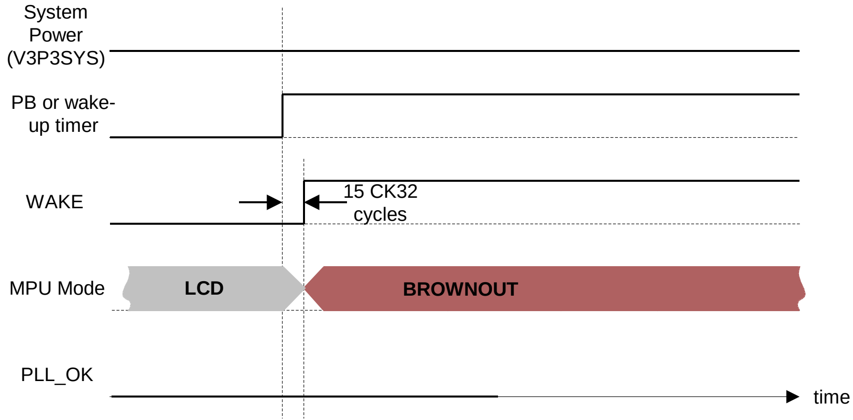



**Figure 25: Wake Up Timing**

## Wake on Timer

If the part is in SLEEP or LCD mode, it can be awakened by the wake-up timer. Until this timer times out, the MPU is in reset due to WAKE being low. When the wake-up timer times out, the WAKE signal rises and within three crystal cycles, the MPU begins to execute. The MPU can determine whether the timer woke it by checking the *AUTOWAKE* interrupt flag (*IE_WAKE*).

The wake-up timer begins timing when the part enters LCD or SLEEP mode. Its duration is controlled by *WAKE_PRD[2:0]* and *WAKE_RES*. *WAKE_RES* selects a timer LSB of either 1 minute (*WAKE_RES*=1) or 2.5 seconds (*WAKE_RES*=0). *WAKE_PRD[2:0]* selects a duration of from 1 to 7 LSBs.

The timer is armed by *WAKE_ARM*=1. It must be armed at least three RTC cycles before *SLEEP* or *LCD_ONLY* is initiated. Setting *WAKE_ARM* presets the timer with the values in *WAKE_RES* and *WAKE_PRD* and readies the timer to start when the MPU writes to *SLEEP* or *LCD_ONLY*. The timer is reset and disarmed whenever the MPU is awake. Thus, if it is desired to wake the MPU periodically (every 5 seconds, for example) the timer must be rearmed every time the MPU is awakened.

## Data Flow

The data flow between CE and MPU is shown in Figure 26. In a typical application, the 32-bit compute engine (CE) sequentially processes the samples from the voltage inputs on pins IA, VA, IB, and VB, performing calculations to measure active power (Wh), reactive power (VARh), $A^2h$, and $V^2h$ for four-quadrant metering. These measurements are then accessed by the MPU, processed further and output using the peripheral devices available to the MPU.

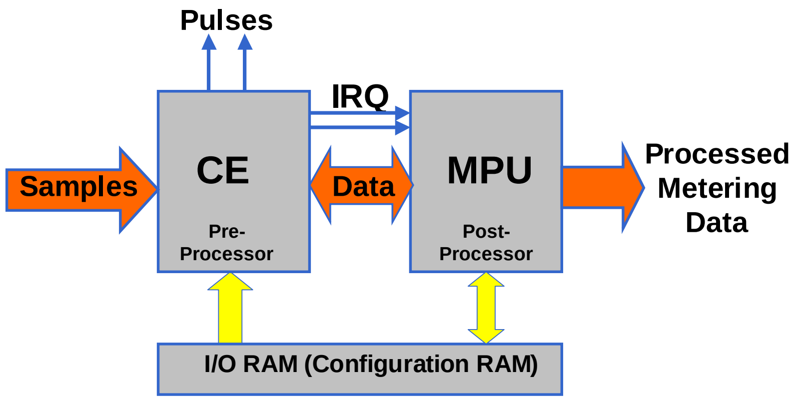



**Figure 26: MPU/CE Data Flow**

## CE/MPU Communication

Figure 27 shows the functional relationship between CE and MPU. The CE is controlled by the MPU via shared registers in the I/O RAM and by registers in the CE DRAM. The CE outputs two interrupt signals to the MPU: CE_BUSY and XFER_BUSY, which are connected to the MPU interrupt service inputs as external interrupts. CE_BUSY indicates that the CE is actively processing data. This signal will occur once every multiplexer cycle. XFER_BUSY indicates that the CE is updating data to the output region of the CE DRAM. This will occur whenever the CE has finished generating a sum by completing an accumulation interval determined by *SUM_CYCLES* * *PRE_SAMPS* samples. Interrupts to the MPU occur on the falling edges of the XFER_BUSY and CE_BUSY signals.

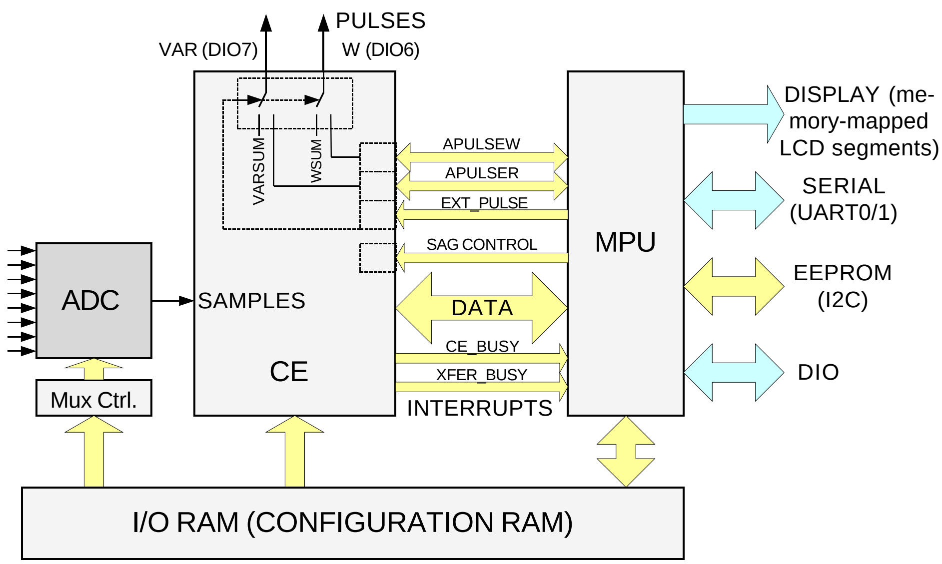



**Figure 27: MPU/CE Communication**

# APPLICATION INFORMATION

## Connection of Sensors (CT, Resistive Shunt)

Figure 28 and Figure 29 show how resistive dividers, current transformers, and restive shunts are connected to the voltage and current inputs of the 71M6521DE/DH/FE.

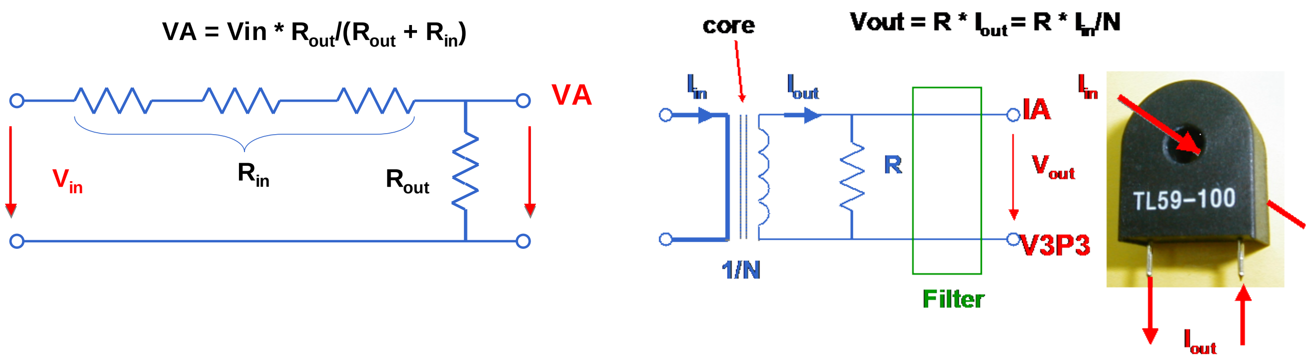



**Figure 28: Resistive Voltage Divider (Left), Current Transformer (Right)**

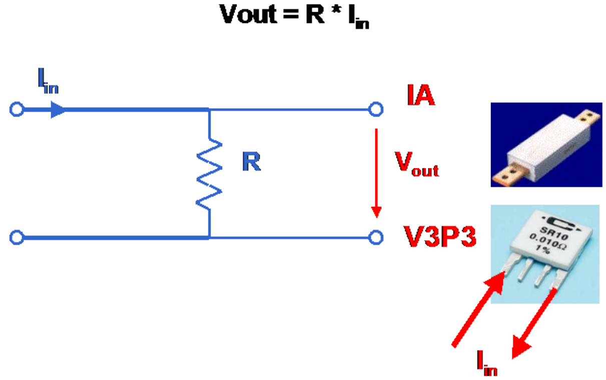



**Figure 29: Resistive Shunt**

## Distinction between 71M6521DE/71M6521FE and 71M6521DH Parts

The 71M6521DH (high-accuracy) part go through an additional process of characterization during production which makes them suitable to high-accuracy performance over temperature.

The first process, applied to all parts is the trimming of the reference voltage to the target value of 1.195 V.

The second process, which is applied only to the high-accuracy parts, is the characterization of the reference voltage over temperature. The coefficients for the reference voltage are stored in trim fuses (I/O RAM registers *TRIMBGA*, *TRIMBGB*, *TRIMM[2:0]*. The MPU can read these trim fuses and calculate the correction coefficients *PPM1* and *PPMC2* per the formulae given in **VREF, VBIAS** section. See Temperature Compensation section for additional details.

The fuse *TRIMBGB* is non-zero for the high-accuracy parts and zero for the regular parts.

## Temperature Measurement

Measurement of absolute temperature uses the on-chip temperature sensor while applying the following formula:

$$T = \frac{(N(T) - N_n)}{S_n} + T_n$$

In the above formula $T$ is the temperature in °C, N(T) is the ADC count at temperature T, $N_n$ is the ADC count at 25°C, $S_n$ is the sensitivity in LSB/°C as stated in the Electrical Specifications, and $T_n$ is +25°C.

**Example:** At 25°C a temperature sensor value of 518,203,584 ($N_n$) is read by the ADC by a 71M6521FE in the 64-pin LQFP package. At an unknown temperature T the value 449.648.000 is read at (N(T)). The absolute temperature is then determined by dividing both $N_n$ and N(T) by 512 to account for the 9-bit shift of the ADC value and then inserting the results into the above formula, using –2220 for LSB/°C:

$$T = \frac{449.648.000 - 518,203,584}{512 \cdot (-2220)} + 25C = 85.3°C$$

It is recommended to base temperature measurements on *TEMP_RAW_X* which is the sum of two consecutive temperature readings thus being higher by a factor of two than the raw sensor readings.

## Temperature Compensation

**Temperature Coefficients:** The internal voltage reference is calibrated during device manufacture.

For the 71M6521DE/FE, the temperature coefficients TC1 and TC2 are given as constants that represent typical component behavior (in µV/°C and µV/°C$^2$, respectively).

For the 71M6521DH, the temperature characteristics of the chip are measured during production and then stored in the fuse registers *TRIMBGA, TRIMBGB, TRIMT* and *TRIMM[2:0].* TC1 and TC2 can be derived from the fuses by using the relations given in the Electrical Specifications section.

Since TC1 and TC2 are given in µV/°C and µV/°C$^2$, respectively, the value of the VREF voltage (1.195 V) has to be taken into account when transitioning to PPM/°C and PPM/°C$^2$. This means that PPMC = 26.84*TC1/1.195, and PPMC2 = 1374*TC2/1.195.

Close examination of the electrical specification (see Table 61) for the parts with regular accuracy reveals that the achievable deviation is not strictly ±40 PPM/°C over the whole temperature range: Only for temperatures for which T-22 > 40 (i.e. T > 62°C) or for which T-22 < -40 (i.e. T < -18°C), the data sheet states ±40 PPM/°C. For temperatures between -18°C and +62°C, the error should be considered constant at ±1,600 PPM, or ±0.16%.

Similar considerations apply to the high-accuracy parts (see Table 62), where the error around the calibration temperature should be considered constant at ±800 PPM, or ±0.08%.

| Parameter | Condition | Min | | | Typ |
|---|---|---|---|---|---|
| VREF(T) deviation from VNOM(T) $\frac{VREF(T) - VNOM(T)}{VNOM(T)} \frac{10^6}{\max(\lvert T-22 \rvert, 40)}$ | | -40 | | +40 | PPM/ºC |

**Table 61: VREF Definition for the Regular Accuracy Parts**

| Parameter | Condition | Min | | | Typ |
|---|---|---|---|---|---|
| VREF(T) deviation from VNOM(T) $\frac{VREF(T)-VNOM(T)}{VNOM(T)} \cdot \frac{10^6}{\max(\lvert T-22\rvert,40)}$ | | -20 | | +20 | PPM/ºC |

**Table 62: VREF Definition for the High-Accuracy Parts**

Figure 30 and Figure 31 show this concept graphically. The “box” from -18°C to +62°C reflects the fact that it is impractical to measure the temperature coefficient of high-quality references at small temperature excursions. For example, at +25°C, the expected error would be ±3°C * 40 PPM/°C, or just 0.012% for the regular-accuracy parts..

The maximum deviation of ±2520 PPM (or 0.252%) for the regular-accuracy parts is reached at the temperature extremes. If the reference voltage is used to measure both voltage and current, the identical errors of ±0.252% add up to a maximum Wh registration error of ±0.504%.

The maximum deviation of ±1260 PPM (or 0.126%) for the high-accuracy parts is reached at the temperature extremes. If the reference voltage is used to measure both voltage and current, the identical errors of ±0.126% add up to a maximum Wh registration error of ±0.252%.

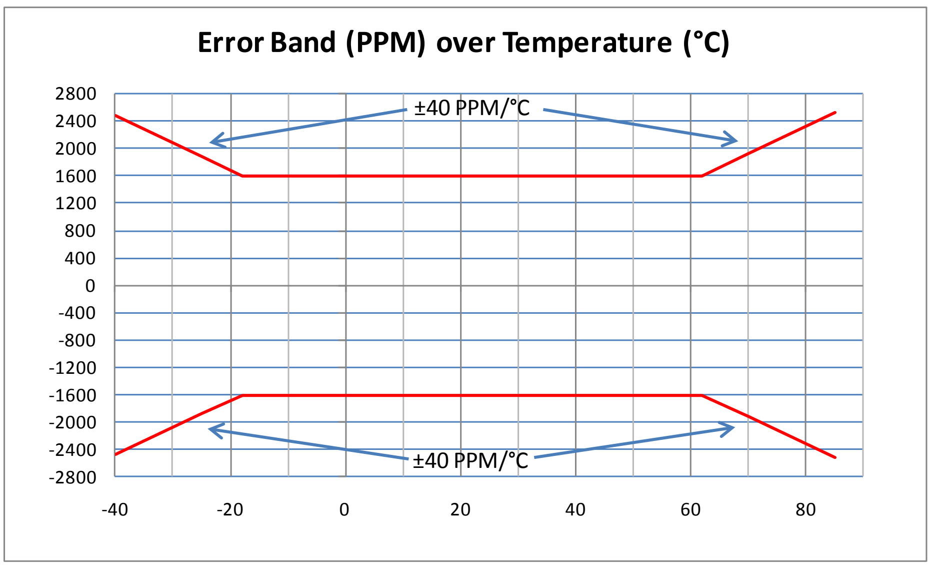



**Figure 30: Error Band for VREF over Temperature (Regular-Accuracy Parts)**

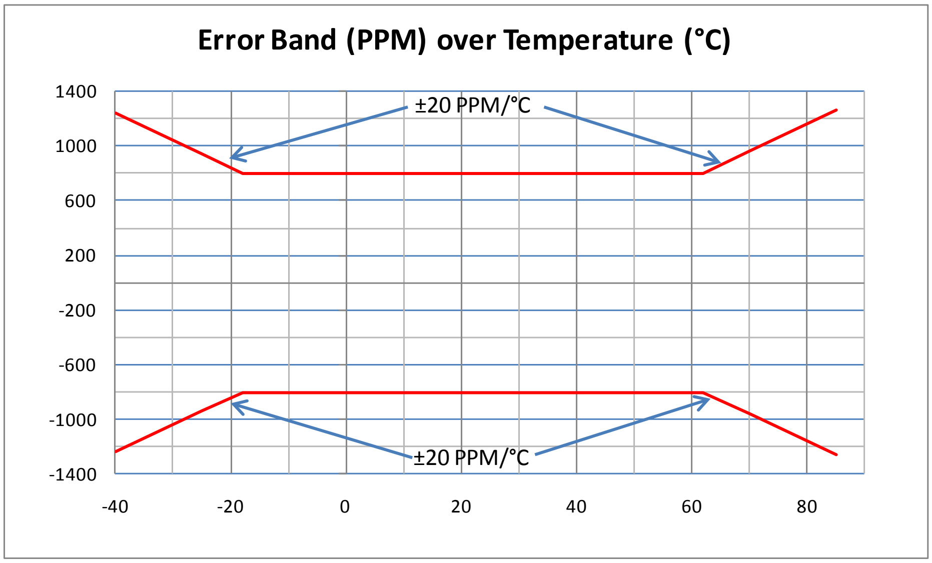



**Figure 31: Error Band for VREF over Temperature (High-Accuracy Parts)**

**Temperature Compensation**: The CE provides the bandgap temperature to the MPU, which then may digitally compensate the power outputs for the temperature dependence of VREF, using the CE register *GAIN_ADJ*. Since the band gap amplifier is chopper-stabilized via the *CHOP_EN* bits, the most significant long-term drift mechanism in the voltage reference is removed.

The MPU, not the CE, is entirely in charge of providing temperature compensation. The MPU applies the following formula to determine *GAIN_ADJ* (address 0x12). In this formula *TEMP_X* is the deviation from nominal or calibration temperature expressed in multiples of 0.1°C:

$$GAIN\_ADJ = 16385 + \frac{TEMP\_X \cdot PPMC}{2^{14}} + \frac{TEMP\_X^2 \cdot PPMC2}{2^{23}}$$

In a production electricity meter, the 71M6521DE/DH/FE is not the only component contributing to temperature dependency. A whole range of components (e.g. current transformers, resistor dividers, power sources, filter capacitors) will contribute temperature effects.

Since the output of the on-chip temperature sensor is accessible to the MPU, temperature-compensation mechanisms with great flexibility are possible. MPU access to *GAIN_ADJ* permits a system-wide temperature correction over the entire meter rather than local to the chip.

## Temperature Compensation and Mains Frequency Stabilization for the RTC

The flexibility provided by the MPU allows for compensation of the RTC using the substrate temperature. To achieve this, the crystal has to be characterized over temperature and the three coefficients *Y_CAL*, *Y_CALC*, and *Y_CAL_C2* have to be calculated. Provided the IC substrate temperatures tracks the crystal temperature the coefficients can be used in the MPU firmware to trigger occasional corrections of the RTC seconds count, using the *RTC_DEC_SEC* or *RTC_INC_SEC* registers in I/O RAM.

**Example:** Let us assume a crystal characterized by the measurements shown in Table 63:

| Deviation from Nominal Temperature [°C] | Measured Frequency [Hz] | Deviation from Nominal Frequency [PPM] |
|---|---|---|
| +50 | 32767.98 | -0.61 |
| +25 | 32768.28 | 8.545 |
| 0 | 32768.38 | 11.597 |
| -25 | 32768.08 | 2.441 |
| -50 | 32767.58 | -12.817 |

**Table 63: Frequency over Temperature**

The values show that even at nominal temperature (the temperature at which the chip was calibrated for energy), the deviation from the ideal crystal frequency is 11.6 PPM, resulting in about one second inaccuracy per day, i.e. more than some standards allow. As Figure 32 shows, even a constant compensation would not bring much improvement, since the temperature characteristics of the crystal are a mix of constant, linear, and quadratic effects.

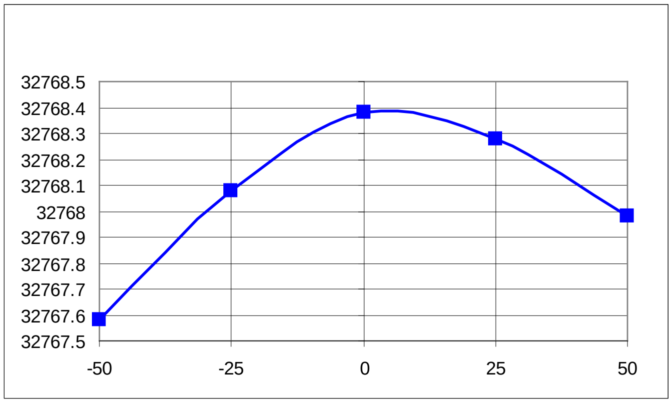



**Figure 32: Crystal Frequency over Temperature**

One method to correct the temperature characteristics of the crystal is to obtain coefficients from the curve in Figure 32 by curve-fitting the PPM deviations. A fairly close curve fit is achieved with the coefficients a = 10.89, b = 0.122, and c = –0.00714 (see Figure 33).

$$f = f_{nom} \cdot \left\{ 1 + \frac{a}{10^6} + T \frac{b}{10^6} + T^2 \frac{c}{10^6} \right\}$$

When applying the inverted coefficients, a curve (see Figure 33) will result that effectively neutralizes the original crystal characteristics.

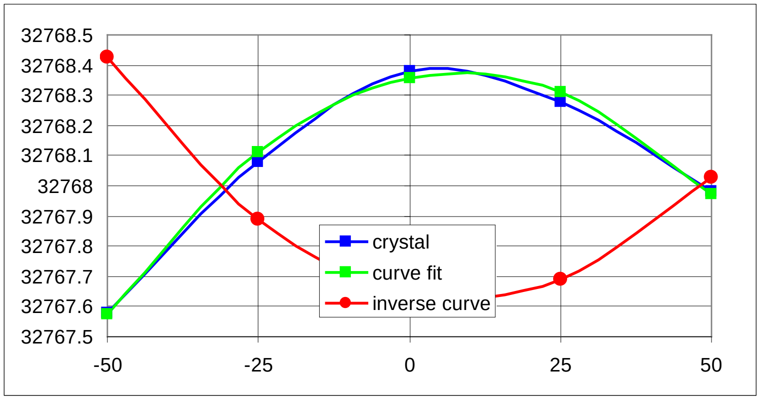



**Figure 33: Crystal Compensation**

The MPU Demo Code supplied with the Teridian Demo Kits has a direct interface for these coefficients and it directly controls the *RTC_DEC_SEC* or *RTC_INC_SEC* registers. The Demo Code uses the coefficients in the form:

$$CORRECTION(ppm) = \frac{Y\_CAL}{10} + T \cdot \frac{Y\_CALC}{100} + T^2 \cdot \frac{Y\_CALC2}{1000}$$

Note that the coefficients are scaled by 10, 100, and 1000 to provide more resolution. For our example case, the coefficients would then become (after rounding):

Y_CAL = 109, Y_CALC = 12, Y_CALC2 = 7

Alternatively, the mains frequency may be used to stabilize or check the function of the RTC. For this purpose, the CE provides a count of the zero crossings detected for the selected line voltage in the *MAIN_EDGE_X* address. This count is equivalent to twice the line frequency, and can be used to synchronize and/or correct the RTC.

## Connecting 5 V Devices

All digital input pins of the 71M6521DE/DH/FE are compatible with external 5 V devices. I/O pins configured as inputs do not require current-limiting resistors when they are connected to external 5 V devices.

## Connecting LCDs

The 71M6521DE/DH/FE has a LCD controller on-chip capable of controlling static or multiplexed LCDs. Figure 34 shows the basic connection for a LCD.

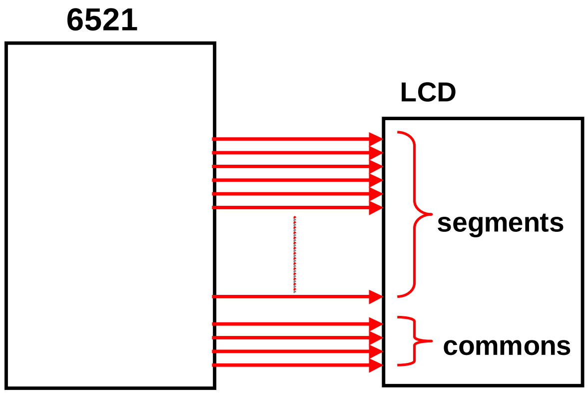



**Figure 34: Connecting LCDs**

The LCD segment pins can be organized in the following groups:

1. Nineteen pins are dedicated LCD segment pins (SEG0 to SEG18).
2. Four pins are dual-function pins CKTEST/SEG19, E_RXTX/SEG38, E_TCLK/SEG33, and E_RST/SEG32.
3. Twelve pins are available as combined DIO and segment pins SEG24/DIO4 to SEG31/DIO11 and SEG34/DIO14 to SEG37/DIO17)
4. The QFN-68 package adds the three combination pins SEG39/DIO19 to SEG41/DIO21.

The split between DIO and LCD use of the combined pins is controlled with the DIO register *LCD_NUM*. *LCD_NUM* can be assigned any number between 0 and 18. The first dual-purpose pin to be allocated as LCD is SEG41/DIO21 (on the 68-pin QFN package). Thus if *LCD_NUM*=2, SEG41 and SEG 40 will be configured as LCD. The remaining SEG39 to SEG24 will be configured as DIO19 to DIO4. DIO1 and DIO2 are always available, if not used for the optical port.

Note that pins CKTEST/SEG19, E_RXTX/SEG38, E_TCLK/SEG33, and E_RST/SEG32 are not affected by *LCD_NUM*.

Table 64 and Table 65 show the allocation of DIO and segment pins as a function of *LCD_NUM* for both package types.

| *LCD_NUM* | SEG in Addition to SEG0-SEG18 | Total Number of LCD Segment Pins Including SEG0-SEG18 | DIO Pins in Addition to DIO1-DIO2 | Total Number of DIO Pins Including DIO1, DIO2 |
|---|---|---|---|---|
| 0 | None | 19 | 4-11,14-17, 19-21 | 18 |
| 1 | 41 | 20 | 4-11, 14-17, 19-20 | 17 |
| 2 | 40-41 | 21 | 4-11, 14-17, 19 | 16 |
| 3 | 39-41 | 22 | 4-11, 14-17 | 15 |
| 4 | 39-41 | 22 | 4-11, 14-17 | 15 |
| 5 | 37, 39-41 | 23 | 4-11, 14-16 | 14 |
| 6 | 36-37, 39-41 | 24 | 4-11, 14-15 | 13 |
| 7 | 35-37, 39-41 | 25 | 4-11, 14 | 12 |
| 8 | 34-37, 39-41 | 26 | 4-11 | 11 |
| 9 | 34-37, 39-41 | 26 | 4-11 | 11 |
| 10 | 34-37, 39-41 | 27 | 4-11 | 11 |
| 11 | 31, 34-37, 39-41 | 27 | 4-10 | 10 |
| 12 | 30-31, 34-37, 39-41 | 28 | 4-9 | 9 |
| 13 | 29-31, 34-37, 39-41 | 29 | 4-8 | 8 |
| 14 | 28-31, 34-37, 39-41 | 30 | 4-7 | 7 |
| 15 | 27-31, 34-37, 39-41 | 31 | 4-6 | 6 |
| 16 | 26-31, 34-37, 39-41 | 32 | 4-5 | 5 |
| 17 | 25-31, 34-37, 39-41 | 33 | 4 | 4 |
| 18 | 24-31, 34-37, 39-41 | 34 | None | 3 |

Note: LCD segment numbers are given without CKTEST/SEG19, E_RXTX/SEG38, E_TCLK/SEG33, and E_RST/SEG32.

**Table 64: LCD and DIO Pin Assignment by *LCD_NUM* for the QFN-68 Package**

| *LCD_NUM* | SEG in Addition to SEG0-SEG18 | Total Number of LCD Segment Pins Including SEG0-SEG18 | DIO Pins in Addition to DIO1-DIO2 | Total Number of DIO Pins Including DIO1, DIO2 |
|---|---|---|---|---|
| 0 | - | 19 | 4-11, 14-17 | 14 |
| 1 | - | 19 | 4-11, 14-17 | 14 |
| 2 | - | 19 | 4-11, 14-17 | 14 |
| 3 | - | 19 | 4-11, 14-17 | 14 |
| 4 | - | 19 | 4-11, 14-17 | 14 |
| 5 | 37 | 20 | 4-11, 14-16 | 13 |
| 6 | 36-37 | 21 | 4-11, 14-15 | 12 |
| 7 | 35-37 | 22 | 4-11, 14 | 11 |
| 8 | 34-37 | 23 | 4-11 | 10 |
| 9 | 34-37 | 23 | 4-11 | 10 |
| 10 | 34-37 | 23 | 4-11 | 10 |
| 11 | 31, 34-37 | 24 | 4-10 | 9 |
| 12 | 30-31, 34-37 | 25 | 4-9 | 8 |
| 13 | 29-31, 34-37 | 26 | 4-8 | 7 |
| 14 | 28-31, 34-37 | 27 | 4-7 | 6 |
| 15 | 27-31, 34-37 | 28 | 4-6 | 5 |
| 16 | 26-31, 34-37 | 29 | 4-5 | 4 |
| 17 | 25-31, 34-37 | 30 | 4 | 3 |
| 18 | 24-31, 34-37 | 31 | None | 2 |

Note: LCD segment numbers are given without CKTEST/SEG19, E_RXTX/SEG38, E_TCLK/SEG33, and E_RST/SEG32.

**Table 65: LCD and DIO Pin Assignment by *LCD_NUM* for the LQFP-64 Package**

## Connecting I$^2$C EEPROMs

I$^2$C EEPROMs or other I$^2$C compatible devices should be connected to the DIO pins DIO4 and DIO5, as shown in Figure 35. Pull-up resistors of roughly 10kΩ to V3P3D (to ensure operation in BROWNOUT mode) should be used for both SCL and SDA signals. The *DIO_EEX* register in I/O RAM must be set to 01 in order to convert the DIO pins DIO4 and DIO5 to I$^2$C pins SCL and SDA

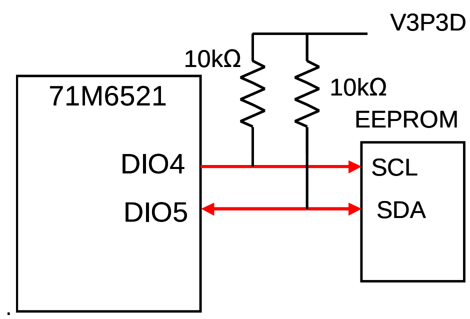



**Figure 35: I$^2$C EEPROM Connection**

## Connecting Three-Wire EEPROMs

µWire EEPROMs and other compatible devices should be connected to the DIO pins DIO4 and DIO5, as shown in Figure 36. DIO5 connects to both the DI and DO pins of the three-wire device. The CS pin must be connected to a vacant DIO pin of the 71M6521DE/DH/FE. A pull-up resistor of roughly 10kΩ to V3P3D (to ensure operation in BROWNOUT mode) should be used for the DI/DO signals, and the CS pin should be pulled down with a resistor to prevent that the three-wire device is selected on power-up, before the 71M6521DE/DH/FE can establish a stable signal for CS. The *DIO_EEX* register in I/O RAM must be set to 10 in order to convert the DIO pins DIO4 and DIO5 to MICROWIRE pins. The pull-up resistor for DIO5 may not be necessary.

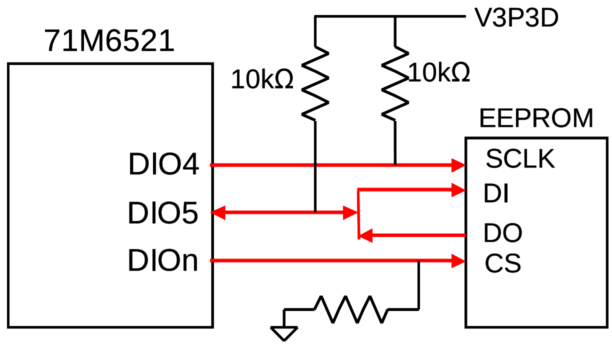



**Figure 36: Three-Wire EEPROM Connection**

## UART0 (TX/RX)

The RX pin should be pulled down by a 10kΩ resistor and additionally protected by a 100pF ceramic capacitor, as shown in Figure 37.

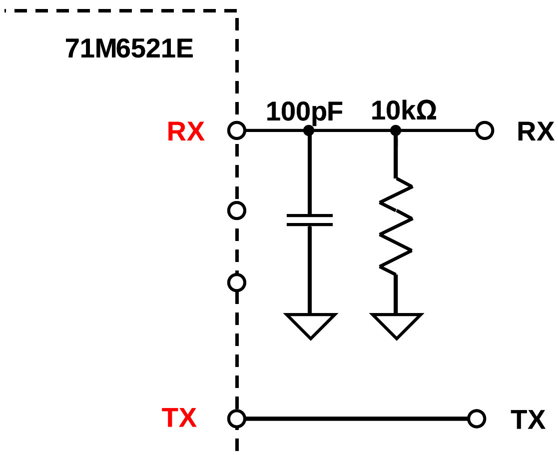



**Figure 37: Connections for the RX Pin**

## Optical Interface

The pins OPT_TX and OPT_RX can be used for a regular serial interface, e.g. by connecting a RS_232 transceiver, or they can be used to directly operate optical components, e.g. an infrared diode and phototransistor implementing a FLAG interface. Figure 38 shows the basic connections. The OPT_TX pin becomes active when the I/O RAM register *OPT_TXDIS* is set to 0.

The polarity of the OPT_TX and OPT_RX pins can be inverted with configuration bits *OPT_TXINV* and *OPT_RXINV*, respectively.

The OPT_TX output may be modulated at 38kHz when system power is present. Modulation is not available in BROWNOUT mode. The *OPT_TXMOD* bit enables modulation. The duty cycle is controlled by *OPT_FDC[1:0],* which can select 50%, 25%, 12.5%, and 6.25% duty cycle. A 6.25% duty cycle means OPT_TX is low for 6.25% of the period.

The receive pin (OPT_RX) may need an analog filter when receiving modulated optical signals.

With modulation, an optical emitter can be operated at higher current than nominal, enabling it to increase the distance along the optical path.

If operation in BROWNOUT mode is desired, the external components should be connected to V3P3D.

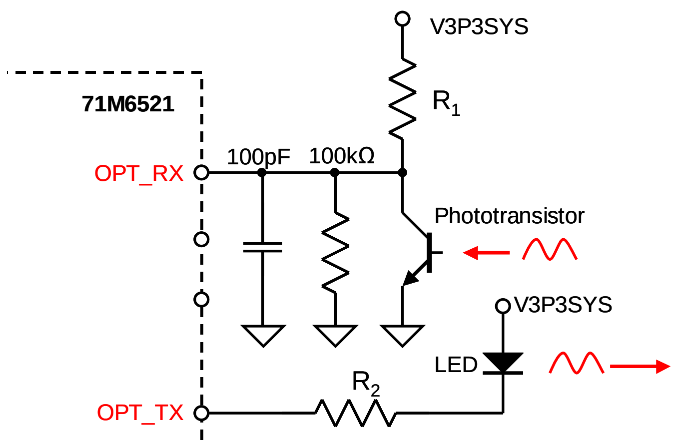



**Figure 38: Connection for Optical Components**

## Connecting V1 and Reset Pins

A voltage divider should be used to establish that V1 is in a safe range when the meter is in mission mode (V1 must be lower than 2.9V in all cases in order to keep the hardware watchdog timer enabled). For proper debugging or loading code into the 71M6521DE/DH/FE mounted on a PCB, it is necessary to have a provision like the header shown above R1 in Figure 39. A shorting jumper on this header pulls V1 up to V3P3 disabling the hardware watchdog timer.

The parallel impedance of R1 and R2 should be approximately 20 to 30kΩ in order to provide hysteresis for the power fault monitor.

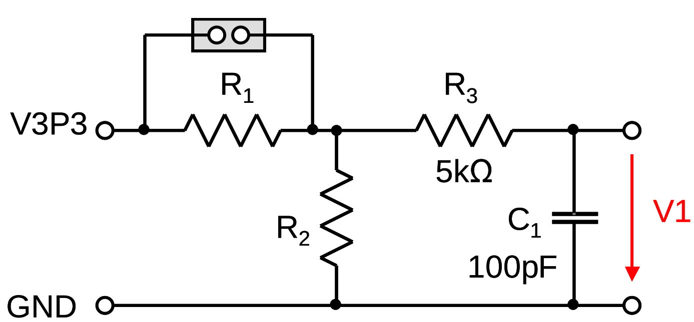



**Figure 39: Voltage Divider for V1**

Even though a functional meter will not necessarily need a reset switch, it is useful to have a reset pushbutton for prototyping, as shown in Figure 40, left side. The RESET signal may be sourced from V3P3SYS (functional in MISSION mode only), V3P3D (MISSION and BROWNOUT modes), VBAT (all modes, if battery is present), or from a combination of these sources, depending on the application. For a production meter, the RESET pin should be protected by the external components shown in Figure 40, right side. $R_1$ should be in the range of 100Ω and mounted as closely as possible to the IC.

Since the 71M6521DE/DH/FE generates its own power-on reset, a reset button or circuitry, as shown in Figure 40, left side, is only required for test units and prototypes.

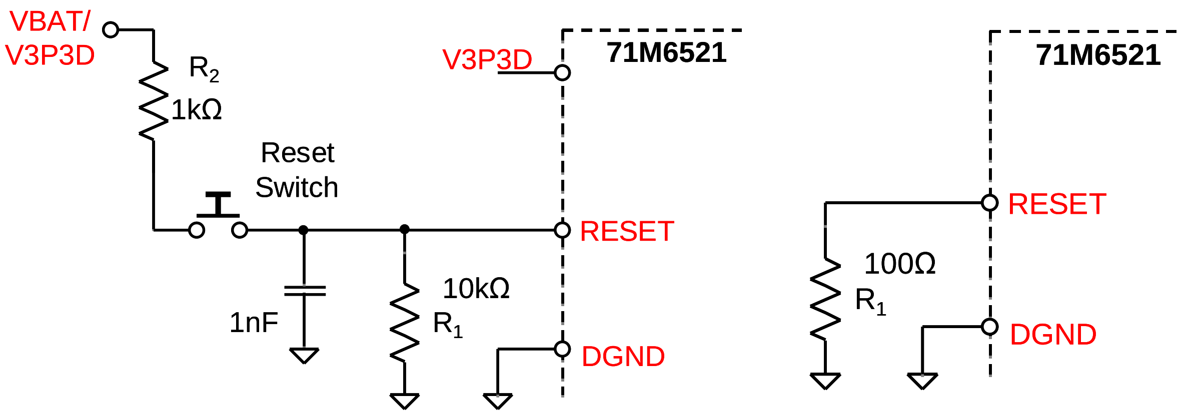



**Figure 40: External Components for RESET: Development Circuit (Left), Production Circuit (Right)**

## Connecting the Emulator Port Pins

Capacitors to ground must be used for protection from EMI. Production boards should have the ICE_E pin connected to ground.

If the ICE pins are used to drive LCD segments, the pull-up resistors should be omitted, as shown in Figure 41, and 22pF capacitors to GNDD should be used for protection from EMI.

**It is important to bring out the ICE_E pin to the programming interface in order to create a way for reprogramming parts that have the flash *SECURE* bit (SFR 0xB2[6]) set.** Providing access to ICE_E ensures that the part can be reset between erase and program cycles, which will enable programming devices to reprogram the part. The reset required is implemented with a watchdog timer reset (i.e. the hardware WDT must be enabled).

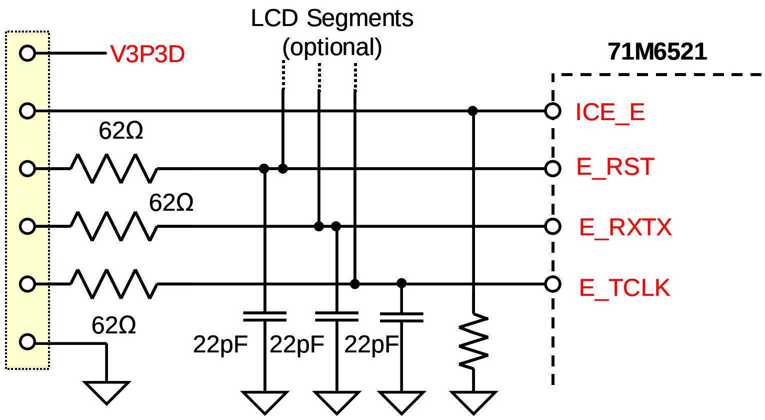



**Figure 41: External Components for the Emulator Interface**

## Crystal Oscillator

The oscillator of the 71M6521DE/DH/FE drives a standard 32.768kHz watch crystal. The oscillator has been designed specifically to handle these crystals and is compatible with their high impedance and limited power handling capability. The oscillator power dissipation is very low to maximize the lifetime of any battery backup device attached to VBAT.

Board layouts with minimum capacitance from XIN to XOUT will require less battery current. Good layouts will have XIN and XOUT shielded from each other.

**Since the oscillator is self-biasing, an external resistor must not be connected across the crystal.**

## Flash Programming

Operational or test code can be programmed into the flash memory using either an in-circuit emulator or the Teridian Flash Programmer Module (TFP-1). The flash programming procedure uses the E_RST, E_RXTX, and E_TCLK pins.

## MPU Firmware Library

All application-specific MPU functions mentioned above under "Application Information" are available as a standard ANSI C library and as ANSI "C" source code. The code is available as part of the Demonstration Kit for the 71M6521DE/DH/FE IC. The Demonstration Kits come with the 71M6521DE/DH/FE IC preprogrammed with demo firmware mounted on a functional sample meter PCB (Demo Board). The Demo Boards allow for quick and efficient evaluation of the IC without having to write firmware or having to supply an in-circuit emulator (ICE).

## Meter Calibration

Once the Teridian 71M6521DE/DH/FE energy meter device has been installed in a meter system, it has to be calibrated for tolerances of the current sensors, voltage dividers and signal conditioning components. The device can be calibrated using the gain and phase adjustment factors accessible to the CE. The gain adjustment is used to compensate for tolerances of components used for signal conditioning, especially the resistive components. Phase adjustment is provided to compensate for phase shifts introduced by the current sensors.

Due to the flexibility of the MPU firmware, any calibration method, such as calibration based on energy, or current and voltage can be implemented. It is also possible to implement segment-wise calibration (depending on current range).

The 71M6521DE/DH/FE supports common industry standard calibration techniques, such as single-point (energy-only), multi-point (energy, Vrms, Irms), and auto-calibration.

# FIRMWARE INTERFACE

## I/O RAM MAP – In Numerical Order

'Not Used' bits are grayed out, contain no memory and are read by the MPU as zero. *RESERVED* bits may be in use and should not be changed. This table lists only the SFR registers that are not generic 8051 SFR registers.

| Name | Addr | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Configuration:** | | | | | | | | | |
| CE0 | 2000 | *EQU[2:0]* | | | *CE_E* | Reserved | | | |
| CE1 | 2001 | *PRE_SAMPS[1:0]* | | *SUM_CYCLES[5:0]* | | | | | |
| CE2 | 2002 | *MUX_DIV[1:0]* | | *CHOP_E[1:0]* | | *RTM_E* | *WD_OVF* | *EX_RTC* | *EX_XFR* |
| COMP0 | 2003 | Not Used | *PLL_OK* | Not Used | Reserved | | Reserved | Reserved | *COMP_STAT[0]* |
| CONFIG0 | 2004 | *VREF_CAL* | *PLS_INV* | *CKOUT_E[1:0]* | | *VREF_DIS* | *MPU_DIV[2:0]* | | |
| CONFIG1 | 2005 | Reserved | Reserved | *ECK_DIS* | *FIR_LEN* | *ADC_E* | *MUX_ALT* | *FLSH66Z* | Reserved |
| VERSION | 2006 | *VERSION[7:0]* | | | | | | | |
| CONFIG2 | 2007 | *OPT_TXE[1:0]* | | *EX_PLL* | *EX_FWCOL* | Reserved | | *OPT_FDC[1:0]* | |
| CE3 | 20A8 | Not Used | Not Used | Not Used | *CE_LCTN[4:0]* | | | | |
| WAKE | 20A9 | *WAKE_ARM* | *SLEEP* | *LCD_ONLY* | Not Used | *WAKE_RES* | *WAKE_PRD[2:0]* | | |
| TMUX | 20AA | Not Used | Not Used | Not Used | *TMUX[4:0]* | | | | |
| **Digital I/O:** | | | | | | | | | |
| DIO0 | 2008 | *DIO_EEX[1:0]* | | *OPT_RXDIS* | *OPT_RXINV* | *DIO_PW* | *DIO_PV* | *OPT_TXMOD* | *OPT_TXINV* |
| DIO1 | 2009 | Not Used | *DIO_R1[2:0]* | | | Not Used | *DI_RPB[2:0]* | | |
| DIO2 | 200A | Not Used | Reserved | | | Not Used | *DIO_R2[2:0]* | | |
| DIO3 | 200B | Not Used | *DIO_R5[2:0]* | | | Not Used | *DIO_R4[2:0]* | | |
| DIO4 | 200C | Not Used | *DIO_R7[2:0]* | | | Not Used | *DIO_R6[2:0]* | | |
| DIO5 | 200D | Not Used | *DIO_R9[2:0]* | | | Not Used | *DIO_R8[2:0]* | | |
| DIO6 | 200E | Not Used | *DIO_R11[2:0]* | | | Not Used | *DIO_R10[2:0]* | | |
| **Real Time Clock:** | | | | | | | | | |
| RTC0 | 2015 | Not Used | Not Used | *RTC_SEC[5:0]* | | | | | |
| RTC1 | 2016 | Not Used | Not Used | *RTC_MIN[5:0]* | | | | | |
| RTC2 | 2017 | Not Used | Not Used | Not Used | *RTC_HR[4:0]* | | | | |
| RTC3 | 2018 | Not Used | Not Used | Not Used | Not Used | Not Used | *RTC_DAY[2:0]* | | |
| RTC4 | 2019 | Not Used | Not Used | Not Used | *RTC_DATE[2:0]* | | | | |
| RTC5 | 201A | Not Used | Not Used | Not Used | Not Used | *RTC_MO[3:0]* | | | |
| RTC6 | 201B | *RTC_YR[7:0]* | | | | | | | |
| RTC7 | 201C | Not Used | Not Used | Not Used | Not Used | Not Used | Not Used | *RTC_DEC_SEC* | *RTC_INC_SEC* |
| WE | 201F | *Write enable for RTC* | | | | | | | |
| **LCD Display Interface:** | | | | | | | | | |
| LCDX | 2020 | Not Used | *BME* | Reserved | *LCD_NUM[4:0]* | | | | |
| LCDY | 2021 | Not Used | *LCD_Y* | *LCD_E* | *LCD_MODE[2:0]* | | | *LCD_CLK[1:0]* | |
| LCDZ | 2022 | Not Used | Not Used | Not Used | Reserved | | | | |
| LCD0 | 2030 | Not Used | | | | *LCD_SEG0[3:0]* | | | |
| … | … | Not Used | | | | … | | | |
| LCD19 | 2043 | Not Used | | | | *LCD_SEG19[3:0]* | | | |
| LCD24 | 2048 | Not Used | | | | *LCD_SEG24[3:0]* | | | |
| … | … | Not Used | | | | … | | | |
| LCD38 | 2056 | Not Used | | | | *LCD_SEG38[3:0]* | | | |
| LCD_BLNK | 205A | *LCD_BLKMAP19[3:0]* | | | | *LCD_BLKMAP18[3:0]* | | | |

| | | |
|---|---|---|
| **RTM Probes:** | | |
| RTM0 | 2060 | *RTM0[7:0]* |
| RTM1 | 2061 | *RTM1[7:0]* |
| RTM2 | 2062 | *RTM2[7:0]* |
| RTM3 | 2063 | *RTM3[7:0]* |
| **Pulse Generator:** | | |
| PLS_W | 2080 | *PLS_MAXWIDTH[7:0]* |
| PLS_I | 2081 | *PLS_INTERVAL[7:0]* |
| | | |

## SFR MAP (SFRs Specific to the Teridian 80515) – In Numerical Order

'Not Used' bits are blacked out and contain no memory and are read by the MPU as zero. *RESERVED* bits are in use and should not be changed. This table lists only the SFR registers that are not generic 8051 SFR registers

| Name | SFR | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Digital I/O:** | | | | | | | | | |
| DIO7 | 80 | *DIO_0[7:4]* (Port 0) | | | | Reserved | *DIO_0[2:1]* | | *PB* |
| DIO8 | A2 | *DIO_DIR0[7:4]* | | | | Reserved | *DIO_DIR0[2:1]* | | Reserved |
| DIO9 | 90 | *DIO_1[7:6]* | | Reserved | | *DIO_1[3:0]* (Port 1) | | | |
| DIO10 | 91 | *DIO_DIR1[7:6]* | | Reserved | | *DIO_DIR1[3:0]* | | | |
| DIO11 | A0 | Not Used | Not Used | *DIO2[5:3]* (QFN-68) * | | | Reserved | *DIO_2[1:0]* (Port 2) | |
| DIO12 | A1 | Not Used | Not Used | *DIO_DIR2[5:3]* (QFN-68) * | | | Reserved | *DIO_DIR2[1:0]* | |
| **Interrupts and WD Timer:** | | | | | | | | | |
| INTBITS | F8 | | *INT6* | *INT5* | *INT4* | *INT3* | *INT2* | *INT1* | *INT0* |
| IFLAGS | E8 | *IE_PLLFALL WD_RST* | *IE_PLLRISE* | *IE_WAKE* | *IE_PB* | *IE_FWCOL1* | *IE_FWCOL0* | *IE_RTC* | *IE_XFER* |
| **Flash:** | | | | | | | | | |
| ERASE | 94 | *FLSH_ERASE[7:0]* | | | | | | | |
| FLSHCTL | B2 | *PREBOOT* | *SECURE* | Not Used | Not Used | Not Used | Not Used | *FLSH_MEEN* | *FLSH_PWE* |
| PGADR | B7 | *FLSH_PGADR[6:0]* | | | | | | | Not Used |
| **Serial EEPROM:** | | | | | | | | | |
| EEDATA | 9E | *EEDATA[7:0]* | | | | | | | |
| EECTRL | 9F | *EECTRL[7:0]* | | | | | | | |

* = Only available on QFN-68 package. Reserved in LQFP-64 package.

# I/O RAM DESCRIPTION – Alphabetical Order

Bits with a **W** (write) direction are written by the MPU into configuration RAM. Typically, they are initially stored in flash memory and copied to the configuration RAM by the MPU. Some of the more frequently programmed bits are mapped to the MPU SFR memory space. The remaining bits are mapped to the address range 0x2xxx. Bits with R (read) direction can be read by the MPU. Columns labeled "**Rst**" and "**Wk**" describe the bit values upon reset and wake, respectively. No entry in one of these columns means the bit is either read-only or is powered by the non-volatile supply and is not initialized. Write-only bits will return zero when they are read.

| Name | Location | Rst | Wk | Dir | Description |
|---|---|---|---|---|---|
| *ADC_E* | 2005[3] | 0 | 0 | R/W | Enables ADC and VREF. When disabled, removes bias current |
| *BME* | 2020[6] | 0 | - | R/W | Battery Measure Enable. When set, a load current is immediately applied to the battery and it is connected to the ADC to be measured on Alternative Mux Cycles. See *MUX_ALT* bit. |
| *CE_E* | 2000[4] | 0 | 0 | R/W | CE enable. |
| *CE_LCTN[4:0]* | 20A8[4:0] | 31 | 31 | R/W | CE program location. The starting address for the CE program is 1024**CE_LCTN*. *CE_LCTN* must be defined before the CE is enabled. |
| *CHOP_E[1:0]* | 2002[5:4] | 0 | 0 | R/W | Chop enable for the reference bandgap circuit. The value of CHOP will change on the rising edge of MUXSYNC according to the value in *CHOP_E:*<br>00-toggle[1] 01-positive 10-reversed 11-toggle<br>[1]except at the mux sync edge at the end of SUMCYCLE. |
| *CKOUT_E[1:0]* | 2004[5,4] | 00 | 00 | R/W | CKTEST Enable. The default is 00<br>00-SEG19,<br>01-CK_FIR (5MHz Mission, 32kHz Brownout)<br>10-Not allowed (reserved for production test)<br>11-Same as 10. |
| *COMP_STAT[0]* | 2003[0] | -- | -- | R | The status of the power fail comparator for V1. |
| *DI_RPB[2:0]*<br>*DIO_R1[2:0]*<br>*DIO_R2[2:0]*<br>*DIO_R4[2:0]*<br>*DIO_R5[2:0]*<br>*DIO_R6[2:0]*<br>*DIO_R7[2:0]*<br>*DIO_R8[2:0]*<br>*DIO_R9[2:0]*<br>*DIO_R10[2:0]*<br>*DIO_R11[2:0]* | 2009[2:0]<br>2009[6:4]<br>200A[2:0]<br>200B[2:0]<br>200B[6:4]<br>200C[2:0]<br>200C[6:4]<br>200D[2:0]<br>200D[6:4]<br>200E[2:0]<br>200E[6:4] | 0<br>0<br>0<br>0<br>0<br>0<br>0<br>0<br>0<br>0<br>0 | 0<br>0<br>0<br>0<br>0<br>0<br>0<br>0<br>0<br>0<br>0 | R/W | Connects dedicated I/O pins DIO2 and DIO4 through DIO11 as well as input pins PB and DIO1 to internal resources. If more than one input is connected to the same resource, the 'MULTIPLE' column below specifies how they are combined.<br>*DIO_Rx* / **Resource** / **MULTIPLE**:<br>000 / NONE / --<br>001 / Reserved / OR<br>010 / T0 (Timer0 clock or gate) / OR<br>011 / T1 (Timer1 clock or gate) / OR<br>100 / High priority IO interrupt (int0 rising) / OR<br>101 / Low priority IO interrupt (int1 rising) / OR<br>110 / High priority IO interrupt (int0 falling) / OR<br>111 / Low priority IO interrupt (int1 falling) / OR |
| *DIO_DIR0[7:4,2:1]* | SFRA2<br>[7:4,2:0] | 0 | 0 | R/W | Programs the direction of pins DIO7-DIO4 and DIO2-DIO1. 1 indicates output. Ignored if the pin is not configured as I/O. See *DIO_PV* and *DIO_PW* for special option for DIO6 and DIO7 outputs. See *DIO_EEX* for special option for DIO4 and DIO5. |

| | | | | | |
|---|---|---|---|---|---|
| *DIO_DIR1[7:6, 3:0]* | SFR91 [7:6,3:0] | 0 | 0 | R/W | Programs the direction of pins DIO15-DIO14, DIO11-DIO8. 1 indicates output. Ignored if the pin is not configured as I/O. |
| *DIO_DIR2 [5:3,2:1]* | SFRA1 [5:3,2:1] | 0 | 0 | R/W | Programs the direction of pins DIO17-DIO16 (and DIO19-DIO21 for the QFN package). 1 indicates output. Ignored if the pin is not configured as I/O. |
| *DIO_0[7:4,2:0]* | SFR80 [7:4,2:0] | 0 | 0 | R/W | The value on the pins DIO7-DIO4 and DIO2-DIO1. Pins configured as LCD will read zero. When written, changes data on pins configured as outputs. Pins configured as LCD or input will ignore write operations. The pushbutton input PB is read on *DIO_0[0]*. |
| *DIO_1[7:6,3:0]* | SFR90 [7:6,3:0] | 0 | 0 | R/W | The value on the pins DIO15-DIO14 and DIO11-DIO8. Pins configured as LCD will read zero. When written, changes data on pins configured as outputs. Pins configured as LCD or input will ignore write operations. |
| *DIO_2[5:3,1:0]* | SFRA0 [5:3,1:0] | 0 | 0 | R/W | The value on the pins DIO17-DIO16 (and DIO19-DIO21 for the QFN package). Pins configured as LCD will read zero. When written, changes data on pins configured as outputs. Pins configured as LCD or input will ignore write operations. |
| *DIO_EEX[1:0]* | 2008[7:6] | 0 | 0 | R/W | When set, converts DIO4 and DIO5 to interface with external EEPROM. DIO4 becomes SDCK and DIO5 becomes bi-directional SDATA. *LCD_NUM* must be less than or equal to 18.<br>**DIO_EEX[1:0]** — **Function**<br>00 — Disable EEPROM interface<br>01 — 2-Wire EEPROM interface<br>10 — 3-Wire EEPROM interface<br>11 — --not used-- |
| *DIO_PV* | 2008[2] | 0 | 0 | R/W | Causes VARPULSE to be output on DIO7, if DIO7 is configured as output. *LCD_NUM* must be less than 15. |
| *DIO_PW* | 2008[3] | 0 | 0 | R/W | Causes WPULSE to be output on DIO6, if DIO6 is configured as output. *LCD_NUM* must be less than 16. |
| *EEDATA[7:0]* | SFR9E | 0 | 0 | R/W | Serial EEPROM interface data |
| *EECTRL[7:0]* | SFR9F | 0 | 0 | R/W | Serial EEPROM interface control |
| *ECK_DIS* | 2005[5] | 0 | 0 | R/W | Emulator clock disable. When one, the emulator clock is disabled. **This bit is to be used with caution! Inadvertently setting this bit will inhibit access to the part with the ICE interface and thus preclude flash erase and programming operations**. If ECK_ENA is set, it should be done at least 1000ms after power-up to give emulators and programming devices enough time to complete an erase operation. |
| *EQU[2:0]* | 2000[7:5] | 0 | 0 | R/W | Specifies the power equation to be used by the CE. |
| *EX_XFR*<br>*EX_RTC*<br>*EX_FWCOL*<br>*EX_PLL* | 2002[0]<br>2002[1]<br>2007[4]<br>2007[5] | 0<br>0<br>0<br>0 | 0<br>0<br>0<br>0 | R/W | Interrupt enable bits. These bits enable the XFER_BUSY, the RTC_1SEC, the FirmWareCollision, and PLL interrupts. Note that if one of these interrupts is to be enabled, its corresponding EX enable bit must also be set. See the Interrupts section for details. |
| *FIR_LEN* | 2005[4] | 0 | 0 | R/W | The length of the ADC decimation FIR filter.<br>1-384 cycles, 0-288 cycles<br>When *FIR_LEN*=1, the ADC has 2.370370x higher gain. |

| | | | | | |
|---|---|---|---|---|---|
| *FLSH_ERASE[7:0]* | SFR94[7:0] | 0 | 0 | W | Flash Erase Initiate<br>*FLSH_ERASE* is used to initiate either the Flash Mass Erase cycle or the Flash Page Erase cycle. Specific patterns are expected for *FLSH_ERASE* in order to initiate the appropriate Erase cycle.<br>(default = 0x00).<br>0x55 – Initiate Flash Page Erase cycle. Must be proceeded by a write to FLSH_PGADR @ SFR 0xB7.<br>0xAA – Initiate Flash Mass Erase cycle. Must be proceeded by a write to FLSH_MEEN @ SFR 0xB2 and the debug (CC) port must be enabled.<br>Any other pattern written to FLSH_ERASE will have no effect. |
| *FLSH_MEEN* | SFRB2[1] | 0 | 0 | W | Mass Erase Enable<br>0 – Mass Erase disabled (default).<br>1 – Mass Erase enabled.<br>**Must be re-written for each new Mass Erase cycle.** |
| *FLSH_PGADR[6:0]* | SFRB7[7:1] | 0 | 0 | W | Flash Page Erase Address<br>*FLSH_PGADR[6:0]* – Flash Page Address (page 0 thru 127) that will be erased during the Page Erase cycle. (default = 0x00).<br>**Must be re-written for each new Page Erase cycle.** |
| *FLSH_PWE* | SFRB2[0] | 0 | 0 | R/W | Program Write Enable<br>0 – MOVX commands refer to XRAM Space, normal operation (default).<br>1 – MOVX @DPTR,A moves A to Program Space (Flash) @ DPTR.<br>This bit is automatically reset after each byte written to flash. Writes to this bit are inhibited when interrupts are enabled. |
| *FOVRIDE* | 20FD[4] | 0 | 0 | R/W | Permits the values written by MPU to temporarily override the values in the fuse register (reserved for production test). |
| *IE_FWCOL0*<br>*IE_FWCOL1* | SFRE8[2]<br>SFRE8[3] | 0<br>0 | 0<br>0 | R/W<br>R/W | Interrupt flags for Firmware Collision Interrupt. See Flash Memory Section for details. |
| *IE_PB* | SFRE8[4] | 0 | -- | R/W | PB flag. Indicates that a rising edge occurred on PB. Firmware must write a zero to this bit to clear it. The bit is also cleared when MPU requests SLEEP or LCD mode. On bootup, the MPU can read this bit to determine if the part was woken with the PB DIO0[0]. |
| *IE_PLLRISE* | SFRE8[6] | 0 | 0 | R/W | Indicates that the MPU was woken or interrupted (int 4) by System power becoming available, or more precisely, by PLL_OK rising. Firmware must write a zero to this bit to clear it |
| *IE_PLLFALL* | SFRE8[7] | 0 | 0 | R/W | Indicates that the MPU has entered BROWNOUT mode because System power has become unavailable (int 4), or more precisely, because PLL_OK fell.<br>Note: this bit will not be set if the part wakes into BROWNOUT mode because of PB or the WAKE timer. Firmware must write a zero to this bit to clear it. |
| *IE_XFER*<br>*IE_RTC* | SFRE8[0]<br>SFRE8[1] | 0<br>0 | 0<br>0 | R/W | Interrupt flags. These flags monitor the XFER_BUSY interrupt and the RTC_1SEC interrupt. The flags are set by hardware and must be cleared by the interrupt handler. Note that IE6, the interrupt 6 flag bit in the MPU must also be cleared when either of these interrupts occur. |
| *IE_WAKE* | SFRE8[5] | 0 | -- | R/W | Indicates that the MPU was woken by the autowake timer. This bit is typically read by the MPU on bootup. Firmware must write a zero to this bit to clear it |
| *INTBITS* | SFRF8[6:0] | -- | -- | R/W | Interrupt inputs. The MPU may read these bits to see the input to external interrupts INT0, INT1, up to INT6. These bits do not have any memory and are primarily intended for debug use. |
| *LCD_BLKMAP19[3:0]*<br>*LCD_BLKMAP18[3:0]* | 205A[7:4]<br>205A[3:0] | 0 | -- | R/W | Identifies which segments connected to SEG18 and SEG19 should blink. 1 means 'blink.' Most significant bit corresponds to COM3. Least significant, to COM0. |
| *LCD_CLK[1:0]* | 2021[1:0] | 0 | -- | R/W | Sets the LCD clock frequency (for COM/SEG pins, not frame rate).<br>Note: $f_w = 32768Hz$<br>00: $f_w/2^9$, 01: $f_w/2^8$, 10: $f_w/2^7$, 11: $f_w/2^6$ |

| | | | | | |
|---|---|---|---|---|---|
| *LCD_E* | 2021[5] | 0 | -- | R/W | Enables the LCD display. When disabled, VLC2, VLC1, and VLC0 are ground as are the COM and SEG outputs. |
| *LCD_MODE[2:0]* | 2021[4:2] | 0 | -- | R/W | The LCD bias mode.<br>000: 4 states, 1/3 bias<br>001: 3 states, 1/3 bias<br>010: 2 states, ½ bias<br>011: 3 states, ½ bias<br>100: static display |
| *LCD_NUM[4:0]* | 2020[4:0] | 0 | -- | R/W | Number of dual-purpose LCD/DIO pins to be configured as LCD. This will be a number between 0 and 18. The first dual-purpose pin to be allocated as LCD is SEG41/DIO21. Thus if *LCD_NUM*=2, SEG41 and SEG 40 will be configured as LCD. The remaining SEG39 to SEG24 will be configured as DIO19 to DIO4.<br>DIO1 and DIO2 (plus DIO3 on the QFN-68 package) are always available, if not used for the optical port.<br>See tables in Application Section. |
| *LCD_ONLY* | 20A9[5] | 0 | 0 | W | Takes the 6521FE/DE to LCD mode. Ignored if system power is present. The part will awaken when autowake timer times out, when push button is pushed, or when system power returns. |
| *LCD_SEG0[3:0]*<br>…<br>*LCD_SEG19[3:0]* | 2030[3:0]<br>…<br>2043[3:0] | 0<br>…<br>0 | --<br>…<br>-- | R/W | LCD Segment Data. Each word contains information for from 1 to 4 time divisions of each segment. In each word, bit 0 corresponds to COM0, on up to bit 3 for COM3. |
| *LCD_SEG24[3:0]*<br>…<br>*LCD_SEG38[3:0]* | 2048[3:0]<br>…<br>2056[3:0] | 0<br>…<br>0 | --<br>…<br>-- | R/W | **These bits are preserved in LCD and SLEEP modes, even if their pin is not configured as SEG. In this case, they can be useful as general-purpose non-volatile storage.** |
| *LCD_Y* | 2021[6] | 0 | 0 | R/W | LCD Blink Frequency (ignored if blink is disabled or if segment is off).<br>0: 1Hz (500ms ON, 500ms OFF)<br>1: 0.5Hz (1s ON, 1s OFF) |
| *MPU_DIV[2:0]* | 2004[2:0] | 0 | 0 | R/W | The MPU clock divider (from 4.9152MHz). These bits may be programmed by the MPU without risk of losing control.<br>000-4.9152MHz, 001-4.9152MHz $/2^1$, …, 111-4.9152MHz $/2^7$<br>*MPU_DIV* remains unchanged when the part enters BROWNOUT mode. |
| *MUX_ALT* | 2005[2] | 0 | 0 | R/W | The MPU asserts this bit when it wishes the MUX to perform ADC conversions on an alternate set of inputs. |

| | | | | | |
|---|---|---|---|---|---|
| *MUX_DIV[1:0]* | 2002[7:6] | 0 | 0 | R/W | The number of states in the input multiplexer.<br>00- illegal<br>01- 4 states 10-3 states 11-2 states |
| *OPT_FDC[1:0]* | 2007[1:0] | 0 | 0 | R/W | Selects OPT_TX modulation duty cycle<br>OPT_FDC / Function<br>00 / 50% Low<br>01 / 25% Low<br>10 / 12.5% Low<br>11 / 6.25% Low |
| *OPT_RXDIS* | 2008[5] | 0 | 0 | R/W | OPT_RX can be configured as an analog input to the optical UART comparator or as a digital input/output, DIO1.<br>0—OPT_RX, 1—DIO1. |
| *OPT_RXINV* | 2008[4] | 0 | 0 | R/W | Inverts result from OPT_RX comparator when 1. Affects only the UART input. Has no effect when OPT_RX is used as a DIO input. |
| *OPT_TXE[1,0]* | 2007[7,6] | 00 | 00 | R/W | Configures the OPT_TX output pin.<br>00—OPT_TX, 01—DIO2, 10—WPULSE, 11—VARPULSE |
| *OPT_TXINV* | 2008[0] | 0 | 0 | R/W | Invert OPT_TX when 1. This inversion occurs before modulation. |
| *OPT_TXMOD* | 2008[1] | 0 | 0 | R/W | Enables modulation of OPT_TX. When *OPT_TXMOD* is set, OPT_TX is modulated when it would otherwise have been zero. The modulation is applied after any inversion caused by *OPT_TXINV*. |
| *PLL_OK* | 2003[6] | 0 | 0 | R | Indicates that system power is present and the clock generation PLL is settled. |
| *PLS_MAXWIDTH [7:0]* | 2080[7:0] | FF | FF | R/W | Determines the maximum width of the pulse (low going pulse). Maximum pulse width is (2*PLS_MAXWIDTH + 1)*$T_I$. Where $T_I$ is PLS_INTERVAL. If PLS_INTERVAL=0, $T_I$ is the sample time (397µs). If 255, disable *MAXWIDTH*. |
| *PLS_INTERVAL [7:0]* | 2081[7:0] | 0 | 0 | R/W | If the FIFO is used, *PLS_INTERVAL must be set to 81.* If *PLS_INTERVAL* = 0, the FIFO is not used and pulses are output as soon as the CE issues them. |
| *PLS_INV* | 2004[6] | 0 | 0 | R/W | Inverts the polarity of WPULSE and VARPULSE. Normally, these pulses are active low. When inverted, they become active high. |
| *PREBOOT* | SFRB2[7] | -- | -- | R | Indicates that preboot sequence is active. |
| *PRE_SAMPS[1:0]* | 2001[7:6] | 0 | 0 | R/W | The duration of the pre-summer, in samples.<br>00-42, 01-50, 10-84, 11-100. |
| *RTC_SEC[5:0]*<br>*RTC_MIN[5:0]*<br>*RTC_HR[4:0]*<br>*RTC_DAY[2:0]*<br>*RTC_DATE[4:0]*<br>*RTC_MO[3:0]*<br>*RTC_YR[7:0]* | 2015<br>2016<br>2017<br>2018<br>2019<br>201A<br>201B | --<br>--<br>--<br>--<br>--<br>--<br>-- | --<br>--<br>--<br>--<br>--<br>--<br>-- | R/W<br>R/W<br>R/W<br>R/W<br>R/W<br>R/W<br>R/W | The RTC interface. These are the 'year', 'month', 'day', 'hour', 'minute' and 'second' parameters of the RTC. The RTC is set by writing to these registers. Year 00 and all others divisible by 4 are defined as leap years.<br>SEC 00 to 59<br>MIN 00 to 59<br>HR 00 to 23 (00=Midnight)<br>DAY 01 to 07 (01=Sunday)<br>DATE 01 to 31<br>MO 01 to 12<br>YR 00 to 99<br>Each write to one of these registers must be preceded by a write to 201F (WE). |

<table>
<tr><th></th><th></th><th></th><th></th><th></th><th></th></tr>
<tr><td>RTC_DEC_SEC<br>RTC_INC_SEC</td><td>201C[1]<br>201C[0]</td><td>0<br>0</td><td>0<br>0</td><td>W</td><td>RTC time correction bits. Only one bit may be pulsed at a time. When pulsed, causes the RTC time value to be incremented (or decremented) by an additional second the next time the RTC_SEC register is clocked. The pulse width may be any value. If an additional correction is desired, the MPU must wait 2 seconds before pulsing one of the bits again. Each write to one of these bits must be preceded by a write to 201F (WE).</td></tr>
<tr><td>RTM_E</td><td>2002[3]</td><td>0</td><td>0</td><td>R/W</td><td>Real Time Monitor enable. When ‘0’, the RTM output is low. This bit enables the two wire version of RTM</td></tr>
<tr><td>RTM0[7:0]<br>RTM1[7:0]<br>RTM2[7:0]<br>RTM3[7:0]</td><td>2060<br>2061<br>2062<br>2063</td><td>0<br>0<br>0<br>0</td><td>0<br>0<br>0<br>0</td><td>R/W</td><td>Four RTM probes. Before each CE code pass, the values of these registers are serially output on the RTM pin. The RTM registers are ignored when RTM_E=0.</td></tr>
<tr><td>SECURE</td><td>SFRB2[6]</td><td>0</td><td>--</td><td>R/W</td><td>Enables security provisions that prevent external reading of flash memory and CE program RAM. This bit is reset on chip reset and may only be set. Attempts to write zero are ignored.</td></tr>
<tr><td>SLEEP</td><td>20A9[6]</td><td>0</td><td>0</td><td>W</td><td>Takes the 6521DE/DH/FE to sleep mode. Ignored if system power is present. The part will wake when the autowake timer times out, when push button is pushed, or when system power returns.</td></tr>
<tr><td>SUM_CYCLES[5:0]</td><td>2001[5:0]</td><td>0</td><td>0</td><td>R/W</td><td>The number of pre-summer outputs summed in the final summer.</td></tr>
<tr><td>TMUX[4:0]</td><td>20AA[4:0]</td><td>2</td><td>--</td><td>R/W</td><td>Selects one of 32 signals for TMUXOUT.
<table>
<tr><th>[4:0]</th><th>Selected Signal</th><th>[4:0]</th><th>Selected Signal</th></tr>
<tr><td>0x00</td><td>DGND (analog)</td><td>0x01</td><td>Reserved</td></tr>
<tr><td>0x02</td><td>Reserved</td><td>0x03</td><td>Reserved</td></tr>
<tr><td>0x04</td><td>Reserved</td><td>0x05</td><td>Reserved</td></tr>
<tr><td>0x06</td><td>VBIAS (analog)</td><td>0x07</td><td>Not used</td></tr>
<tr><td>0x08</td><td>Reserved</td><td>0x09</td><td>Reserved</td></tr>
<tr><td>0x0A</td><td>Reserved</td><td>0x0B -0x13</td><td>Reserved</td></tr>
<tr><td>0x14</td><td>RTM (Real time output from CE)</td><td>0x15</td><td>WDTR_E, comparator 1 Output AND V1LT3)</td></tr>
<tr><td>0x16 – 0x17</td><td>Not used</td><td>0x18</td><td>RXD, from optical interface, after optional inversion</td></tr>
<tr><td>0x19</td><td>MUX_SYNC</td><td>0x1A</td><td>CK_10M</td></tr>
<tr><td>0x1B</td><td>CK_MPU</td><td>0x1C</td><td>Reserved</td></tr>
<tr><td>0x1D</td><td>RTCLK_2P5</td><td>0x1E</td><td>CE_BUSY</td></tr>
<tr><td>0x1F</td><td>XFER_BUSY</td><td></td><td></td></tr>
</table></td></tr>
<tr><td>TRIM[7:0]</td><td>20FF</td><td>0</td><td>0</td><td>R/W</td><td>Contains TRIMT[7:0], TRIMBGA,TRIMBGB or TRIMM[2:0] depending on the value written to TRIMSEL[3:0]. If TRIMBGB = 0, the device is a 71M6521DE/FE, else it is a 71M6521DH.</td></tr>
<tr><td>TRIMSEL[3:0]</td><td>20FD[3:0]</td><td>0</td><td>0</td><td>R/W</td><td>Selects the temperature trim fuse to be read with the TRIM register:
<table>
<tr><th>TRIMSEL[3:0]</th><th>Trim Fuse</th><th>Purpose</th></tr>
<tr><td>1</td><td>TRIMT[7:0]</td><td>Trim for the magnitude of VREF</td></tr>
<tr><td>4</td><td>TRIMM[2:0]</td><td rowspan="3">Trim values related to temperature compensation</td></tr>
<tr><td>5</td><td>TRIMBGA</td></tr>
<tr><td>6</td><td>TRIMBGB</td></tr>
</table></td></tr>
</table>

| | | | | | |
|---|---|---|---|---|---|
| *VERSION[7:0]* | 2006 | -- | -- | R | The version index. This word may be read by firmware to determine the silicon version.<br>VERSION[7:0] : Silicon Version<br>0000 0110 : A06 |
| *VREF_CAL* | 2004[7] | 0 | 0 | R/W | Brings VREF to VREF pad. This feature is disabled when *VREF_DIS*=1. |
| *VREF_DIS* | 2004[3] | 0 | 1 | R/W | Disables the internal voltage reference. |
| *WAKE_ARM* | 20A9[7] | 0 | -- | W | Arm the autowake timer. Writing a 1 to this bit arms the autowake timer and presets it with the values presently in *WAKE_PRD* and *WAKE_RES*. The autowake timer is reset and disarmed whenever the MPU is in MISSION mode or BROWNOUT mode. The timer must be armed at least three RTC cycles before the SLEEP or LCD-ONLY mode is commanded. |
| *WAKE_PRD* | 20A9[2:0] | 001 | -- | R/W | Sleep time. Time=*WAKE_PRD[2:0]***WAKE_RES*. Default=001. Maximum value is 7. |
| *WAKE_RES* | 20A9[3] | 0 | -- | R/W | Resolution of WAKE timer: 1 – 1 minute, 0 – 2.5 seconds. |

| | | | | | |
|---|---|---|---|---|---|
| *WD_RST* | SFRE8[7] | 0 | 0 | W | WD timer bit: Possible operations to this bit are:<br>Read: Gets the status of the flag IE_PLLFALL<br>Write 0: Clears the flag<br>Write 1:.Resets the WDT |
| *WD_OVF* | 2002[2] | 0 | 0 | R/W | The WD overflow status bit. This bit is set when the WD timer overflows. It is powered by the non-volatile supply and at bootup will indicate if the part is recovering from a WD overflow or a power fault. This bit should be cleared by the MPU on bootup. It is also automatically cleared when RESET is high. |
| *WE* | 201F7:0] | -- | -- | W | Write operations on the RTC registers must be preceded by a write operation to *WE*. |

# CE Interface Description

## CE Program

The CE program is supplied as a data image that can be merged with the MPU operational code for meter applications. Typically, the CE program covers most applications and does not need to be modified. For EQU = 0 and EQU = 1, CE code CE21A04_2 should be used. For EQU = 2, CE code image CE21A03_2 should be used. The description in this section applies to CE code revision CE21A03_2.

## Formats

All CE words are 4 bytes. Unless specified otherwise, they are in 32-bit two's complement (-1 = 0xFFFFFFFF). 'Calibration' parameters are defined in flash memory (or external EEPROM) and must be copied to CE data memory by the MPU before enabling the CE. 'Internal' variables are used in internal CE calculations. 'Input' variables allow the MPU to control the behavior of the CE code. 'Output' variables are outputs of the CE calculations. The corresponding MPU address for the most significant byte is given by 0x1000 + 4 x CE_address and 0x1003 + 4 x CE_address for the least significant byte.

## Constants

Constants used in the CE Data Memory tables are:

- $F_S$ = 32768Hz/13 = 2520.62Hz.
- $F_0$ is the fundamental frequency.
- *IMAX* is the external rms current corresponding to 250mV pk at the inputs IA and IB.
- *VMAX* is the external rms voltage corresponding to 250mV pk at the VA and VB inputs.
- $N_{ACC}$, the accumulation count for energy measurements is *PRE_SAMPS*SUM_CYCLES*.
- Accumulation count time for energy measurements is *PRE_SAMPS*SUM_CYCLES*/$F_S$.

The system constants *IMAX* and *VMAX* are used by the MPU to convert internal quantities (as used by the CE) to external, i.e. metering quantities. Their values are determined by the off-chip scaling of the voltage and current sensors used in an actual meter. The LSB values used in this document relate digital quantities at the CE or MPU interface to external meter input quantities. For example, if a SAG threshold of 80V peak is desired at the meter input, the digital value that should be programmed into *SAG_THR* would be 80V/*SAG_THR*LSB, where *SAG_THR*LSB is the LSB value in the description of *SAG_THR*.

The parameters *EQU*, *CE_E*, *PRE_SAMPS,* and *SUM_CYCLES* essential to the function of the CE are stored in I/O RAM (see I/O RAM section).

## Environment

Before starting the CE using the *CE_E* bit, the MPU has to establish the proper environment for the CE by implementing the following steps:

- Load the CE data into CE DRAM.
- Establish the equation to be applied in EQU.
- Establish the accumulation period and number of samples in *PRE_SAMPS* and *SUM_CYCLES*.
- Establish the number of cycles per ADC mux frame.
- Set *PLS_INTERVAL*[7:0] to 81.
- Set *FIR_LEN* to 1 and *MUX_DIV* to 1.

There must be thirteen 32768Hz cycles per ADC mux frame (see System Timing Diagram, Figure 16). This means that the product of the number of cycles per frame and the number of conversions per frame must be 12 (allowing for one settling cycle). The required configuration is *FIR_LEN* = 1 (three cycles per conversion) and *MUX_DIV* = 1 (4 conversions per mux frame).

During operation, the MPU is in charge of controlling the multiplexer cycles, for example by inserting an alternate multiplexer sequence at regular intervals using *MUX_ALT*. This enables temperature measurement. The polarity of chopping circuitry must be altered for each sample. It must also alternate for each alternate multiplexer reading. This is accomplished by maintaining *CHOP_E* = 00.

## CE Calculations

The CE performs the precision computations necessary to accurately measure energy. These computations include offset cancellation, products, product smoothing, product summation, frequency detection, VAR calculation, sag detection, peak detection, and voltage phase measurement. All data computed by the CE is dependent on the selected meter equation as given by *EQU* (in I/O RAM). Although *EQU*=0 and *EQU*=2 have the same element mapping, the MPU code can use the value of *EQU* to decide if element 2 is used for tamper detection (typically done by connecting VB to VA) or as a second independent element.

| ***EQU*** | **Watt & VAR Formula** (WSUM/VARSUM) | **Element Input Mapping** | | | |
|---|---|---|---|---|---|
| | | *W0SUM/ VAR0SUM* | *W1SUM/ VAR1SUM* | *I0SQSUM* | *I1SQSUM* |
| 0 | VA IA (1 element, 2W 1ϕ) with tamper detection | VA*IA | VA*IB | IA | IB |
| 1 | VA*(IA-IB)/2 (1 element, 3W 1ϕ) | VA*(IA-IB)/2 | VA*IB/2 | IA-IB | IB |
| 2 | VA*IA + VB*IB (2 element, 4W 2ϕ) | VA*IA | VB*IB | IA | IB |

## CE STATUS

Since the CE_BUSY interrupt occurs at 2520.6Hz, it is desirable to minimize the computation required in the interrupt handler of the MPU. The MPU can read the CE status word at every CE_BUSY interrupt.

| **CE Address** | **Name** | **Description** |
|---|---|---|
| 0x7A | *CESTATUS* | See description of CE status word below |

The CE Status Word is used for generating early warnings to the MPU. It contains sag warnings for VA as well as F0, the derived clock operating at the fundamental input frequency. *CESTATUS* provides information about the status of voltage and input AC signal frequency, which are useful for generating early power fail warnings, e.g. to initiate necessary data storage. *CESTATUS* represents the status flags for the preceding CE code pass (CE busy interrupt). Sag alarms are not remembered from one code pass to the next. The CE Status word is refreshed at every CE_BUSY interrupt.

The significance of the bits in *CESTATUS* is shown in the table below:

| ***CESTATUS* [bit]** | **Name** | **Description** |
|---|---|---|
| 31-29 | Not Used | These unused bits will always be zero. |
| 28 | *F0* | *F0* is a square wave at the exact fundamental input frequency. |
| 27 | *RESERVED* | |
| 26 | *SAG_B* | Normally zero. Becomes one when VB remains below *SAG_THR* for *SAG_CNT* samples. Will not return to zero until VB rises above *SAG_THR*. |
| 25 | *SAG_A* | Normally zero. Becomes one when VA remains below *SAG_THR* for *SAG_CNT* samples. Will not return to zero until VA rises above *SAG_THR*. |
| 24-0 | Not Used | These unused bits will always be zero. |

The CE is initialized by the MPU using *CECONFIG* (*CESTATE*.). This register contains in packed form *SAG_CNT*, *FREQSEL*, *EXT_PULSE*, *I0_SHUNT*, *I1_SHUNT*, *PULSE_SLOW*, and *PULSE_FAST*.

| **CE Address** | **Name** | **Default** | **Description** |
|---|---|---|---|
| 0x10 | *CECONFIG* | 0x5020 | See description of *CECONFIG* below |

The significance of the bits in *CECONFIG* is shown in the table below:

*IA_SHUNT* and/or *IB_SHUNT* can configure their respective current inputs to accept shunt resistor sensors. In this case the CE provides an additional gain of 8 to the selected current input. *WRATE* may need to be adjusted based on the values of IA*_SHUNT* and IB*_SHUNT*. Whenever *IA_SHUNT* or *IB_SHUNT* are set to 1, *In_8* (in the equation for Kh) is assigned a value of 8.

The CE pulse generator can be controlled by either the MPU (external) or CE (internal) variables. Control is by the MPU if *EXT_PULSE* = 1. In this case, the MPU controls the pulse rate by placing values into *APULSEW* and *APULSER*. By setting *EXT_PULSE* = 0, the CE controls the pulse rate based on W0SUM_X + W1SUM_X (and VAR0SUM_X + *VAR1SUM_X*).

If *EXT_PULSE* is 1, and if *EQU* = 2, the pulse inputs are *W0SUM_X+W1SUM_X* and *VAR0SUM_X+VAR1SUM_X* . In this case, creep cannot be controlled since creep is an MPU function. If *EXT_PULSE = 1* and *EQU* = 0, the pulse inputs are *W0SUM_X* if *I0SQSUM_X* > *I1SQSUM_X*, and *W1SUM_X*, if *I1SQSUM_X* > *I0SQSUM_X*.

Note: The 6521 Demo Code creep function halts both internal and external pulse generation.

<table>
<tr><th>CECONFIG [bit]</th><th>Name</th><th>Default</th><th>Description</th></tr>
<tr><td>[15:8]</td><td>SAG_CNT</td><td>80 (0x50)</td><td>Number of consecutive voltage samples below SAG_THR before a sag alarm is declared. The maximum value is 255. SAG_THR is at address 0x14.</td></tr>
<tr><td>[7]</td><td>--</td><td>0</td><td>Unused</td></tr>
<tr><td>[6]</td><td>FREQSEL</td><td>0</td><td>Selected phase for frequency monitor (0 = A, 1 = B).</td></tr>
<tr><td>[5]</td><td>EXT_PULSE</td><td>1</td><td>When zero, causes the pulse generators to respond to WSUM_X and VARSUM_X. Otherwise, the generators respond to values the MPU places in APULSEW and APULSER.</td></tr>
<tr><td>[4]</td><td>--</td><td>0</td><td>Unused</td></tr>
<tr><td>[3]</td><td>IB_SHUNT</td><td>0</td><td>When 1, the current gain of channel B is increased by 8. The gain factor controlled by In_SHUNT is referred to as In_8 throughout this document.</td></tr>
<tr><td>[2]</td><td>IA_SHUNT</td><td>0</td><td>When 1, the current gain of channel A is increased by 8.</td></tr>
<tr><td>[1]</td><td>PULSE_FAST</td><td>0</td><td rowspan="2">When PULSE_SLOW = 1, the pulse generator input is reduced by a factor of 64. When PULSE_FAST = 1, the pulse generator input is increased 16x. These two parameters control the pulse gain factor X (see table below). Allowed values are either 1 or 0. Default is 0 (X = 6).<br>
<table>
<tr><th>X</th><th>PULSE_SLOW</th><th>PULSE_FAST</th></tr>
<tr><td>$1.5 * 2^{2} = 6$</td><td>0</td><td>0</td></tr>
<tr><td>$1.5 * 2^{6} = 96$</td><td>0</td><td>1</td></tr>
<tr><td>$1.5 * 2^{-4} = 0.09375$</td><td>1</td><td>0</td></tr>
<tr><td>1.5</td><td>1</td><td>1</td></tr>
</table></td></tr>
<tr><td>[0]</td><td>PULSE_SLOW</td><td>0</td></tr>
</table>

## CE TRANSFER VARIABLES

When the MPU receives the XFER_BUSY interrupt, it knows that fresh data is available in the transfer variables. The transfer variables can be categorized as:

1. Fundamental energy measurement variables
2. Instantaneous (RMS) values
3. Other measurement parameters
4. Pulse generation variables
5. Current shunt variables
6. Calibration parameters

### Fundamental Energy Measurement Variables

The table below describes each transfer variable for fundamental energy measurement. All variables are signed 32 bit integers. Accumulated variables such as WSUM are internally scaled so they have at least 2x margin before overflow when the integration time is 1 second. Additionally, the hardware will not permit output values to 'fold back' upon overflow.

| CE Address | Name | Description |
|---|---|---|
| 0x76 | *W0SUM_X* | The sum of Watt samples from each wattmeter element (*In_8* is the gain configured by *IA_SHUNT* or *IB_SHUNT*). LSB = 6.6952*$10^{-13}$ *VMAX IMAX / In_8* Wh. |
| 0x72 | *W1SUM_X* | |
| 0x75 | *VAR0SUM_X* | The sum of VAR samples from each wattmeter element (*In_8* is the gain configured by *IA_SHUNT* or *IB_SHUNT*). LSB = 6.6952*$10^{-13}$ *VMAX IMAX / In_8* Wh. |
| 0x71 | *VAR1SUM_X* | |

*WxSUM_X* is the Wh value accumulated for element 'X' in the last accumulation interval and can be computed based on the specified LSB value.

For example with *VMAX* = 600V and *IMAX* = 208A, LSB (for *WxSUM_X* ) is 0.08356 µWh.

### Instantaneous Energy Measurement Variables

The Frequency measurement is computed using the Frequency locked loop for the selected phase.

*IxSQSUM_X* and *VxSQSUM* are the squared current and voltage samples acquired during the last accumulation interval. *INSQSUM_X* can be used for computing the neutral current.

| CE Address | Name | Description |
|---|---|---|
| 0x79 | *FREQ_X* | Fundamental frequency. LSB $\equiv \frac{F_S}{2^{32}} \approx 0.587 \cdot 10^{-6}$ *Hz* |
| 0x77 | *I0SQSUM_X* | The sum of squared current samples from each element. LSB = 6.6952*$10^{-13}$ $IMAX^2 / In\_8^2$ $A^2h$ |
| 0x73 | *I1SQSUM_X* | |
| 0x78 | *V0SQSUM_X* | The sum of squared voltage samples from each element. LSB= 6.6952*$10^{-13}$ $VMAX^2$ $V^2h$ |
| 0x74 | *V1SQSUM_X* | |
| 0x7D | *WSUM_ACCUM* | These are roll-over accumulators for WPULSE and VPULSE respectively. |
| 0x7E | *VSUM_ACCUM* | |

The RMS values can be computed by the MPU from the squared current and voltage samples as follows:

$$Ix_{RMS} = \sqrt{\frac{IxSQSUM \cdot LSB \cdot 3600 \cdot F_S}{N_{ACC}}} \qquad Vx_{RMS} = \sqrt{\frac{VxSQSUM \cdot LSB \cdot 3600 \cdot F_S}{N_{ACC}}}$$

### Other Measurement Parameters

*MAINEDGE_X* is useful for implementing a real-time clock based on the input AC signal. *MAINEDGE_X* is the number of half-cycles accounted for in the last accumulated interval for the AC signal.

*TEMP_RAW* may be used by the MPU to monitor chip temperature or to implement temperature compensation.

| CE Address | Name | Default | Description |
|---|---|---|---|
| 0x7C | *MAINEDGE_X* | N/A | The number of zero crossings of the selected voltage in the previous accumulation interval. Zero crossings are either direction and are debounced. |
| 0x7B | *TEMP_RAW_X* | N/A | Filtered, unscaled reading from the temperature sensor. |
| 0x12 | *GAIN_ADJ* | 16384 | Scales all voltage and current inputs. 16384 provides unity gain. |
| 0x14 | *SAG_THR* | 443000 | The threshold for sag warnings. The default value is equivalent to 80V RMS if VMAX = 600V. The LSB value is VMAX * $4.255 \cdot 10^{-7}$V (peak). |

*GAIN_ADJ* is a scaling factor for measurements based on the temperature. *GAIN_ADJ* is controlled by the MPU for temperature compensation.

**Pulse Generation**

| CE Address | Name | Default | Description |
|---|---|---|---|
| 0x11 | *WRATE* | 122 | Kh = *VMAX***IMAX**47.1132 / (*In_8***WRATE**$N_{ACC}$*X) Wh/pulse. The default value results in a Kh of 3.2Wh/pulse when 2520 samples are taken in each accumulation interval (and VMAX=600, IMAX = 208, In_8 = 1, X = 6). The maximum value for *WRATE* is $2^{15} – 1$. |
| 0x0E | *APULSEW* | 0 | Watt pulse generator input (see *DIO_PW* bit). The output pulse rate is: *APULSEW* * $F_S$ * $2^{-32}$ * *WRATE* * *X* * $2^{-14}$. This input is buffered and can be loaded during a computation interval. The change will take effect at the beginning of the next interval. |
| 0x0F | *APULSER* | 0 | VAR pulse generator input (see *DIO_PV* bit). The output pulse rate is: *APULSER* * $F_S$*$2^{-32}$ * *WRATE* * *X* * $2^{-14}$. This input is buffered and can be loaded during a computation interval. The change will take effect at the beginning of the next interval. |

*WRATE* controls the number of pulses that are generated per measured Wh and VARh quantities. The lower *WRATE* is the slower the pulse rate for measured energy quantity. The metering constant Kh is derived from *WRATE* as the amount of energy measured for each pulse. That is, if Kh = 1Wh/pulse, a power applied to the meter of 120V and 30A results in one pulse per second. If the load is 240V at 150A, ten pulses per second will be generated.

The maximum pulse rate is 7.5kHz.

The maximum time jitter is 67µs and is independent of the number of pulses measured. Thus, if the pulse generator is monitored for 1 second, the peak jitter is 67ppm. After 10 seconds, the peak jitter is 6.7ppm.

The average jitter is always zero. If it is attempted to drive either pulse generator faster than its maximum rate, it will simply output at its maximum rate without exhibiting any rollover characteristics. The actual pulse rate, using *WSUM* as an example, is:

$$RATE = \frac{WRATE \cdot WSUM \cdot F_S \cdot X}{2^{46}} Hz,$$

where $F_S$ = sampling frequency (2520.6Hz), X = Pulse speed factor

**CE Calibration Parameters**

The table below lists the parameters that are typically entered to effect calibration of meter accuracy.

| CE Address | Name | Default | Description |
|---|---|---|---|
| 0x08 | *CAL_IA* | 16384 | These constants control the gain of their respective channels. The nominal value for each parameters is $2^{14}$ = 16384. The gain of each channel is directly proportional to its CAL parameter. Thus, if the gain of a channel is 1% slow, CAL should be scaled by 1/(1 – 0.01). |
| 0x09 | *CAL_VA* | 16384 | |
| 0x0A | *CAL_IB* | 16384 | |
| 0x0B | *CAL_VB* | 16384 | |
| 0x0C | *PHADJ_A* | 0 | These two constants control the CT phase compensation. No compensation occurs when *PHADJ_X* = 0. As *PHADJ_X* is increased, more compensation (lag) is introduced. Range: $\pm 2^{15} - 1$. If it is desired to delay the current by the angle $\Phi$:<br>$PHADJ\_X = 2^{20} \frac{0.02229 \cdot TAN\Phi}{0.1487 - 0.0131 \cdot TAN\Phi}$ at 60Hz<br>$PHADJ\_X = 2^{20} \frac{0.0155 \cdot TAN\Phi}{0.1241 - 0.009695 \cdot TAN\Phi}$ at 50Hz |
| 0x0D | *PHADJ_B* | 0 | |

**Other CE Parameters**

The table below shows CE parameters used for suppression of noise due to scaling and truncation effects.

| CE Address | Name | Default | Description |
|---|---|---|---|
| 0x13 | *QUANTA* | 0 | This parameter is added to the Watt calculation for element 0 to compensate for input noise and truncation.<br>LSB = (*VMAX***IMAX / In_8*) *7.4162*$10^{-10}$ W |
| 0x18 | *QUANTB* | 0 | This parameter is added to the Watt calculation for element 1 to compensate for input noise and truncation. Same LSB as *QUANTA*. |
| 0x15 | *QUANT_VARA* | 0 | This parameter is added to the VAR calculation for element A to compensate for input noise and truncation.<br>LSB = (*VMAX***IMAX / In_8*) * 7.4162*$10^{-10}$ W |
| 0x1B | *QUANT_VARB* | 0 | This parameter is added to the VAR calculation for element B to compensate for input noise and truncation. Same LSB as for *QUANT_VARA*. |
| 0x16 | *QUANT_I* | 0 | This parameter is added to compensate for input noise and truncation in the squaring calculations for $I^2$. *QUANT_I* affects only *I0SQSUM* and *I1SQSUM*.<br>LSB = ($IMAX^2/In\_8^2$)*7.4162*$10^{-10}$ $A^2$ |

# ELECTRICAL SPECIFICATIONS

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| **Supplies and Ground Pins:** | |
| V3P3SYS, V3P3A | –0.5 V to 4.6 V |
| VBAT | -0.5 V to 4.6 V |
| GNDD | -0.5 V to +0.5 V |
| **Analog Output Pins:** | |
| V3P3D | -10 mA to 10 mA,<br>-0.5 V to 4.6 V |
| VREF | -10 mA to +10 mA,<br>-0.5 V to V3P3A+0.5 V |
| V2P5 | -10 mA to +10 mA,<br>-0.5 V to 3.0V |
| **Analog Input Pins:** | |
| IA, VA, IB, VB, V1 | -10 mA to +10 mA<br>-0.5 V to V3P3A+0.5 V |
| XIN, XOUT | -10 mA to +10 mA<br>-0.5 V to 3.0V |
| **All Other Pins:** | |
| Configured as SEG or COM drivers | -1 mA1 mA to +1 mA1 mA,<br>-0.5 to V3P3D+0.5 |
| Configured as Digital Inputs | -10 mA to +10 mA,<br>-0.5 to 6 V |
| Configured as Digital Outputs | -15 mA to +15 mA,<br>-0.5 V to V3P3D+0.5 V |
| All other pins | –0.5 V to V3P3D+0.5 V |
| | |
| Operating junction temperature (peak, 100ms) | 140 °C |
| Operating junction temperature (continuous) | 125 °C |
| Storage temperature | –45 °C to +165 °C |
| Solder temperature – 10 second duration | 250 °C |
| ESD stress on all pins | ±4 kV |

Stresses beyond Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to GNDA.

## RECOMMENDED EXTERNAL COMPONENTS

| NAME | FROM | TO | FUNCTION | VALUE | UNIT |
|---|---|---|---|---|---|
| C1 | **V3P3A** | **AGND** | Bypass capacitor for 3.3 V supply | ≥0.1±20% | µF |
| C2 | **V3P3D** | **DGND** | Bypass capacitor for 3.3 V output | 0.1±20% | µF |
| CSYS | **V3P3SYS** | **DGND** | Bypass capacitor for V3P3SYS | ≥1.0±30% | µF |
| C2P5 | **V2P5** | **DGND** | Bypass capacitor for V2P5 | 0.1±20% | µF |
| XTAL | **XIN** | **XOUT** | 32.768 kHz crystal – electrically similar to ECS .327-12.5-17X or Vishay XT26T, load capacitance 12.5 pF | 32.768 | kHz |
| CXS † | **XIN** | **AGND** | Load capacitor for crystal (exact value depends on crystal specifications and parasitic capacitance of board). | 27±10% | pF |
| CXL † | **XOUT** | **AGND** | | 27±10% | pF |

† Depending on trace capacitance, higher or lower values for CXS and CXL must be used. Capacitance from XIN to GNDD and XOUT to GNDD (combining pin, trace and crystal capacitance) should be 35pF to 37pF.

## RECOMMENDED OPERATING CONDITIONS

| PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| 3.3V Supply Voltage (**V3P3SYS, V3P3A**) V3P3A and V3P3SYS must be at the same voltage | Normal Operation | 3.0 | 3.3 | 3.6 | V |
| | Battery Backup | 0 | | 3.6 | V |
| **VBAT** | No Battery | Externally Connect to V3P3SYS | | | |
| | Battery Backup<br>BRN and LCD modes<br>SLEEP mode | <br>3.0<br>2.0 | | <br>3.8<br>3.8 | <br>V<br>V |
| **Operating Temperature** | | -40 | | +85 | ºC |
| Maximum input voltage on DIO/SEG pins configured as DIO input. * | MISSION mode<br>BROWNOUT mode<br>LCD mode | | | V3P3SYS+0.3<br>VBAT+0.3<br>VBAT+0.3 | V<br>V<br>V |

*Exceeding this limit will distort the LCD waveforms on other pins.

# PERFORMANCE SPECIFICATIONS

### INPUT LOGIC LEVELS

| PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Digital high-level input voltage†, $V_{IH}$ | | 2 | | | V |
| Digital low-level input voltage†, $V_{IL}$ | | | | 0.8 | V |
| Input pull-up current, $I_{IL}$<br>E_RXTX,<br>E_RST, CKTEST<br>Other digital inputs | VIN=0 V, ICE_E=1 | <br>10<br>10<br>-1 | <br><br><br>0 | <br>100<br>100<br>1 | <br>µA<br>µA<br>µA |
| Input pull down current, $I_{IH}$<br>ICE_E<br>PB<br>Other digital inputs | VIN=V3P3D | <br>10<br>-1<br>-1 | <br><br>0<br>0 | <br>100<br>1<br>1 | <br>µA<br>µA<br>µA |

†In battery powered modes, digital inputs should be below 0.3V or above 2.5 V to minimize battery current.

### OUTPUT LOGIC LEVELS

| PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Digital high-level output voltage $V_{OH}$ | $I_{LOAD}$ = 1 mA | V3P3D –0.4 | | | V |
| | $I_{LOAD}$ = 15 mA | V3P3D-0.6[1] | | | V |
| Digital low-level output voltage $V_{OL}$ | $I_{LOAD}$ = 1 mA | 0 | | 0.4 | V |
| | $I_{LOAD}$ = 15 mA | | | 0.8[1] | V |
| **OPT_TX** $V_{OH}$ (**V3P3D**-**OPT_TX**) | $I_{SOURCE}$=1 mA | | | 0.4 | V |
| **OPT_TX** $V_{OL}$ | $I_{SINK}$=20 mA | | | 0.7[1] | V |

[1]Guaranteed by design; not production tested.

### POWER-FAULT COMPARATOR

| PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Offset Voltage<br>**V1-VBIAS** | | -20 | | +15 | mV |
| Hysteresis Current<br>**V1** | Vin = VBIAS – 100 mV | 0.8 | | 1.2 | µA |
| Response Time<br>**V1** | +100 mV overdrive<br>-100 mV overdrive | 2<br>10 | 5 | 10<br>100 | µs<br>µs |
| WDT Disable Threshold (**V1**-**V3P3A**) | | -400 | | -10 | mV |

### BATTERY MONITOR

*BME=1*

| PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Load Resistor | | 27 | 45 | 63 | kΩ |
| LSB Value - does not include the 9-bit left shift at CE input. | *FIR_LEN*=0<br>*FIR_LEN*=1 | -6.0<br>-2.6 | -5.4<br>-2.3 | -4.9<br>-2.0 | µV<br>µV |
| Offset Error | | -200 | -72 | +100 | mV |

**SUPPLY CURRENT**

| PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **V3P3A** + **V3P3SYS** current | Normal Operation,<br>**V3P3A=V3P3SYS**=3.3 V<br>MPU_DIV=3 (614kHz) CKOUT_E=00,<br>CE_EN=1,<br>RTM_E=0,<br>ECK_DIS=1,<br>ADC_E=1,<br>ICE_E=0 | | 6.1 | 7.7 | mA |
| **VBAT** current | | -300 | | +300 | nA |
| **V3P3A + V3P3SYS** current vs. MPU clock frequency | Same conditions as above | | 0.5 | | mA/ MHz |
| **V3P3A + V3P3SYS** current, write flash | Normal Operation as above, except write flash at maximum rate, CE_E=0, ADC_E=0 | | 9.1 | 10 | mA |
| **VBAT current** † | VBAT=3.6 V<br>BROWNOUT mode, <25°C<br>BROWNOUT mode, >25°C<br><br>LCD Mode, 25°C<br>LCD mode, over temperature<br>SLEEP Mode, 25°C<br>Sleep mode, over temperature | | <br>48<br>65[1]<br><br>5.7<br><br>2.9<br> | <br>120<br>150[1]<br><br>8.5<br>15[1]<br>5.0<br>10[1] | <br>µA<br>µA<br><br>µA<br>µA<br>µA<br>µA |

†Current into V3P3A and V3P3SYS pins is not zero if voltage is applied at these pins in brownout, LCD or sleep modes.

[1]Guaranteed by design; not production tested.

**V3P3D SWITCH**

| PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| On resistance – V3P3SYS to V3P3D | $\| I_{V3P3D} \| \le 1$ mA | | | 10 | Ω |
| On resistance – VBAT to V3P3D | $\| I_{V3P3D} \| \le 1$ mA | | | 40 | Ω |

**2.5 V VOLTAGE REGULATOR**

Unless otherwise specified, load = 5 mA

| PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Voltage overhead **V3P3-V2P5** | Reduce V3P3 until V2P5 drops 200mV | | | 440 | mV |
| PSSR **ΔV2P5/ΔV3P3** | RESET=0, iload=0 | -3 | | +3 | mV/V |

**LOW POWER VOLTAGE REGULATOR**

Unless otherwise specified, V3P3SYS=V3P3A=0, PB=GND (BROWNOUT)

| PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **V2P5** | ILOAD=0 | 2.0 | 2.5 | 2.7 | V |
| **V2P5** load regulation | ILOAD=0 mA to 1 mA1 mA | | | 30 | mV |
| VBAT voltage requirement | ILOAD=1 mA,<br>Reduce VBAT until REG_LP_OK=0 | | | 3.0 | V |
| PSRR **ΔV2P5**/**ΔVBAT** | ILOAD=0 | -50 | | 50 | mV/V |

### CRYSTAL OSCILLATOR

| PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Maximum Output Power to Crystal | Crystal connected | | | 1 | µW |
| XIN to XOUT Capacitance | | | 3 | | pF |
| Capacitance to DGND<br>XIN<br>XOUT | | | <br>5<br>5 | | <br>pF<br>pF |

### VREF, VBIAS

Unless otherwise specified, *VREF_DIS*=0

| PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **VREF** output voltage, VNOM(25) | Ta = 22ºC | 1.193 | 1.195 | 1.197 | V |
| **VREF** chop step | | | | 50 | mV |
| **VREF** output impedance | *VREF_CAL* =1,<br>ILOAD = 10 µA, -10 µA | | | 2.5 | kΩ |
| **VNOM** definition[2] | $VNOM(T) = VREF(22) + (T-22)TC1 + (T-22)^2 TC2$ | | | | V |
| -- If TRIMBGA and TRIMBGB not available -- | | | | | |
| **VREF** temperature coefficients<br>TC1<br>TC2 | | <br>+7.0<br>-0.341 | | | <br>µV/ºC<br>µV/°C[2] |
| **VREF(T)** deviation from VNOM(T)<br>$\frac{VREF(T)-VNOM(T)}{VNOM(T)} \frac{10^6}{\max(\lvert T-22\rvert,40)}$ | Ta = -40ºC to +85ºC | -40[1] | | +40[1] | ppm/ºC |
| -- If TRIMBGA and TRIMBGB are available (71M6521DH) -- | | | | | |
| Define the following variables:<br>$TEMP_{22,1} \equiv TEMP\_RAW\_X/2^{10}$ --*where TEMP_RAW_X is measured with FIRLEN=1*<br>$TEMP_{22,0} = \frac{TEMP_{22,1}}{2.3704}$ --*this calculates the value of TEMP22 if measured with FIRLEN=0*<br>$\gamma = 0.1 \cdot TRIMBGB - 0.143 \cdot (TRIMM + 0.5)$<br>$\xi = \frac{TEMP_{22,0} - (500 \cdot TRIMBGA + 370000)}{900}$<br>$\eta = (56.2 - TRIMT) \cdot 0.55$ | | | | | |
| VNOM temperature coefficients (Δ*v* and ΔT are defined in the section entitled “Voltage Reference”)<br>TC1<br>TC2 | $\eta + 19\gamma - 0.065\gamma\xi + 0.34\xi + 8.0$<br>$0.015\gamma - 0.0013\xi - 0.35$ | | | | <br>µV/ºC<br>µV/ºC[2] |
| **VREF(T)** deviation from VNOM(T)<br>$\frac{VREF(T)-VNOM(T)}{VNOM(T)} \frac{10^6}{\max(\lvert T-22\rvert,40)}$ | Ta = -40ºC to +85ºC | -20[1] | | +20[1] | ppm/ºC |
| **VREF** aging | | | ±25 | | ppm/ year |
| **VBIAS** voltage | Ta = 25ºC<br>Ta = -40ºC to 85ºC | (-1%)<br>(-4%)[1] | 1.6<br>1.6[1] | (+1%)<br>(+4%)[1] | V<br>V |

[1]Guaranteed by design; not production tested.

[2] This relationship describes the nominal behavior of VREF at different temperatures.

**LCD DRIVERS**

Applies to all COM and SEG pins.

| PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| VLC2 Max Voltage | With respect to VLCD | -0.1 | | +0.1 | V |
| VLC1 Voltage,<br>1/3 bias<br>½ bias | <br>With respect to 2*VLC2/3<br>With respect to VLC2/2 | <br>-4<br>-3 | | <br>0<br>+2 | <br>%<br>% |
| VLC0 Voltage,<br>1/3 bias<br>½ bias | <br>With respect to VLC2/3<br>With respect to VLC2/2 | <br>-3<br>-3 | | <br>+2<br>+2 | <br>%<br>% |

VLCD is V3P3SYS in MISSION mode and VBAT in BROWNOUT and LCD modes.

**ADC CONVERTER, V3P3A REFERENCED**

*FIR_LEN*=0, *VREF_DIS*=0, LSB values do not include the 9-bit left shift at CE input.

| PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Recommended Input Range<br>(Vin-**V3P3A**) | | -250 | | 250 | mV peak |
| Voltage to Current Crosstalk:<br>$\frac{10^6 * Vcrosstalk}{Vin}\cos(\angle Vin - \angle Vcrosstalk)$ | *Vin* = 200 mV peak, 65 Hz, on VA<br><br>*Vcrosstalk* = largest measurement on IA or IB | -10[1] | | 10[1] | μV/V |
| THD (First 10 harmonics)<br>250mV-pk<br>20mV-pk | Vin=65 Hz,<br>64 kpts FFT, Blackman-Harris window | | <br>-75<br>-90 | | <br>dB<br>dB |
| Input Impedance | Vin=65 Hz | 40 | | 90 | kΩ |
| Temperature coefficient of Input Impedance | Vin=65 Hz | | 1.7 | | Ω/°C |
| LSB size | *FIR_LEN*=0<br>*FIR_LEN*=1 | | 357<br>151 | | nV/LSB |
| Digital Full Scale | *FIR_LEN*=0<br>*FIR_LEN*=1 | | ±884736<br>±2097152 | | LSB |
| ADC Gain Error vs<br>%Power Supply Variation<br>$\frac{10^6 \Delta Nout_{PK} 357nV / V_{IN}}{100 \Delta V3P3A / 3.3}$ | Vin=200 mV pk, 65 Hz<br>V3P3A=3.0 V, 3.6 V | | | 50 | ppm/% |
| Input Offset (Vin-**V3P3A**) | | -10 | | 10 | mV |

[1]Guaranteed by design; not production tested.

**TEMPERATURE SENSOR**

| PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Nominal Sensitivity ($S_n$) † | $T_A$=25ºC, $T_A$=75ºC, *FIR_LEN* = 1 Nominal relationship: $N(T)= S_n*(T-T_n)+N_n$ | | -2180 | | LSB/ºC |
| Nominal ($N_n$) †† | | | 1.0 | | $10^6$ LSB |
| Temperature Error† $ERR = T - \left( \frac{(N(T) - N_n)}{S_n} + T_n \right)$ | $T_A$ = -40ºC to +85ºC Tn = 25°C | -10[1] | | +10[1] | ºC |

[1]Guaranteed by design; not production tested.

† LSB values do not include the 9-bit left shift at CE input.

†† $N_n$ is measured at $T_n$ during meter calibration and is stored in MPU or CE for use in temperature calculations.

# TIMING SPECIFICATIONS

## RAM AND FLASH MEMORY

| PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| CE DRAM wait states | CKMPU = 4.9 MHz | 5 | | | Cycles |
| | CKMPU = 1.25 MHz | 2 | | | Cycles |
| | CKMPU = 614 kHz | 1 | | | Cycles |
| Flash Read Pulse Width | V3P3A=V3P3SYS=0 BROWNOUT MODE | 30 | | 100 | ns |
| Flash write cycles | -40°C to +85°C | 20,000 | | | Cycles |
| Flash data retention | 25°C | 100 | | | Years |
| Flash data retention | 85°C | 10 | | | Years |
| Flash byte writes between page or mass erase operations | | | | 2 | Cycles |

## FLASH MEMORY TIMING

| PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Write Time per Byte | | | | 42 | µs |
| Page Erase (512 bytes) | | | | 20 | ms |
| Mass Erase | | | | 200 | ms |

## EEPROM INTERFACE

| PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Write Clock frequency ($I^2C$) | CKMPU=4.9 MHz, Using interrupts | | 78 | | kHz |
| | CKMPU=4.9 MHz, “bit-banging” DIO4/5 | | 150 | | kHz |
| Write Clock frequency (3-wire) | CKMPU=4.9 MHz | | 500 | | kHz |

## RESET and V1

| PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Reset pulse fall time | | | | 1[1] | µs |
| Reset pulse width | | 5 | | | µs |

[1]Guaranteed by design; not production tested.

## RTC

| PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Range for date | | 2000 | - | 2255 | year |

## TYPICAL PERFORMANCE DATA

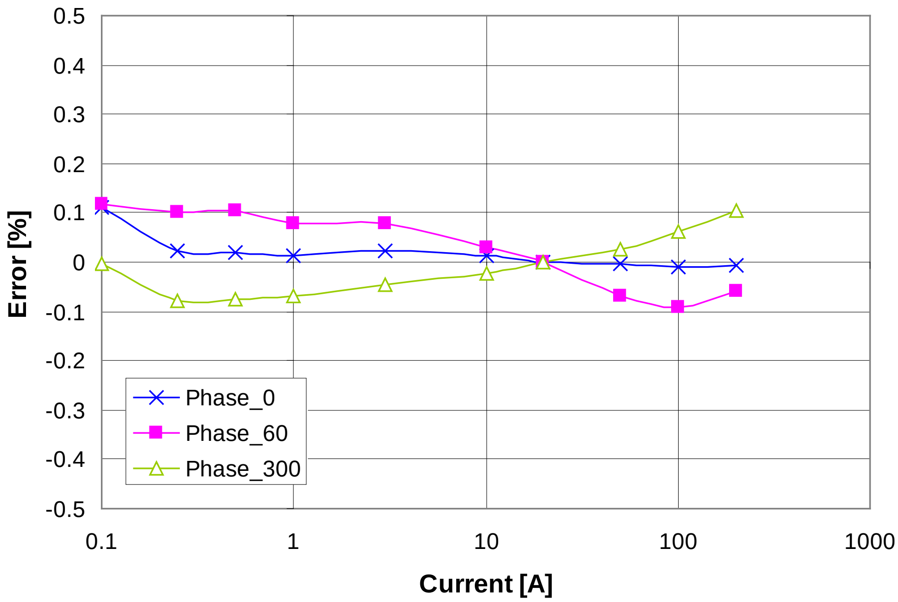
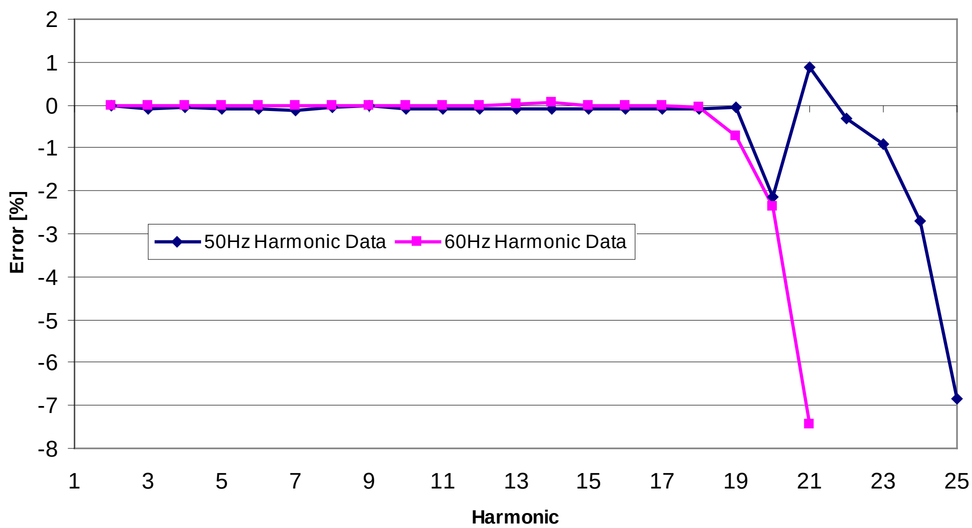



**Figure 42: Wh Accuracy, 0.1A to 200A at 240V/50Hz and Room Temperature**




Measured at current distortion amplitude of 40% and voltage distortion amplitude of 10%.

**Figure 43: Meter Accuracy over Harmonics at 240V, 30A**

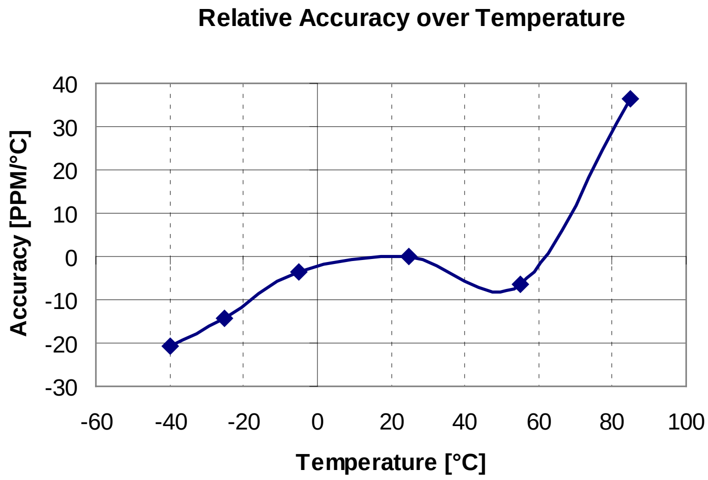
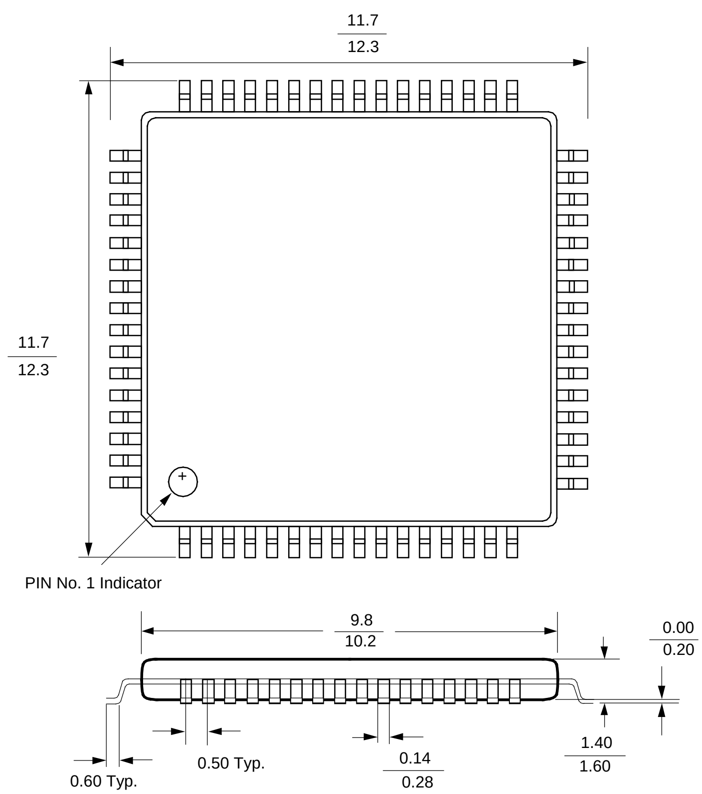


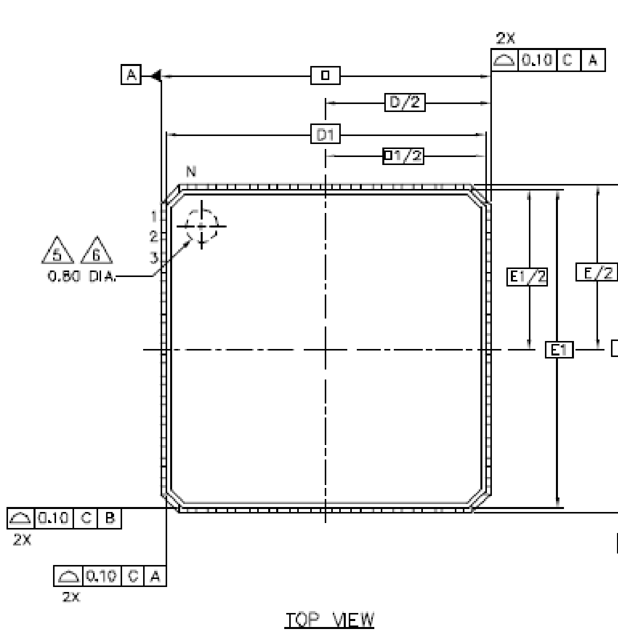

**Figure 44: Typical Meter Accuracy over Temperature Relative to 25°C (71M6521FE)**

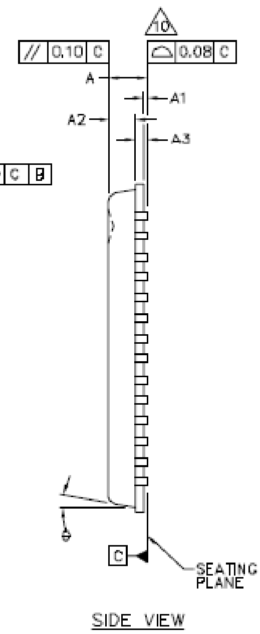
## PACKAGE OUTLINE (LQFP 64)

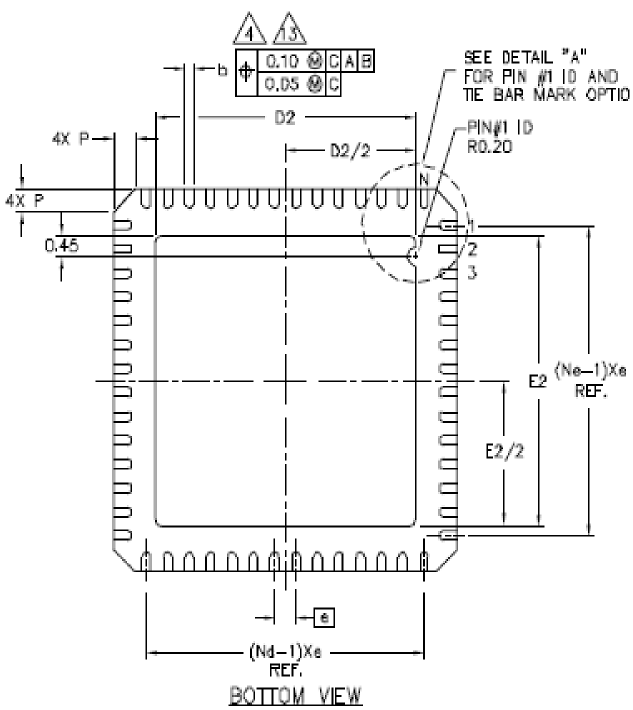



**NOTE: Controlling dimensions are in mm**

## PACKAGE OUTLINE (QFN 68)



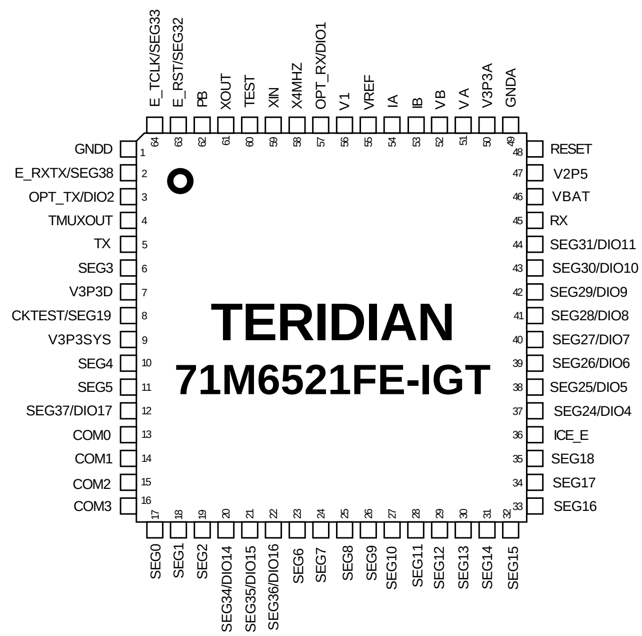




**Dimensions (in mm):**

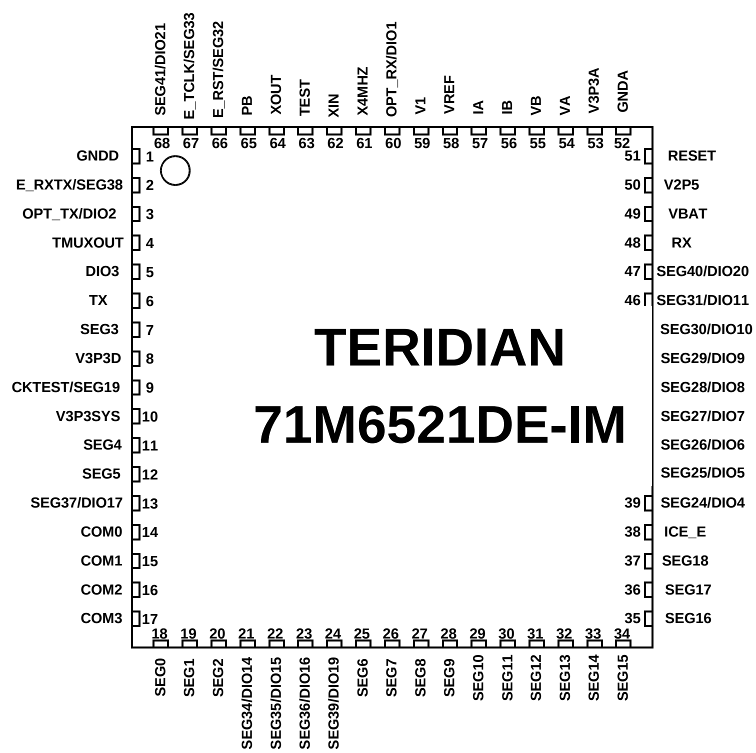
| Symbol | Min. | Nom. | Max. | Comment |
|---|---|---|---|---|
| e | | 0.4 BSC | | Pin pitch (C-C) |
| Nd | | 17 | | Pins per row |
| Ne | | 17 | | Pins per column |
| A | | 0.85 | 0.90 | Total height |
| A1 | 0.00 | 0.01 | 0.05 | |
| A2 | | 0.65 | 0.70 | |
| A3 | | 0.20 REF | | |
| b | 0.15 | 0.20 | 0.25 | Pin width *) |
| D | | 8.00 BSC | | Total width |
| D1 | | 7.75 BSC | | |
| D2 | | 6.3 | | Exposed pad **) |
| E | | 8.00 BSC | | Total length |
| E1 | | 7.75 BSC | | |
| E2 | | 6.3 | | Exposed pad |
| b | 0.15 | 0.20 | 0.25 | Pad width |
| P | 0.24 | 0.42 | 0.60 | 45° corner |
| θ | | | 12° | Angle |

*) Pin length is nominally 0.4mm (min. 0.3mm, max 0.4mm)
**) Exposed pad is internally connected to GNDD.

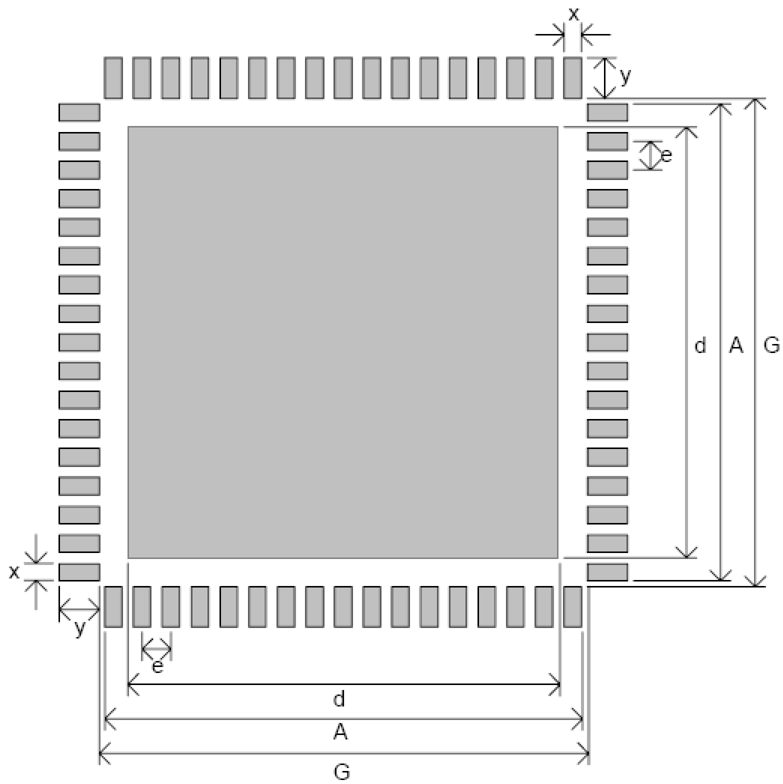
## PINOUT (LQFP-64)




## PINOUT (QFN 68)



## Recommended PCB Land Pattern for the QFN-68 Package




Recommended PCB Land Pattern Dimensions

| Symbol | Description | Typical Dimension |
|---|---|---|
| e | Lead pitch | 0.4mm |
| x | Pad width | 0.23mm |
| y | Pad length, see note 3 | 0.8mm |
| d | See note 1 | 6.3mm |
| A | | 6.63mm |
| G | | 7.2mm |

Note 1: Do not place unmasked vias in region denoted by dimension “d”.

Note 2: Soldering of bottom internal pad is not required for proper operation.

Note 3: The ‘y’ dimension has been elongated to allow for hand soldering and reworking. Production assembly may allow this dimension to be reduced as long as the ‘G’ dimension is maintained.

# PIN DESCRIPTIONS

## Power/Ground Pins:

| Name | Type | Circuit | Description |
|---|---|---|---|
| GNDA | P | -- | Analog ground: This pin should be connected directly to the ground plane. |
| GNDD | P | -- | Digital ground: This pin should be connected directly to the ground plane. |
| V3P3A | P | -- | Analog power supply: A 3.3V power supply should be connected to this pin, must be the same voltage as V3P3SYS. |
| V3P3SYS | P | -- | System 3.3V supply. This pin should be connected to a 3.3V power supply. |
| V3P3D | O | 13 | Auxiliary voltage output of the chip, controlled by the internal 3.3V selection switch. In mission mode, this pin is internally connected to V3P3SYS. In BROWNOUT mode, it is internally connected to VBAT. This pin is high impedance in LCD and sleep mode. |
| VBAT | P | 12 | Battery backup power supply. A battery or super-capacitor is to be connected between VBAT and GNDD. If no battery is used, connect VBAT to V3P3SYS. |
| V2P5 | O | 10 | Output of the internal 2.5 V regulator. A 0.1µF capacitor to GNDA should be connected to this pin. |

## Analog Pins:

| Name | Type | Circuit | Description |
|---|---|---|---|
| IA, IB | I | 6 | Line Current Sense Inputs: These pins are voltage inputs to the internal A/D converter. Typically, they are connected to the outputs of current sensors. **Unused pins must be connected to V3P3A.** |
| VA, VB | I | 6 | Line Voltage Sense Inputs: These pins are voltage inputs to the internal A/D converter. Typically, they are connected to the outputs of resistor dividers. **Unused pins must be connected to V3P3A or tied to the voltage sense input that is in use.** |
| V1 | I | 7 | Comparator Input: This pin is a voltage input to the internal power-fail comparator. The input voltage is compared to the internal BIAS voltage (1.6 V). If the input voltage is above VBIAS, the comparator output will be high (1). If the comparator output is lower, a voltage fault will occur and the chip will be forced to battery mode. |
| VREF | O | 9 | Voltage Reference for the ADC. This pin is normally disabled by setting the *VREF_CAL* bit in the I/O RAM and can then be left unconnected. If enabled, a 0.1µF capacitor to GNDA should be connected. |
| XIN<br>XOUT | I | 8 | Crystal Inputs: A 32kHz crystal should be connected across these pins. Typically, a 27pF capacitor is also connected from each pin to GNDA. It is important to minimize the capacitance between these pins. See the crystal manufacturer datasheet for details. |

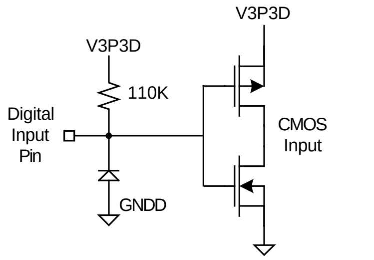
Pin types: P = Power, O = Output, I = Input, I/O = Input/Output
The circuit number denotes the equivalent circuit, as specified under “I/O Equivalent Circuits”.

## Digital Pins:

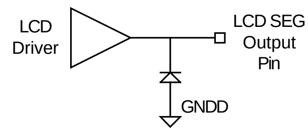
| Name | Type | Circuit | Description |
|---|---|---|---|
| COM3,<br>COM2,<br>COM1,<br>COM0 | O | 5 | LCD common outputs: These 4 pins provide the select signals for the LCD display. |
| SEG0…SEG18 | O | 5 | Dedicated LCD segment output pins. |
| SEG24/DIO4…<br>SEG31/DIO11 | I/O | 3, 4, 5 | Multi-use pins, configurable as either LCD SEG driver or DIO. (DIO4 = SCK, DIO5 = SDA when configured as EEPROM interface, WPULSE = DIO6, VARPULSE = DIO7 when configured as pulse outputs). **If unused, these pins must be configured as outputs.** |
| SEG34/DIO14…<br>SEG37/DIO17 | I/O | 3, 4, 5 | Multi-use pins, configurable as either LCD SEG driver or DIO. **If unused, these pins must be configured as outputs.** |
| SEG39/DIO19…<br>SEG41/DIO21 | I/O | 3, 4, 5 | Multi-use pins, configurable as LCD driver or DIO (QFN 68 package only). **If unused, these pins must be configured as outputs.** |
| E_RXTX/SEG38<br>E_RST/SEG32 | I/O | 1, 4, 5 | Multi-use pins, configurable as either emulator port pins (when ICE_E pulled high) or LCD SEG drivers (when ICE_E tied to GND). |
| E_TCLK/SEG33 | O | 4, 5 | |
| ICE_E | I | 2 | ICE enable. When zero, E_RST, E_TCLK, and E_RXTX become SEG32, SEG33, and SEG38 respectively. For production units, this pin should be pulled to GND to disable the emulator port. This pin should be brought out to the programming interface in order to create a way for reprogramming parts that have the *SECURE* bit set. |
| CKTEST/SEG19 | O | 4, 5 | Multi-use pin, configurable as either Clock PLL output or LCD segment driver. Can be enabled and disabled by *CKOUT_EN*. |
| TMUXOUT | O | 4 | Digital output test multiplexer. Controlled by *TMUX*[4:0]. |
| OPT_RX/DIO1 | I/O | 3, 4, 7 | Multi-use pin, configurable as Optical Receive Input or general DIO. When configured as OPT_RX, this pin receives a signal from an external photo-detector used in an IR serial interface. **If unused, this pin must be configured as an output or terminated to V3P3D or GNDD.** |
| OPT_TX/DIO2 | I/O | 3, 4 | Multi-use pin, configurable as Optical LED Transmit Output, WPULSE, RPULSE, or general DIO. When configured as OPT_TX, this pin is capable of directly driving an LED for transmitting data in an IR serial interface. **If unused, this pin must be configured as an output or terminated to V3P3D or GNDD.** |
| DIO3 | I/O | 3, 4 | DIO pin **(QFN 68 package only)** |
| RESET | I | 3 | This input pin resets the chip into a known state. For normal operation, this pin is connected to GNDD. To reset the chip, this pin should be pulled high. No external reset circuitry is necessary. |
| RX | I | 3 | UART input. **If unused, this pin must be terminated to V3P3D or GNDD.** |
| TX | O | 4 | UART output. |
| TEST | I | 7 | Enables Production Test. **Must be grounded in normal operation.** |
| PB | I | 3 | Push button input. A rising edge sets the *IE_PB* flag and causes the part to wake up if it is in SLEEP or LCD mode. PB does not have an internal pull-up or pull-down. **If unused, this pin must be terminated to GNDD.** |
| X4MHZ | I | 3 | **This pin must be connected to GNDD.** |

Pin types: P = Power, O = Output, I = Input, I/O = Input/Output
The circuit number denotes the equivalent circuit, as specified on the following page.

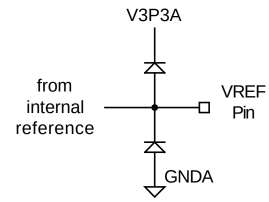
## I/O Equivalent Circuits:



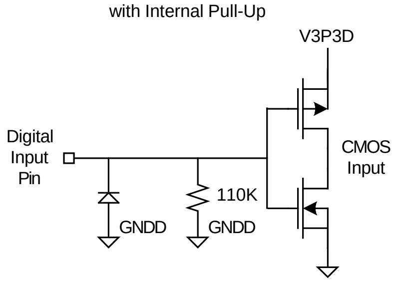

**Digital Input Equivalent Circuit**
**Type 1:**
Standard Digital Input or
pin configured as DIO Input
with Internal Pull-Up



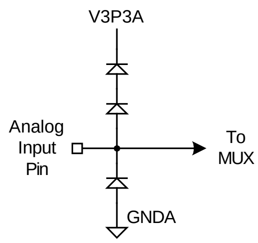

**LCD Output Equivalent Circuit**
**Type 5:**
LCD SEG or
pin configured as LCD SEG



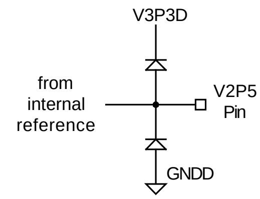

**VREF Equivalent Circuit**
**Type 9:**
VREF



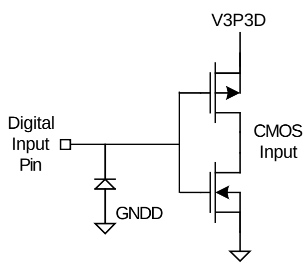

**Digital Input**
**Type 2:**
Pin configured as DIO Input
with Internal Pull-Down



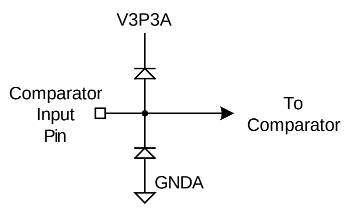

**Analog Input Equivalent Circuit**
**Type 6**:
ADC Input



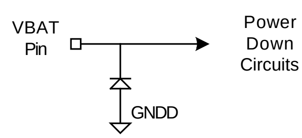

**V2P5 Equivalent Circuit**
**Type 10:**
V2P5



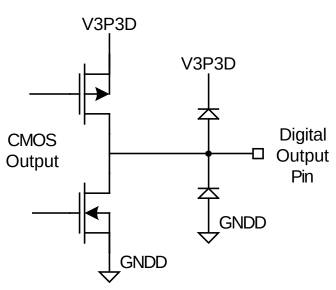

**Digital Input Type 3:**
Standard Digital Input or
pin configured as DIO Input



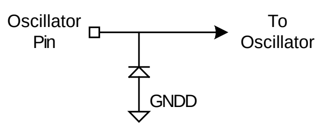

**Comparator Input Equivalent**
**Circuit Type 7:**
Comparator Input



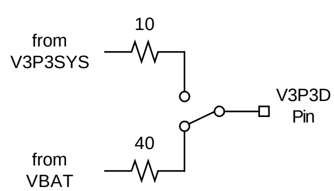

**VBAT Equivalent Circuit**
**Type 12:**
VBAT Power




**Digital Output Equivalent Circuit**
**Type 4:**
Standard Digital Output or
pin configured as DIO Output




**Oscillator Equivalent Circuit**
**Type 8:**
Oscillator I/O




**V3P3D Equivalent Circuit**
**Type 13:**
V3P3D

## ORDERING INFORMATION

| PART | PART DESCRIPTION (Package) | Accuracy (ppm/°C) | FLASH MEMORY SIZE (KB) | PACKAGING | ORDERING NUMBER | PACKAGE MARKING |
|---|---|---|---|---|---|---|
| 71M6521DE | 64-pin LQFP, lead(Pb)-free | ±40 | 16 | Bulk | 71M6521DE-IGT/F | 71M6521DE-IGT |
| 71M6521DE | 64-pin LQFP, lead(Pb)-free | ±40 | 16 | Tape & Reel | 71M6521DE-IGTR/F | 71M6521DE-IGT |
| 71M6521DH* | 64-pin LQFP, lead(Pb)-free | ±20 | 16 | Bulk | 71M6521DH-IGT/F | 71M6521DH-IGT |
| 71M6521DH* | 64-pin LQFP, lead(Pb)-free | ±20 | 16 | Tape & Reel | 71M6521DH-IGTR/F | 71M6521DH-IGT |
| 71M6521FE | 64-pin LQFP, lead(Pb)-free | ±40 | 32 | Bulk | 71M6521FE-IGT/F | 71M6521FE-IGT |
| 71M6521FE | 64-pin LQFP, lead(Pb)-free | ±40 | 32 | Tape & Reel | 71M6521FE-IGTR/F | 71M6521FE-IGT |
| 71M6521DE | 68-pin QFN, lead(Pb)-free | ±40 | 16 | Bulk | 71M6521DE-IM/F | 71M6521DE-IM |
| 71M6521DE | 68-pin QFN, lead(Pb)-free | ±40 | 16 | Tape & Reel | 71M6521DE-IMR/F | 71M6521DE-IM |
| 71M6521FE | 68-pin QFN, lead(Pb)-free | ±40 | 32 | Bulk | 71M6521FE-IM/F | 71M6521FE-IM |
| 71M6521FE | 68-pin QFN, lead(Pb)-free | ±40 | 32 | Tape & Reel | 71M6521FE-IMR/F | 71M6521FE-IM |

**Future product—contact factory for availability.*

# REVISION HISTORY

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 1.1 | 10/10 | Added the note “Guaranteed by design; not production tested.” to several *Performance Specifications* table parameters ($V_{OH}$ and $V_{OL}$ in the *Output Logic Levels* table; VBAT current in the *Supply Current* table; VREF(T) deviation from VNOM(T) and VBIAS voltage in the *VREF, VBIAS* table; Voltage to Current Crosstalk in the *ADC Converter,* Voltage to Current Crosstalk *V3P3A Referenced* table; Temperature Error in the *Temperature Sensor* table) and Timing Specifications table parameters (Reset pulse fall time in the *RESET and V1* table) | 89–93 |
| | | Changed the Response Time (V1) condition from ±100mV overdrive to split +100mV and -100mV overdrive conditions with new MIN and MAX numbers for -100mV in the *Power-Fault Comparator* table | 89 |
| | | Added < 25°C and > 25°C to BROWNOUT mode in the VBAT current parameter of *the Supply Current* table | 90 |
| | | Changed the XIN to XOUT Capacitance parameter from 3pF (max) to 3pF (typ) and changed XIN/XOUT for Capacitance to DGND from 5pF (max) to 5pF (typ) in the *Crystal Oscillator* table | 91 |
| | | Changed the THD (First 10 harmonics) parameters for 250mV-pk and 20mV-pk from -75dB (max) and -90dB (max) to -75dB (typ) and -90dB (typ) in the *ADC Converter, V3P3A Referenced* table | 92 |
| | | Deleted the *Optical Interface* parameters table | 93 |
| 2 | 11/11 | Added part type 71M6521DH | All |
| | | Added description of 71M6521DH in Hardware Overview | 10 |
| | | Added specification of temperature coefficients TC1/TC2 in Electrical Specifications for 71M6521DH | 93 |
| | | Separated numbers from units by one space, e.g. 5 mA. | All |
| | | Rephrased accuracy statement on title page (“up to 0.1% Wh accuracy over 2,000:1 current range”). Added 20 ppm/°C for 71M6521DH. | 1 |
| | | Added explanation of how TC1 and TC2 are generated for the 71M6521DH from the TRIMBGA, *TRIMBGB*, *TRIM*, and *TRIMT* fuses. | 61 |
| | | Corrected ALT MUX Sequence in Table 1 | 11 |
| | | Updated Ordering Information Table (71M6521DH future product). | 105 |
| | | Added 71M6521DH version to header. | All |
| | | Added 71M6521DH to FLASH memory description. | 39 |
| | | Changed TRIMM to TRIMM[2:0]. | 61 |
| | | Added formula to convert TC1/TC2 to PPMC1/PPMC2. | 61 |
| | | Added explanation of “box” temperature concept. | 61-62 |
| | | Added description of TRIMSEL[3:0] and TRIM[7:0] to I/O RAM DESCRIPTION. | 80 |
| | | Added VREF(T) deviation from VNOM(T) description for 71M6521DH in VREF, VBIAS section. | 93 |
| | | Added section explaining the distinction between 71M6521DE/71M6521FE and 71M6521DH parts. | 60 |

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