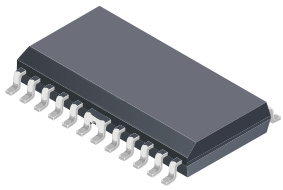
Dual Full-Bridge PWM Motor Driver

Features and Benefits

- 750 mA continuous output current
- 45 V output sustaining voltage
- Internal clamp diodes
- Internal PWM current control
- Low output saturation voltage
- Internal thermal shutdown circuitry
- Pin compatible with UDx2916
- DMOS outputs

Package: 24-pin batwing wide SOIC (package LB)



Not to scale

Description

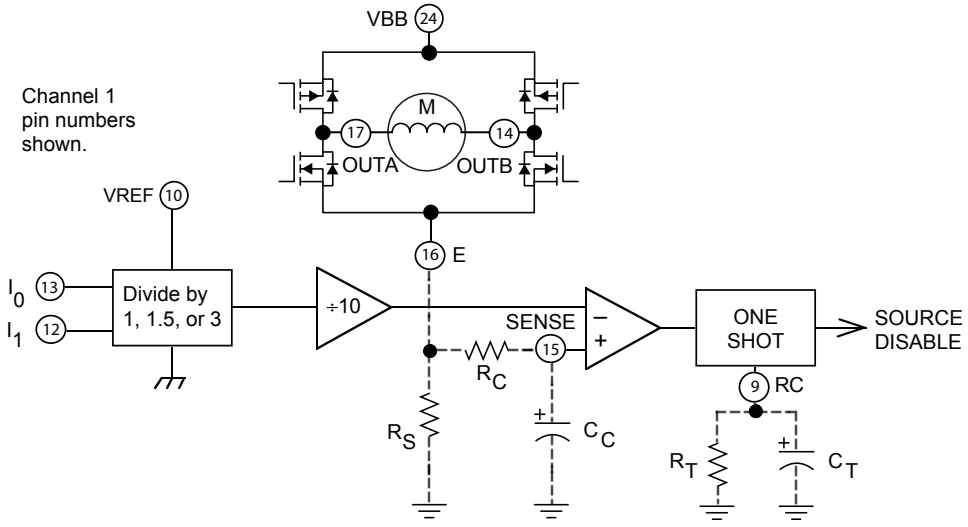
The A4970 motor driver drives both windings of a bipolar stepper motor or bidirectionally controls two DC motors. Both bridges are capable of sustaining 45 V and include internal pulse-width modulation (PWM) control of the output current to 750 mA.

For PWM current control, the maximum output current is determined by user selection of a reference voltage and sensing resistor. Two logic-level inputs select output current limits of 0%, 33%, 67%, or 100% of the maximum level. A PHASE input to each bridge determines load current direction.

Intrinsic diodes in the MOSFET output structure protect against inductive transients. Internally generated delays prevent crossover currents when switching current direction. Special power-up sequencing is not required. Thermal protection circuitry disables the outputs if the chip temperature exceeds safe operating limits.

The device is supplied in a 24-pin surface-mount wide SOIC with two pairs of batwing leads (LB). The webbed-pin construction provides for maximum package power dissipation in the smallest possible construction. The package is lead (Pb) free, with 100% matte tin leadframe plating.

PWM Current-Control Circuitry



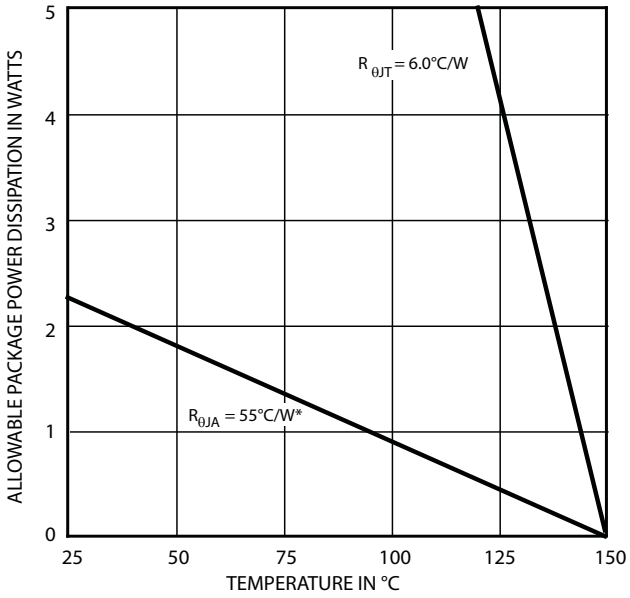
Selection Guide

Part Number	Package	Packing	Ambient Temperature (°C)
A4970GLBTR-T	24-pin batwing SOICW	1000 per reel	–40 to 105
A4970SLBTR-T	24-pin batwing SOICW	1000 per reel	–20 to 85

Absolute Maximum Ratings

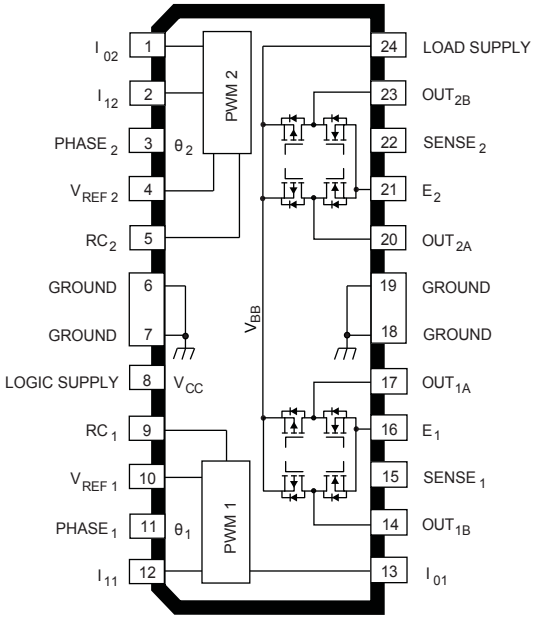
Characteristic	Symbol	Notes		Rating	Units
Motor Supply Voltage	V_{BB}			45	V
Logic Supply Voltage	V_{CC}			6.0	V
Input Voltage	V_{IN}	I0x, I1x, PHASEx pins		–0.3 to 6.0	V
Reference Input Voltage	V_{REF}	VREF pin		–0.3 to 8.0	V
Output Emitter Voltage	V_E			750	mV
Sense Voltage	V_{SENSE}			750	mV
Output Current*	I_{OUT}	Peak	Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified current rating or T_J(max)	1.0	A
		Continuous		750	mA
Package Power Dissipation	P_D	See graph		—	W
Operating Ambient Temperature	T_A	Range G		–40 to 105	ºC
		Range S		–20 to 85	ºC
Maximum Junction Temperature	T_J(max)			150	ºC
Storage Temperature	T_{stg}			–55 to 150	ºC

Power Dissipation



*Measured on a single-layer board, with 1 sq. in. of 2 oz copper area.
For additional information, refer to the Allegro Web site.

Pin-out Diagram



ELECTRICAL CHARACTERISTICS Valid at T_A = 25°C, $T_J \le$ 150°C, V_{BB} = 45 V, V_{CC} = 4.75 to 5.25 V, V_{REF} = 5.0 V, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Output Drivers (OUTA or OUTB)						
Motor Supply Range	V_{BB}		7.45	–	45	V
Output Leakage Current	I_{CEX}	I0 = I1 = 2.4 V, V_{OUT} = 45.0 V	–	< 1.0	50	µA
		V_{OUT} = 0.0 V	–	< –1.0	–50	µA
Output MOSFET On Resistance	$R_{DS(on)}$	Sink Driver, I_{OUT} = 750 mA	–	0.3	0.75	Ω
		Source Driver, I_{OUT} = –750 mA	–	1.0	1.85	Ω
Clamp Diode Leakage Current	I_R	V_R = 45 V	–	< 1.0	50	µA
Clamp Diode Forward Voltage	V_F	I_F = 750 mA	–	0.95	2	V
Driver Supply Current	$I_{BB(ON)}$	Both bridges on, I0 = I1 = 0.8 V, no load	–	5	10	mA
	$I_{BB(OFF)}$	Both bridges off, I0 = I1 = 2.4 V, no load	–	3	7.5	mA
Control Logic						
Input Voltage	$V_{IN(1)}$	All inputs	2.4	–	–	V
	$V_{IN(0)}$	All inputs	–	–	0.8	V
Input Current	$I_{IN(1)}$	V_{IN} = 2.4 V	–	<1.0	20	µA
		V_{IN} = 0.8 V	–	– 3.0	–200	µA
Reference Voltage Range	V_{REF}	Operating	1.5	–	7.5	V
Reference Input Current	I_{REF}	V_{REF} = 7.5 V	–	–	150	µA
Current Limit Threshold	V_{REF}/V_{SENSE}	I0 = I1 = 0.8 V	9.5	10	10.5	–
		I0 = 2.4 V, I1 = 0.8 V	13.5	15	16.5	–
		I0 = 0.8 V, I1 = 2.4 V	25.5	30	34.5	–
Thermal Shutdown Temperature	T_J		–	170	–	°C
Total Logic Supply Current	$I_{CC(ON)}$	I0 = I1 = 0.8 V, no load	–	3.0	7.5	mA
	$I_{CC(OFF)}$	I0 = I1 = 2.4 V, no load	–	3.5	7.5	mA
Fixed Off-Time	t_{off}	R_T = 56 kΩ, C_T = 820 pF	42	46	50	µs
V_{CC} Undervoltage Lockout (UVLO) Threshold	V_{CCUVLO}	V_{CC} rising	–	4	–	V
V_{CC} Undervoltage Lockout (UVLO) Threshold	$V_{CCUVLOHYS}$		–	200	–	mV

APPLICATIONS INFORMATION

PWM CURRENT CONTROL

The A4970 dual bridges drive both windings of a bipolar stepper motor. Output current is sensed and controlled independently in each bridge by an external sense resistor, R_S, internal comparator, and monostable multivibrator.

When the bridge is turned on, current increases in the motor winding and it is sensed by the external sense resistor until the sense voltage, V_{SENSE}, reaches the level set at the comparator input:

$$I_{TRIP} = V_{REF}/10\ R_S$$

The comparator then triggers the monostable, which turns off the source driver of the bridge.

The actual load current peak will be slightly higher than the trip point (especially for low-inductance loads) because of the internal logic and switching delays. This delay, t_d, is typically 2 µs. After turn-off, the motor current decays, circulating through the ground-clamp diode and sink transistor. The source driver off-time (and therefore the magnitude of the current decrease) is determined by the external RC timing components of the monostable:

$$t_{off} = R_T C_T$$

where:

R_T = 20 to 100 kΩ, and
C_T = 100 to 1000 pF.

The fixed off-time should be short enough to keep the current chopping above the audible range (< 46 µs) and long enough to properly regulate the current. Because only slow-decay current control is available, short off times (< 10 µs) require additional efforts to ensure proper current regulation. Factors that can negatively affect the ability to properly regulate the current when using short off times include: higher motor-supply voltage, light load, and longer than necessary blank time.

When the source driver is re-enabled, the winding current (the sense voltage) is again allowed to rise to the comparator's threshold. This cycle repeats itself, maintaining the average motor winding current at the desired level.

Loads with high distributed capacitances may result in high turn-on current peaks. This peak (appearing across R_S) will attempt to trip the comparator, resulting in erroneous current control or high-frequency oscillations. An external $R_C C_C$ time delay should be used to further delay the action of the comparator.

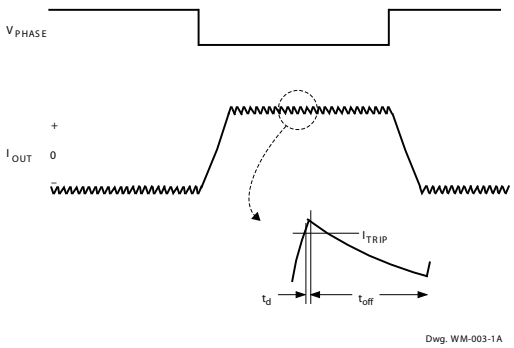
The time constant for the delay to produce suitable blank time can be estimated using:

$$R_C C_C = 0.0114 \times R_T C_T$$

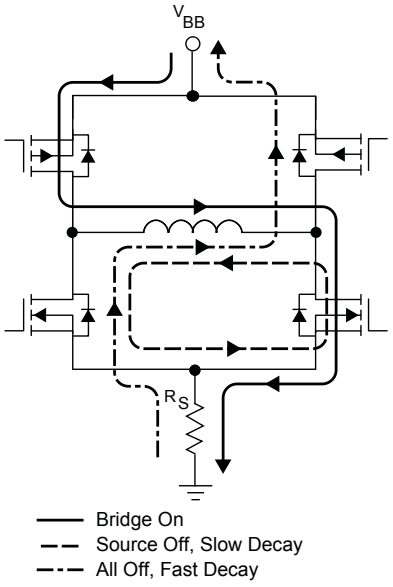
This equation assumes that the current control loop duty cycle is greater than 5% and the voltage on the SENSE pin will reach 99% of the target value set for V_{SENSE}. These assumptions will apply to the majority of applications and can be regarded as a starting value for further optimization by calculation or waveform measurement.

Depending on load type, many applications will not require these external components (SENSE connected to E).

PWM OUTPUT CURRENT WAVE FORM



LOAD CURRENT PATHS



LOGIC CONTROL OF OUTPUT CURRENT

Two logic level inputs (I_0 and I_1) allow digital selection of the motor winding current at 100%, 67%, 33%, or 0% of the maximum level per the table. The 0% output current condition turns off all drivers in the bridge and can be used as an OUTPUT ENABLE function.

CURRENT-CONTROL TRUTH TABLE

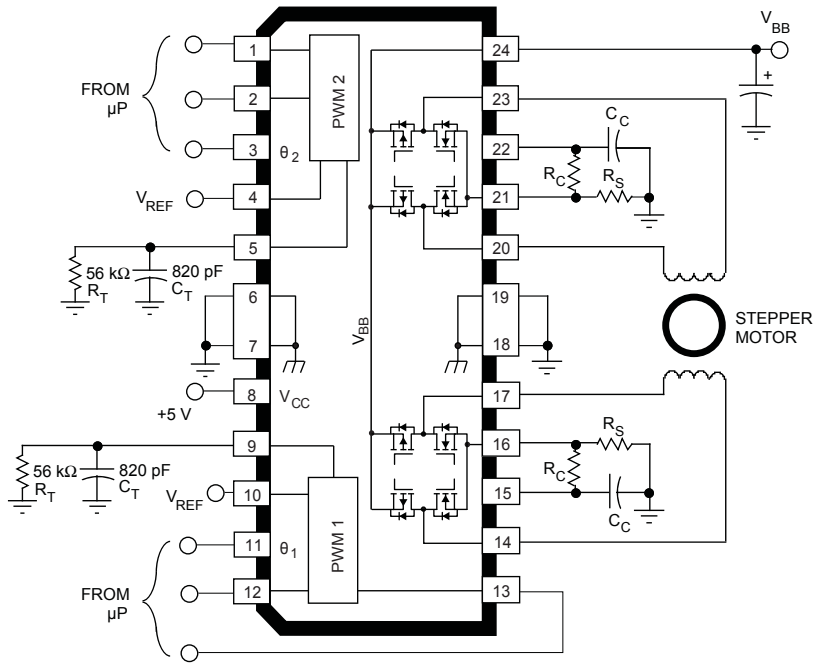
I_0	I_1	Output Current
L	L	$V_{REF}/10\ R_S = I_{TRIP}$
H	L	$V_{REF}/15\ R_S = 2/3\ I_{TRIP}$
L	H	$V_{REF}/30\ R_S = 1/3\ I_{TRIP}$
H	H	0

These logic level inputs greatly enhance the implementation of microprocessor controlled drive formats.

During half-step operations, the I_0 and I_1 allow the microprocessor to control the motor at a constant torque between all positions in an eight-step sequence. This is accomplished by digitally selecting 100% drive current when only one phase is on and 67% drive current when two phases are on. Logic highs on both I_0 and I_1 turn-off all drivers to allow rapid current decay when switching phases. This helps to ensure proper motor operation at high step rates.

The logic control inputs can also be used to select a reduced current level (and reduced power dissipation) for "hold" conditions and/or increased current (and available torque) for start-up conditions.

TYPICAL APPLICATION



GENERAL

The PHASE input to each bridge determines the direction motor winding current flows. An internally generated dead time (approximately 2 µs) prevents crossover currents that can occur when switching the PHASE input.

All four drivers in the bridge output can be turned-off between steps ($I_0 = I_1 \geq 2.4$ V), resulting in a fast current decay through the internal output clamp and flyback diodes. The fast current decay is desirable in half-step and high-speed applications. The PHASE, I_0,and I_1 inputs float high.

Varying the reference voltage, V_{REF} , provides continuous control of the peak load current for micro-stepping applications.

Thermal protection circuitry turns-off all drivers when the junction temperature reaches +170°C. It is only intended to protect the device from failures due to excessive junction temperature and should not imply that output short circuits are permitted. The output drivers are re-enabled when the junction temperature cools to +145°C.

The A4970 output drivers are optimized for 500 mA operating current. Under normal operating conditions, when combined with the excellent thermal properties of the package designs, this allows continuous operation of both bridges simultaneously at 500 mA.

TRUTH TABLE

PHASE	OUT_A	OUT_B
H	H	L
L	L	H

APPLICATION NOTES

Current Sensing

To minimize current sensing inaccuracies caused by ground trace IR drops, each current-sensing resistor should have a separate return to the ground terminal of the device. For low-value sense resistors, the IR drops in the PCB can be significant and should be taken into account. The use of sockets should be avoided as their contact resistance can cause variations in the effective value of R_S.

Generally, larger values of R_S reduce the aforementioned effects but can result in excessive heating and power loss in the sense resistor. The selected value of R_S should not cause the maximum operating voltage of 0.75 V (V_{REF}(max)/10), for the VE terminal, to be exceeded. The recommended value of R_S is in the range of:

$$R_S = 0.50 / I_{TRIP}(\text{max}) .$$

If desired, the reference input voltage can be filtered by placing a capacitor from VREF to ground. The ground return for this capacitor as well as the bottom of any resistor divider used should be independent of the high-current power-ground trace to avoid changes in VREF due to IR drops.

Thermal Considerations

For normal operation it is recommended that the maximum operating junction temperature be 145°C, which is below the operating range of the TSD system. The junction temperature can be measured best by attaching a thermocouple to the batwing of the device and measuring the tab temperature, T_{TAB}. The junction temperature can then be approximated by using the formula:

$$T_J = T_{TAB} + (2 \times I_{LOAD} \times V_F \times R_{\theta JT}) \ ,$$

where V_F can be chosen from the electrical specification table for the given level of I_{LOAD}. The value for $R_{\theta JT}$ is approximately 6°C/W.

The power dissipation of the batwing package can be improved 20% to 30% by adding a section of printed circuit board copper (typically 6 to 18 square centimeters) connected to the batwing terminals of the device.

The thermal performance in applications that run at high load currents, high duty cycles, or both, can be improved by adding external diodes from each output to ground in parallel with the internal diodes. Fast-recovery (≤200 ns) diodes should be used to minimize switching losses.

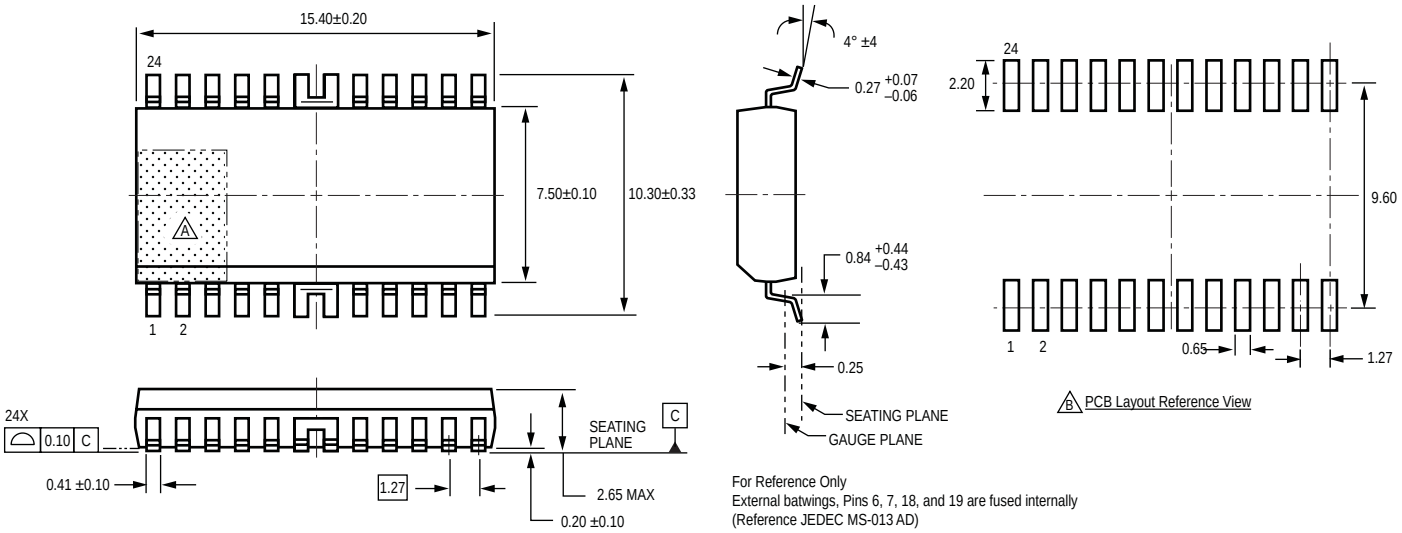
Load Supply Terminal

The load supply terminal, VBB, should be decoupled with an electrolytic capacitor (≥47 µF is recommended), placed as close to the device as is physically practical. To minimize the effect of system ground IR drops on the logic and reference input signals, the system ground should have a low-resistance return to the load supply voltage.

Fixed Off-Time Selection

With increasing values of t_{OFF}, switching losses decrease, low-level load current regulation improves, EMI reduces, PWM frequency decreases, and ripple current increases. The value of t_{OFF} can be chosen for optimization of these parameters. For applications where audible noise is a concern, typical values of t_{OFF} should be chosen in the range of 15 to 35 µs.

Package LB, 24-pin SOICW
External batwings, Pins 6, 7, 18, and 19 are fused internally



For Reference Only
External batwings, Pins 6, 7, 18, and 19 are fused internally
(Reference JEDEC MS-013 AD)
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Reference pad layout (reference IPC SOIC127P1030X265-24M)
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

Revision History

Revision	Revision Date	Description of Revision
Rev. 1	December 19, 2011	Add G temperature range

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