GM71V64400C

16,777,216 WORDS x 4 BIT
CMOS DYNAMIC RAM

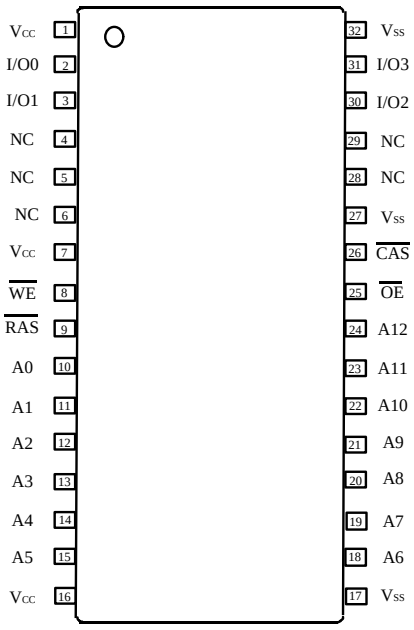
Description

The GM71V64400C is the second generation dynamic RAM organized 16,777,216 words by 4 bits. The GM71V64400C utilizes 0.35um CMOS Silicon Gate Process Technology as well as advanced circuit techniques for wide operating margins, both internally and to the system user. System oriented features include single power supply of 3.3V¡ Ø.3V tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

The GM71V64400C offers Fast Page Mode as a high speed access mode.

Pin Configuration

32 SOJ / TSOP II



(Top View)

Features

- 16,777,216 Words x 4 Bit
- Fast Page Mode Capability
- Fast Access Time & Cycle Time

(Unit: ns)

	t_{RAC}	t_{AA}	t_{CAC}	t_{RC}	t_{PC}
GM71V64400C-5	50	25	13	90	35
GM71V64400C-6	60	30	15	110	40
GM71V64400C-7	70	35	18	130	45

- Low Power
- Active : 432 mW / 396 mW / 360 mW (MAX)
  - Standby : 3.6 mW (CMOS level :MAX)
- $\overline{RAS}$ Only Refresh, $\overline{CAS}$ before $\overline{RAS}$ Refresh, Hidden Refresh Capability
- LVTTL
- 8192 Refresh Cycles/64 ms
- Single Power Supply of 3.3V¡ Ø.3V with a built-in VBB generator

Pin Description

Pin	Function	Pin	Function
A0-A12	Address Inputs	$\overline{WE}$	Write Enable
A0-A12	Refresh Address Inputs	I/O0 - I/O3	Data Input / Data Output
$\overline{RAS}$	Row Address Strobe	V_{CC}	Power (+3.3V)
$\overline{CAS}$	Column Address Strobe	V_{SS}	Ground
$\overline{OE}$	Output Enable	NC	No Connection

Ordering Information

Type No.	Access Time	Package
GM71V64400CJ-5 GM71V64400CJ-6 GM71V64400CJ-7	50ns 60ns 70ns	400 Mil 32Pin Plastic SOJ
GM71V64400CT-5 GM71V64400CT-6 GM71V64400CT-7	50ns 60ns 70ns	400 Mil 32Pin Plastic TSOP II

Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature under Bias	0 to 70	¡ É
T_{STG}	Storage Temperature (Plastic)	-55 to 125	¡ É
V_{IN}/V_{OUT}	Voltage on any Pin Relative to V_{SS}	-0.5 to V_{CC} + 0.5 (MAX ; 4.6V)	V
V_{CC}	Voltage on V_{CC} Relative to V_{SS}	-0.5 to 4.6	V
I_{OUT}	Short Circuit Output Current	50	§ Ì
P_D	Power Dissipation	1.0	W

*Note : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

Recommended DC Operating Conditions (T_A = 0 ~ 70¡ É)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
V_{IH}	Input High Voltage	2.0	-	Vcc+0.3	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V

DC Electrical Characteristics: (V_{CC} = 3.3V¡ Ø0.3V, T_A = 0 ~ 70¡ É

Symbol	Parameter		Min	Max	Unit	Note
V_{OH}	Output Level Output "H" Level Voltage (I_{OUT} = -2§ Ì		2.4	-	V	
V_{OL}	Output Level Output "L" Level Voltage (I_{OUT} = 2§ Ì		-	0.4	V	
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} min)	50ns	-	120	§ Ì	1, 2
		60ns	-	110		
		70ns	-	100		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$ = V_{IH}, D_{OUT} = High-Z)		-	2	§ Ì	
I_{CC3}	$\overline{RAS}$-Only Refresh Current Average Power Supply Current $\overline{RAS}$-Only Refresh Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min)	50ns	-	120	§ Ì	2
		60ns	-	110		
		70ns	-	100		
I_{CC4}	Fast Page Mode Current Average Power Supply Current Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	50ns	-	110	§ Ì	1, 3
		60ns	-	100		
		70ns	-	90		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$¡ ÝV_{CC}-0.2V, D_{OUT} = High-Z)		-	0.5	§ Ì	
I_{CC6}	$\overline{CAS}$-before-$\overline{RAS}$ Refresh Current (t_{RC} = t_{RC} min)	50ns	-	140	§ Ì	
		60ns	-	130		
		70ns	-	120		
I_{CC7}	Standby Current $\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{OUT} = Enable		-	5	§ Ì	1
$I_{I(L)}$	Input Leakage Current, Any Input (0V¡ ÝV_{IN}¡ ÝV_{CC})		-5	5	§ Ë	
$I_{O(L)}$	Output Leakage Current (D_{OUT} is Disabled, 0V¡ ÝV_{OUT}¡ ÝV_{CC})		-5	5	§ Ë	

Note: 1. I_{CC} depends on output load condition when the device is selected. $I_{CC(max)}$ is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

Capacitance (V_{CC} = 3.3V ± 0.3V, T_A = 25°C)

Symbol	Parameter	Typ	Max	Unit	Note
C_{I1}	Input Capacitance (Address, Data-In)	-	5	pF	1
C_{I2}	Input Capacitance (Clocks)	-	7	pF	1
C_O	Output Capacitance (Data-Out)	-	7	pF	1, 2

Note: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{OUT}.

AC Characteristics (V_{CC} = 3.3V ± 0.3V, T_A = 0 ~ 70°C, See Notes 1, 14,15,16)

Test Conditions

Input rise and fall times : 5ns
Input timing reference levels : V_{IL}/V_{IH} = 0.8/2.4V
Output timing reference levels : V_{OL}/V_{OH} = 0.8/2.0V
Output load : 1 TTL gate+C_L (100pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	GM71V64400C-5		GM71V64400C-6		GM71V64400C-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	90	-	110	-	130	-	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	30	-	40	-	50	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	10	-	10	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	50	10000	60	10000	70	10000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	13	10000	15	10000	20	10000	ns	
t_{ASR}	Row Address Set-up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	10	-	ns	
t_{ASC}	Column Address Set-up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	10	-	15	-	15	-	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	37	20	45	20	50	ns	8
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	25	15	30	15	35	ns	9
t_{RSH}	$\overline{RAS}$ Hold Time	13	-	15	-	20	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	50	-	60	-	70	-	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	5	-	ns	
t_{ODD}	$\overline{OE}$ to D_{IN} Delay Time	13	-	15	-	20	-	ns	
t_{DZO}	$\overline{OE}$ Delay Time from D_{IN}	0	-	0	-	0	-	ns	
t_{DZC}	$\overline{CAS}$ Set-up Time from D_{IN}	0	-	0	-	0	-	ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{REF}	Refresh Period (8192 Cycles)	-	64	-	64	-	64	ms	

Read Cycles

Symbol	Parameter	GM71V64400C-5		GM71V64400C-6		GM71V64400C-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	-	50	-	60	-	70	ns	2,3,17
t_{CAC}	Access Time from $\overline{CAS}$	-	13	-	15	-	20	ns	3,4 13,17
t_{AA}	Access Time from Column Address	-	25	-	30	-	35	ns	3,5 13,17
t_{OAC}	Access Time from $\overline{OE}$	-	13	-	15	-	20	ns	3,17
t_{RCS}	Read Command Set-up Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	-	0	-	0	-	ns	
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	-	0	-	0	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	25	-	30	-	35	-	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	25	-	30	-	35	-	ns	
t_{OFF}	Output Buffer Turn-off Time	0	13	0	15	0	20	ns	6
t_{OEZ}	Output Buffer Turn-off Time from $\overline{OE}$	0	13	0	15	0	20	ns	6
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	13	-	15	-	20	-	ns	
t_{OEP}	$\overline{OE}$ Pulse width	13	-	15	-	20	-	ns	

Write Cycles

Symbol	Parameter	GM71V64400C-5		GM71V64400C-6		GM71V64400C-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{WCS}	Write Command Set-up Time	0	-	0	-	0	-	ns	10
t_{WCH}	Write Command Hold Time	10	-	15	-	15	-	ns	
t_{WP}	Write Command Pulse Width	10	-	10	-	10	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	-	15	-	20	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	13	-	15	-	20	-	ns	
t_{DS}	Data-in Set-up Time	0	-	0	-	0	-	ns	11
t_{DH}	Data-in Hold Time	10	-	15	-	15	-	ns	11

Read-Modify-Write Cycles

Symbol	Parameter	GM71V64400C-5		GM71V64400C-6		GM71V64400C-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RWC}	Read-Modify-Write Cycle Time	133	-	155	-	185	-	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	73	-	85	-	100	-	ns	10
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	36	-	40	-	50	-	ns	10
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	48	-	55	-	65	-	ns	10
t_{OEH}	$\overline{OE}$ Hold Time from $\overline{WE}$	13	-	15	-	20	-	ns	

Refresh Cycle

Symbol	Parameter	GM71V64400C-5		GM71V64400C-6		GM71V64400C-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{CSR}	$\overline{CAS}$ Set-up Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	10	-	10	-	10	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	10	-	10	-	10	-	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	10	-	10	-	10	-	ns	
t_{CPN}	$\overline{CAS}$ Precharge Time in Normal Mode	10	-	10	-	10	-	ns	

Fast Page Mode Cycles

Symbol	Parameter	GM71V64400C-5		GM71V64400C-6		GM71V64400C-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	35	-	40	-	45	-	ns	
t_{CP}	Fast Page Mode $\overline{CAS}$ Precharge Time	10	-	10	-	10	-	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	-	100,000	-	100,000	-	100,000	ns	12
t_{ACP}	Access Time from $\overline{CAS}$ Precharge	-	30	-	35	-	40	ns	3,13 17
t_{RHCP}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	30	-	35	-	40	-	ns	
t_{CPW}	Fast Page Mode Read-Modify-Write Cycle $\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	50	-	55	-	65	-	ns	10
t_{PRWC}	Fast Page Mode Read-Modify-Write Cycle Time	76	-	85	-	100	-	ns	10

Test Mode Cycles

Symbol	Parameter	GM71V64400C-5		GM71V64400C-6		GM71V64400C-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{WS}	Test Mode $\overline{WE}$ Set-up Time	0	-	0	-	0	-	ns	
t_{WH}	Test Mode $\overline{WE}$ Hold Time	10	-	10	-	10	-	ns	

Counter Test Cycles

Symbol	Parameter	GM71V64400C-5		GM71V64400C-6		GM71V64400C-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{CPT}	$\overline{CAS}$ Precharge Time in Counter Test Cycle	40	-	40	-	40	-	ns	

Notes:

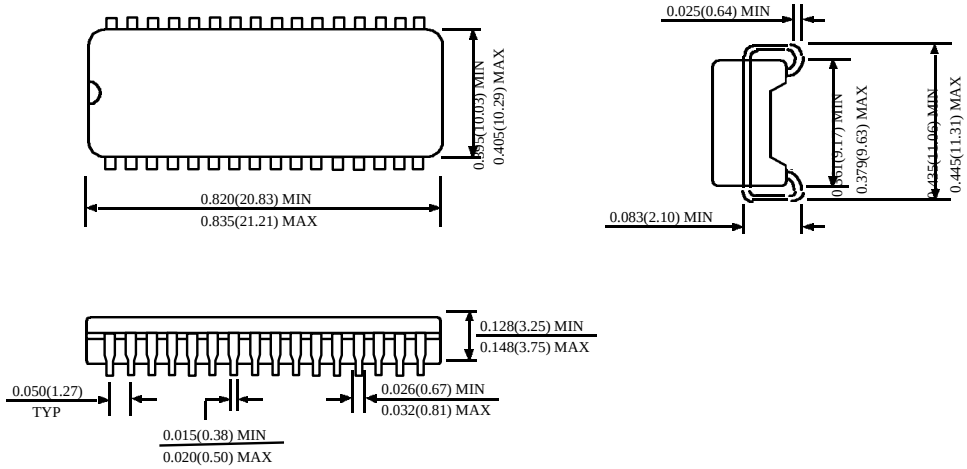
1. AC Measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 1 TTL loads and 100§ Ü
4. Assumes that $t_{RCD} \geq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$.
5. Assumes that $t_{RCD} \geq t_{RCD}(max)$ and $t_{RAD} \geq t_{RAD}(max)$.
6. $t_{OFF}(max)$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. $V_{IH}(min)$ and $V_{IL}(max)$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the $t_{RCD}(max)$ limit insures that $t_{RAC}(max)$ can be met, $t_{RCD}(max)$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD}(max)$ limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the $t_{RAD}(max)$ limit insures that $t_{RAC}(max)$ can be met, $t_{RAD}(max)$ is specified as a reference point only; if t_{RAD} is greater than the specified $t_{RAD}(max)$ limit, then access time is controlled exclusively by t_{AA}.

10. t_{WCS}, t_{RWD}, t_{CWD} t_{CPW} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if t_{WCS} ¡ Ãt_{WCS}(min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if t_{RWD}¡ Ãt_{RWD}(min), t_{CWD}¡ Ãt_{CWD}(min), t_{AWD}¡ Ãt_{AWD}(min) and t_{CPW}¡ Ãt_{CPW}(min), the cycle is a read- modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or a read modify write cycle.
12. t_{RASP} defines $\overline{RAS}$ pulse width in fast page mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 100§ Ás required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ refresh cycles is required.
15. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
16. Test mode operation specified in this data sheet is 2-bit test function controlled by control address bits - - - CA0. This test mode operation can be performed by $\overline{WE}$-and-$\overline{CAS}$-before-$\overline{RAS}$ (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of two test bits accord each other, the condition of the output data is high level. When the state of two test bits do not accord, the condition of the output data is low level. In order to end this test mode operation, perform a $\overline{RAS}$ only refresh cycle or a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.
17. In a test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC}, t_{OAC} and t_{ACP} is delayed for 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

Package Dimension

Unit: Inches (mm)

32 SOJ



32 TSOP (TYPE II)