

**FEATURES**

- 35 nSec maximum acquisition time to 0.01%
- 30 nSec maximum hold-mode settling to 0.01%
- 1 pSec aperture uncertainty
- 150 MHz small-signal bandwidth
- 545 mW power dissipation
- Small 14-pin DIP package
- CMOS control signal

**PRODUCT OVERVIEW**

The SHM-43 sample-hold utilizes a proprietary architecture in delivering an acquisition time of 35 nanoseconds maximum to 0.01% and 20 nanoseconds maximum to 0.1% accuracy.

Operation requires +15V and ±5V supplies and the analog input range is ±2V. Packaged in a small 14-pin DIP, the SHM-43 offers a CMOS compatible sample command while dissipating just 545 milliwatts.

The SHM-43 has been designed for applications that demand fast acquisition times (25 nS,

±0.01%), fast hold mode settling (20nS, ±0.01%), wide bandwidth, and the ability to drive resistive (100Ω), and capacitive (50 pF) loads with no compromise in performance. These features make the SHM-43 an ideal choice for driving flash A/D converters in applications such as radar and communications.

Two temperature ranges are offered: the commercial 0 to +70 °C and military -55 to +125 °C.

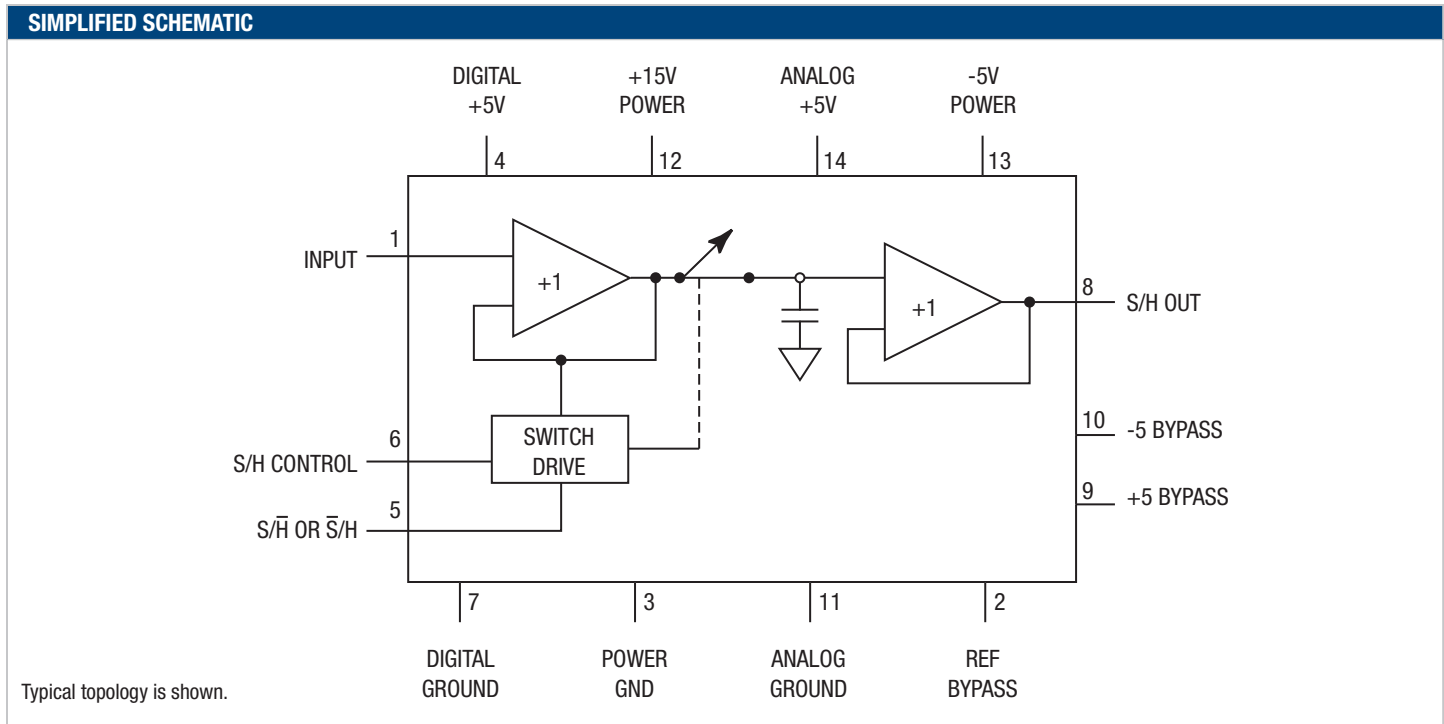


Figure 1. Simplified Block Diagram



**ORDERING GUIDE SUMMARY**

Model Number	Temperature Range
SHM-43MC	0 to +70 °C
SHM-43MM	-55 to +125 °C

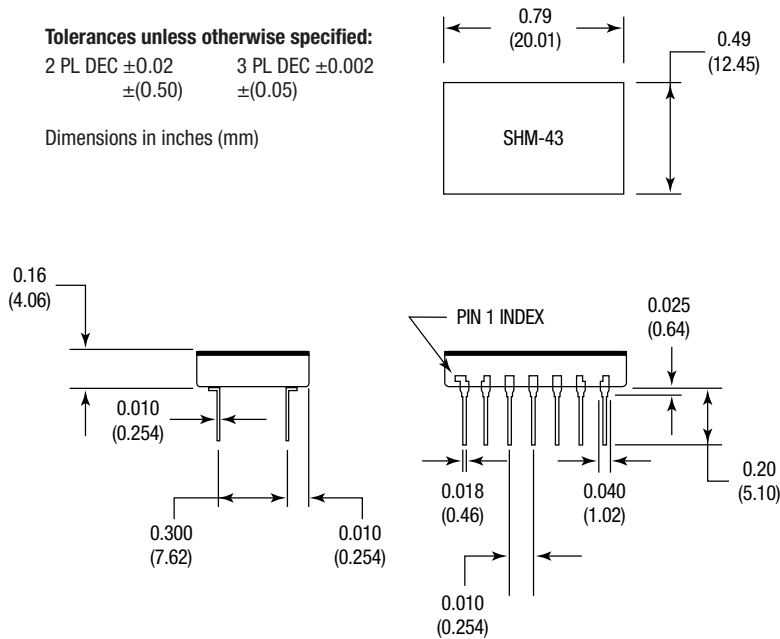
Contact Murata Power Solutions for availability of MIL-STD-883 versions.

**MECHANICAL DIMENSIONS**

**Tolerances unless otherwise specified:**

2 PL DEC ±0.02     3 PL DEC ±0.002  
 ±(0.50)     ±(0.05)

Dimensions in inches (mm)



**INPUT/OUTPUT CONNECTIONS**

Pin	Function	Pin	Function
1	Input	8	S/H Out
2	Ref Bypass	9	+5 Bypass
3	Power Gnd	10	-5 Bypass
4	Digital +5V	11	Analog Ground
5	S/H or S/H	12	+15V Power
6	S/H Control	13	-15V Power
7	Digital Ground	14	Analog +5V

**Functional Specifications**

Apply over the operating temperature range, ±1 Volt input range, 100Ω load, +15V, ±5V nominal supplies, unless otherwise specified.

PARAMETERS	MIN	TYP	MAX	UNITS
Input Voltage Range	-2	—	+2	Volts
Input Impedance	50	160	—	Kohms
<b>Digital Inputs</b> (Digital Supply = +5V)				
<b>Logic Levels</b>				
Logic 1	3.8	—	—	Vdc
Logic 0	—	—	1.35	Vdc
<b>Logic Loading</b>				
Logic 1	—	1	5	µA
Logic 0	—	1	5	µA
<b>OUTPUTS</b>				
Voltage Range	±2	—	—	V
Output Current	50	—	—	mA
Output Impedance (DC)	—	0.1	0.25	Ohms
Stable Capacitive Load	50	—	—	pF
<b>PERFORMANCE</b>				
<b>Nonlinearity, DC (±1V)</b>				
+25 °C	—	—	0.01	%
0 to +70 °C	—	—	0.01	%
-55 to +125 °C	—	—	0.02	%
<b>Sample Mode Offset, +25 °C</b>				
0 to +70 °C	—	±5	±30	mV
-55 to +125 °C	—	±25	±35	mV
<b>Pedestal, 25 °C</b>				
0 to +70 °C	—	±5	±15	mV
-55 to +125 °C	—	—	±20	mV
<b>Gain, +25 °C</b>				
Gain Error, +25 °C	—	—	±2	%
0 to +70 °C	—	—	±2.25	%
-55 to +125 °C	—	—	±2.25	%
<b>Aperture Delay, +25 °C</b>				
0 to +70 °C	—	5	10	nSec.
-55 to +125 °C	—	10	20	nSec.
<b>Aperture Jitter, +25 °C</b>				
0 to +70 °C	—	1	3	pS
-55 to +125 °C	—	2	6	pS
<b>Slew Rate</b>				
Full Power BW, ±1.5V	—	190	250	V/µSec.
Small Signal Bandwidth	20	25	—	MHz
<b>Harmonic Distortion</b>				
±1V, DC to 5 MHz	100	50	—	MHz
±1V, 5 to 10 MHz, +25 °C	-70	-74	—	dB
0 to +70 °C	-60	-70	—	dB
-55 to +125 °C	-50	—	—	dB
Acq Time 0.01%, ±1V, +25 °C ①	-50	—	—	dB
0 to +70 °C	—	25	35	nSec.
-55 to +125 °C	—	—	35	nSec.
Acq Time 0.1%, ±1V, +25 °C ①	—	—	45	nSec.
0 to +70 °C	—	15	25	nSec.
-55 to +125 °C	—	—	35	nSec.
<b>Hold Mode Settling,</b>				
0.01%, +25 °C	—	20	30	nSec.
0 to +70 °C	—	—	50	nSec.
-55 to +125 °C	—	—	50	nSec.

PERFORMANCE, CONT.	MIN	TYP	MAX	UNITS
<b>Hold Mode Settling,</b>				
0.1%, +25 °C	—	—	30	nSec.
0 to +70 °C	—	—	35	nSec.
-55 to +125 °C	—	—	35	nSec.
Output Noise, Hold Mode	—	50	100	µV rms
Feedthrough Rejection 2V Step	-76	-80	—	dB
<b>Droop Rate, +25 °C</b>				
0 to +70 °C	—	1	5	µV/µS
-55 to +125 °C	—	25	50	µV/µS

**POWER SUPPLY REQUIREMENTS**

Range	MIN	TYP	MAX	UNITS
<b>Analog +5V</b>				
Analog +5V	+4.75	+5.0	+5.25	Vdc
Digital +5V	+4.75	+5.0	+5.25	Vdc
-5V	-4.75	-5.0	-5.25	Vdc
+15V	+14.25	+15.0	+15.75	Vdc
<b>Current Usage</b>				
Analog +5V	—	+38	+45	mA
Digital +5V	—	+1.0	+50	mA
-5V	—	-47	-50	mA
+15V	—	8	12	mA
Power Dissipation	—	545	655	mW
Power Supply Rejection Ratio	-52	-60	—	dB

**ENVIRONMENTAL**

<b>Operating Temp. Range</b>				
-MC, ambient	0	—	+70	°C
-MM, case	-55	—	+125	°C
<b>Storage Temp. Range</b>				
	-65	—	+150	°C
Package Type	14-Pin metal DIP			

① Murata Power Solutions (DATEL) uses the conservative definition of Acquisition time, which includes the Aperture Delay time.

**Absolute Maximum Ratings**

PARAMETERS	LIMITS	UNITS
+15V supply (pin 12)	-0.5 to +18	Vdc
+5V supply (pin 4, 14)	-0.5 to +7	Vdc
-5V supply (pin 13)	+0.5 to -7	Vdc
Analog input (pin 1)	+5V Supply +1 -5V Supply -1	Vdc Vdc
Digital inputs (pins 5, 6)	-0.5 to +7	Vdc
Lead temperature (10 sec.)	300	°C
Short circuit to ground	70	mA
Output shorted to any supply will cause permanent damage.		

**TECHNICAL NOTES**

- Bypass the ±5V analog, +5V digital, +15V supplies with a 1µF, 25V tantalum capacitor in parallel with a 0.01 µF ceramic capacitor mounted as close to the pin as possible.  
To achieve optimum performance-
- Additional bypass capacitors are necessary, because of internal high switching speeds, and high slew rates of internal components. REF BYPASS (pin 2), +5 BYPASS (pin 9), and -5 BYPASS (pin 10) are internal connections that must be bypassed with a minimum 1µF tantalum capacitor mounted as close to the pin as possible. The polarity of the connections are shown on the test circuit drawing, Figure 2.
- As with all high speed analog circuits, it is essential that good grounding techniques be used. Tie all ground pins together at a single ground point beneath the device, and use a short low impedance run to the ground of the analog power supplies. The ground point should be a solid ground plane under the device and any associated data converter.
- The offset, pedestal, and gain errors of the SHM-43 are laser trimmed at Murata Power Solutions (DATEL) and no external compensation capabilities have been provided. This prevents introducing noise through the offset adjust terminals of the S/H amplifier and guarantees excellent gain linearity, offset drift, and pedestal performance.

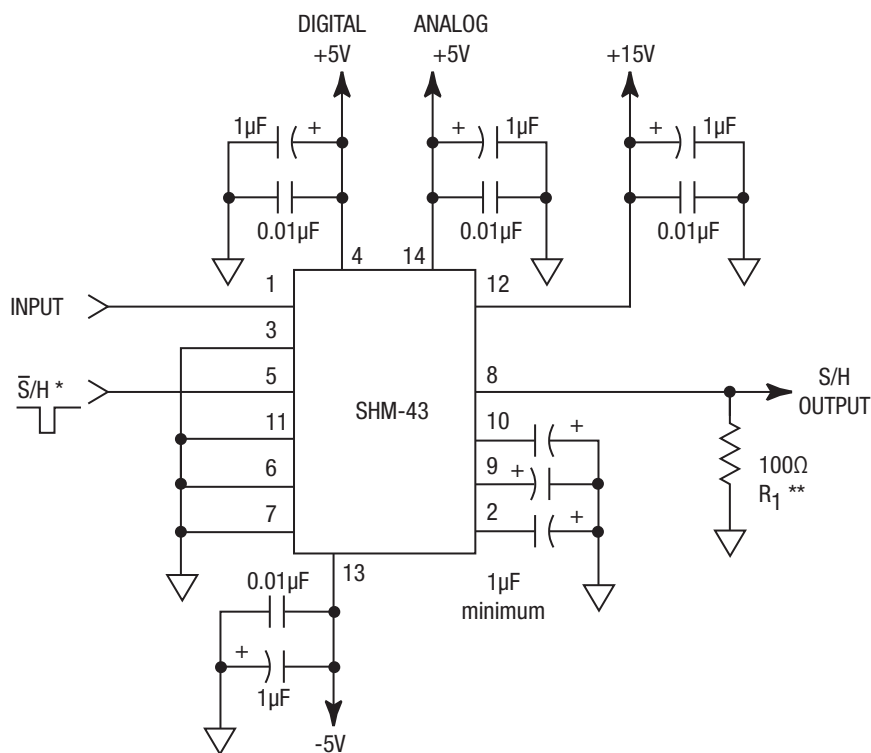


Figure 2. Test Circuit Connections

\* Connections shown for  $\bar{S}/H$ ; if opposite polarity sample hold command is desired, connect S/H CONTROL (pin 6) to DIGITAL +5V (pin 4). Using the opposite polarity S/H command will not effect speed or accuracy.

\*\* The SHM-43 MS been optimized for driving 100Ω loads. R1 should be chosen so that the total load on the S/H is 100Ω.

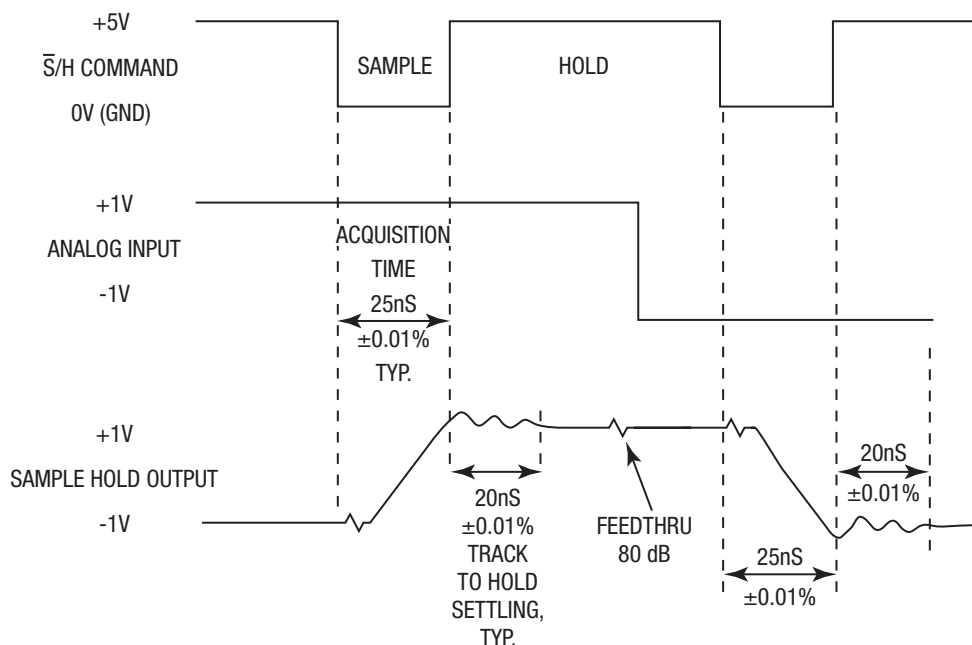


Figure 3. Test Method for Circuit Shown In Figure 2

