512 Kbit (64K x8) Page-Write EEPROM
SST29EE512

Data Sheet

FEATURES:

- **Single Voltage Read and Write Operations**
  - 4.5-5.5V for SST29EE512
- **Superior Reliability**
  - Endurance: 100,000 Cycles (typical)
  - Greater than 100 years Data Retention
- **Low Power Consumption**
  - Active Current: 20 mA (typical)
  - Standby Current: 10 µA (typical)
- **Fast Page-Write Operation**
  - 128 Bytes per Page, 512 Pages
  - Page-Write Cycle: 5 ms (typical)
  - Complete Memory Rewrite: 2.5 sec (typical)
  - Effective Byte-Write Cycle Time: 39 µs (typical)
- **Fast Read Access Time**
  - 4.5-5.5V operation: 70 ns
- **Latched Address and Data**
- **Automatic Write Timing**
  - Internal V_{PP} Generation
- **End of Write Detection**
  - Toggle Bit
  - Data# Polling
- **Hardware and Software Data Protection**
- **Product Identification can be accessed via Software Operation**
- **TTL I/O Compatibility**
- **JEDEC Standard**
  - Flash EEPROM Pinouts and command sets
- **Packages Available**
  - 32-lead PLCC
  - 32-lead TSOP (8mm x 20mm)
  - 32-pin PDIP
- **All non-Pb (lead-free) devices are RoHS compliant**

PRODUCT DESCRIPTION

The SST29EE512 is a 64K x8 CMOS, Page-Write EEPROM manufactured with SST's proprietary, high-performance CMOS SuperFlash technology. The split-gate cell design and thick-oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The SST29EE512 writes with a single power supply. Internal Erase/Program is transparent to the user. The SST29EE512 conforms to JEDEC standard pin assignments for byte-wide memories.

Featuring high performance Page-Write, the SST29EE512 provides a typical Byte-Write time of 39 µsec. The entire memory, i.e., 64 KByte, can be written page-by-page in as little as 2.5 seconds, when using interface features such as Toggle Bit or Data# Polling to indicate the completion of a Write cycle. To protect against inadvertent write, the SST29EE512 have on-chip hardware and Software Data Protection schemes. Designed, manufactured, and tested for a wide spectrum of applications, the SST29EE512 is offered with a guaranteed Page-Write endurance of 10,000 cycles. Data retention is rated at greater than 100 years.

The SST29EE512 is suited for applications that require convenient and economical updating of program, configuration, or data memory. For all system applications, the SST29EE512 significantly improves performance and reliability, while lowering power consumption. The SST29EE512 improves flexibility while lowering the cost for program, data, and configuration storage applications.

To meet high density, surface mount requirements, the SST29EE512 is offered in 32-lead PLCC and 32-lead TSOP packages. A 600-mil, 32-pin PDIP package is also available. See Figures 1, 2, and 3 for pin assignments.

Device Operation

The SST Page-Write EEPROM offers in-circuit electrical write capability. The SST29EE512 does not require separate Erase and Program operations. The internally timed Write cycle executes both erase and program transparently to the user. The SST29EE512 has industry standard optional Software Data Protection, which SST recommends always to be enabled. The SST29EE512 is compatible with industry standard EEPROM pinouts and functionality.

Read

The Read operations of the SST29EE512 is controlled by CE# and OE#, both have to be low for the system to obtain data from the outputs. CE# is used for device selection. When CE# is high, the chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either CE# or OE# is high. Refer to the Read cycle timing diagram for further details (Figure 4).

Write

The Page-Write to the SST29EE512 should always use the JEDEC Standard Software Data Protection (SDP) three-byte command sequence. The SST29EE512 contains the optional JEDEC approved Software Data Protection scheme. SST recommends that SDP always be enabled, thus, the description of the Write operations will be given using the SDP enabled format. **The three-byte SDP Enable and SDP Write commands are identical; therefore, any time a SDP Write command is issued, Software Data Protection is automatically assured.** The first time the three-byte SDP command is given, the device becomes SDP enabled. Subsequent issuance of the same command bypasses the data protection for the page being written. At the end of the desired Page-Write, the entire device remains protected. For additional descriptions, please see the application notes *The Proper Use of JEDEC Standard Software Data Protection* and *Protecting Against Unintentional Writes When Using Single Power Supply Flash Memories*.

The Write operation consists of three steps. Step 1 is the three-byte load sequence for Software Data Protection. Step 2 is the byte-load cycle to a page buffer of the SST29EE512. Steps 1 and 2 use the same timing for both operations. Step 3 is an internally controlled Write cycle for writing the data loaded in the page buffer into the memory array for nonvolatile storage. During both the SDP three-byte load sequence and the byte-load cycle, the addresses are latched by the falling edge of either CE# or WE#, whichever occurs last. The data is latched by the rising edge of either CE# or WE#, whichever occurs first. The internal Write cycle is initiated by the T_{BLCO} timer after the rising edge of WE# or CE#, whichever occurs first. The Write cycle, once initiated, will continue to completion, typically within 5 ms. See Figures 5 and 6 for WE# and CE# controlled Page-Write cycle timing diagrams and Figures 15 and 17 for flowcharts.

The Write operation has three functional cycles: the Software Data Protection load sequence, the page-load cycle, and the internal Write cycle. The Software Data Protection consists of a specific three-byte load sequence that allows writing to the selected page and will leave the SST29EE512 protected at the end of the Page-Write. The page-load cycle consists of loading 1 to 128 Bytes of data into the page buffer. The internal Write cycle consists of the T_{BLCO} time-out and the write timer operation. During the Write operation, the only valid reads are Data# Polling and Toggle Bit.

The Page-Write operation allows the loading of up to 128 Bytes of data into the page buffer of the SST29EE512 before the initiation of the internal Write cycle. During the internal Write cycle, all the data in the page buffer is written simultaneously into the memory array. Hence, the Page-Write feature of SST29EE512 allows the entire memory to be written in as little as 2.5 seconds. During the internal Write cycle, the host is free to perform additional tasks, such as to fetch data from other locations in the system to set up the write to the next page. In each Page-Write operation, all the bytes that are loaded into the page buffer must have the same page address, i.e. A_7 through A_{16}. Any byte not loaded with user data will be written to FFH.

See Figures 5 and 6 for the Page-Write cycle timing diagrams. If after the completion of the three-byte SDP load sequence or the initial byte-load cycle, the host loads a second byte into the page buffer within a byte-load cycle time (T_{BLC}) of 100 µs, the SST29EE512 will stay in the page-load cycle. Additional bytes are then loaded consecutively. The page-load cycle will be terminated if no additional byte is loaded into the page buffer within 200 µs (T_{BLCO}) from the last byte-load cycle, i.e., no subsequent WE# or CE# high-to-low transition after the last rising edge of WE# or CE#. Data in the page buffer can be changed by a subsequent byte-load cycle. The page-load period can continue indefinitely, as long as the host continues to load the device within the byte-load cycle time of 100 µs. The page to be loaded is determined by the page address of the last byte loaded.

Software Chip-Erase

The SST29EE512 provides a Chip-Erase operation, which allows the user to simultaneously clear the entire memory array to the “1” state. This is useful when the entire device must be quickly erased.

The Software Chip-Erase operation is initiated by using a specific six-byte load sequence. After the load sequence, the device enters into an internally timed cycle similar to the Write cycle. During the Erase operation, the only valid read is Toggle Bit. See Table 4 for the load sequence, Figure 10 for timing diagram, and Figure 19 for the flowchart.

Write Operation Status Detection

The SST29EE512 provides two software means to detect the completion of a Write cycle, in order to optimize the system Write cycle time. The software detection includes two status bits: Data# Polling (DQ_7) and Toggle Bit (DQ_6). The end of write detection mode is enabled after the rising WE# or CE# whichever occurs first, which initiates the internal Write cycle.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the Write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either DQ_7 or DQ_6. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the Write cycle, otherwise the rejection is valid.

Data# Polling (DQ_7)

When the SST29EE512 is in the internal Write cycle, any attempt to read DQ_7 of the last byte loaded during the byte-load cycle will receive the complement of the true data. Once the Write cycle is completed, DQ_7 will show true data. Note that even though DQ_7 may have valid data immediately following the completion of an internal Write operation, the remaining data outputs may still be invalid: valid data on the entire data bus will appear in subsequent successive Read cycles after an interval of 1 µs. See Figure 7 for Data# Polling timing diagram and Figure 16 for a flowchart.

Toggle Bit (DQ_6)

During the internal Write cycle, any consecutive attempts to read DQ_6 will produce alternating ‘0’s and ‘1’s, i.e., toggling between 0 and 1. When the Write cycle is completed, the toggling will stop. The device is then ready for the next operation. See Figure 8 for Toggle Bit timing diagram and Figure 16 for a flowchart. The initial read of the Toggle Bit will typically be a “1”.

Data Protection

The SST29EE512 provide both hardware and software features to protect nonvolatile data from inadvertent writes.

Hardware Data Protection

Noise/Glitch Protection: A WE# or CE# pulse of less than 5 ns will not initiate a Write cycle.

V_{DD} Power Up/Down Detection: The Write operation is inhibited when V_{DD} is less than 2.5V.

Write Inhibit Mode: Forcing OE# low, CE# high, or WE# high will inhibit the Write operation. This prevents inadvertent writes during power-up or power-down.

Software Data Protection (SDP)

The SST29EE512 provides the JEDEC approved optional Software Data Protection scheme for all data alteration operations, i.e., Write and Chip-Erase. With this scheme, any Write operation requires the inclusion of a series of three byte-load operations to precede the data loading operation. The three-byte load sequence is used to initiate the Write cycle, providing optimal protection from inadvertent Write operations, e.g., during the system power-up or power-down. The SST29EE512 is shipped with the Software Data Protection disabled.

The software protection scheme can be enabled by applying a three-byte sequence to the device, during a page-load cycle (Figures 5 and 6). The device will then be automatically set into the data protect mode. Any subsequent Write operation will require the preceding three-byte sequence. See Table 4 for the specific software command codes and Figures 5 and 6 for the timing diagrams. To set the device into the unprotected mode, a six-byte sequence is required. See Table 4 for the specific codes and Figure 9 for the timing diagram. If a Write is attempted while SDP is enabled the device will be in a non-accessible state for ~ 300 µs. SST recommends Software Data Protection always be enabled. See Figure 17 for flowcharts.

The SST29EE512 Software Data Protection is a global command, protecting (or unprotecting) all pages in the entire memory array once enabled (or disabled). Therefore using SDP for a single Page-Write will enable SDP for the entire array. Single pages by themselves cannot be SDP enabled or disabled, although the page addressed during the SDP write will be written.

Single power supply reprogrammable nonvolatile memories may be unintentionally altered. SST strongly recommends that Software Data Protection (SDP) always be enabled. The SST29EE512 should be programmed using the SDP command sequence. SST recommends the SDP Disable Command Sequence not be issued to the device prior to writing.

Please refer to the following Application Notes for more information on using SDP:

- *Protecting Against Unintentional Writes When Using Single Power Supply Flash Memories*
- *The Proper Use of JEDEC Standard Software Data Protection*

Product Identification

The Product Identification mode identifies the device as the SST29EE512 and manufacturer as SST. This mode is accessed via software. For details, see Table 4, Figure 11 for the software ID entry, and Read timing diagram and Figure 18 for the ID entry command sequence flowchart.

TABLE 1: PRODUCT IDENTIFICATION

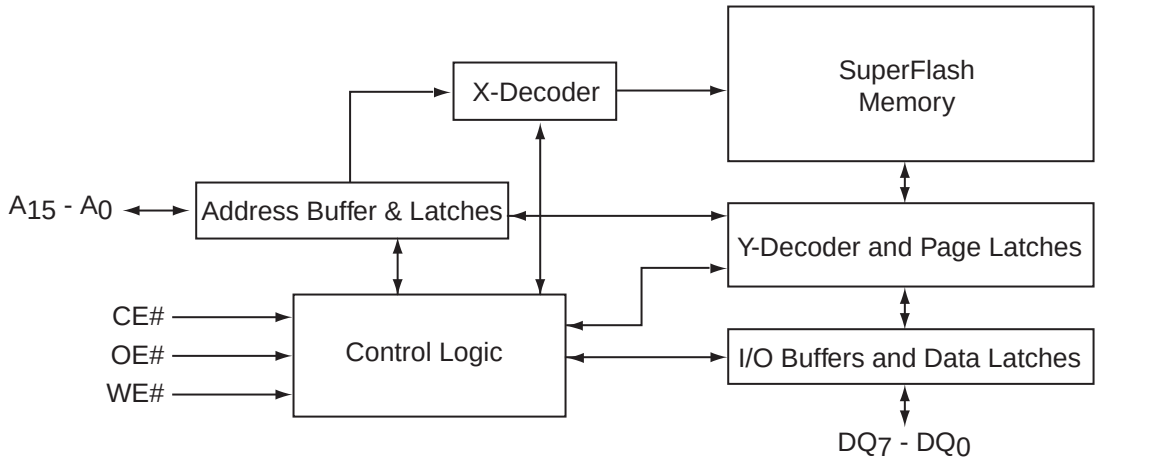
	Address	Data
Manufacturer's ID	0000H	BFH
Device ID		
SST29EE512	0001H	5DH

T1.3 1060

Product Identification Mode Exit

In order to return to the standard Read mode, the Software Product Identification mode must be exited. Exiting is accomplished by issuing the Software ID Exit (reset) operation, which returns the device to the Read operation. The Reset operation may also be used to reset the device to the Read mode after an inadvertent transient condition that apparently causes the device to behave abnormally, e.g., not read correctly. See Table 4 for software command codes, Figure 12 for timing waveform, and Figure 18 for a flowchart.

FUNCTIONAL BLOCK DIAGRAM



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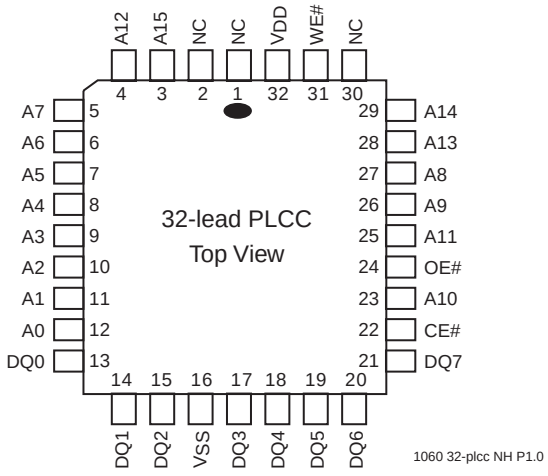


FIGURE 1: PIN ASSIGNMENTS FOR 32-LEAD PLCC

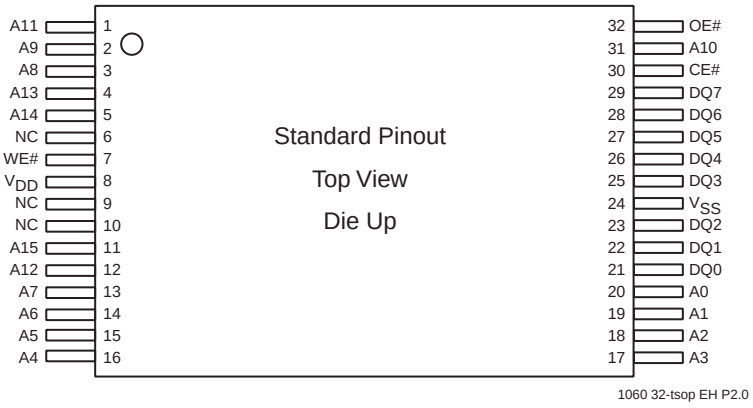


FIGURE 2: PIN ASSIGNMENTS FOR 32-LEAD TSOP

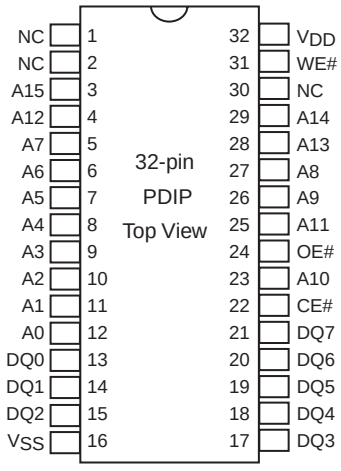


FIGURE 3: PIN ASSIGNMENTS FOR 32-PIN PDIP

TABLE 2: PIN DESCRIPTION

Symbol	Pin Name	Functions
A_{15}-A_7	Row Address Inputs	To provide memory addresses. Row addresses define a page for a Write cycle.
A_6-A_0	Column Address Inputs	Column Addresses are toggled to load page data
DQ_7-DQ_0	Data Input/output	To output data during Read cycles and receive input data during Write cycles. Data is internally latched during a Write cycle. The outputs are in tri-state when OE# or CE# is high.
CE#	Chip Enable	To activate the device when CE# is low.
OE#	Output Enable	To gate the data output buffers.
WE#	Write Enable	To control the Write operations.
V_{DD}	Power Supply	To provide: 5.0V supply (4.5-5.5V) for SST29EE512
V_{SS}	Ground	
NC	No Connection	Unconnected pins.

T2.3 1060

TABLE 3: OPERATION MODES SELECTION

Mode	CE#	OE#	WE#	DQ	Address
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	A_{IN}
Page-Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}	A_{IN}
Standby	V_{IH}	X[1]	X	High Z	X
Write Inhibit	X	V_{IL}	X	High Z/ D_{OUT}	X
	X	X	V_{IH}	High Z/ D_{OUT}	X
Software Chip-Erase	V_{IL}	V_{IH}	V_{IL}	D_{IN}	A_{IN}, See Table 4
Product Identification					
Software Mode	V_{IL}	V_{IH}	V_{IL}	Manufacturer's ID (BFH) Device ID[2]	See Table 4
SDP Enable Mode	V_{IL}	V_{IH}	V_{IL}		See Table 4
SDP Disable Mode	V_{IL}	V_{IH}	V_{IL}		See Table 4

T3.4 1060

1. X can be V_{IL} or V_{IH}, but no other value.
2. Device ID = 5DH for SST29EE512

TABLE 4: SOFTWARE COMMAND SEQUENCE

Command Sequence	1st Bus Write Cycle		2nd Bus Write Cycle		3rd Bus Write Cycle		4th Bus Write Cycle		5th Bus Write Cycle		6th Bus Write Cycle	
	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data
Software Data Protect Enable & Page-Write	5555H	AAH	2AAAH	55H	5555H	A0H	Addr[2]	Data				
Software Chip-Erase[3]	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Software ID Entry[4,5]	5555H	AAH	2AAAH	55H	5555H	90H						
Software ID Exit	5555H	AAH	2AAAH	55H	5555H	F0H						
Alternate Software ID Entry[6]	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	60H

T4.4 1060

1. Address format A_{14}-A_0 (Hex), Address A_{15} can be V_{IL} or V_{IH}, but no other value."
2. Page-Write consists of loading up to 128 Bytes (A_6-A_0)
3. The software Chip-Erase function is not supported by the industrial temperature part. Please contact SST if you require this function for an industrial temperature part.
4. The device does not remain in Software Product ID mode if powered down.
5. With A_{14}-A_1 = 0; SST Manufacturer's ID = BFH, is read with A_0 = 0, SST29EE512 Device ID = 5DH, is read with A_0 = 1
6. Alternate six-byte Software Product ID Command Code

Note: This product supports both the JEDEC standard three-byte command code sequence and SST's original six-byte command code sequence. For new designs, SST recommends that the three-byte command code sequence be used.

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias . . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential . . . . . -0.5V to V_{DD}+0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential . . . . . -2.0V to V_{DD}+2.0V
Voltage on A_9 Pin to Ground Potential . . . . . -0.5V to 14.0V
Package Power Dissipation Capability (T_A = 25°C) 1.0W
Through Hole Lead Soldering Temperature (10 Seconds) . . . . . 300°C
Surface Mount Solder Reflow Temperature[1] . . . . . 260°C for 10 seconds
Output Short Circuit Current[2] . . . . . 100 mA

1. Excluding certain with-Pb 32-PLCC units, all packages are 260°C capable in both non-Pb and with-Pb solder versions. Certain with-Pb 32-PLCC package types are capable of 240°C for 10 seconds; please consult the factory for the latest information.
2. Outputs shorted for no more than one second. No more than one output shorted at a time.

OPERATING RANGE FOR SST29EE512

Range	Ambient Temp	V_{DD}
Commercial	0°C to +70°C	4.5-5.5V
Industrial	-40°C to +85°C	4.5-5.5V

AC CONDITIONS OF TEST

Input Rise/Fall Time . . . . . 10 ns
Output Load . . . . . 1 TTL Gate and C_L = 100 pF
See Figures 13 and 14

TABLE 5: DC OPERATING CHARACTERISTICS V_{DD} = 4.5-5.5V FOR SST29EE512

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
I_{DD}	Power Supply Current				Address input=V_{ILT}/V_{IHT}, at f=1/T_{RC} Min, V_{DD}=V_{DD} Max
	Read		30	mA	CE#=OE#=V_{IL}, WE#=V_{IH}, all I/Os open
	Program and Erase		50	mA	CE#=WE#=V_{IL}, OE#=V_{IH}, V_{DD}=V_{DD} Max
I_{SB1}	Standby V_{DD} Current (TTL input)		3	mA	CE#=OE#=WE#=V_{IH}, V_{DD}=V_{DD} Max
I_{SB2}	Standby V_{DD} Current (CMOS input)		50	µA	CE#=OE#=WE#=V_{DD} -0.3V, V_{DD}=V_{DD} Max
I_{LI}	Input Leakage Current		1	µA	V_{IN}=GND to V_{DD}, V_{DD}=V_{DD} Max
I_{LO}	Output Leakage Current		10	µA	V_{OUT}=GND to V_{DD}, V_{DD}=V_{DD} Max
V_{IL}	Input Low Voltage		0.8	V	V_{DD}=V_{DD} Min
V_{IH}	Input High Voltage	2.0		V	V_{DD}=V_{DD} Max
V_{OL}	Output Low Voltage		0.4	V	I_{OL}=2.1 mA, V_{DD}=V_{DD} Min
V_{OH}	Output High Voltage	2.4		V	I_{OH}=-400 µA, V_{DD}=V_{DD} Min

T5.2 1060

TABLE 6: RECOMMENDED SYSTEM POWER-UP TIMINGS

Symbol	Parameter	Minimum	Units
$T_{PU-READ}$[1]	Power-up to Read Operation	100	µs
$T_{PU-WRITE}$[1]	Power-up to Write Operation	5	ms

T6.0 1060

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 7: CAPACITANCE (T_A = 25°C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$[1]	I/O Pin Capacitance	$V_{I/O}$ = 0V	12 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	6 pF

T7.0 1060

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 8: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}[1]	Endurance	10,000	Cycles	JEDEC Standard A117
T_{DR}[1]	Data Retention	100	Years	JEDEC Standard A103
I_{LTH}[1]	Latch Up	100	mA	JEDEC Standard 78

T8.5 1060

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

AC CHARACTERISTICS

TABLE 9: READ CYCLE TIMING PARAMETERS FOR SST29EE512

Symbol	Parameter	Min	Max	Units
T_{RC}	Read Cycle Time	70		ns
T_{CE}	Chip Enable Access Time		70	ns
T_{AA}	Address Access Time		70	ns
T_{OE}	Output Enable Access Time		30	ns
T_{CLZ}[1]	CE# Low to Active Output	0		ns
T_{OLZ}[1]	OE# Low to Active Output	0		ns
T_{CHZ}[1]	CE# High to High-Z Output		20	ns
T_{OHZ}[1]	OE# High to High-Z Output		20	ns
T_{OH}[1]	Output Hold from Address Change	0		ns

T9.3 1060

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 10: PAGE-WRITE CYCLE TIMING PARAMETERS

Symbol	Parameter	Min	Max	Units
T_{WC}	Write Cycle (Erase and Program)		10	ms
T_{AS}	Address Setup Time	0		ns
T_{AH}	Address Hold Time	50		ns
T_{CS}	WE# and CE# Setup Time	0		ns
T_{CH}	WE# and CE# Hold Time	0		ns
T_{OES}	OE# High Setup Time	0		ns
T_{OEH}	OE# High Hold Time	0		ns
T_{CP}	CE# Pulse Width	70		ns
T_{WP}	WE# Pulse Width	70		ns
T_{DS}	Data Setup Time	35		ns
T_{DH}[1]	Data Hold Time	0		ns
T_{BLC}[1]	Byte Load Cycle Time	0.05	100	µs
T_{BLCO}[1]	Byte Load Cycle Time	200		µs
T_{IDA}[1]	Software ID Access and Exit Time		10	µs
T_{SCE}	Software Chip-Erase		20	ms

T10.6 1060

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

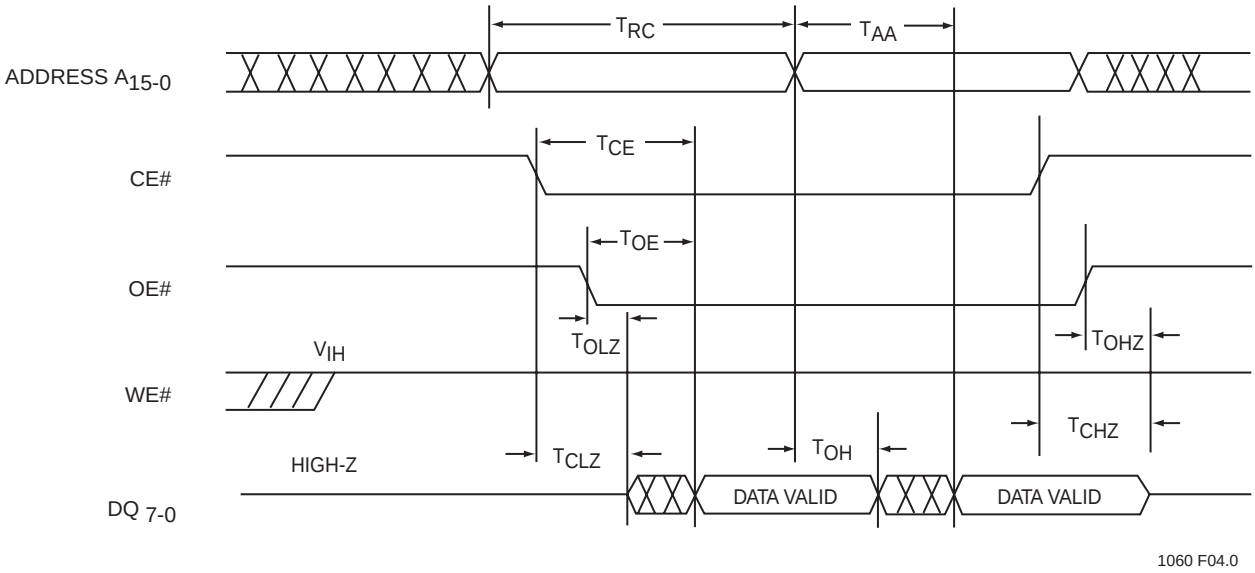


FIGURE 4: READ CYCLE TIMING DIAGRAM

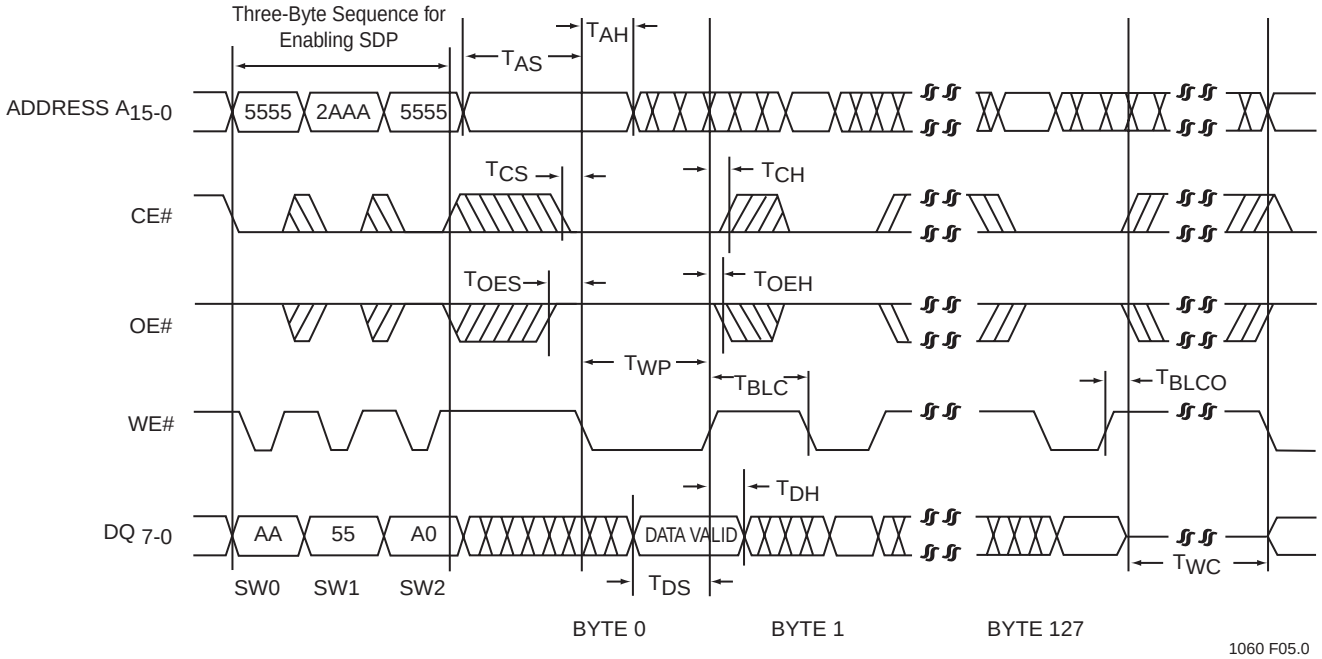


FIGURE 5: WE# CONTROLLED PAGE-WRITE CYCLE TIMING DIAGRAM

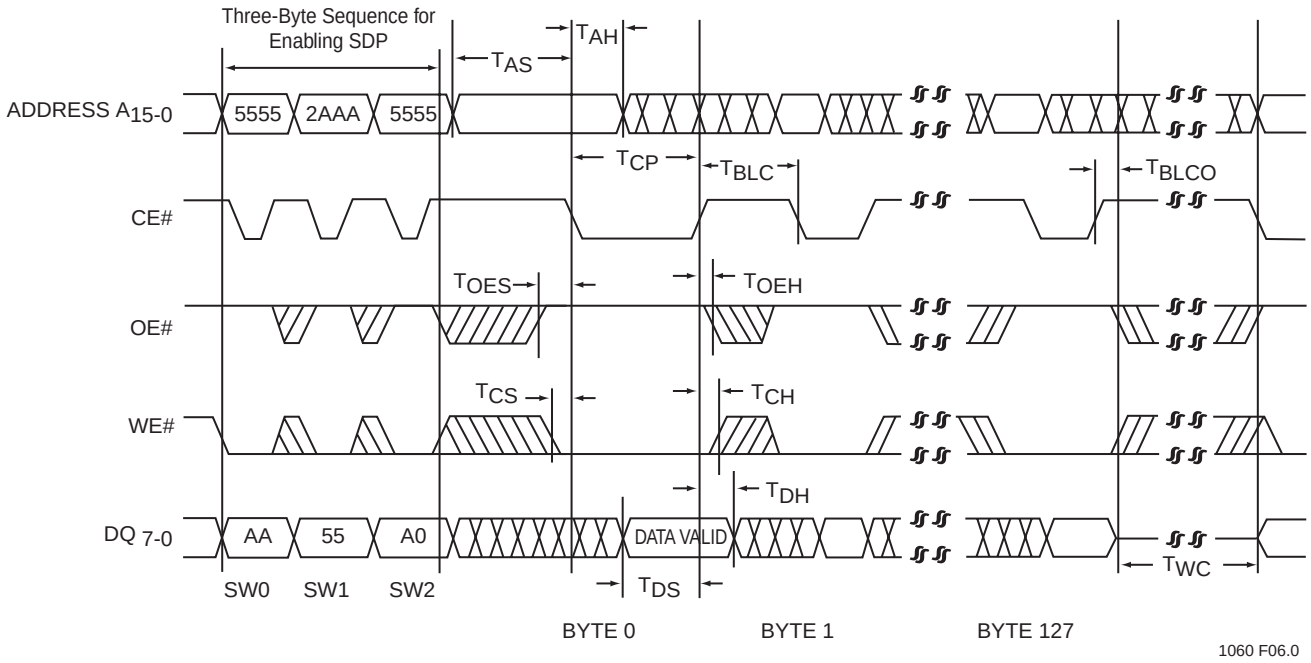


FIGURE 6: CE# CONTROLLED PAGE-WRITE CYCLE TIMING DIAGRAM

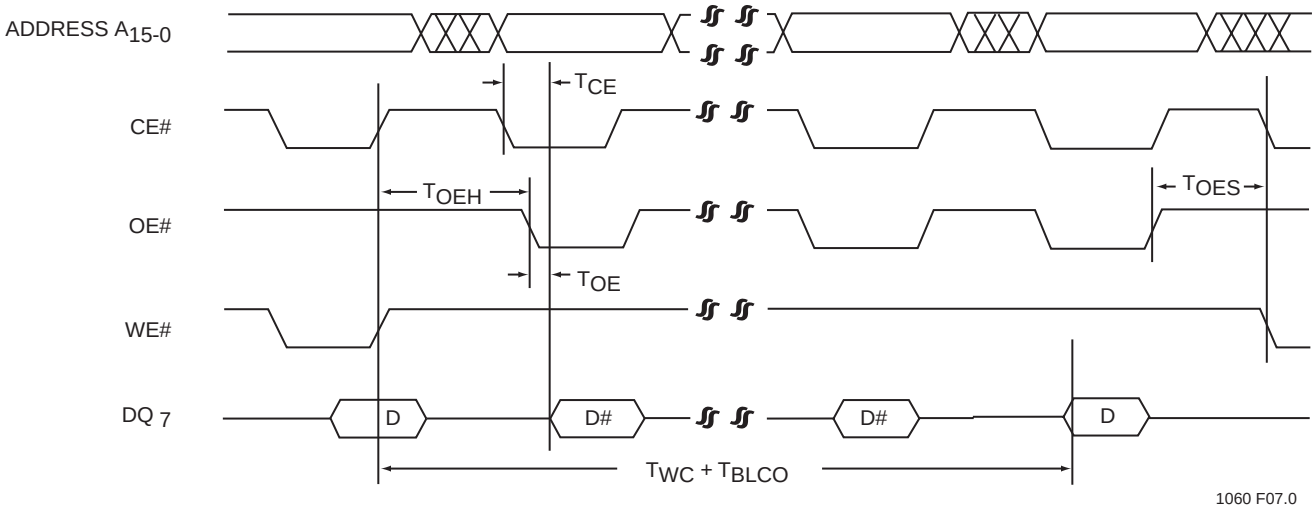


FIGURE 7: DATA# POLLING TIMING DIAGRAM

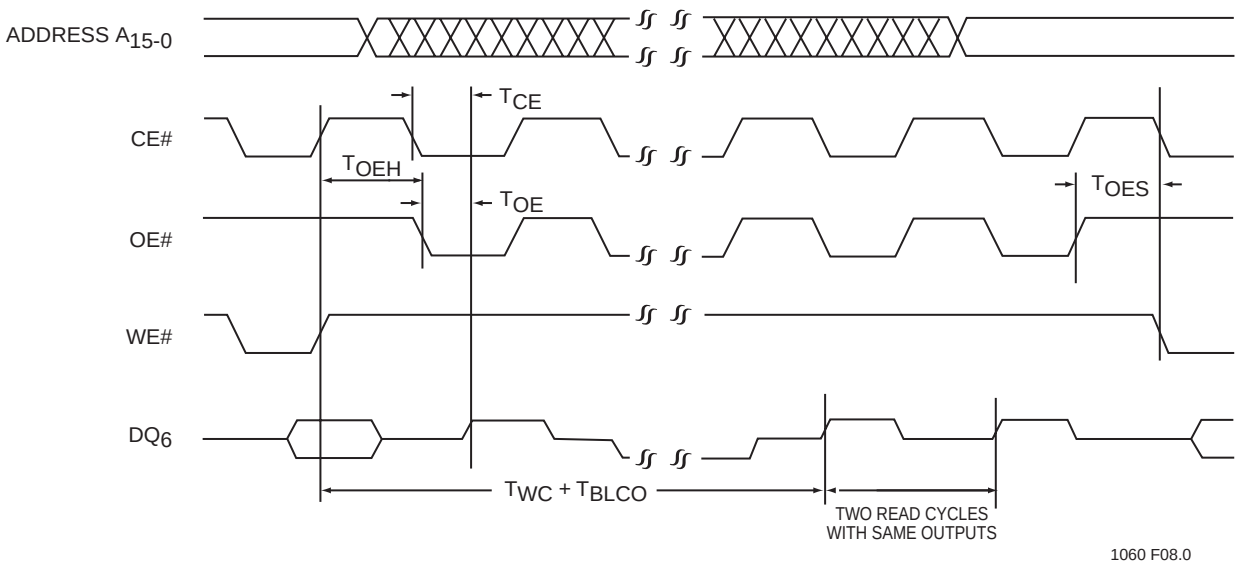


FIGURE 8: TOGGLE BIT TIMING DIAGRAM

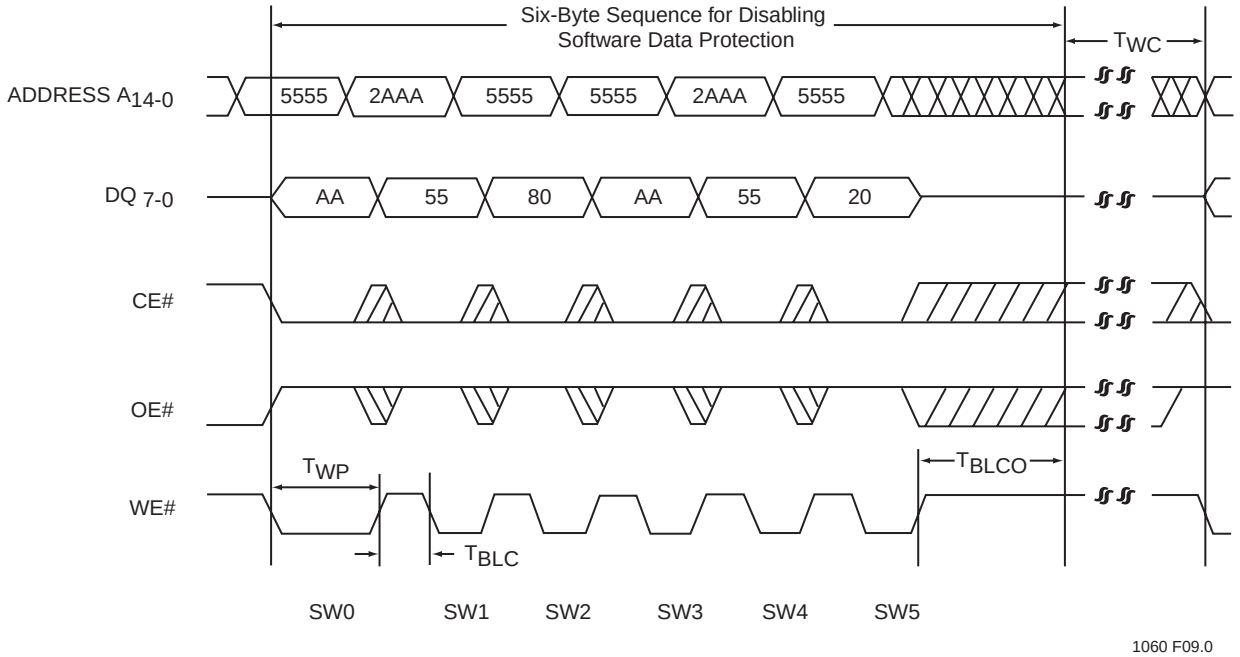


FIGURE 9: SOFTWARE DATA PROTECT DISABLE TIMING DIAGRAM

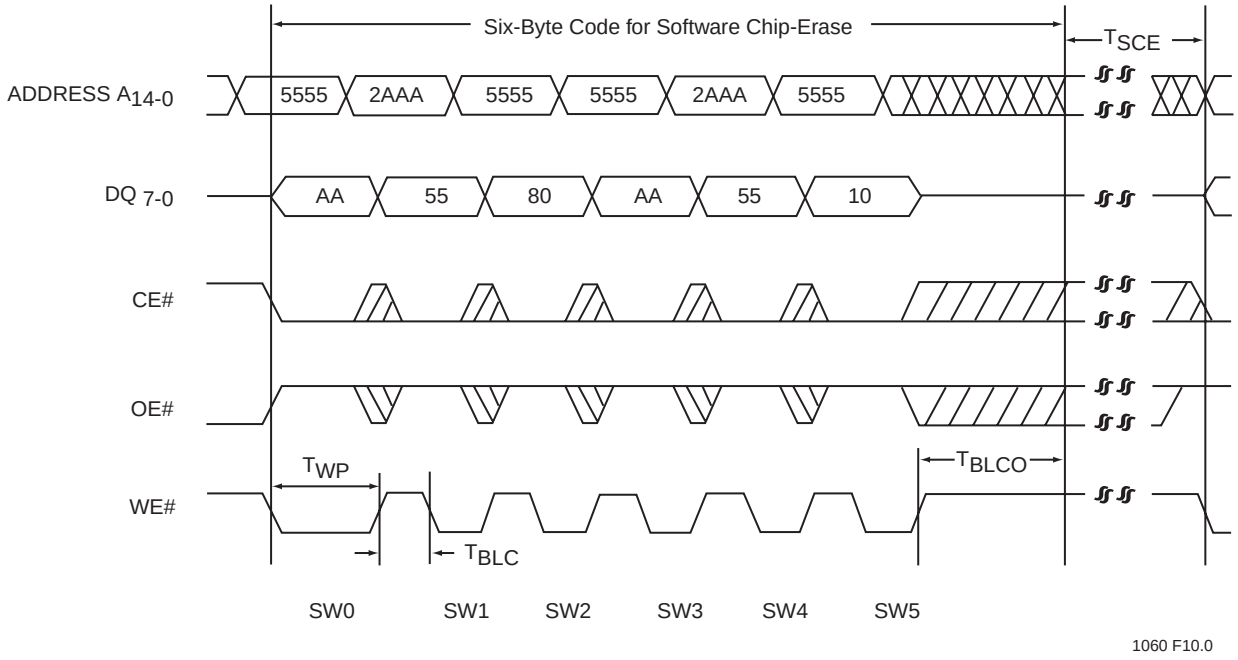


FIGURE 10: SOFTWARE CHIP-ERASE TIMING DIAGRAM

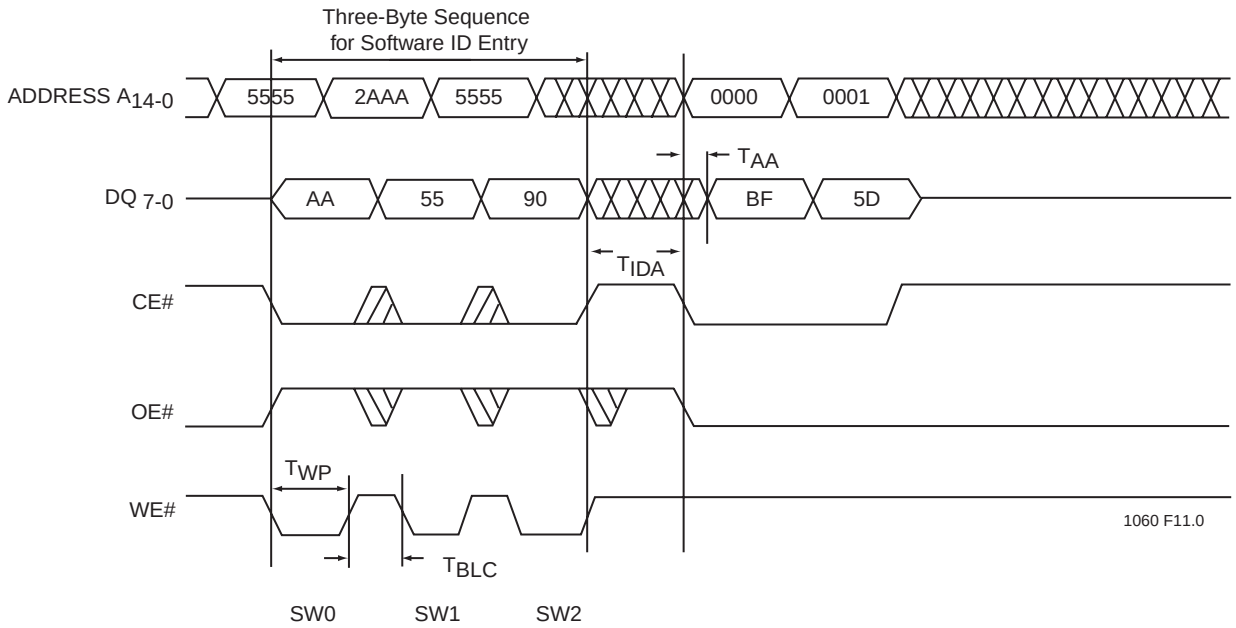


FIGURE 11: SOFTWARE ID ENTRY AND READ

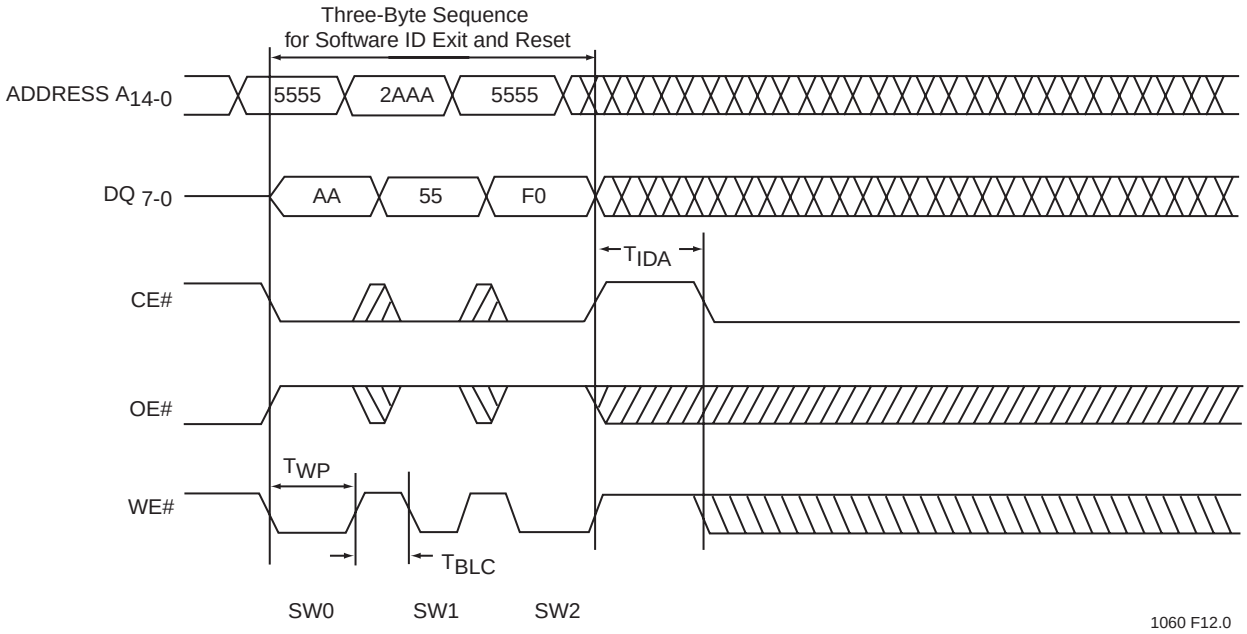
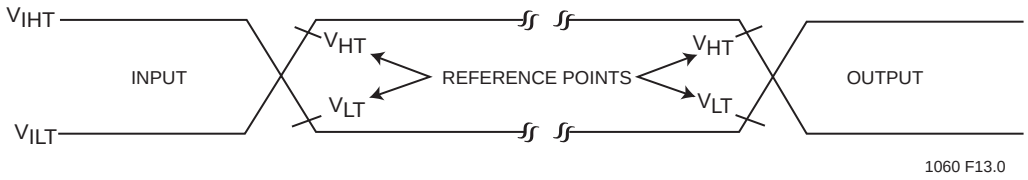


FIGURE 12: SOFTWARE ID EXIT AND RESET



AC test inputs are driven at V_{IHT} (2.4V) for a logic "1" and V_{ILT} (0.4 V) for a logic "0". Measurement reference points for inputs and outputs are V_{HT} (2.0 V) and V_{LT} (0.8 V). Input rise and fall times (10% ↔ 90%) are <10 ns.

Note: V_{HT} - V_{HIGH} Test
V_{LT} - V_{LOW} Test
V_{IHT} - V_{INPUT} HIGH Test
V_{ILT} - V_{INPUT} LOW Test

FIGURE 13: AC INPUT/OUTPUT REFERENCE WAVEFORMS

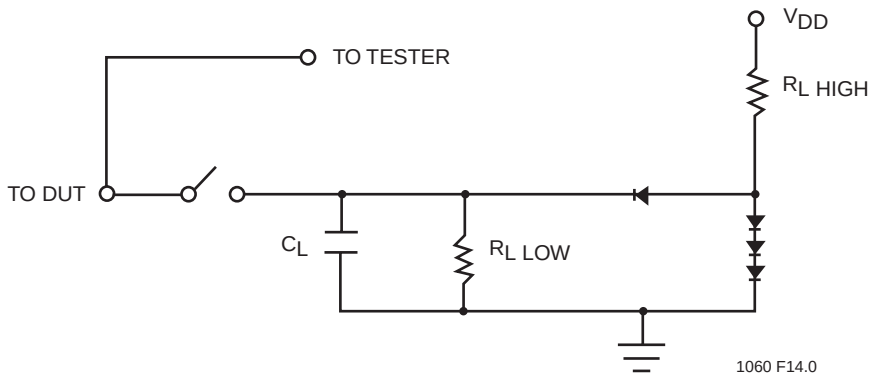


FIGURE 14: A TEST LOAD EXAMPLE

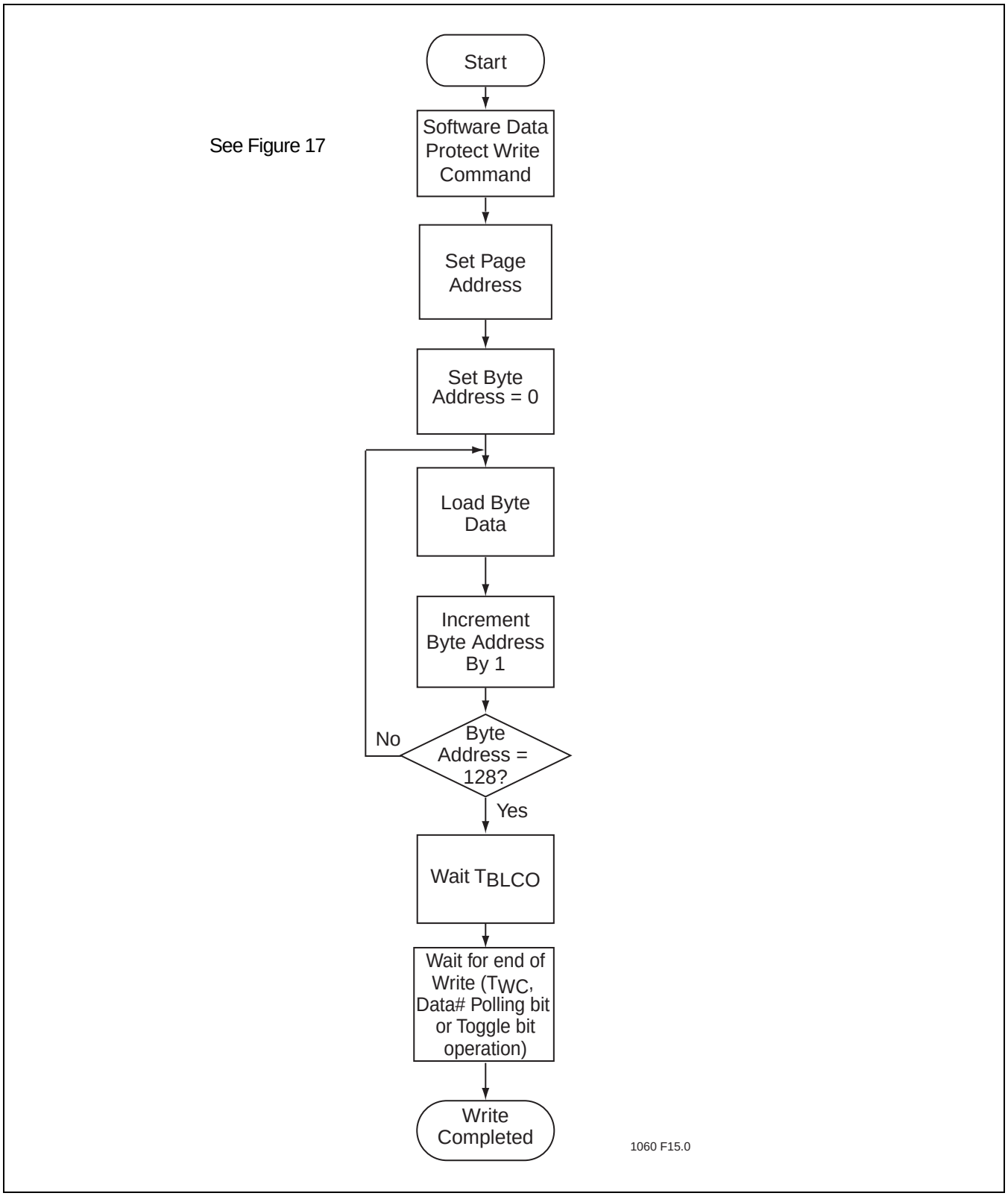


FIGURE 15: WRITE ALGORITHM

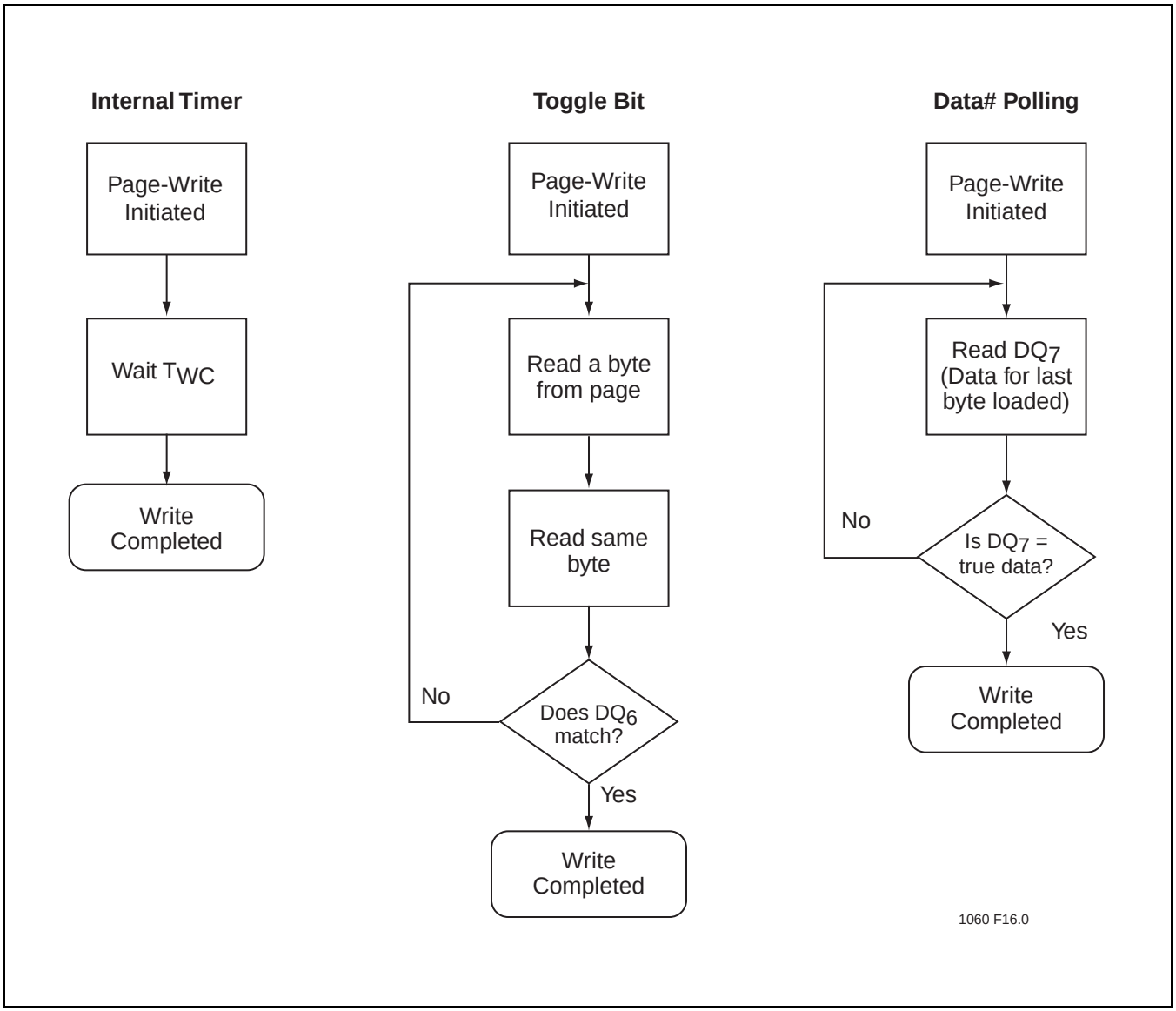


FIGURE 16: WAIT OPTIONS

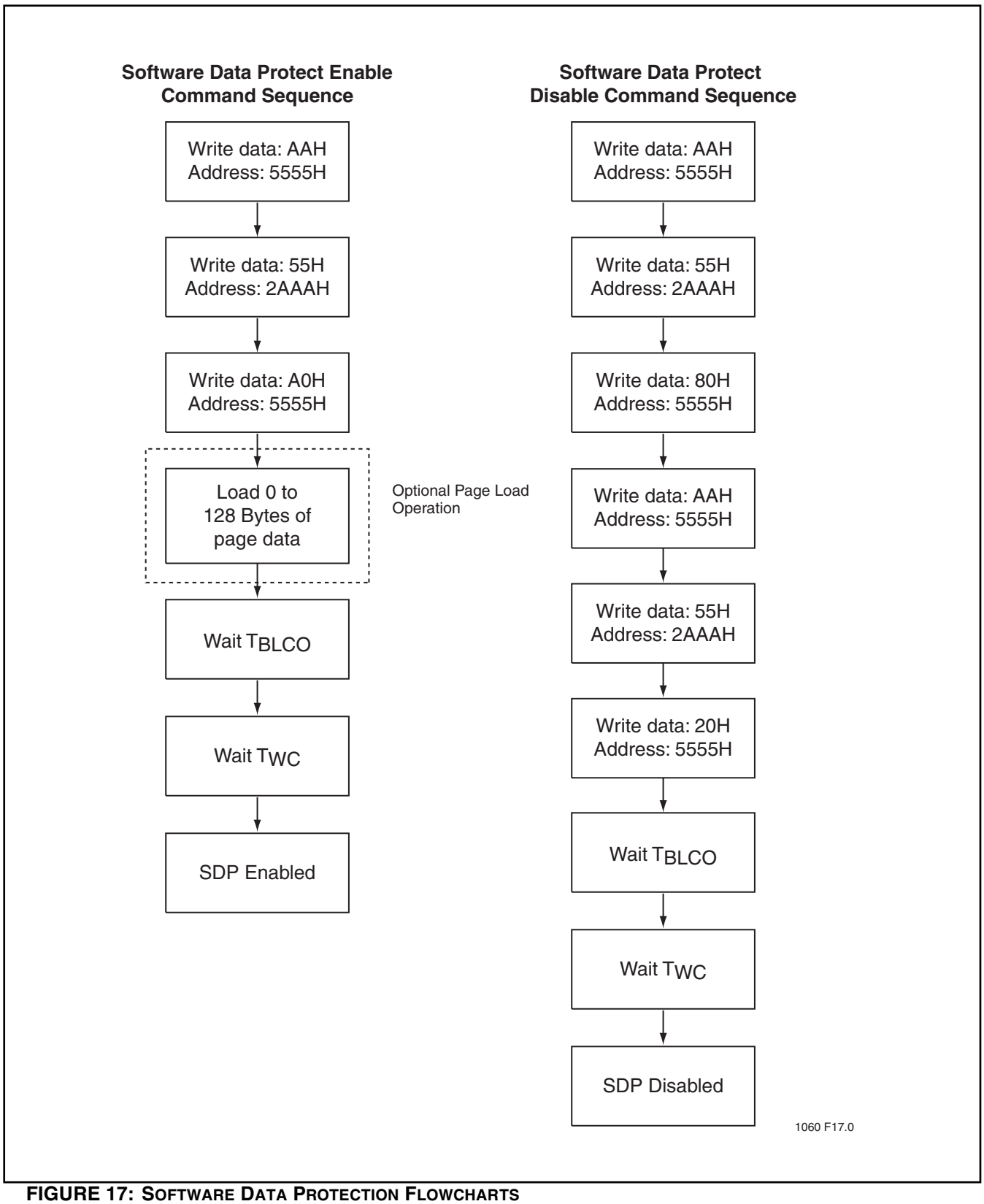


FIGURE 17: SOFTWARE DATA PROTECTION FLOWCHARTS

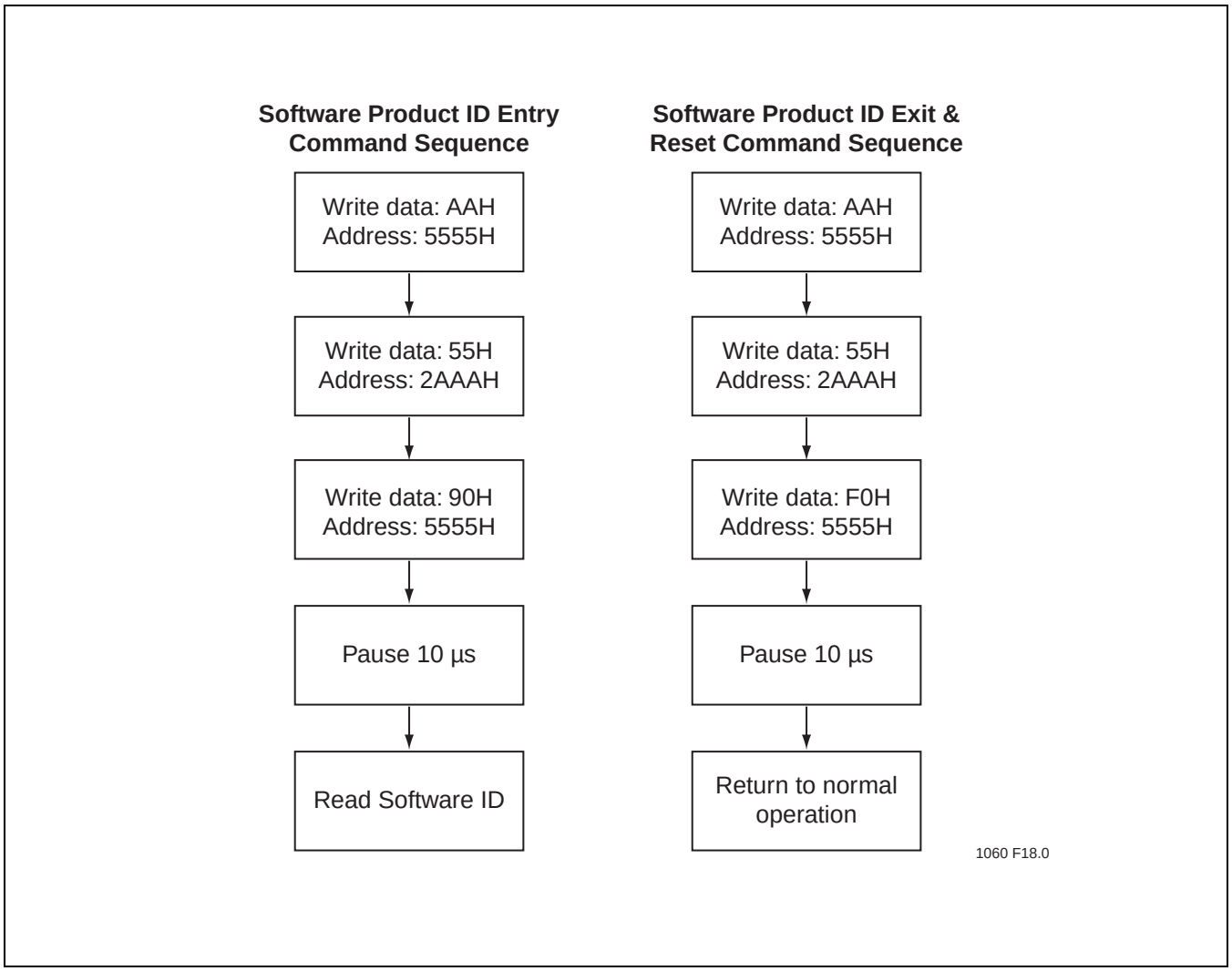


FIGURE 18: SOFTWARE PRODUCT COMMAND FLOWCHARTS

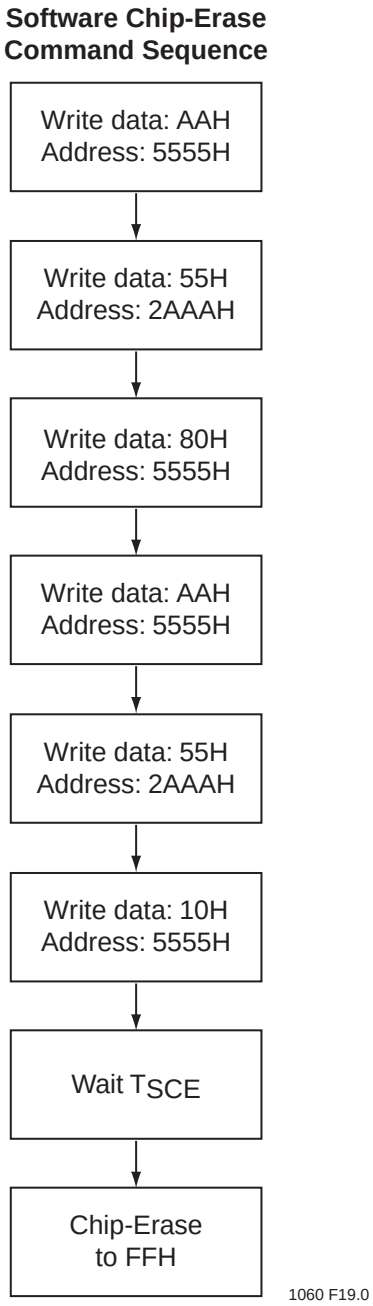
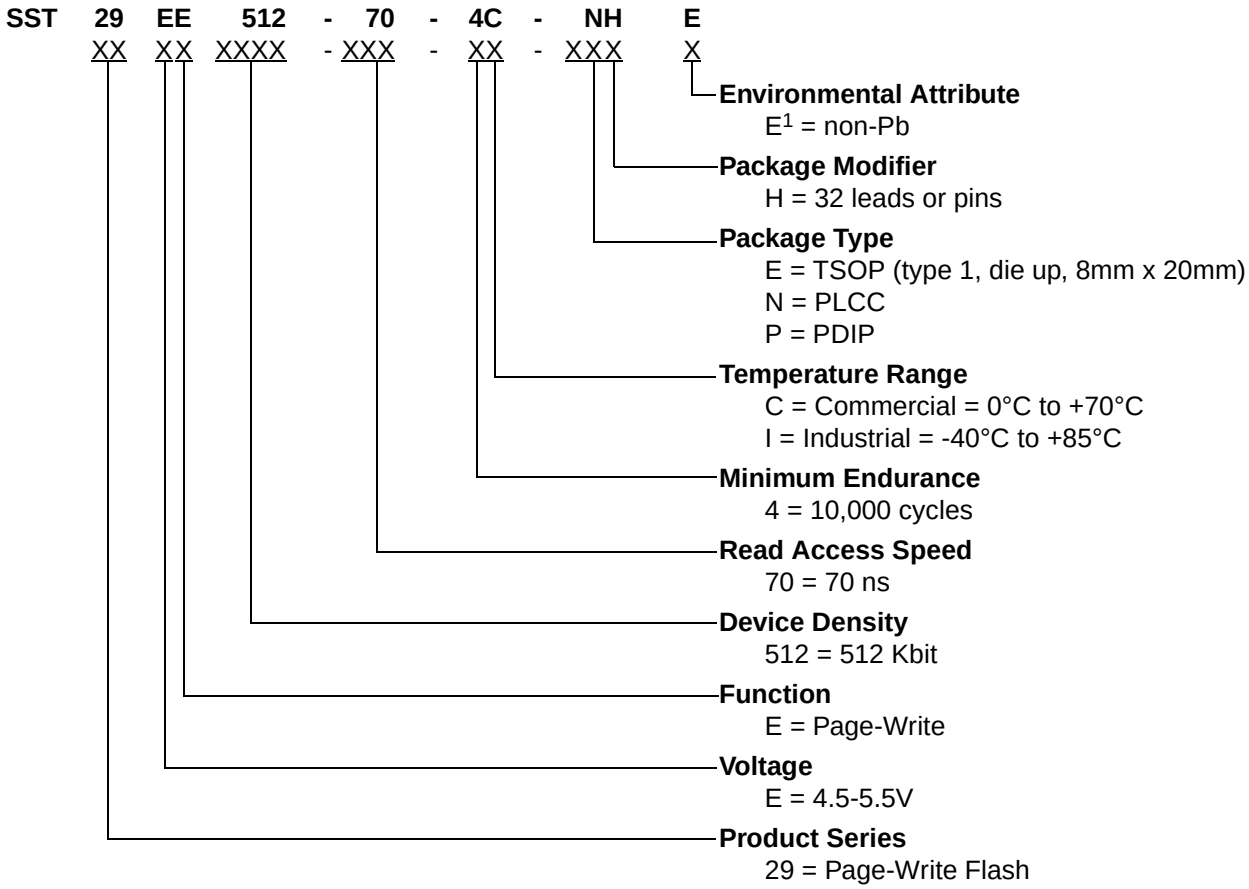


FIGURE 19: SOFTWARE CHIP-ERASE COMMAND CODES

PRODUCT ORDERING INFORMATION



1. Environmental suffix “E” denotes non-Pb solder.
SST non-Pb solder devices are “RoHS Compliant”.

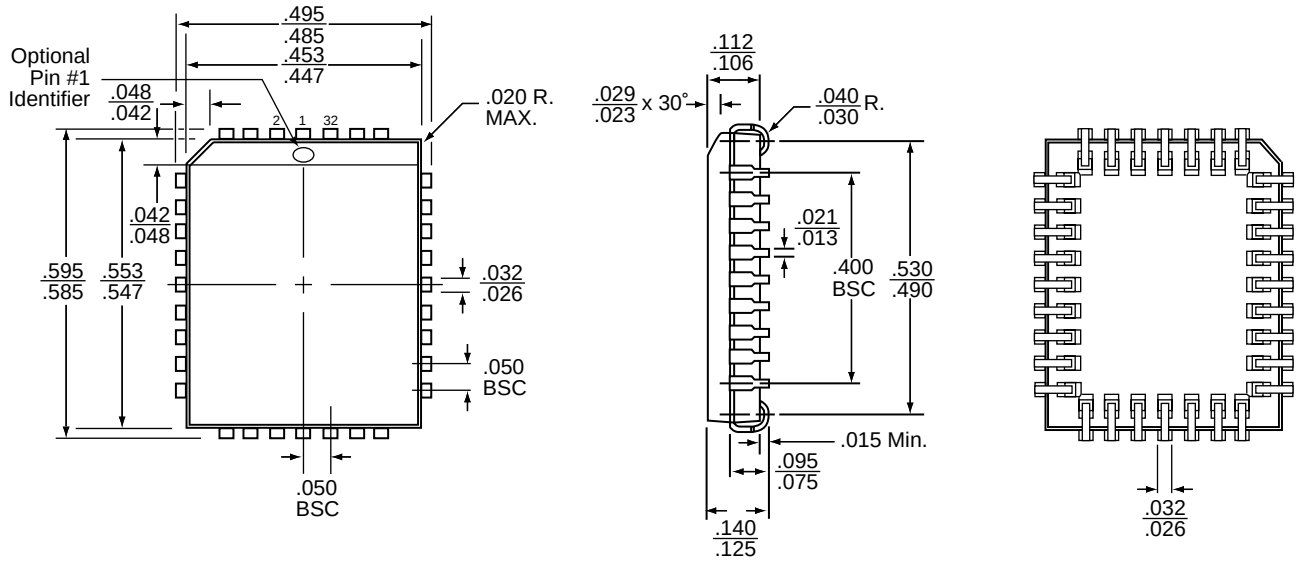
Valid combinations for SST29EE512

SST29EE512-70-4C-NH	SST29EE512-70-4C-EH	SST29EE512-70-4C-PH
SST29EE512-70-4C-NHE	SST29EE512-70-4C-EHE	
SST29EE512-70-4I-NH	SST29EE512-70-4I-EH	
SST29EE512-70-4I-NHE	SST29EE512-70-4I-EHE	

Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Note: The software Chip-Erase function is not supported by the industrial temperature part.
Please contact SST if this function is required in an industrial temperature part.

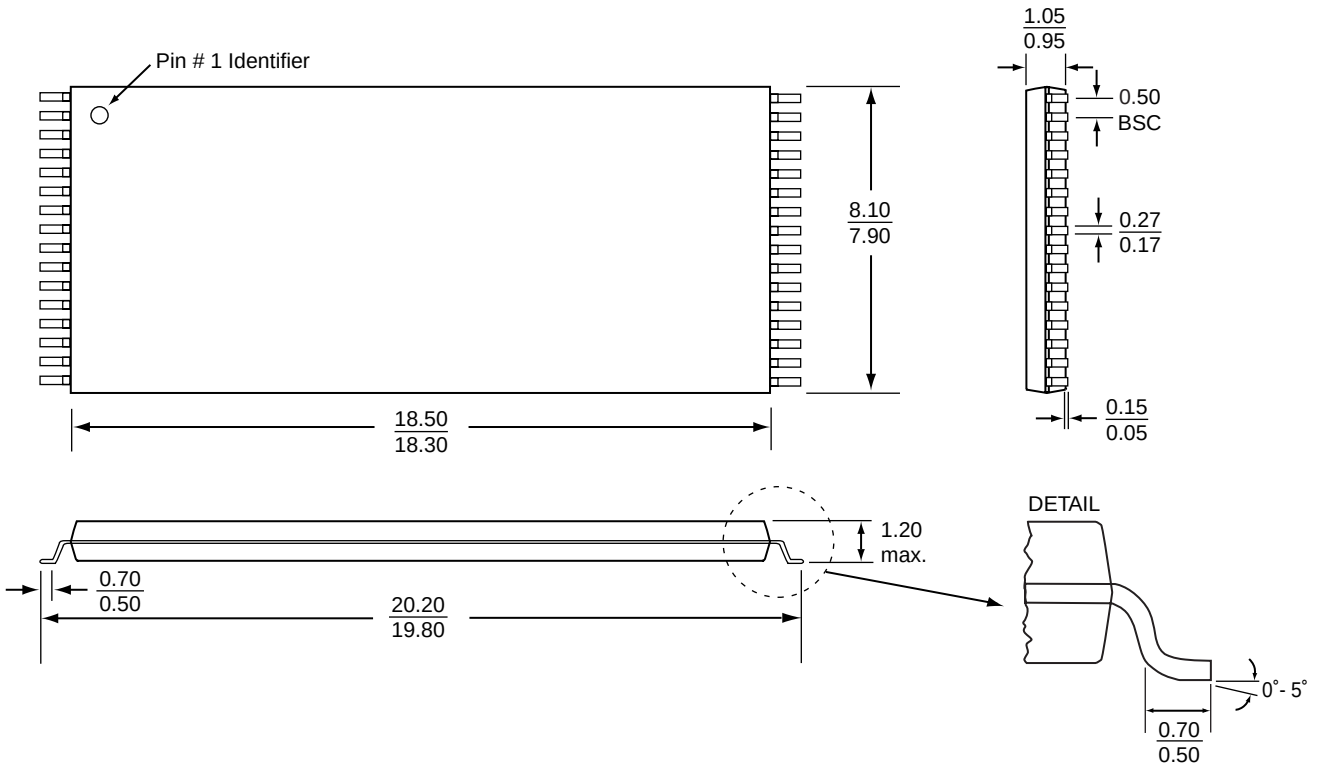
PACKAGING DIAGRAMS



Note: 1. Complies with JEDEC publication 95 MS-016 AE dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in inches (max/min).
3. Dimensions do not include mold flash. Maximum allowable mold flash is .008 inches.
4. Coplanarity: 4 mils.

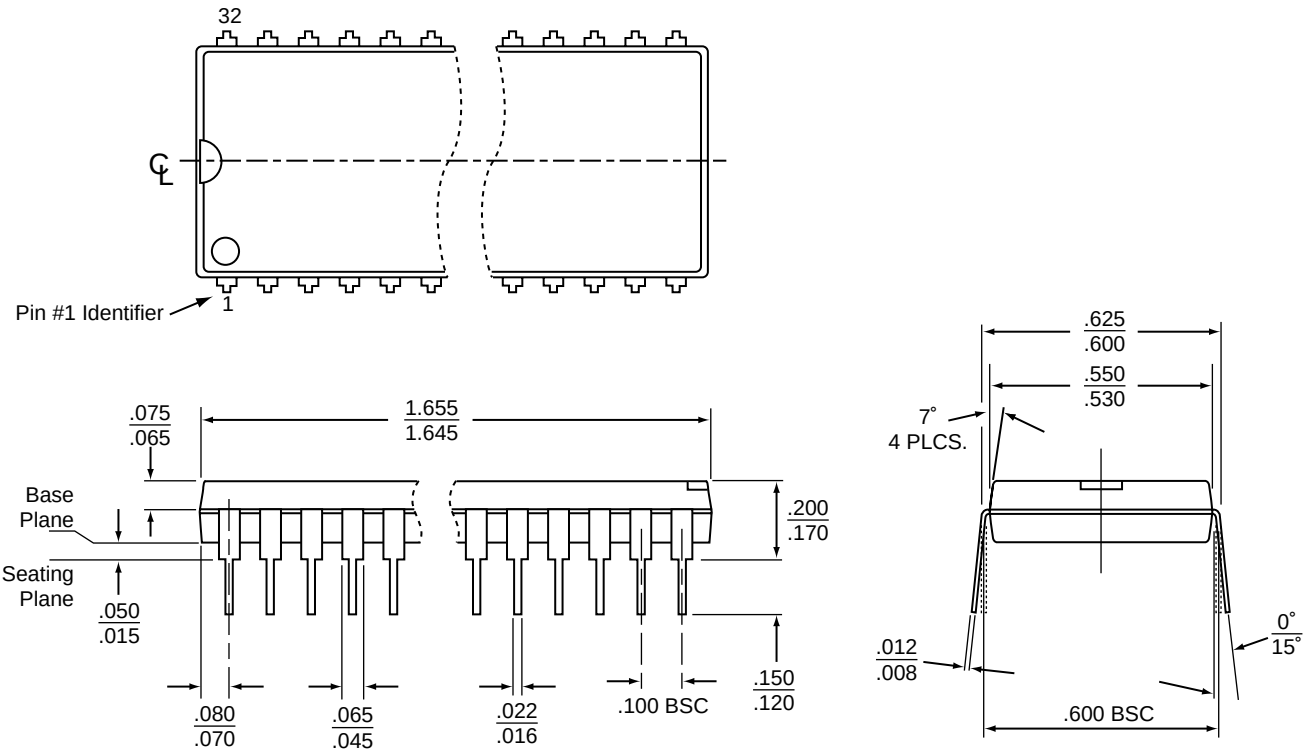
32-plcc-NH-3

32-LEAD PLASTIC LEAD CHIP CARRIER (PLCC)
SST PACKAGE CODE: NH



Note: 1. Complies with JEDEC publication 95 MO-142 BD dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in millimeters (max/min).
3. Coplanarity: 0.1 mm
4. Maximum allowable mold flash is 0.15 mm at the package ends, and 0.25mm between leads.

32-LEAD THIN SMALL OUTLINE PACKAGE (TSOP) 8MM X 20MM
SST PACKAGE CODE: EH



Note: 1. Complies with JEDEC publication 95 MO-015 AP dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in inches (max/min).
3. Dimensions do not include mold flash. Maximum allowable mold flash is .010 inches.

32-pdip-PH-3

32-PIN PLASTIC DUAL IN-LINE PINS (PDIP)
SST PACKAGE CODE: PH

Data Sheet

TABLE 11: REVISION HISTORY

Number	Description	Date
06	• 2002 Data Book	May 2002
07	• WH package is no longer offered • Removed the SST29EE512 90 ns Read Access Time • Removed the SST29LE512 200 ns Read Access Time • Removed the SST29VE512 250 ns Read Access Time • Clarified I_{DD} Write to be Program and Erase in Table 6 on page 9	Mar 2003
08	• 2004 Data Book • Added non-Pb MPNs and removed footnote (See page 22)	Nov 2003
09	• Removed 2.7V and 3V devices and associated MPNs refer to EOL Product Data Sheet S71060(01). • Added RoHS compliance information on page 1 and in the "Product Ordering Information" on page 22 • Clarified the Solder Temperature Profile under "Absolute Maximum Stress Ratings" on page 8	Sep 2005