M51285BFP

NTSC/PAL ENCODER

DESCRIPTION

The M51285BFP is a semiconductor integrated circuit developed for PIP (picture in picture), digital special playback etc. The circuit, formed on the 42 pin plastic flat package, encodes R-Y, B-Y color signals and luminance signals into video signals, and is usable both in NTSC and PAL systems.

FEATURES

- Low power dissipation (supply voltage: 5V; circuit current: 35mA Typ.)
- Applicable to NTSC and PAL systems
- Chroma level of sub display screen tracks the burst level of main display screen.
- No need to adjust carrier balance
- 4fsc VCXO is adopted for accurate modulation axle.
- Killer level can be set from outside.
- Internal carrier can be modulated with FREE RUN mode.
- Pedestals of main and sub display screens agree.
- Usable for a variety of special playback signal processing patterns

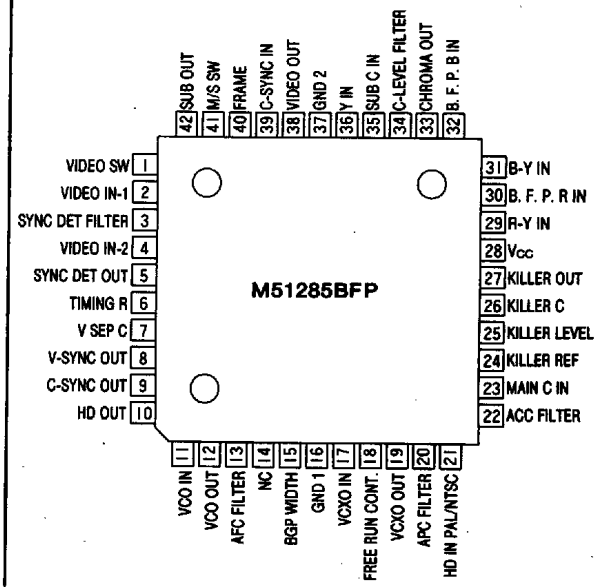
APPLICATION

NTSC/PAL SYSTEM VCR,TV

RECOMMENDED OPERATING CONDITION

Rated supply voltage 5.0V
Supply voltage range ..... 4.5~5.5V

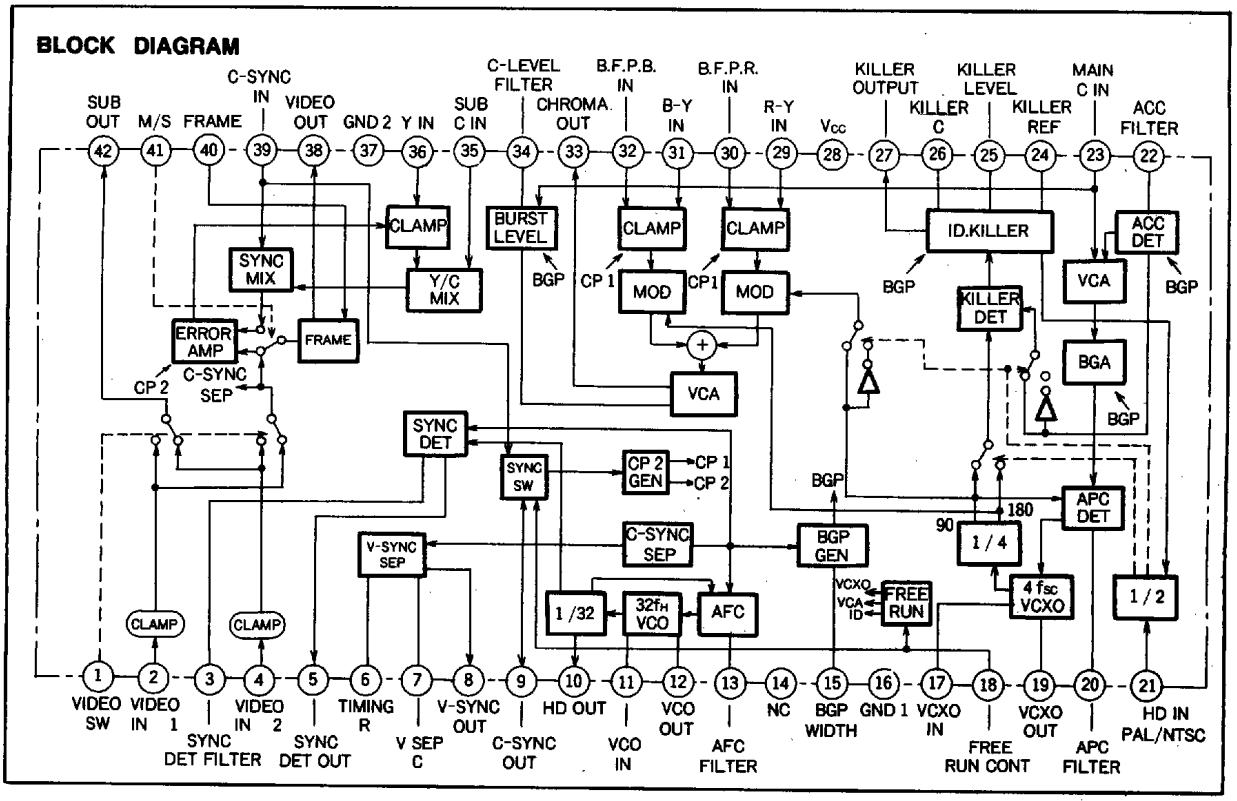
PIN CONFGURATION (TOP VIEW)



Outline 42P6-B

NC : No connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	5.5	V
Pd	Power dissipation	560	mW
K_θ	Thermal derating	5.6	mW/℃
Topr	Operating temperature	−20∼75	℃
Tstg	Storage temperature	−40∼125	℃

ELECTRICAL CHARACTERISTICS (Ta=25℃, unless otherwise noted)

Input/output Pin Characteristics

Input/Output	Input/output type	Measuring item		Limits			Unit
				Min.	Typ.	Max.	
IN	NPN open base	Input current		0	0.8	1.6	μA
IN	NPN emitter follower (SYNC clamp input)	Bias current		10	20	30	μA
IN	NPN emitter follower (SYNC clamp input)	Bias current		10	20	30	μA
OUT	NPN collector (with pull-up resistor)	Pull-up resistance		30	39	50	kΩ
OUT	NPN emitter follower (with bias resistor)	Bias resistance		15	20	25	kΩ
OUT	NPN emitter follower (with bias resistor)	Bias resistance		12	15	18	kΩ
OUT	NPN emitter follower (with bias resistor)	Bias resistance		12	15	18	kΩ
IN	Resistor	Resistance		2.4	3.3	4.2	kΩ
OUT	NPN emitter follower	Bias current		320	460	600	μA
IN	Resistor	Resistance		3.7	5.0	6.3	kΩ
IN	PNP open base (with input limiter)	Input current	V_{IB}>3.0V	−1.0		0	μA
			V_{IB}<2.0V	−100		0	μA
OUT	NPN emitter follower	Bias current		0.8	1.0	1.8	mA
IN	NPN open base	Input current		0	0.8	1.6	μA
IN	Resistor	Resistance		7	10	13	kΩ
IN	NPN open base	Input current		0		1.0	μA
OUT	NPN follower (with bias resistor)	Bias resistance		36	51	66	kΩ
IN	NPN open base (pedestal clamp input)	Input current		−100	0	100	nA
IN	NPN open base	Input current		0		1.0	μA
IN	NPN open base (pedestal clamp input)	Input current		−100	0	100	nA
IN	NPN open base	Input current		0		1.0	μA
OUT	NPN emitter follower	Bias current		385	550	715	μA
IN	Resistor	Resistance		7	10	13	kΩ
IN	NPN open base (pedestal clamp input)	Input current		0	0.8	2.0	μA
OUT	NPN emitter follower	Bias current		385	550	715	μA
IN	NPN open base	Input current		0		3.0	μA
IN	NPN open base	Input current		0		1.6	μA
IN	NPN open base	Input current		0		1.6	μA
OUT	NPN emitter follower	Bias current		385	550	715	μA

AFC

Symbol	Parameter	Input pin	Test pin	Test conditions		Limits Min.	Limits Typ.	Limits Max.	Unit
$V_{SDETMIN}$	SYNC separation (signal) minimum input level	②	⑨	SG1 SYNC length variable, 15.734kHz		150			mV_{P-P}
td-CSYNC	C-SYNC output delay (leading edge)	②	⑨	SG1 SYNC length 280mV_{P-P}, 15.734kHz		400	800	1200	nsec
W-CSYNC	C-SYNC output pulse width	②	⑨	SG1 SYNC length 280mV_{P-P}, 15.734kHz		4.0	5.0	6.0	μsec
$V_{H-CSYNC}$	C-SYNC output "H" voltage	②	⑨	SG1 SYNC length 280mV_{P-P}, 15.734kHz		3.6	4.0		V
tdf-V	V-SYNC output delay (leading edge)	②	⑨	SG1 SYNC length 280mV_{P-P}, 15.734kHz		5	10	15	μsec
tdb-V	V-SYNC output delay (trailing edge)	②	⑨	SG1 SYNC length 280mV_{P-P}, 15.734kHz		0	2	5	μsec
V_{H-V}	V-SYNC output "H" voltage	②	⑧	SG1 SYNC length 280mV_{P-P}, 15.734kHz		3.6	4.0		V
td-HD	HD pulse output delay (leading edge)	②	⑩	SG1 SYNC length 280mV_{P-P}, 15.734kHz		1.5	2.0	2.5	μsec
W-HD	HD pulse width	②	⑩	SG1 SYNC length 280mV_{P-P}, 15.734kHz		3.6	4.0	4.2	μsec
V_{H-HD}	HD output "H" voltage	②	⑩	SG1 SYNC length 280mV_{P-P}, 15.734kHz		3.6	4.0		V
AFC-1	AFC pull-in range (positive side)	②	⑤		NTSC	500	750		Hz
					PAL	500	800		
AFC-2	AFC pull-in range (negative side)	②	⑤		NTSC	500	1000		Hz
					PAL	500	1000		
V_{H-SDET}	SYNC DET output "H" voltage	—	⑤	SG1 No signal		4.5			V
V_{L-SDET}	SYNC DET output "L" voltage	②	⑤	SG1 SYNC length 280mV_{P-P}, 15.734kHz AFC locked				0.5	V

PLL

Symbol	Parameter	Input pin	Test pin	Test conditions		Limits Min.	Limits Typ.	Limits Max.	Unit
$V_{LCK-MIN}$	APC lock minimum input burst level	②㉓	㉗	Pin ② SYNC length 280 mV_{P-P}, 15.724kHz Pin ㉓ Burst level on the decrease.		50			mV_{P-P}
APC-1	APC pull-in range (positive side)	②㉓	㉗		NTSC	200	500		Hz
					PAL	200	500		
APC-2	APC pull-in range (negative side)	②㉓	㉗		NTSC	300	800		Hz
					PAL	300	800		
V_{KILLER}	Killer sensitivity	②㉓	㉗		NTSC	−35	−30	−25	dB
					PAL	−32	−27	−22	
V_{H-KILL}	Killer output "H" voltage	—	㉗	SG4 burst 0mV_{P-P}		3.8	4.2		V
V_{L-KILL}	Killer output "L" voltage	②㉓	㉗	SG4 burst 140mV_{P-P}			0	0.5	V
fo	VCXO free running frequency	—	⑲	SW2 (Side 2)	NTSC	3.56	3.58	3.60	MHz
					PAL	4.41	4.43	4.45	MHz
V_{TH-HD}	HD IN threshold voltage	㉑				1.0	1.8	2.6	V
V_{TH-HP}	NTSC/PAL threshold voltage	㉑				3.0	3.8	4.6	V

MOD

Symbol	Parameter	Input pin	Test pin	Test conditions		Limits Min.	Limits Typ.	Limits Max.	Unit
G_{MOD}	Modulation gain	②	㉙ ㉛	TP33	$G_{MOD} = \frac{Vo\ (V_{P-P})}{0.5\ (V_{P-P})}$	R-Y	0.7	1.0	1.3	—
						B-Y	0.7	1.0	1.3	
A_{BF-MOD}	Burst modulation gain		㉚ ㉜	TP33		R-Y	0.1	0.25	0.4	V_{P-P}
						B-Y	0.1	0.25	0.4	
D_{MOD}	Maximum input color difference amplitude		㉙ ㉛	TP33		R-Y	0.4	0.7		V_{P-P}
						B-Y	0.4	0.7		
LK_{MOD}	Carrier leak		—	TP33	SW2 (side 2)			20	40	mV_{P-P}
TR	Chroma tracking		㉓	TP33			1.5	2	2.5	—
O_{MOD}	Modulation angle			TP33	Difference between R-Y modulation angle and B-Y modulation angle		80	90	100	deg.

$$G_{MOD} = \frac{\text{Chroma output amplitude TP } ㉝}{\text{Color difference input amplitude } ㉙ \text{ or } ㉛}$$

$$TR = \frac{\text{Chroma output (parent burst = 280 mV}_{P-P})}{\text{Chroma output (parent burst = 140 mV}_{P-P})}$$

Y/C MIX, Video SW

Symbol	Parameter	Input pin	Test pin	Test conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
dV_{SYNC}	Video clamp SYNC contraction	②	②	SG1 SYNC 280mV_{P-P}		10	30	mV
G_{VSUB}	SUB amplifier gain	②	㊷		7	8.3	9.5	dB
G_{VMAIN}	MAIN amplifier gain	②	㊳		4	5.5	7	dB
V_{FRAME}	Frame pulse output	②㊵	㊳	Pin ② SG1 280mV_{P-P}	550	600	650	mV_{P-P}
V_{SYNC}	SYNC output level	②	㊳	Pin ② SG1 280mV_{P-P}	500	550	600	mV_{P-P}
G_{VMIX}	Y/C MIX amplifier gain	②㉟㊱	㊴	Pin ② SG1 280mV_{P-P}	10	12	14	dB
D_{YMIX}	Y input D range	②㊱	㊴	Pin ② SG1 280mV_{P-P} V_{CC}, SW9, 12 ON Pin ㊶	400	450		V_{P-P}
D_{CMIX}	C input D range	②㉟	㊴	Pin ② SG1, Pin㊶, 280mV_{P-P} V_{CC}, SW8, 12 ON	400	450		mV_{P-P}
V_{OF-PED}	Set pedestal offset	②㊶	㊸	Pin ② SG1 280mV_{P-P}, SW12 ON Apply 5 V_{P-P} rectangular wave of approximately 30 kHz synchronizing with SG1 to pin ㊶ (from GND).	0	15	30	mV

Entire circuit

Symbol	Parameter	Input pin	Test pin	Test conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
V_{CCR}	Operating current	—	—	Operation should be normal in the application circuit.	45	5.0	5.5	V
I_{CC}	Current dissipation	—	㉘	V_{CC}=5.0V	24	35	46	mA

ELECTRICAL CHARACTERISTICS TEST METHOD

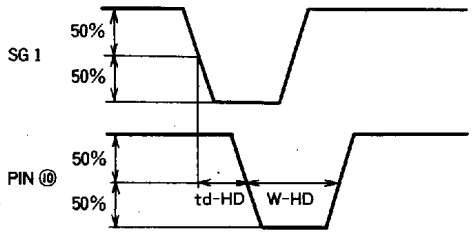
AFC

$V_{SDETMIN}$

Observe the SYNC separate out (signal) at PIN ⑨. Decrease the synchronizing signal of SG 1 gradually; the synchronizing signal amplitude when the SYNC separate out (signal) begins to be disturbed is $V_{SDETMIN}$.

td-csync

Observe the SYNC separate out (signal) at PIN ⑨ and the synchronizing signal of SG 1 semultaneously, the time difference, shown in the following figure, is td-csync.



W-csync

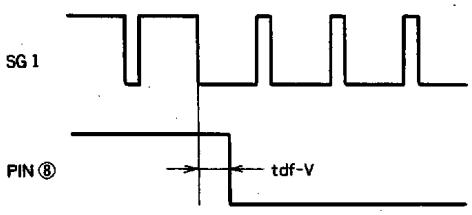
Using the same measuring method as in (A-2), the pulse width, shown in the above figure, is W-csync.

V_H-sync

The "H" voltage of the SYNC separate out signal observed at PIN ⑨ is V_H-sync.

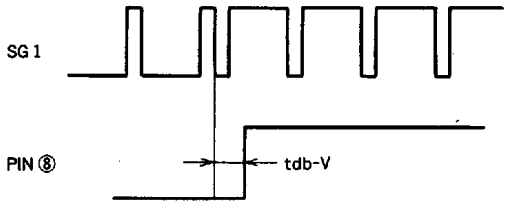
tdf-v

Observing the vertical SYNC separate out (signal) at PIN ⑧ and the vertical synchronizing signal of SG 1 simultaneously, the time difference in the first transition, shown in the following figure, is tdf-v.



tdb-v

Using the same measuring method as in (A-5), the time difference in the last transition shown, in the following figure, is tdb-v.

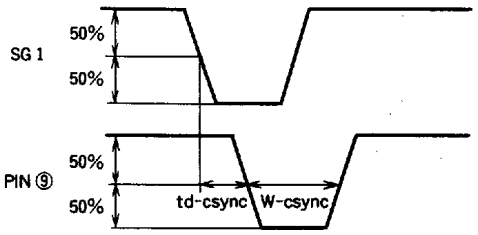


V_H-V

The "H" voltage of the SYNC separate out (signal) observed at PIN ⑧ is V_H-V.

td-HD

Observing the HD output signal of PIN ⑩ and the synchronizing signal of SG 1 simultaneously, the time difference, shown in the following figure, is td-HD.



W-HD

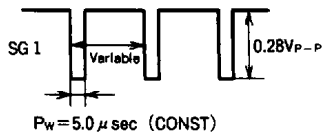
Using the same measuring method as in (A-8), the pulse width, shown in the above figure, is W-HD.

V_H-HD

The "H" voltage of the HD output signal observed at PIN ⑩ is V_H-HD.

CPR_{AFCP}

For SG1, use a pulse wave with constant Pw=5.0 μsec and variable frequency, as shown in the figure to the right. The amplitude is 0.28Vp-p. The measuring point is at PIN5.The output voltage of PIN ⑤ is "L" when AFC is locked. The pulse frequency when the output of PIN ⑤ changes from "H" to "L" as the frequency is decreased gradually from around 20kHz is f_H, and CAR_{AFCP} is expressed as follows.



$$CAR_{AFCP} = \begin{cases} f_H\text{-}15.734[kHz]\ (NTSC) \\ f_H\text{-}15.625[kHz]\ (PAL) \end{cases}$$

CPR_{AFCN}

Use the same measuring method given in (A-11). In this case, decrease the frequency gradually from around 10kHz; the pulse frequency when the output of PIN ⑤ changes from "H" to "L" is f_L, and CPR_{AFCN} is expressed as:

$$CPR_{AFCN} = \begin{cases} 15.734\text{-}f_L\ [kHz]\ (NTSC) \\ 15.625\text{-}f_L\ [kHz]\ (PAL) \end{cases}$$

$V_{H\text{-}SDET}$

The output DC voltage of PIN ⑤ when the output of SG1 carries no signal is $V_{H\text{-}SDET}$.

$V_{L\text{-}SDET}$

The output DC voltage of PIN ⑤ when SG1 is the standard video signal is $V_{L\text{-}SDET}$.

PLL

$V_{CLK\text{-}MIN}$

First,adjust the free running frequency. Set SW2 to 2 and vary TC1 while measuring the output frequency of PIN㉝(high impedance buffer is necessary)in order to adjust it to 3.579545MHz for NTSC or 4.43619MHz for PAL.
After adjusting the free running frequency, return SW2 to 1. While decreasing the burst signal amplitude of SG4 gradually, the burst signal amplitude right before the burst signal and VCXO output signal of PIN ⑲ step out is $V_{CLK\text{-}MIN}$.

CPR_{APCP}

After adjusting the free running frequency by the method given in (P-1), make sure SW2 has been returned to 1. Use continuous sine waves as the signal source for SG4 whose amplitude is 280mVp-p. The frequency when APC is locked by gradually decreasing the frequency from approximately the free running frequency +5kHz is f_H, and CPR_{APCP} is expressed as:

$$CPR_{APCP} = \begin{cases} f_H\text{-}3579545\ [Hz]\ (NTSC) \\ f_H\text{-}4433619\ [Hz]\ (PAL) \end{cases}$$

CPR_{APCL}

The frequency when APC is locked by gradually in creasing the frequency from the free running frequency -5kHz using the same method given in (P-2) is f_L, and CPR_{APCL} is expressed as:

$$CPR_{APCL} = \begin{cases} 3579545\text{-}f_L\ [Hz]\ (NTSC) \\ 4433619\text{-}f_H\ [Hz]\ (PAL) \end{cases}$$

V_{KILLER}

After adjusting the free running frequency by the same method given in (P-1), return SW2 to 1. Set VS1 to 2.5V and gradually decrease the burst signal amplitude of SG4. The burst signal amplitude right before the output DC voltage of PIN㉗changes from "L" to "H" is V_{BMIN}[mVp-p], and V_{KILLER} is expressed as:

$$V_{KILLER} = 20 \log \frac{V_{BMIN}}{280\ [mVp\text{-}p]}$$

$V_{H\text{-}KILL}$

While following the method given in (P-4), when the burst signal amplitude of SG4 becomes 0mVp-p, the DC voltage of PIN ㉗ is $V_{H\text{-}KILL}$

$V_{L\text{-}KILL}$

While following the method given in (P-4), when the burst signal amplitude of SG4 becomes 280mVp-p, the DC voltage of PIN ㉗ is $V_{L\text{-}KILL}$

fo

This parameter is a measure of the dispersion of free running frequency when TC 1 is fixed after adjusting VCXO free running frequency. When TC1=17pF for NTSC or 21pF for PAL, and SW2 is set to 2, the frequency at PIN㉝ is fo.

$V_{TH\text{-}HD}$

This parameter indicates the pulse voltage of external HD pulses (PIN㉑) for normal operation of F/F of IC in PAL. The "H" voltage of HD pulses should be MAX or higher and the "L" voltage should be MIN or lower.

$V_{TH\text{-}NP}$

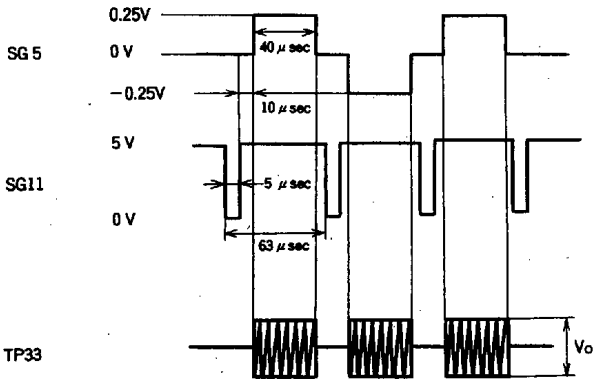
NTSC mode becomes active if the voltage of PIN㉑becomes $V_{TH\text{-}NP}$ or higher. Therefore, it is necessary that the voltage of PIN㉑ be MAX or higher in NTSC, or that the "H" voltage of HD pulses in PAL be MIN or lower.

MOD

G_{MOD}

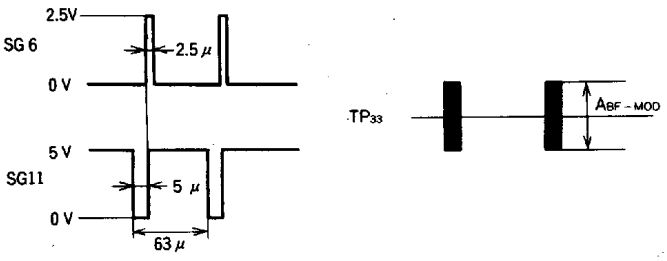
To measure R-Y input, set SW4 to 2, SW2 to 2, and SW10 to 1. To measure B-Y input, set SW6 to 2, SW2 to 2, and SW10 to 1. Input the waveforms shown in the following figure from SG5 and SG11 respectively, and read Vo from the waveform observed at TP33. Calculate G_{MOD} is given by the following expression.

$$G_{MOD} = \frac{Vo\ [Vp\text{-}p]}{0.5\ [Vp\text{-}p]}$$



$A_{BF\text{-}MOD}$

To measure R-Y B.F.P. input, set SW5 to 2, SW2 to 2, and SW10 to 1. To measure B-Y B.F.P. input, set SW7 to 2, SW2 to 2, and SW10 to 1. Input the waveforms shown in the following figure from SG6 and SG11 respectively, and measure $A_{BF\text{-}MOD}$ from the waveform observed at TP_{33}.

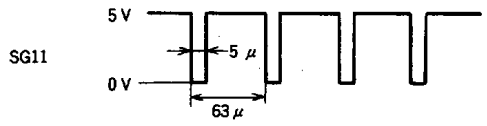


D_{MOD}

Under the same measuring conditions given in (M-1), increase the amplitude of SG5 gradually; the amplitude of SG5 right before the output of TP_{33} reaches saturation is D_{MOD}.

LK_{MOD}

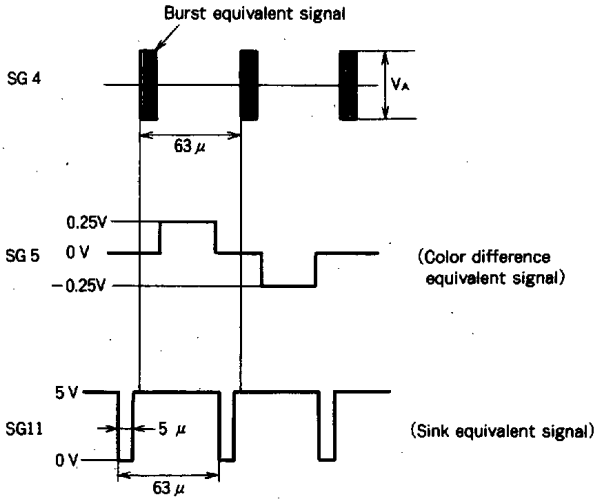
Set SW2 to 2 and SW10 to 1, and input the waveform shown in the following figure from SG11; the output amplitude measured at TP_{33} is LK_{MOD}.



TR

Set SW5 to 2 and SW10 to 1, and input the waveforms Δ shown in the following figure from SG4,SG5 and SG11respectively.The amplitude of the waveform observed at TP_{33} is V_{140} when V_A=140mVp-p, and V_{280} when V_A=280mVp-p; TR is given by the following expression.

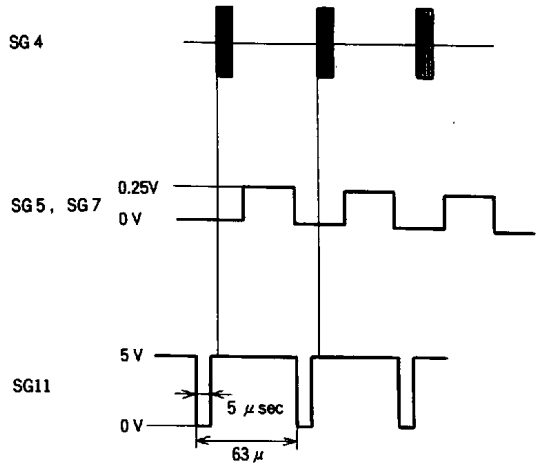
$$TR = \frac{V_{280}}{V_{140}}$$



θ MOD

The measure of the phase of the burst equivalent signal of SG4 is Odeg. Set SW10 to 1 and input the waveforms △ shown in the following figure from SG5, SG7 and SG11. The phase at TP_{33} when SW4 is set to 2 is θ_1, and the phase at TP_{33} when SW4 is set to 1 and SW6 to 2 is θ_2. θ_{MOD} is given by the following expression.

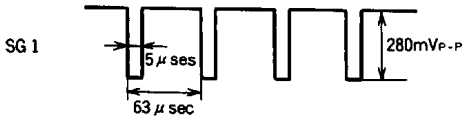
$$\theta_{MOD} = |\theta_1 - \theta_2| \text{ [deg]}$$



Y/C MIX,Video SW

dVsync

Input 280mVp-p sink from SG1 as shown in the following figure. Measure the p-p value of the sink waveform after the clamp condenser, and the difference between it and the input is dVsync.



GVSUB

The output p-p value of PIN ㊷ when SW1 is set to 2 and a 1.0Vp-p,setup 0.75% color bar composite video signal is input from SG2 is V_{42OUT}.GVSUB is given by the following expression.

$$G_{VSUB} = 20 \log \frac{V_{42OUT}}{1.0} \text{ [dB]}$$

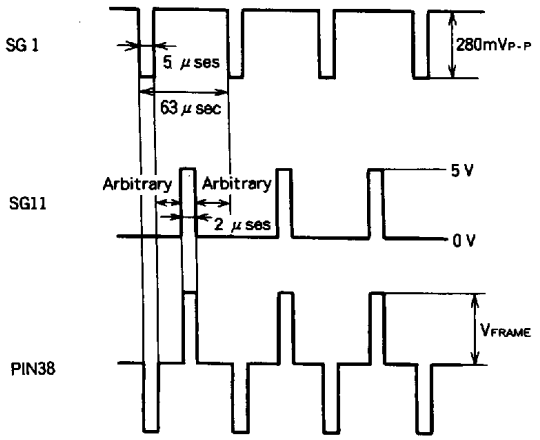
GVMAIN

The output p-p value of PIN㊳ when a 1. 0Vp-p 100% white Y video signal is input from SG1 is V_{38OUT}.GVMAIN is given by the following expression.

$$G_{VMAIN} = 20 \log \frac{V_{38OUT}}{1.0} \text{ [dB]}$$

VFRAME

Set SW1 to 2 , SW11 to 2, input the waveforms shown in the following figure from SG1 and SG2 respectively, and measure VFRAME of the waveform output from PIN㊳ as shown below.



Vsync

Measure the p-p value of the sink pulse output at PIN㊳ under the same measuring conditions given in (V-1); the value obtained is Vsync.

GVMIX

Input a waveform under the same conditions given in (V-1) from SG1 and set SW12 to 2, and SW8 and SW9 to 1. The p-p value of the composite video signal output to PIN ㊳, when a Y signal that is an attenuated signal of a 1.0Vp-p 75% color bar video signal synchronized with SG1 at -12dB is input from SG11 and a chroma signal that is an attenuated signal of the above color bar video signal at -12dB is input from SG9, is V_{38OUT} [Vp-p]. GVMIX is given by the following expression.

$$G_{VMIX} = 20 \log \frac{V_{38OUT}}{0.5} \text{ [dB]}$$

DYMIX

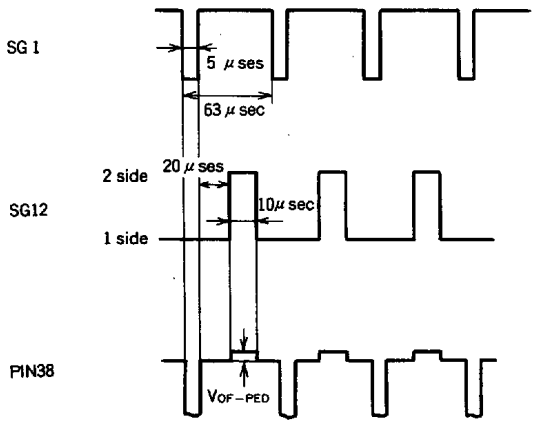
Input a waveform under the same conditions given in (V-1) from SG1, set SW12 to 2 and SW9 to 1, and input a luminance signal synchronized with SG1 from SG11. The amplitude of the input when the output of PIN ㊳ begins to be distorted as the amplitude is increased is DYMIX.

DCMIX

Input a waveform under the same conditions given in (V-1) from SG1, set SW12 to 2 and SW8 to 1, and input a chroma signal synchronized with SG1 from SG10. The amplitude of the input when the output of PIN ㊳ begins to be distorted as the amplitude is increased is DCMIX.

V_{OF-PED}

Input a waveform under the same conditions given in (V-1) from SG1, change SW12 according to the timing shown below. Measure the part of the waveform output at PIN ㊳ as shown below. The measurement obtained is V_{OF-PED}.



Entire Circuit

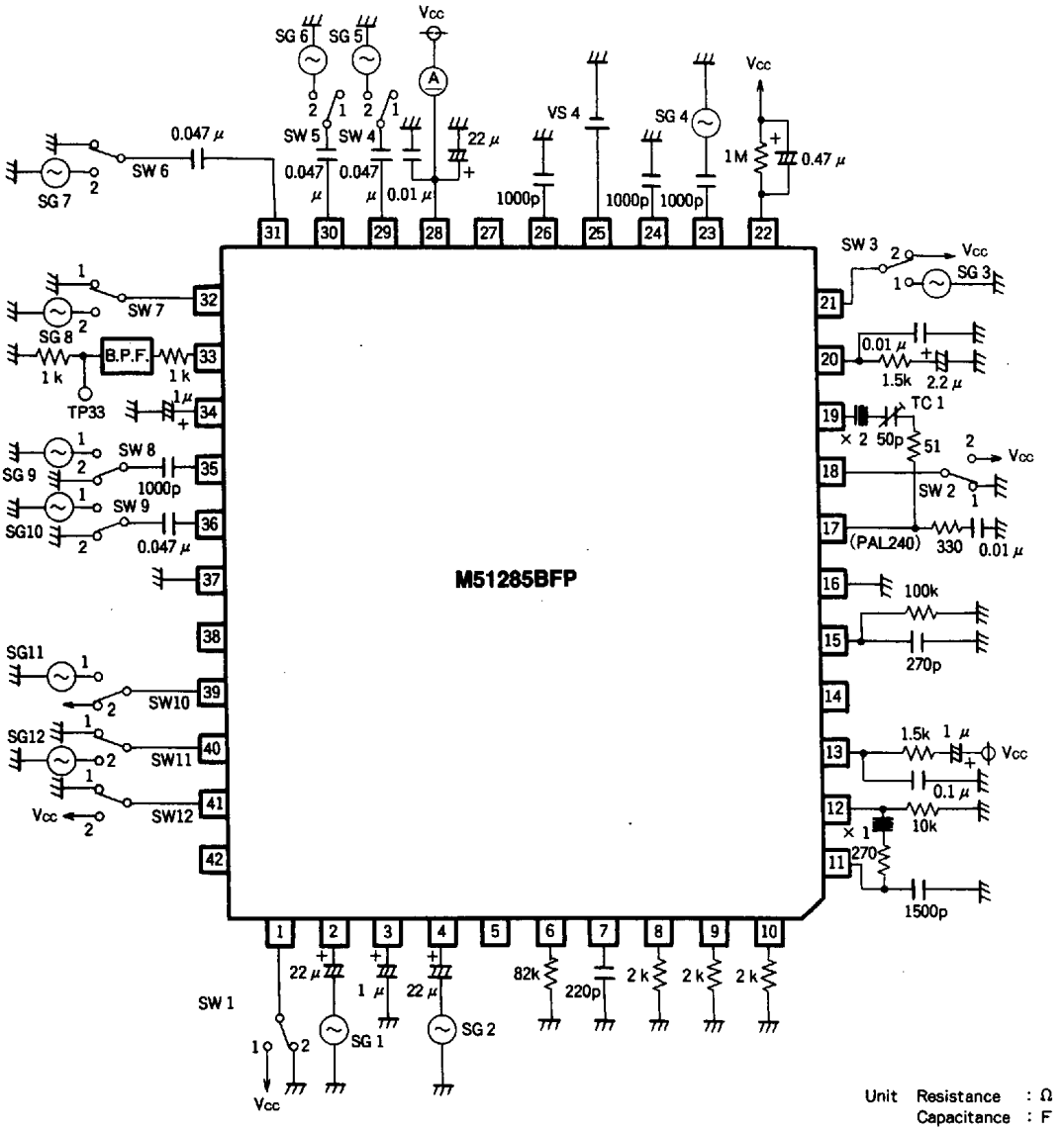
VccR

Operation should be normal, matching the application circuit example given.

Icc

The current flowing into PIN ㉘ in the application circuit example is Icc.

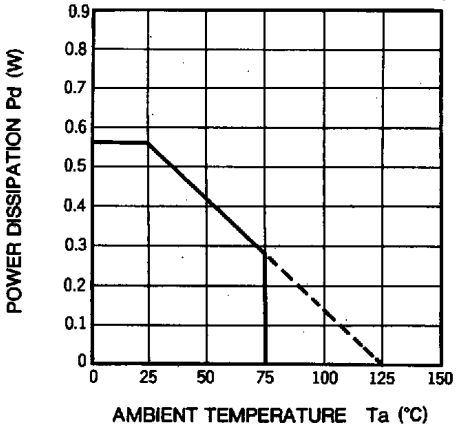
TEST CIRCUIT



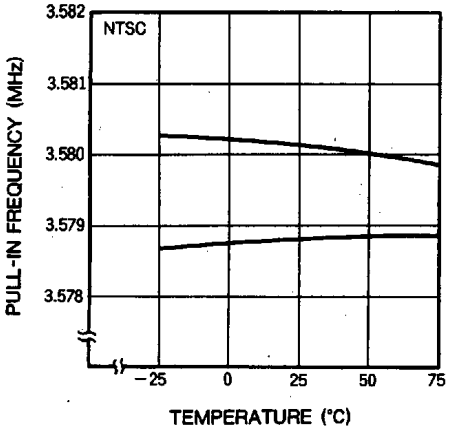
(Note) SWs 1 through 12 should be connected as conditioned in this circuit diagram unless they are otherwise specified in the measuring methods. SG1 and SG2 are both 1.0 V_{P-P} 100% white Y signals, and SG4 is 280 mV_{P-P} chroma burst signal source synchronizing with SG1.

TYPICAL CHARACTERISTICS

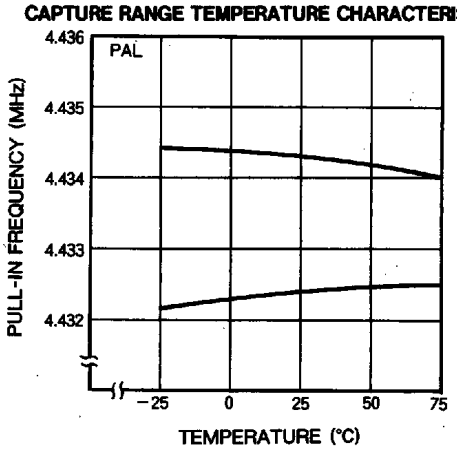
THERMAL DERATING (MAXIMUM RATING)



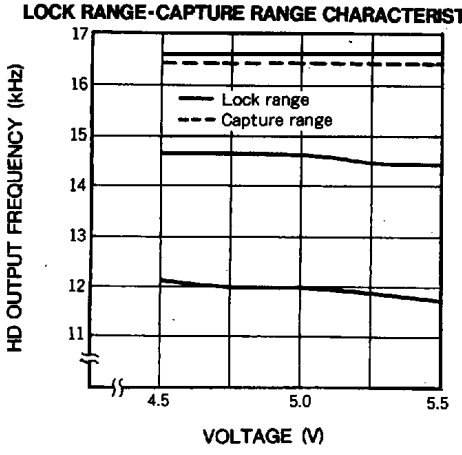
CAPTURE RANGE TEMPERATURE CHARACTERISTIC



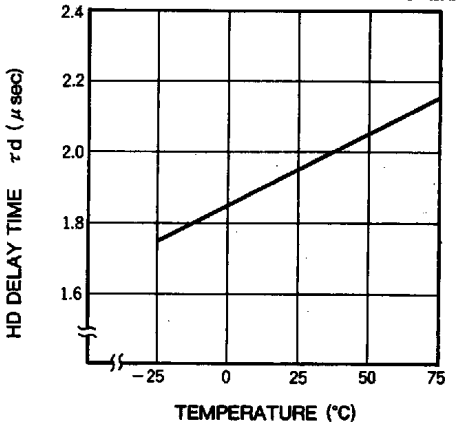
CAPTURE RANGE TEMPERATURE CHARACTERISTIC



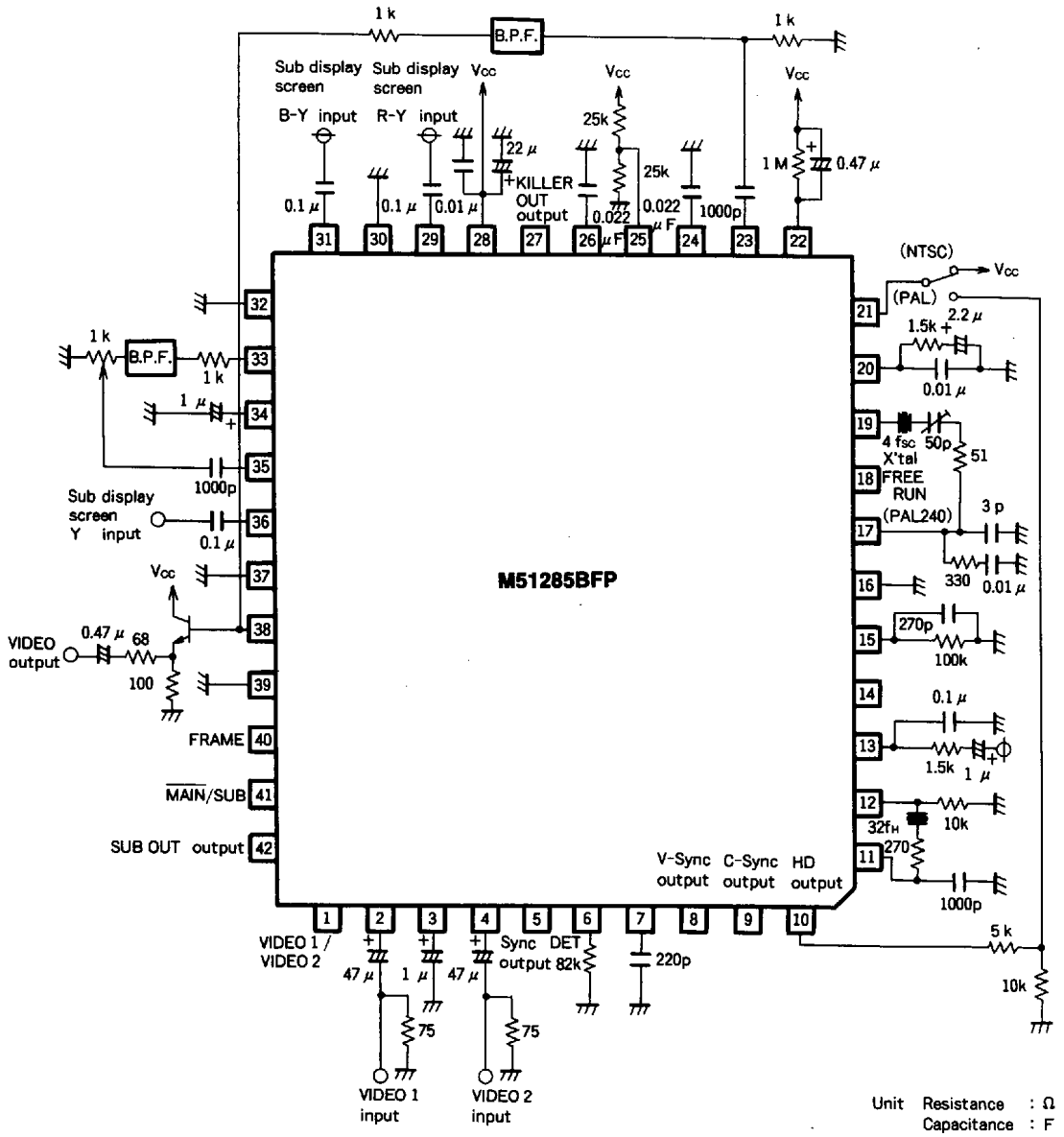
LOCK RANGE-CAPTURE RANGE CHARACTERISTICS



HD PULSE DELAY TIME TEMPERATURE CHARACTERISTIC



APPLICATION EXAMPLE



* Input to pins ㉙, ㉛ and ㊳ should be provided at sufficiently low impedance.

PRECAUTIONS FOR APPLICATION

ID detection level is linked with KILLER LEVEL adjustment at pin ㉙. For stable operation of ID in the PAL mode, KILLER LEVEL should be kept under 2.8V. For the use in the free run mode in PAL, the application circuit shown here is recommended