RX210 Group
Renesas MCUs

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50-MHz 32-bit RX MCUs, 78 DMIPS, up to 512-KB flash memory, 12-bit AD, 10-bit DA, ELC, MPC, RTC, up to 9 comms interfaces; incorporating functions for IEC60730 compliance

Features

■ 32-bit RX CPU core
- Max. operating frequency: 50 MHz
  Capable of 78 DMIPS in operation at 50 MHz
- Accumulator handles 64-bit results (for a single instruction) from 32- × 32-bit operations
- Multiplication and division unit handles 32- × 32-bit operations (multiplication instructions take one CPU clock cycle)
- Fast interrupt
- CISC Harvard architecture with 5-stage pipeline
- Variable-length instructions, ultra-compact code
- On-chip debugging circuit

■ Low-power design and architecture
- Operation from a single 1.62- to 5.5-V supply
- 1.62-V operation available (at up to 20 MHz)
- Deep software standby mode with RTC remaining usable
- Four low-power modes

■ On-chip flash memory for code, no wait states
- 50-MHz operation, 20-ns read cycle
- No wait states for reading at full CPU speed
- 128- to 512-Kbyte capacities
- User code programmable via the SCI
- Programmable at 1.62 V
- For instructions and operands

■ On-chip data flash memory
- Eight Kbytes
- Erasing and programming impose no load on the CPU.

■ On-chip SRAM, no wait states
- 20- to 64-Kbyte size capacities

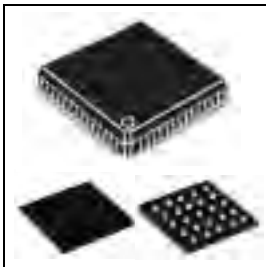
■ DMA
- DMACA: Incorporates four channels
- DTC: Four transfer modes

■ ELC
- Module operation can be initiated by event signals without going through interrupts.
- Modules can operate while the CPU is sleeping.

■ Reset and supply management
- Nine types of reset, including the power-on reset (POR)
- Low voltage detection (LVD) with voltage settings

■ Clock functions
- Frequency of external clock: Up to 20 MHz
- Frequency of the oscillator for sub-clock generation: 32.768 kHz
- PLL circuit input: 4 to 12.5 MHz
- On-chip low- and high-speed oscillators, dedicated on-chip low-speed oscillator for the IWDT
- Generation of a dedicated 32.768-kHz clock for the RTC
- Clock frequency accuracy measurement circuit (CAC)

■ Real-time clock
- Adjustment functions (30 seconds, leap year, and error)
- Time capture function
- Time capture on event-signal input through external pins
- RTC capable of initiating return from deep software standby mode



PLQP0100KB-A 14 × 14 mm, 0.5-mm pitch
PLQP0080KB-A 12 × 12 mm, 0.5-mm pitch
PLQP0080JA-A 14 × 14 mm, 0.65-mm pitch
PLQP0064KB-A 10 × 10 mm, 0.5-mm pitch
PLQP0064GA-A 14 × 14 mm, 0.8-mm pitch

PTLG0100JA-A 7 × 7 mm, 0.65-mm pitch

■ Independent watchdog timer
- 125-kHz on-chip low-speed oscillator produces a dedicated clock signal to drive IWDT operation.

■ Useful functions for IEC60730 compliance
- Self-diagnostic and disconnection-detection functions for the AD converter, clock-frequency accuracy-measurement circuit, independent watchdog timer, functions to assist in RAM testing, etc.

■ Up to nine communications interfaces
- SCI with many useful functions (up to seven interfaces)
- Asynchronous mode, clock synchronous mode, smart card interface
- I^2C bus interface: Transfer at up to 1 Mbps, capable of SMBus operation (1 interface)
- RSPI (1)

■ External address space
- Four CS areas (4 × 16 Mbytes)
- 8- or 16-bit bus space is selectable per area

■ Up to 14 extended-function timers
- 16-bit MTU2: input capture, output capture, complementary PWM output, phase counting mode (6 channels)
- 8-bit TMR (4 channels)
- 16-bit compare-match timers (4 channels)

■ 12-bit A/D converter
- Capable of conversion within 1 µs
- Sample-and-hold circuits (for three channels)
- Three-channel synchronized sampling available
- Self-diagnostic function and analog input disconnection detection assistance function

■ 10-bit D/A converter

■ Analog comparator

■ Programmable I/O ports
- 5-V tolerant, open drain, input pull-up, switching of driving ability

■ MPC
- Multiple locations are selectable for I/O pins of peripheral functions

■ Temperature sensor

■ Operating temp. range
- -40 °C to +85°C

1. Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications in outline, and Table 1.2 gives a comparison of the functions of products in different packages.
Table 1.1 is for products with the greatest number of functions, so numbers of peripheral modules and channels will differ in accord with the package. For details, see Table 1.2, Comparison of Functions for Different Packages.

Table 1.1 Outline of Specifications (1 / 3)

Classification	Module/Function	Description
CPU	CPU	• Maximum operating frequency: 50 MHz • 32-bit RX CPU • Minimum instruction execution time: One instruction per state (cycle of the system clock) • Address space: 4-Gbyte linear • Register set of the CPU General purpose: Sixteen 32-bit registers Control: Eight 32-bit registers Accumulator: One 64-bit register • Basic instructions: 73 • DSP instructions: 9 • Addressing modes: 10 • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32 x 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits
Memory	ROM	• ROM capacity: 512 Kbytes (max.) • Three on-board programming modes Boot mode (The user mat and the user boot mat are programmable via the SCI.) User boot mode User program mode • Parallel programmer mode (for off-board programming)
	RAM	RAM capacity: 64 Kbytes (max.)
	E2 data flash	E2 data flash capacity: 8 Kbytes
MCU operating mode		Single-chip mode, on-chip ROM enabled expansion mode, and on-chip ROM disabled expansion mode (software switching)
Clock	Clock generation circuit	• Main clock oscillator, sub-clock oscillator, Low-speed on-chip oscillator, high-speed on-chip oscillator, PLL frequency synthesizer, and dedicated low-speed on-chip oscillator for IWDT • Oscillation stop detection • Measuring circuit for accurcy of clock frequency (clock-accurcy check: CAC) • Independent frequency-division and multiplication settings for the system clock (ICLK), peripheral module clock (PCLK), external bus clock (BCLK), and flashIF clock (FCLK) The CPU and system sections such as other bus masters run in synchronization with the system clock (ICLK): 50 MHz (at max.) Peripheral modules run in synchronization with the peripheral module clock (PCLK): 32 MHz (at max.) Devices connected to the external bus run in synchronization with the external bus clock (BCLK): 12.5 MHz (at max.) The flash peripheral circuit runs in synchronization with the flash peripheral clock (FCLK): 32 MHz (at max.)
Reset		Pin reset, power-on reset, voltage-monitoring reset, watchdog timer reset, independent watchdog timer reset, deep software standby reset, and software reset
Voltage detection	Voltage detection circuit (LVD)	• When the voltage on VCC falls below the voltage detection level, an internal reset or internal interrupt is generated. Voltage detection circuit 0 is capable of selecting the detection voltage from 4 levels Voltage detection circuit 1 is capable of selecting the detection voltage from 16 levels Voltage detection circuit 2 is capable of selecting the detection voltage from 16 levels
Low power consumption	Low power consumption facilities	• Module stop function • Four low power consumption modes Sleep mode, all-module clock stop mode, software standby mode, and deep software standby mode
Interrupt	Interrupt control unit (ICU)	• Interrupt vectors: 117 • External interrupts: 9 (NMI and IRQ0 to IRQ7 pins) • Non-maskable interrupts: 6 (the NMI pin, oscillation stop detection interrupt, voltage-monitoring interrupt 1, voltage-monitoring interrupt 2, WDT interrupt, and IWDT interrupt) • 16 levels specifiable for the order of priority

Table 1.1 Outline of Specifications (2 / 3)

Classification	Module/Function	Description
External bus extension		• The external address space can be divided into four areas (CS0 to CS3), each with independent control of access settings. Capacity of each area: 16 Mbytes (CS0 to CS3) A chip-select signal (CS0# to CS3#) can be output for each area. Each area is specifiable as an 8- or 16-bit bus space The data arrangement in each area is selectable as little or big endian (only for data). Bus format: Separate bus, multiplex bus • Wait control • Write buffer facility
DMA	DMA controller (DMACA)	• 4 channels • Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Software trigger, external interrupts, and interrupt requests from peripheral functions
	Data transfer controller (DTC)	• Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Interrupts • Chain transfer function
I/O ports	Programmable I/O ports	100-pin LQFP/80-pin LQFP/64-pin LQFP • I/O pin: 84/64/48 • Input: 1/1/1 • Pull-up resistors: 85/65/49 • Open-drain outputs: 54/44/35 • 5-V tolerance: 4/4/2
Event link controller (ELC)		• Event signals of 59 types can be directly connected to the module • Operations of timer modules are selectable at event input • Capable of event link operation for ports B and E
Multifunction pin controller (MPC)		• Capable of selecting input/output function from multiple pins
Timers	Multi-function timer pulse unit 2 (MTU2)	• (16 bits x 6 channels) x 1 unit • Time bases for the six 16-bit timer channels can be provided via up to 16 pulse-input/output lines and three pulse-input lines • Select from among eight or seven counter-input clock signals for each channel (PCLK/1, PCLK/4, PCLK/16, PCLK/64, PCLK/256, PCLK/1024, TCLKA, TCLKB, TCLKC, TCLKD) other than channel 5, for which only four signals are available. • Input capture function • 21 output compare/input capture registers • Pulse output mode • Complementary PWM output mode • Reset synchronous PWM mode • Phase-counting mode • Generation of triggers for A/D converter conversion
	Port output enable2 (POE2)	Controls the high-impedance state of the MTU2's waveform output pins from multiple pins
	8-bit timer (TMR)	• (8 bits x 2 channels) x 2 units • Select from among seven internal clock signals (PCLK, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, PCLK/8192) and one external clock signal • Capable of output of pulse trains with desired duty cycles or of PWM signals • The 2 channels of each unit can be cascaded to create a 16-bit timer • Capable of generating baud-rate clocks for SCI5, SCI6, and SCI12
	Compare match timer (CMT)	• (16 bits x 2 channels) x 2 units • Select from among four clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512)
	Watchdog timer (WDT)	• 14 bits x 1 channel • Select from among 6 counter-input clock signals (PCLK/4, PCLK/64, PCLK/128, PCLK/512, PCLK/2048, PCLK/8192)
	Independent watchdog timer (IWDT)	• 14 bits x 1 channel • Counter-input clock: Dedicated low-speed on-chip oscillator for IWDT Frequency divided by 1, 16, 32, 64, 128, or 256
	Realtime clock (RTC)	• Clock source: Subclock • Time/calendar • Interrupt sources: Alarm interrupt, periodic interrupt, and carry interrupt • Time-capture facility for three values

Table 1.1 Outline of Specifications (3 / 3)

Classification	Module/Function	Description
Communication function	Serial communications interfaces (SCIc, SCId)	• 7 channels (channel 0, 1, 5, 6, 8, 9: SCIc, channel 12: SCId) • Serial communications modes: Asynchronous, clock synchronous, and smart-card interface • On-chip baud rate generator allows selection of the desired bit rate • Choice of LSB-first or MSB-first transfer • Average transfer rate clock can be input from TMR timers (SCL5, SCL6, and SCL12) • Simple IIC • Simple SPI • Master/slave mode supported (SCId only) • Start frame and information frame are included (SCId only)
	I^2C bus interface (RIIC)	• 1 channel • Communications formats: I^2C bus format/SMBus format • Master/slave selectable • Supports the first mode
	Serial peripheral interface (RSPI)	• 1 channel • RSPI transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPI clock (RSPCK) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) • Capable of handling serial transfer as a master or slave • Data formats • Choice of LSB-first or MSB-first transfer The number of bits in each transfer can be changed to any number of bits from 8 to 16, 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • Double buffers for both transmission and reception
12-bit A/D converter		• 12 bits (16 channels x 1 unit) • 12-bit resolution • Conversion time: 1.0 μs per channel (in operation with ADCLK at 50 MHz) • Operating modes Scan mode (single-cycle scan mode, continuous scan mode, and group scan mode) • Sample-and-hold function • Self-diagnosis for the A/D converter • Assistance in detecting disconnected analog inputs • Double-trigger mode (duplexing of A/D-converted data) • A/D conversion start conditions Conversion can be started by software, a conversion start trigger from a timer (MTU2), an external trigger signal, or ELC.
Temperature sensor		• Outputs the voltage that changes depending on the temperature • PGA gain switchable: Four levels according to the voltage range
D/A converter		• 2 channels • 10-bit resolution • Output voltage: 0 V to VREFH
CRC calculator (CRC)		• CRC code generation for arbitrary amounts of data in 8-bit units • Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$ • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable.
Comparator A		• 2 channels • Comparison of reference voltage and analog input voltage
Comparator B		• 2 channels • Comparison of reference voltage and analog input voltage
Power supply voltage/ Operating frequency		VCC = 1.62 to 1.8 V: 20 MHz, VCC = 1.8 to 2.7 V: 32 MHz, VCC = 2.7 to 5.5 V: 50 MHz
Supply current		TBD mA (typ.)
Operating temperature		–40 to +85°C
Package		100-pin TFLGA (PTLG0100JA-A) 100-pin LQFP (PLQP0100KB-A) 80-pin LQFP (PLQP0080KB-A) 80-pin LQFP (PLQP0080JA-A) 64-pin LQFP (PLQP0064KB-A) 64-pin LQFP (PLQP0064GA-A)

Table 1.2 Comparison of Functions for Different Packages

Module/Functions		RX210 Group		
		100 Pins	**80 Pins**	**64 Pins**
External bus	CS areas: 4 (CS0 to CS3)	Supported	Not supported	Not supported
Interrupt	External interrupts	NMI, IRQ0 to IRQ7		
DMA	DMA controller (DMAC)	4 channels (DMAC0 to DMAC3)		
	Data transfer controller (DTC)	Supported		
Timers	Multi-function timer pulse unit 2 (MTU2)	6 channels (MTU0 to MTU5)		
	Port output enable 2 (POE2)	POE0# to POE3#, POE8#		
	8-bit timer (TMR)	2 channels × 2 units		
	Compare match timer (CMT)	2 channels × 2 units		
	Realtime clock (RTC)	Supported		
	Watchdog timer (WDT)	Supported		
	Independent watchdog timer (IWDT)	Supported		
Communication function	Serial communications interface (SCIc)	6 channels (SCI0, 1, 5, 6, 8, 9)		5 channels (SCI1, 5, 6, 8, 9)
	Serial communications interface (SCId)	1 channel (SCI12)		
	I^2C bus interface (RIIC)	1 channel		
	Serial peripheral interface (RSPI)	1 channel		
12-bit A/D converter		16 channels (AN000 to AN015)	14 channels (AN000 to AN013)	12 channels (AN000 to AN004, AN006, AN008 to AN013)
Temperature sensor		Supported		
D/A converter		2 channels		
CRC calculator (CRC)		Supported		
Event link controller (ELC)		Supported		
Comparator A		2 channels		
Comparator B		2 channels		
Package		100-pin TFLGA 100-pin LQFP	80-pin LQFP	64-pin LQFP

1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part no., memory capacity, and package type.

Table 1.3 List of Products

Group	Part No.	Package	ROM Capacity	RAM Capacity	E2 Data Flash	Operating Frequency (Max.)
RX210	R5F52108ADFP	PLQP0100KB-A	512 Kbytes	64 Kbytes	8 Kbytes	50 MHz
	R5F52108ADFG	T.B.D	512 Kbytes			
	R5F52108ADFN	PLQP0080KB-A	512 Kbytes			
	R5F52108ADFF	PLQP0080JA-A	512 Kbytes			
	R5F52108ADFM	PLQP0064KB-A	512 Kbytes			
	R5F52108ADFK	PLQP0064GA-A	512 Kbytes			
	R5F52108ADLJ	PTLG0100JA-A	512 Kbytes			
	R5F52107ADFP	PLQP0100KB-A	384 Kbytes			
	R5F52107ADFG	T.B.D	384 Kbytes			
	R5F52107ADFN	PLQP0080KB-A	384 Kbytes			
	R5F52107ADFF	PLQP0080JA-A	384 Kbytes			
	R5F52107ADFM	PLQP0064KB-A	384 Kbytes			
	R5F52107ADFK	PLQP0064GA-A	384 Kbytes			
	R5F52107ADLJ	PTLG0100JA-A	384 Kbytes			
	R5F52106ADFP	PLQP0100KB-A	256 Kbytes	32 Kbytes		
	R5F52106ADFG	T.B.D	256 Kbytes			
	R5F52106ADFN	PLQP0080KB-A	256 Kbytes			
	R5F52106ADFF	PLQP0080JA-A	256 Kbytes			
	R5F52106ADFM	PLQP0064KB-A	256 Kbytes			
	R5F52106ADFK	PLQP0064GA-A	256 Kbytes			
	R5F52106ADLJ	PTLG0100JA-A	256 Kbytes			
	R5F52105ADFP	PLQP0100KB-A	128 Kbytes	20 Kbytes		
	R5F52105ADFG	T.B.D	128 Kbytes			
	R5F52105ADFN	PLQP0080KB-A	128 Kbytes			
	R5F52105ADFF	PLQP0080JA-A	128 Kbytes			
	R5F52105ADFM	PLQP0064KB-A	128 Kbytes			
	R5F52105ADFK	PLQP0064GA-A	128 Kbytes			
	R5F52105ADLJ	PTLG0100JA-A	128 Kbytes			

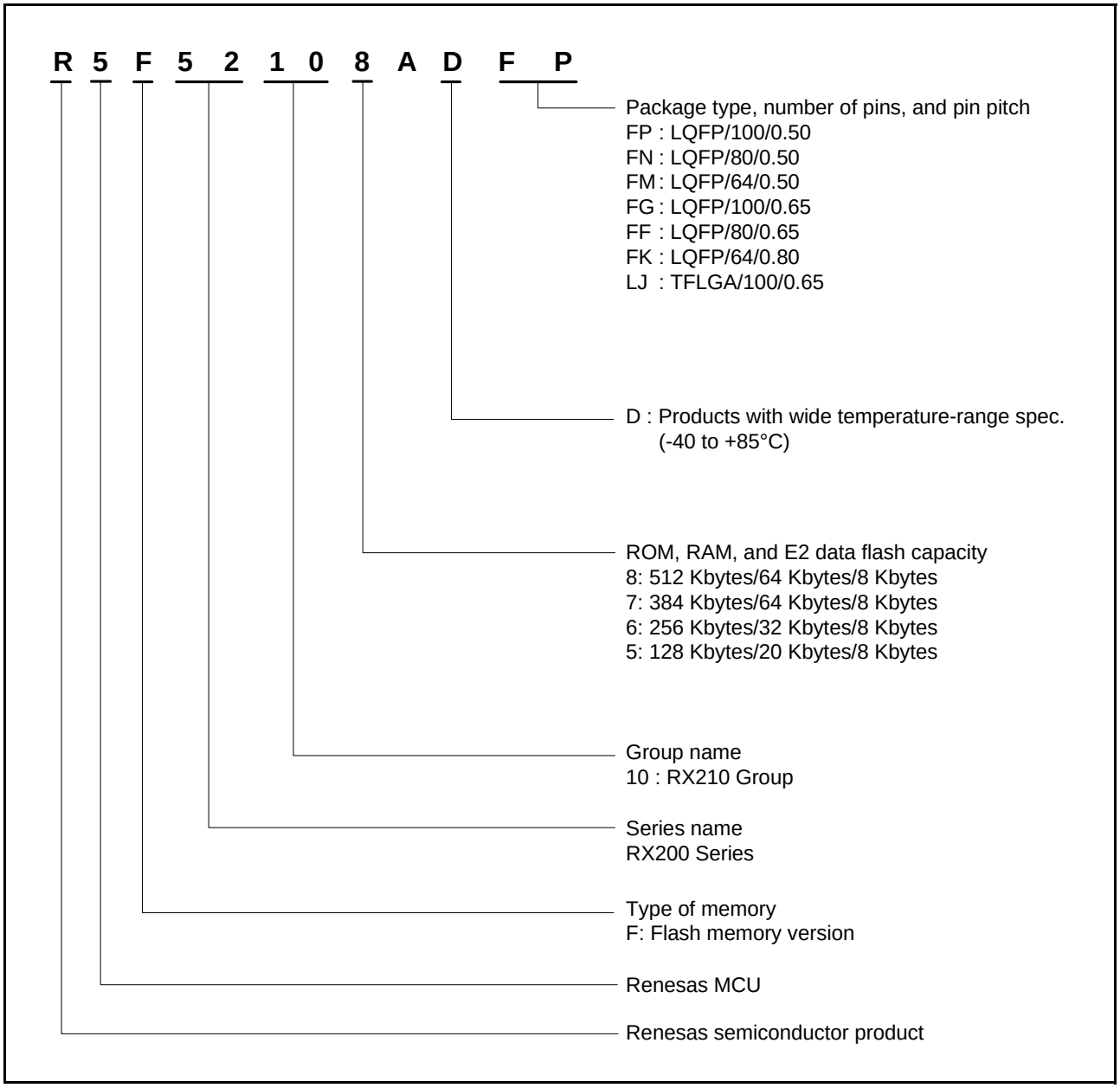
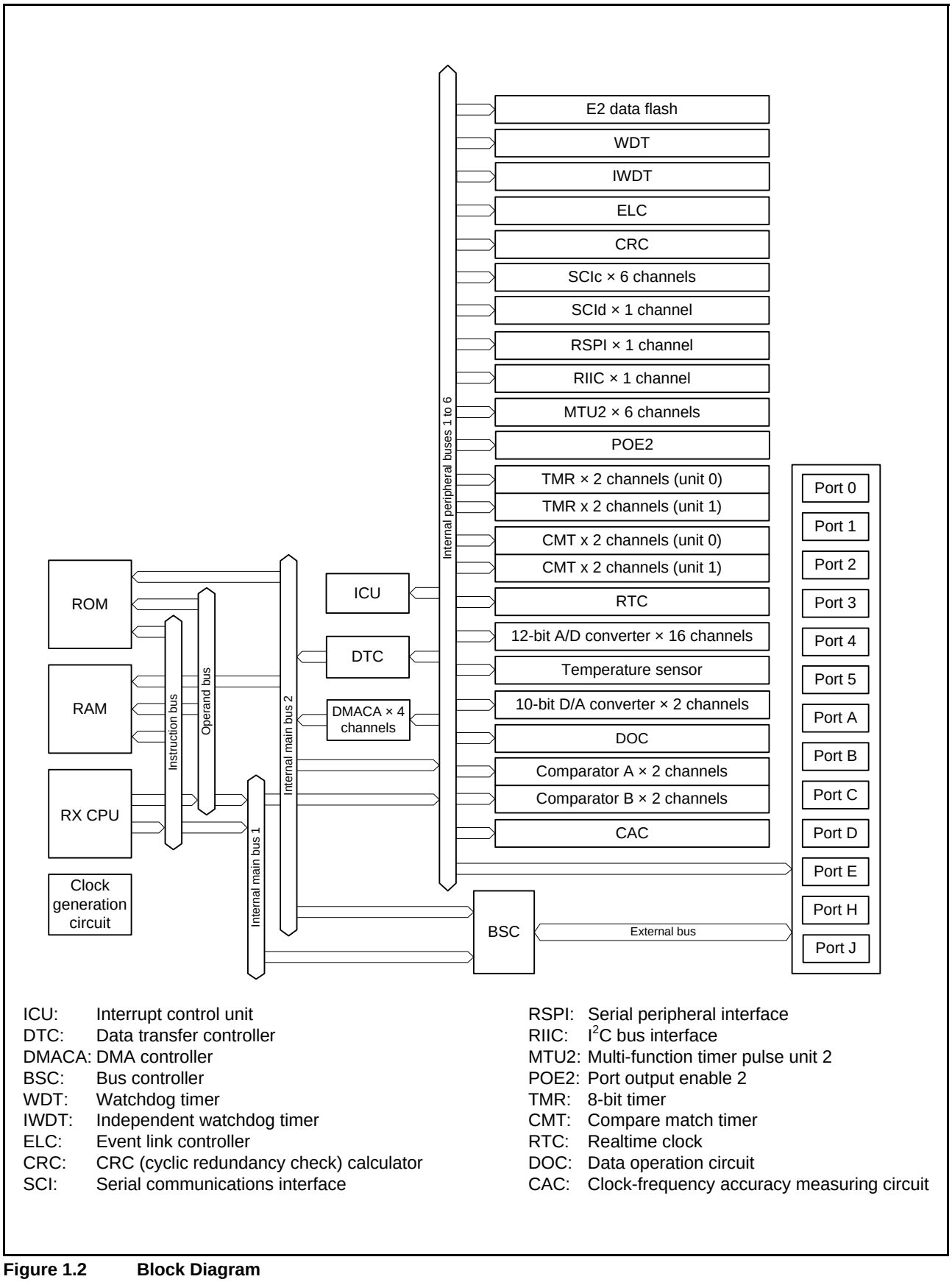


Figure 1.1 How to Read the Product Part No., Memory Capacity, and Package Type

1.3 Block Diagram

Figure 1.2 shows a block diagram.



ICU: Interrupt control unit
DTC: Data transfer controller
DMACA: DMA controller
BSC: Bus controller
WDT: Watchdog timer
IWDT: Independent watchdog timer
ELC: Event link controller
CRC: CRC (cyclic redundancy check) calculator
SCI: Serial communications interface
RSPI: Serial peripheral interface
RIIC: I^2C bus interface
MTU2: Multi-function timer pulse unit 2
POE2: Port output enable 2
TMR: 8-bit timer
CMT: Compare match timer
RTC: Realtime clock
DOC: Data operation circuit
CAC: Clock-frequency accuracy measuring circuit

Figure 1.2 Block Diagram

1.4 Pin Functions

Table 1.4 lists the pin functions.

Table 1.4 Pin Functions (1 / 4)

Classifications	Pin Name	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply.
	VCL	Input	Connect this pin to VSS via a 0.1μF capacitor. The capacitor should be placed close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
Clock	XTAL	Output	Pins for connecting a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	BCLK	Output	Outputs the external bus clock for external devices.
	XCIN	Input	Input/output pins for the subclock generation circuit. Connect a crystal resonator between XCIN and XCOUT.
	XCOUT	Output	
Operating mode control	MD	Input	Pins for setting the operating mode. The signal levels on this pin must not be changed during operation.
System control	RES#	Input	Reset signal input pin. This LSI enters the reset state when this signal goes low.
CAC	CACREF	Input	Input pin for the measuring circuit for clock frequency precision.
On-chip emulator	FINED	I/O	FINE interface pin.
	FINEC	Input	Clock pin for FINE interface.
Address bus	A0 to A23	Output	Output pins for the address.
Data bus	D0 to D15	I/O	Input and output pins for the bidirectional data bus.
Bus control	RD#	Output	Strobe signal which indicates that reading from the external bus interface space is in progress.
	WR#	Output	Strobe signal which indicates that writing to the external bus interface space is in progress, in single-write strobe mode.
	WR0#, WR1#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0, and D15 to D8) is valid in writing to the external bus interface space, in byte strobe mode.
	BC0#, BC1#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0 and D15 to D8) is valid in access to the external bus interface space, in single-write strobe mode.
	CS0# to CS3#	Output	Select signals for areas 0 to 3.
	WAIT#	Input	Input pins for wait request signals in access to the external space.
	ALE	Output	Address latch signal when address/data multiplexed bus is selected.
Interrupt (ICU)	NMI	Input	Non-maskable interrupt request signal.
	IRQ0 to IRQ7	Input	Interrupt request signals.

Table 1.4 Pin Functions (2 / 4)

Classifications	Pin Name	I/O	Description
Multi-function timer pulse unit 2 (MTU2)	MTIOC0A, MTIOC0B MTIOC0C, MTIOC0D	I/O	The TGRA0 to TGRD0 input capture input/output compare output/ PWM output pins.
	MTIOC1A, MTIOC1B	I/O	The TGRA1 and TGRB1 input capture input/output compare output/ PWM output pins.
	MTIOC2A, MTIOC2B	I/O	The TGRA2 and TGRB2 input capture input/output compare output/ PWM output pins.
	MTIOC3A, MTIOC3B MTIOC3C, MTIOC3D	I/O	The TGRA3 to TGRD3 input capture input/output compare output/ PWM output pins.
	MTIOC4A, MTIOC4B MTIOC4C, MTIOC4D	I/O	The TGRA4 to TGRD4 input capture input/output compare output/ PWM output pins.
	MTIC5U, MTIC5V, MTIC5W	Input	The TGRU5, TGRV5, and TGRW5 input capture input/external pulse input pins.
	MTCLKA, MTCLKB, MTCLKC, MTCLKD	Input	Input pins for external clock signals.
Port output enable 2 (POE2)	POE0# to POE3#, POE8#	Input	Input pins for request signals to place the MTU2 pins in the high impedance state.
8-bit timer (TMR)	TMO0 to TMO3	Output	Compare match output pins.
	TMCI0 to TMCI3	Input	Input pins for external clocks to be input to the counter.
	TMRI0 to TMRI3	Input	Input pins for the counter reset.
Realtime clock (RTC)	RTCOUT	Output	Output pin for 1-Hz clock.
	RTCIC0 to RTCIC2	Input	Tamper resistant event input pins.
Serial communications interface (SCIc)	• Asynchronous mode/clock synchronous mode		
	SCK0, SCK1, SCK5, SCK6, SCK8, SCK9	I/O	Input/output pins for clock signals
	RXD0, RXD1, RXD5, RXD6, RXD8, RXD9	Input	Input pins for received data
	TXD0, TXD1, TXD5, TXD6, TXD8, TXD9	Output	Output pins for transmitted data
	CTS0#, CTS1#, CTS5#, CTS6#, CTS8#, CTS9#	Input	Input pins for controlling the start of transmission and reception
	RTS0#, RTS1#, RTS5#, RTS6#, RTS8#, RTS9#	Output	Output pins for controlling the start of transmission and reception
	• Simple I^2C mode		
	SSCL0, SSCL1, SSCL5, SSCL6, SSCL8, SSCL9	I/O	Input/output pins for the I^2C clock
	SSDA0, SSDA1, SSDA5, SSDA6, SSDA8, SSDA9	I/O	Input/output pins for the I^2C data
	• Simple SPI mode		
	SCK0, SCK1, SCK5, SCK6, SCK8, SCK9	I/O	Input/output pins for the clock
	SMISO0, SMISO1, SMISO5, SMISO6, SMISO8, SMISO9	I/O	Input/output pins for slave transmission of data
	SMOSI0, SMOSI1, SMOSI5, SMOSI6, SMOSI8, SMOSI9	I/O	Input/output pins for master transmission of data
	SS0# to SS11#	Input	Chip-select input pins

Table 1.4 Pin Functions (3 / 4)

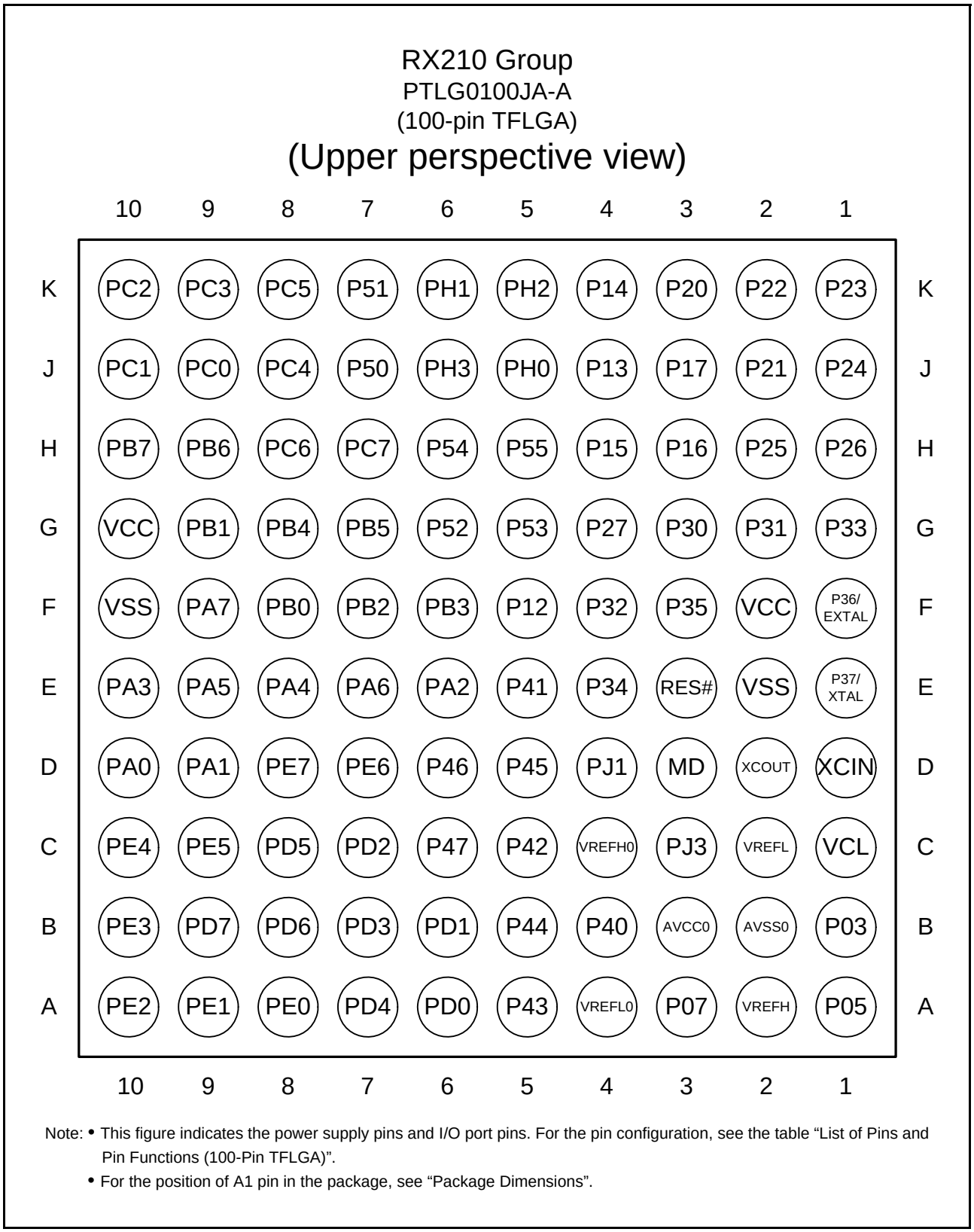
Classifications	Pin Name	I/O	Description
Serial communications interface (SCId)	• Asynchronous mode/clock synchronous mode		
	SCK12	I/O	Input/output pin for the clock signal
	RXD12	Input	Input pin for received data
	TXD12	Output	Output pin for transmitted data
	CTS12#	Input	Input pin for controlling the start of transmission and reception
	RTS12#	Output	Output pin for controlling the start of transmission and reception
	• Simple I^2C mode		
	SSCL12	I/O	Input/output pin for the I^2C clock
	SSDA12	I/O	Input/output pin for the I^2C data
	• Simple SPI mode		
	SCK12	I/O	Input/output pin for the clock
	SMISO12	I/O	Input/output pin for slave transmit data
	SMOSI12	I/O	Input/output pin for master transmit data
	SS12#	Input	Chip-select input pin
	• Extended serial mode		
	RXDX12	Input	Input pin for data reception by SCId
	TXDX12	Output	Output pin for data transmission by SCId
	SIOX12	I/O	Input/output pin for data reception or transmission by SCId
I^2C bus interface (RIIC)	SCL	I/O	Input/output pin for I^2C bus interface clocks. Bus can be directly driven by the NMOS open drain output.
	SDA	I/O	Input/output pin for I^2C bus interface data. Bus can be directly driven by the NMOS open drain output.
Serial peripheral interface (RSPI)	RSPCKA	I/O	Clock input/output pin for the RSPI.
	MOSIA	I/O	Input or output data output from the master for the RSPI.
	MISOA	I/O	Input or output data output from the slave for the RSPI.
	SSLA0	I/O	Input/output pin to select the slave for the RSPI.
	SSLA1 to SSLA3	Output	Output pins to select the slave for the RSPI.
12-bit A/D converter	AN000 to AN015	Input	Input pin for the analog signals to be processed by the A/D converter.
	ADTRG0#	Input	Input pin for the external trigger signals that start the A/D conversion.
D/A converter	DA0, DA1	Output	Output pins for the analog signals to be processed by the D/A converter.
Comparator A	CMPA1	Input	Input pin for the comparator A1 analog signals.
	CMPA2	Input	Input pin for the comparator A2 analog signals.
	CVREFA	Input	Input pin for the comparator reference voltage.
Comparator B	CMPB0	Input	Input pin for the comparator B0 analog signals.
	CVREFB0	Input	Input pin for the comparator B0 reference voltage.
	CMPB1	Input	Input pin for the comparator B1 analog signals.
	CVREFB1	Input	Input pin for the comparator B1 reference voltage.

Table 1.4 Pin Functions (4 / 4)

Classifications	Pin Name	I/O	Description
Analog power supply	AVCC0	Input	Analog voltage supply pin for the 12-bit A/D converter. Connect this pin to VCC if the 12-bit A/D converter is not to be used.
	AVSS0	Input	Analog ground pin for the 12-bit A/D converter. Connect this pin to VSS if the 12-bit A/D converter is not to be used.
	VREFH0	Input	Analog reference voltage supply pin for the 12-bit A/D converter. Connect this pin to VCC if the 12-bit A/D converter is not to be used.
	VREFL0	Input	Analog reference ground pin for the 12-bit A/D converter. Connect this pin to VSS if the 12-bit A/D converter is not to be used.
	VREFH	Input	Analog voltage supply pin for the D/A converter. Connect this pin to VCC if the D/A converter is not to be used.
	VREFL	Input	Analog ground pin for the D/A converter. Connect this pin to VSS if the D/A converter is not to be used.
I/O ports	P03, P05, P07	I/O	3-bit input/output pins.
	P12 to P17	I/O	6-bit input/output pins.
	P20 to P27	I/O	8-bit input/output pins.
	P30 to P37	I/O	8-bit input/output pins. (P35 input pins)
	P40 to P47	I/O	8-bit input/output pins.
	P50 to P55	I/O	6-bit input/output pins.
	PA0 to PA7	I/O	8-bit input/output pins.
	PB0 to PB7	I/O	8-bit input/output pins.
	PC0 to PC7	I/O	8-bit input/output pins.
	PD0 to PD7	I/O	8-bit input/output pins.
	PE0 to PE7	I/O	8-bit input/output pins.
	PH0 to PH3	I/O	4-bit input/output pins.
	PJ1, PJ3	I/O	2-bit input/output pins.

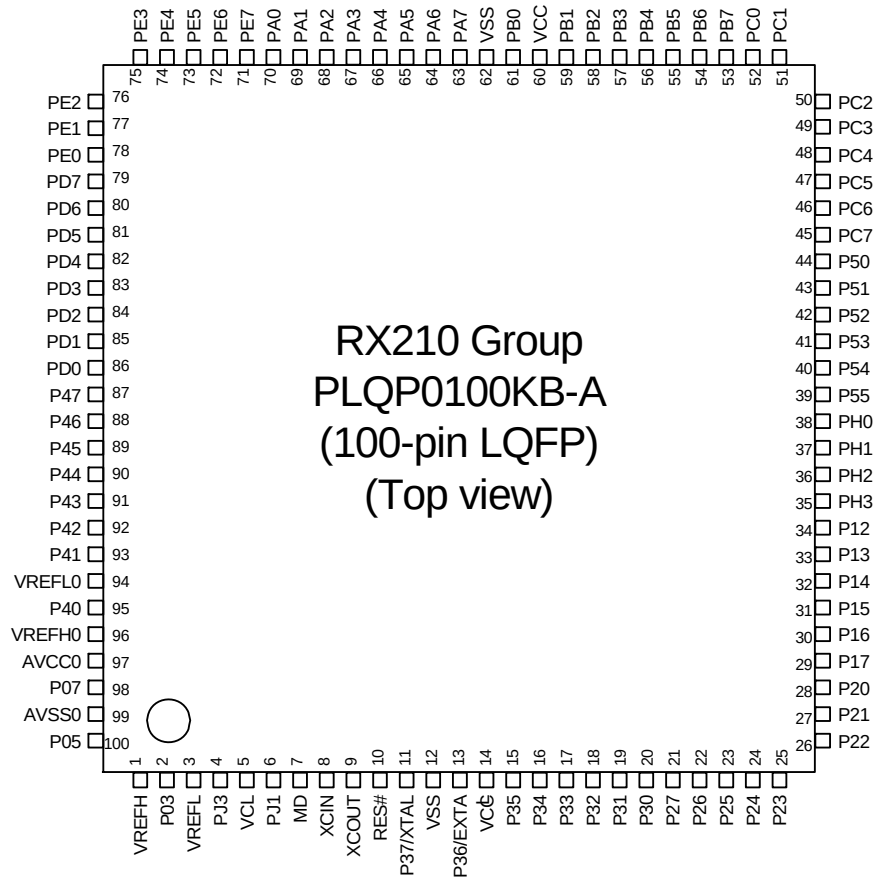
1.5 Pin Assignments

Figure 1.4 to Figure 1.6 show the pin assignments. Table 1.5 to Table 1.8 show the lists of pins and pin functions.



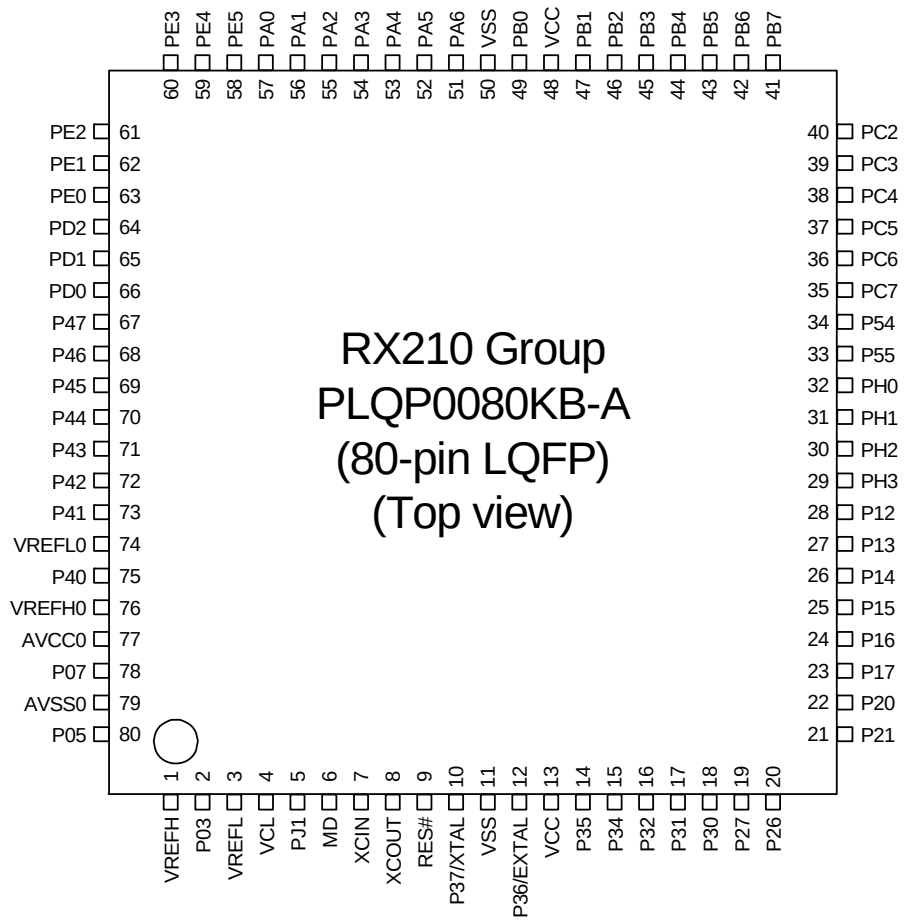
Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see the table “List of Pins and Pin Functions (100-Pin TFLGA)”.
• For the position of A1 pin in the package, see “Package Dimensions”.

Figure 1.3 Pin Assignments of the 100-Pin TFLGA (Upper Perspective View)



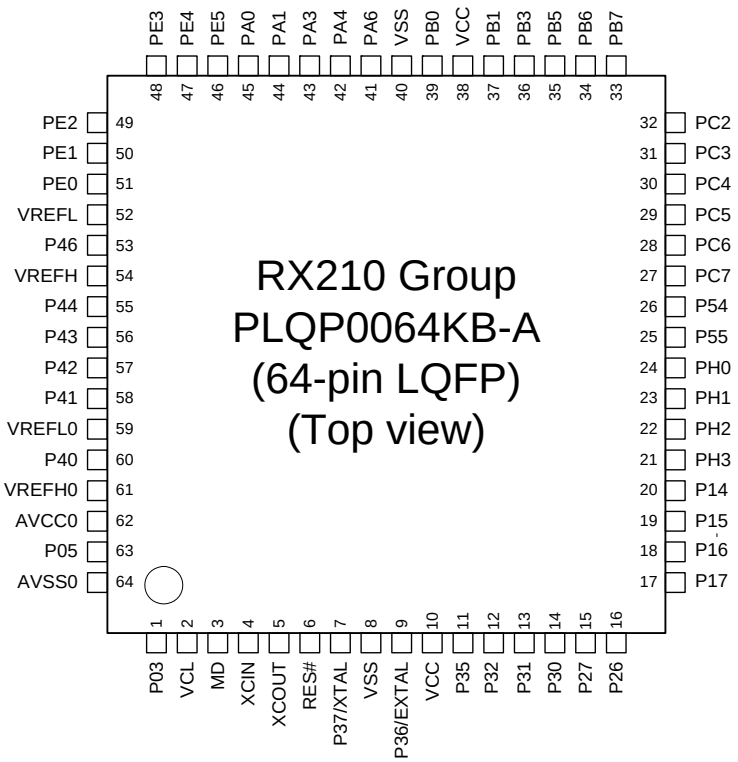
Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see the table “List of Pins and Pin Functions (100-Pin LQFP)”.

Figure 1.4 Pin Assignments of the 100-Pin LQFP



Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see the table “List of Pins and Pin Functions (80-Pin LQFP)”.

Figure 1.5 Pin Assignments of the 80-Pin LQFP



Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see the table “List of Pins and Pin Functions (64-Pin LQFP)”.

Figure 1.6 Pin Assignments of the 64-Pin LQFP

Table 1.5 List of Pins and Pin Functions (100-Pin TFLGA) (1 / 3)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU2, TMR, POE2)	Communications (SCIc, SCId, RSPI, RIIC)	Others
A1		P05				DA1
A2	VREFH					
A3		P07				ADTRG0#
A4	VREFL0					
A5		P43				AN003
A6		PD0	D0[A0/D0]			IRQ0
A7		PD4	D4[A4/D4]	POE3#		IRQ4
A8		PE0	D8[A8/D8]		SCK12	AN008
A9		PE1	D9[A9/D9]	MTIOC4C	TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12	AN009/CMPB0
A10		PE2	D10[A10/D10]	MTIOC4A	RXD12/RXDX12/ SMISO12/SSCL12	IRQ7-DS/AN010/ CVREFB0
B1		P03				DA0
B2	AVSS0					
B3	AVCC0					
B4		P40				AN000
B5		P44				AN004
B6		PD1	D1[A1/D1]	MTIOC4B		IRQ1
B7		PD3	D3[A3/D3]	POE8#		IRQ3
B8		PD6	D6[A6/D6]	MTIC5V/POE1#		IRQ6
B9		PD7	D7[A7/D7]	MTIC5U/POE0#		IRQ7
B10		PE3	D11[A11/D11]	MTIOC4B/POE8#	CTS12#/RTS12#/SS12#	AN011/CMPA1
C1	VCL					
C2	VREFL					
C3		PJ3		MTIOC3C	CTS6#/RTS6#/SS6#	
C4	VREFH0					
C5		P42				AN002
C6		P47				AN007
C7		PD2	D2[A2/D2]	MTIOC4D		IRQ2
C8		PD5	D5[A5/D5]	MTIC5W/POE2#		IRQ5
C9		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B		IRQ5/AN013
C10		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A		AN012/CMPA2
D1	XCIN					
D2	XCOUT					
D3	MD					FINED
D4		PJ1		MTIOC3A		
D5		P45				AN005
D6		P46				AN006
D7		PE6	D14[A14/D14]			IRQ6/AN014
D8		PE7	D15[A15/D15]			IRQ7/AN015
D9		PA1	A1	MTIOC0B/MTCLKC	SCK5/SSLA2	CVREFA
D10		PA0	A0/BC0#	MTIOC4A	SSLA1	CACREF
E1	XTAL	P37				
E2	VSS					
E3	RES#					
E4		P34		MTIOC0A/TMCI3/ POE2#	SCK6	IRQ4
E5		P41				AN001
E6		PA2	A2		RXD5/SMISO5/SSCL5/ SSLA3	

Table 1.5 List of Pins and Pin Functions (100-Pin TFLGA) (2 / 3)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU2, TMR, POE2)	Communications (SCIc, SCId, RSPI, RIIC)	Others
E7		PA6	A6	MTIC5V/MTCLKB/ TMCI3/POE2#	CTS5#/RTS5#/SS5#/ MOSIA	
E8		PA4	A4	MTIC5U/MTCLKA/ TMRI0	TXD5/SMOSI5/SSDA5/ SSLA0	IRQ5-DS/CVREFB1
E9		PA5	A5		RSPCKA	
E10		PA3	A3	MTIOC0D/MTCLKD	RXD5/SMISO5/SSCL5	IRQ6-DS/CMPB1
F1	EXTAL	P36				
F2	VCC					
F3		P35				NMI
F4		P32		MTIOC0C/TMO3	TXD6/SMOSI6/SSDA6	IRQ2-DS/RTCOUT/ RTCIC2
F5		P12		TMCI1	SCL	IRQ2
F6		PB3	A11	MTIOC0A/MTIOC4A/ TMO0/POE3#	SCK6	
F7		PB2	A10		CTS6#/RTS6#/SS6#	
F8		PB0	A8	MTIC5W	RXD6/SMISO6/SSCL6/ RSPCKA	
F9		PA7	A7		MISOA	
F10	VSS					
G1		P33		MTIOC0D/TMRI3/ POE3#	RXD6/SMISO6/SSCL6	IRQ3-DS
G2		P31		MTIOC4D/TMCI2	CTS1#/RTS1#/SS1#	IRQ1-DS/RTCIC1
G3		P30		MTIOC4B/TMRI3/ POE8#	RXD1/SMISO1/SSCL1	IRQ0-DS/RTCIC0
G4		P27	CS3#	MTIOC2B/TMCI3	SCK1	FINEC
G5	BCLK	P53				
G6		P52	RD#			
G7		PB5	A13	MTIOC2A/MTIOC1B/ TMRI1/POE1#	SCK9	
G8		PB4	A12		CTS9#/RTS9#/SS9#	
G9		PB1	A9	MTIOC0C/MTIOC4C/ TMCI0	TXD6/SMOSI6/SSDA6	IRQ4-DS
G10	VCC					
H1		P26	CS2#	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1	
H2		P25	CS1#	MTIOC4C/MTCLKB		ADTRG0#
H3		P16		MTIOC3C/MTIOC3D/ TMO2	TXD1/SMOSI1/SSDA1/ MOSIA/SCL-DS	IRQ6/RTCOUT/ ADTRG0#
H4		P15		MTIOC0B/MTCLKB/ TMCI2	RXD1/SMISO1/SSCL1	IRQ5
H5		P55	WAIT#	MTIOC4D/TMO3		
H6		P54	ALE	MTIOC4B/TMCI1		
H7		PC7	A23/CS0#	MTIOC3A/TMO2/ MTCLKB	TXD8/SMOSI8/SSDA8/ MISOA	CACREF
H8		PC6	A22/CS1#	MTIOC3C/MTCLKA/ TMCI2	RXD8/SMISO8/SSCL8/ MOSIA	
H9		PB6	A14	MTIOC3D	RXD9/SMISO9/SSCL9	
H10		PB7	A15	MTIOC3B	TXD9/SMOSI9/SSDA9	
J1		P24	CS0#	MTIOC4A/MTCLKA/ TMRI1		
J2		P21		MTIOC1B/TMCI0	RXD0/SMISO0/SSCL0	
J3		P17		MTIOC3A/MTIOC3B/ TMO1/POE8#	SCK1/MISOA/ SDA-DS	IRQ7
J4		P13		MTIOC0B/TMO3	SDA	IRQ3
J5		PH0				CACREF

Table 1.5 List of Pins and Pin Functions (100-Pin TFLGA) (3 / 3)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU2, TMR, POE2)	Communications (SCIc, SCId, RSPI, RIIC)	Others
J6		PH3		TMCI0		
J7		P50	WR0#/WR#			
J8		PC4	A20/CS3#	MTIOC3D/MTCLKC/ TMCI1/POE0#	SCK5/CTS8#/RTS8#/ SS8#/SSLA0	
J9		PC0	A16	MTIOC3C	CTS5#/RTS5#/SS5#/ SSLA1	
J10		PC1	A17	MTIOC3A	SCK5/SSLA2	
K1		P23		MTIOC3D/MTCLKD	CTS0#/RTS0#/SS0#	
K2		P22		MTIOC3B/MTCLKC/ TMO0	SCK0	
K3		P20		MTIOC1A/TMRI0	TXD0/SMOSI0/SSDA0	
K4		P14		MTIOC3A/MTCLKA/ TMRI2	CTS1#/RTS1#/SS1#	IRQ4
K5		PH2		TMRI0		IRQ1
K6		PH1		TMO0		IRQ0
K7		P51	WR1#/BC1#/WAIT#			
K8		PC5	A21/CS2#/WAIT#	MTIOC3B/MTCLKD/ TMRI2	SCK8/RSPCKA	
K9		PC3	A19	MTIOC4D	TXD5/SMOSI5/SSDA5	
K10		PC2	A18	MTIOC4B	RXD5/SMISO5/SSCL5/ SSLA3	

Note: • Pin names to which –DS is appended are for pins that can be used to trigger release from deep software standby mode.

Table 1.6 List of Pins and Pin Functions (100-Pin LQFP) (1 / 3)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU2, TMR, POE2)	Communications (SCIc, SCId, RSPI, RIIC)	Others
1	VREFH					
2		P03				DA0
3	VREFL					
4		PJ3		MTIOC3C	CTS6#/RTS6#/SS6#	
5	VCL					
6		PJ1		MTIOC3A		
7	MD					FINED
8	XCIN					
9	XCOUT					
10	RES#					
11	XTAL	P37				
12	VSS					
13	EXTAL	P36				
14	VCC					
15		P35				NMI
16		P34		MTIOC0A/TMCI3/ POE2#	SCK6	IRQ4
17		P33		MTIOC0D/TMRI3/ POE3#	RXD6/SMISO6/SSCL6	IRQ3-DS
18		P32		MTIOC0C/TMO3	TXD6/SMOSI6/SSDA6	IRQ2-DS/RTCOUT/ RTCIC2
19		P31		MTIOC4D/TMCI2	CTS1#/RTS1#/SS1#	IRQ1-DS/RTCIC1
20		P30		MTIOC4B/TMRI3/ POE8#	RXD1/SMISO1/SSCL1	IRQ0-DS/RTCIC0
21		P27	CS3#	MTIOC2B/TMCI3	SCK1	FINEC
22		P26	CS2#	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1	
23		P25	CS1#	MTIOC4C/MTCLKB		ADTRG0#
24		P24	CS0#	MTIOC4A/MTCLKA/ TMRI1		
25		P23		MTIOC3D/MTCLKD	CTS0#/RTS0#/SS0#	
26		P22		MTIOC3B/MTCLKC/ TMO0	SCK0	
27		P21		MTIOC1B/TMCI0	RXD0/SMISO0/SSCL0	
28		P20		MTIOC1A/TMRI0	TXD0/SMOSI0/SSDA0	
29		P17		MTIOC3A/MTIOC3B/ TMO1/POE8#	SCK1/MISOA/ SDA-DS	IRQ7
30		P16		MTIOC3C/MTIOC3D/ TMO2	TXD1/SMOSI1/SSDA1/ MOSIA/SCL-DS	IRQ6/RTCOUT/ ADTRG0#
31		P15		MTIOC0B/MTCLKB/ TMCI2	RXD1/SMISO1/SSCL1	IRQ5
32		P14		MTIOC3A/MTCLKA/ TMRI2	CTS1#/RTS1#/SS1#	IRQ4
33		P13		MTIOC0B/TMO3	SDA	IRQ3
34		P12		TMCI1	SCL	IRQ2
35		PH3		TMCI0		
36		PH2		TMRI0		IRQ1
37		PH1		TMO0		IRQ0
38		PH0				CACREF
39		P55	WAIT#	MTIOC4D/TMO3		
40		P54	ALE	MTIOC4B/TMCI1		
41	BCLK	P53				
42		P52	RD#			

Table 1.6 List of Pins and Pin Functions (100-Pin LQFP) (2 / 3)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU2, TMR, POE2)	Communications (SCIc, SCId, RSPI, RIIC)	Others
43		P51	WR1#/BC1#/WAIT#			
44		P50	WR0#/WR#			
45		PC7	A23/CS0#	MTIOC3A/TMO2/ MTCLKB	TXD8/SMOSI8/SSDA8/ MISOA	CACREF
46		PC6	A22/CS1#	MTIOC3C/MTCLKA/ TMCI2	RXD8/SMISO8/SSCL8/ MOSIA	
47		PC5	A21/CS2#/WAIT#	MTIOC3B/MTCLKD/ TMRI2	SCK8/RSPCKA	
48		PC4	A20/CS3#	MTIOC3D/MTCLKC/ TMCI1/POE0#	SCK5/CTS8#/RTS8#/ SS8#/SSLA0	
49		PC3	A19	MTIOC4D	TXD5/SMOSI5/SSDA5	
50		PC2	A18	MTIOC4B	RXD5/SMISO5/SSCL5/ SSLA3	
51		PC1	A17	MTIOC3A	SCK5/SSLA2	
52		PC0	A16	MTIOC3C	CTS5#/RTS5#/SS5#/ SSLA1	
53		PB7	A15	MTIOC3B	TXD9/SMOSI9/SSDA9	
54		PB6	A14	MTIOC3D	RXD9/SMISO9/SSCL9	
55		PB5	A13	MTIOC2A/MTIOC1B/ TMRI1/POE1#	SCK9	
56		PB4	A12		CTS9#/RTS9#/SS9#	
57		PB3	A11	MTIOC0A/MTIOC4A/ TMO0/POE3#	SCK6	
58		PB2	A10		CTS6#/RTS6#/SS6#	
59		PB1	A9	MTIOC0C/MTIOC4C/ TMCI0	TXD6/SMOSI6/SSDA6	IRQ4-DS
60	VCC					
61		PB0	A8	MTIC5W	RXD6/SMISO6/SSCL6/ RSPCKA	
62	VSS					
63		PA7	A7		MISOA	
64		PA6	A6	MTIC5V/MTCLKB/ TMCI3/POE2#	CTS5#/RTS5#/SS5#/ MOSIA	
65		PA5	A5		RSPCKA	
66		PA4	A4	MTIC5U/MTCLKA/ TMRI0	TXD5/SMOSI5/SSDA5/ SSLA0	IRQ5-DS/CVREFB1
67		PA3	A3	MTIOC0D/MTCLKD	RXD5/SMISO5/SSCL5	IRQ6-DS/CMPB1
68		PA2	A2		RXD5/SMISO5/SSCL5/ SSLA3	
69		PA1	A1	MTIOC0B/MTCLKC	SCK5/SSLA2	CVREFA
70		PA0	A0/BC0#	MTIOC4A	SSLA1	CACREF
71		PE7	D15[A15/D15]			IRQ7/AN015
72		PE6	D14[A14/D14]			IRQ6/AN014
73		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B		IRQ5/AN013
74		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A		AN012/CMPA2
75		PE3	D11[A11/D11]	MTIOC4B/POE8#	CTS12#/RTS12#/SS12#	AN011/CMPA1
76		PE2	D10[A10/D10]	MTIOC4A	RXD12/RXDX12/ SMISO12/SSCL12	IRQ7-DS/AN010/ CVREFB0
77		PE1	D9[A9/D9]	MTIOC4C	TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12	AN009/CMPB0
78		PE0	D8[A8/D8]		SCK12	AN008
79		PD7	D7[A7/D7]	MTIC5U/POE0#		IRQ7
80		PD6	D6[A6/D6]	MTIC5V/POE1#		IRQ6
81		PD5	D5[A5/D5]	MTIC5W/POE2#		IRQ5

Table 1.6 List of Pins and Pin Functions (100-Pin LQFP) (3 / 3)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU2, TMR, POE2)	Communications (SCIc, SCId, RSPI, RIIC)	Others
82		PD4	D4[A4/D4]	POE3#		IRQ4
83		PD3	D3[A3/D3]	POE8#		IRQ3
84		PD2	D2[A2/D2]	MTIOC4D		IRQ2
85		PD1	D1[A1/D1]	MTIOC4B		IRQ1
86		PD0	D0[A0/D0]			IRQ0
87		P47				AN007
88		P46				AN006
89		P45				AN005
90		P44				AN004
91		P43				AN003
92		P42				AN002
93		P41				AN001
94	VREFL0					
95		P40				AN000
96	VREFH0					
97	AVCC0					
98		P07				ADTRG0#
99	AVSS0					
100		P05				DA1

Note: • Pin names to which –DS is appended are for pins that can be used to trigger release from deep software standby mode.

Table 1.7 List of Pins and Pin Functions (80-Pin LQFP) (1 / 2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU2, TMR, POE2)	Communications (SCIc, SCId, RSPI, RIIC)	Others
1	VREFH				
2		P03			DA0
3	VREFL				
4	VCL				
5		PJ1	MTIOC3A		
6	MD				FINED
7	XCIN				
8	XCOUT				
9	RES#				
10	XTAL	P37			
11	VSS				
12	EXTAL	P36			
13	VCC				
14		P35			NMI
15		P34	MTIOC0A/TMCI3/POE2#	SCK6	IRQ4
16		P32	MTIOC0C/TMO3	TXD6/SMOSI6/SSDA6	IRQ2-DS/RTCOUT/ RTCIC2
17		P31	MTIOC4D/TMCI2	CTS1#/RTS1#/SS1#	IRQ1-DS/RTCIC1
18		P30	MTIOC4B/TMRI3/POE8#	RXD1/SMISO1/SSCL1	IRQ0-DS/RTCIC0
19		P27	MTIOC2B/TMCI3	SCK1	FINEC
20		P26	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1	
21		P21	MTIOC1B/TMCI0	RXD0/SMISO0/SSCL0	
22		P20	MTIOC1A/TMRI0	TXD0/SMOSI0/SSDA0	
23		P17	MTIOC3A/MTIOC3B/TMO1/ POE8#	SCK1/MISOA/ SDA-DS	IRQ7
24		P16	MTIOC3C/MTIOC3D/TMO2	TXD1/SMOSI1/SSDA1/MOSIA/ SCL-DS	IRQ6/RTCOUT/ ADTRG0#
25		P15	MTIOC0B/MTCLKB/TMCI2	RXD1/SMISO1/SSCL1	IRQ5
26		P14	MTIOC3A/MTCLKA/TMRI2	CTS1#/RTS1#/SS1#	IRQ4
27		P13	MTIOC0B/TMO3	SDA	IRQ3
28		P12	TMCI1	SCL	IRQ2
29		PH3	TMCI0		
30		PH2	TMRI0		IRQ1
31		PH1	TMO0		IRQ0
32		PH0			CACREF
33		P55	MTIOC4D/TMO3		
34		P54	MTIOC4B/TMCI1		
35		PC7	MTIOC3A/TMO2/MTCLKB	TXD8/SMOSI8/SSDA8/MISOA	CACREF
36		PC6	MTIOC3C/MTCLKA/TMCI2	RXD8/SMISO8/SSCL8/MOSIA	
37		PC5	MTIOC3B/MTCLKD/TMRI2	SCK8/RSPCKA	
38		PC4	MTIOC3D/MTCLKC/TMCI1/ POE0#	SCK5/CTS8#/RTS8#/SS8#/ SSLA0	
39		PC3	MTIOC4D	TXD5/SMOSI5/SSDA5	
40		PC2	MTIOC4B	RXD5/SMISO5/SSCL5/SSLA3	
41		PB7	MTIOC3B	TXD9/SMOSI9/SSDA9	
42		PB6	MTIOC3D	RXD9/SMISO9/SSCL9	
43		PB5	MTIOC2A/MTIOC1B/TMRI1/ POE1#	SCK9	
44		PB4		CTS9#/RTS9#/SS9#	
45		PB3	MTIOC0A/MTIOC4A/TMO0/ POE3#	SCK6	

Table 1.7 List of Pins and Pin Functions (80-Pin LQFP) (2 / 2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU2, TMR, POE2)	Communications (SCIc, SCId, RSPI, RIIC)	Others
46		PB2		CTS6#/RTS6#/SS6#	
47		PB1	MTIOC0C/MTIOC4C/TMCI0	TXD6/SMOSI6/SSDA6	IRQ4-DS
48	VCC				
49		PB0	MTIC5W	RXD6/SMISO6/SSCL6/RSPCKA	
50	VSS				
51		PA6	MTIC5V/MTCLKB/TMCI3/ POE2#	CTS5#/RTS5#/SS5#/MOSIA	
52		PA5		RSPCKA	
53		PA4	MTIC5U/MTCLKA/TMRI0	TXD5/SMOSI5/SSDA5/SSLA0	IRQ5-DS/CVREFB1
54		PA3	MTIOC0D/MTCLKD	RXD5/SMISO5/SSCL5	IRQ6-DS/CMPB1
55		PA2		RXD5/SMISO5/SSCL5/SSLA3	
56		PA1	MTIOC0B/MTCLKC	SCK5/SSLA2	CVREFA
57		PA0	MTIOC4A	SSLA1	CACREF
58		PE5	MTIOC4C/MTIOC2B		IRQ5/AN013
59		PE4	MTIOC4D/MTIOC1A		AN012/CMPA2
60		PE3	MTIOC4B/POE8#	CTS12#/RTS12#/SS12#	AN011/CMPA1
61		PE2	MTIOC4A	RXD12/RXDX12/SMISO12/ SSCL12	IRQ7-DS/AN010/ CVREFB0
62		PE1	MTIOC4C	TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12	AN009/CMPB0
63		PE0		SCK12	AN008
64		PD2	MTIOC4D		IRQ2
65		PD1	MTIOC4B		IRQ1
66		PD0			IRQ0
67		P47			AN007
68		P46			AN006
69		P45			AN005
70		P44			AN004
71		P43			AN003
72		P42			AN002
73		P41			AN001
74	VREFL0				
75		P40			AN000
76	VREFH0				
77	AVCC0				
78		P07			ADTRG0#
79	AVSS0				
80		P05			DA1

Note: • Pin names to which –DS is appended are for pins that can be used to trigger release from deep software standby mode.

Table 1.8 List of Pins and Pin Functions (64-Pin LQFP) (1 / 2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU2, TMR, POE2)	Communication (SCIc, SCId, RSPI, RIIC)	Others
1		P03			DA0
2	VCL				
3	MD				FINED
4	XCIN				
5	XCOUT				
6	RES#				
7	XTAL	P37			
8	VSS				
9	EXTAL	P36			
10	VCC				
11		P35			NMI
12		P32	MTIOC0C/TMO3	TXD6/SMOSI6/SSDA6	IRQ2-DS/RTCOUT/ RTCIC2
13		P31	MTIOC4D/TMCI2	CTS1#/RTS1#/SS1#	IRQ1-DS/RTCIC1
14		P30	MTIOC4B/TMRI3/POE8#	RXD1/SMISO1/SSCL1	IRQ0-DS/RTCIC0
15		P27	MTIOC2B/TMCI3	SCK1	FINEC
16		P26	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1	
17		P17	MTIOC3A/MTIOC3B/TMO1/ POE8#	SCK1/MISOA/SDA-DS	IRQ7
18		P16	MTIOC3C/MTIOC3D/TMO2	TXD1/SMOSI1/SSDA1/MOSIA/ SCL-DS	IRQ6/RTCOUT/ ADTRG0#
19		P15	MTIOC0B/MTCLKB/TMCI2	RXD1/SMISO1/SSCL1	IRQ5
20		P14	MTIOC3A/MTCLKA/TMRI2	CTS1#/RTS1#/SS1#	IRQ4
21		PH3	TMCI0		
22		PH2	TMRI0		IRQ1
23		PH1	TMO0		IRQ0
24		PH0			CACREF
25		P55	MTIOC4D/TMO3		
26		P54	MTIOC4B/TMCI1		
27		PC7	MTIOC3A/TMO2/MTCLKB	TXD8/SMOSI8/SSDA8/MISOA	CACREF
28		PC6	MTIOC3C/MTCLKA/TMCI2	RXD8/SMISO8/SSCL8/MOSIA	
29		PC5	MTIOC3B/MTCLKD/TMRI2	SCK8/RSPCKA	
30		PC4	MTIOC3D/MTCLKC/TMCI1/ POE0#	SCK5/CTS8#/RTS8#/SS8#/ SSLA0	
31		PC3	MTIOC4D	TXD5/SMOSI5/SSDA5	
32		PC2	MTIOC4B	RXD5/SMISO5/SSCL5/SSLA3	
33		PB7	MTIOC3B	TXD9/SMOSI9/SSDA9	
34		PB6	MTIOC3D	RXD9/SMISO9/SSCL9	
35		PB5	MTIOC2A/MTIOC1B/TMRI1/ POE1#	SCK9	
36		PB3	MTIOC0A/MTIOC4A/TMO0/ POE3#	SCK6	
37		PB1	MTIOC0C/MTIOC4C/TMCI0	TXD6/SMOSI6/SSDA6	IRQ4-DS
38	VCC				
39		PB0	MTIC5W	RXD6/SMISO6/SSCL6/RSPCKA	
40	VSS				
41		PA6	MTIC5V/MTCLKB/TMCI3/ POE2#	CTS5#/RTS5#/SS5#/MOSIA	
42		PA4	MTIC5U/MTCLKA/TMRI0	TXD5/SMOSI5/SSDA5/SSLA0	IRQ5-DS/CVREFB1
43		PA3	MTIOC0D/MTCLKD	RXD5/SMISO5/SSCL5	IRQ6-DS/CMPB1
44		PA1	MTIOC0B/MTCLKC	SCK5/SSLA2	CVREFA

Table 1.8 List of Pins and Pin Functions (64-Pin LQFP) (2 / 2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU2, TMR, POE2)	Communication (SCIc, SCId, RSPI, RIIC)	Others
45		PA0	MTIOC4A	SSLA1	CACREF
46		PE5	MTIOC4C/MTIOC2B		IRQ5/AN013
47		PE4	MTIOC4D/MTIOC1A		AN012/CMPA2
48		PE3	MTIOC4B/POE8#	CTS12#/RTS12#/SS12#	AN011/CMPA1
49		PE2	MTIOC4A	RXD12/RXDX12/SMISO12/ SSCL12	IRQ7-DS/AN010/ CVREFB0
50		PE1	MTIOC4C	TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12	AN009/CMPB0
51		PE0		SCK12	AN008
52	VREFL				
53		P46			AN006
54	VREFH				
55		P44			AN004
56		P43			AN003
57		P42			AN002
58		P41			AN001
59	VREFL0				
60		P40			AN000
61	VREFH0				
62	AVCC0				
63		P05			DA1
64	AVSS0				

Note: • Pin names to which –DS is appended are for pins that can be used to trigger release from deep software standby mode.

2. CPU

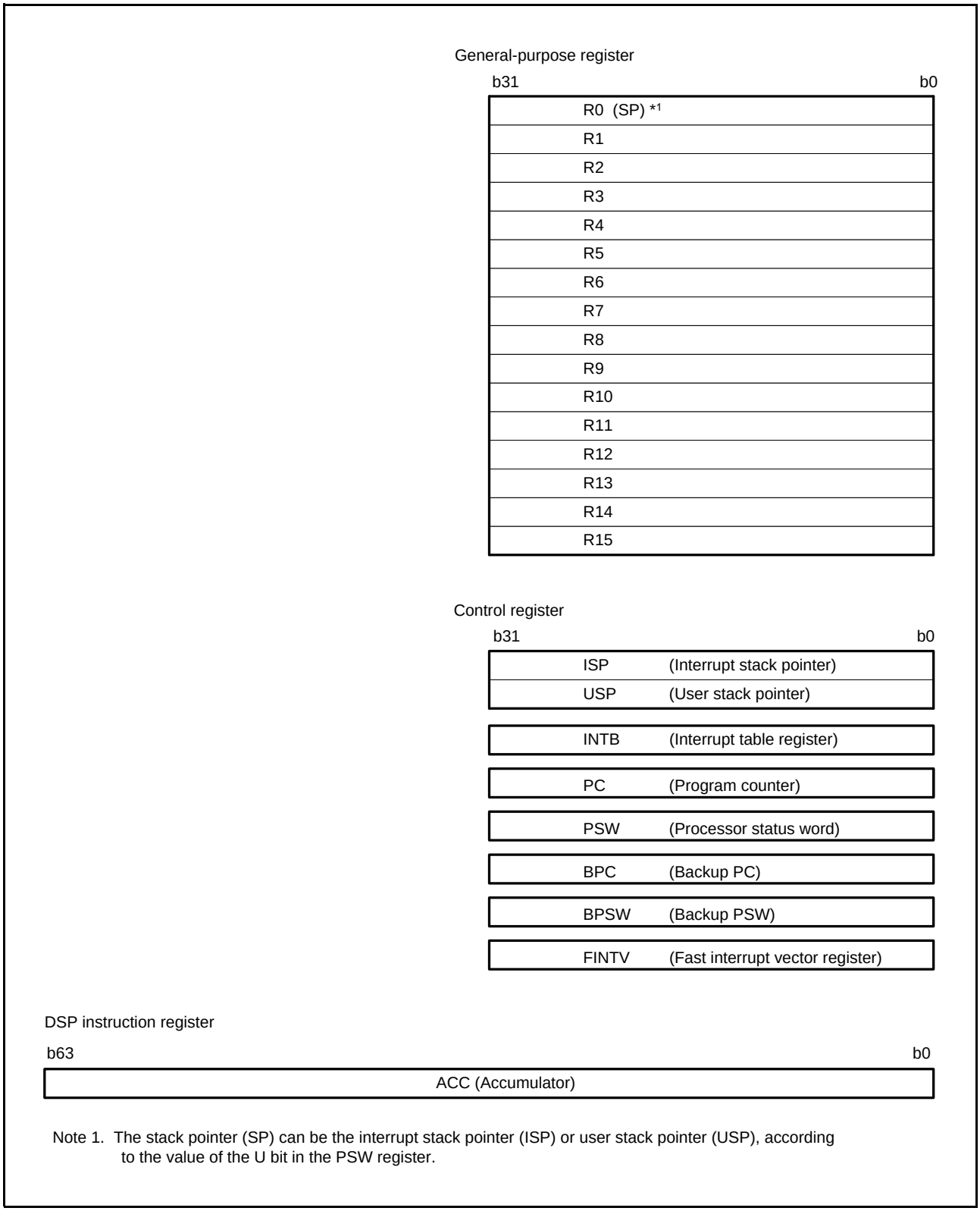
The RX210 Group is an MCU with the high-speed, high-performance RX CPU as its core.
A variable-length instruction format has been adopted for the RX CPU. Allocating the more frequently used instructions to the shorter instruction lengths facilitates the development of efficient programs that take up less memory.
The CPU has 73 basic instructions and and nine DSP instructions, for a total of 82 instructions. It has 10 addressing modes and caters to register–register operations, register–memory operations, immediate–register operations, immediate–memory operations, memory–memory transfer, and bitwise operations. High-speed operation was realized by achieving execution in a single cycle not only for register–register operations, but also for other types of multiple instructions. The CPU includes an internal multiplier and an internal divider for high-speed multiplication and division.
The RX CPU has a five-stage pipeline for processing instructions. The stages are instruction fetching, instruction decoding, execution, memory access, and write-back. In cases where pipeline processing is drawn-out by memory access, subsequent operations may in fact be executed earlier. By adopting “out-of-order completion” of this kind, the execution of instructions is controlled to optimize numbers of clock cycles.

2.1 Features

- High instruction execution rate: One instruction in one clock cycle
- Address space: 4-Gbyte linear
- Register set of the CPU
  General purpose: Sixteen 32-bit registers
  Control: Eight 32-bit registers
  Accumulator: One 64-bit register
- Basic instructions: 73 (arithmetic/logic instructions, data-transfer instructions, branch instructions, bit-manipulation instructions, string-manipulation instructions, and system-manipulation instructions)
  Relative branch instructions to suit branch distances
  Variable-length instruction format (lengths from one to eight bytes)
  Short formats for frequently used instructions
- DSP instructions: 9
  Supports 16-bit × 16-bit multiplication and multiply-and-accumulate operations.
  Rounds the data in the accumulator.
- Addressing modes: 10
- Five-stage pipeline
  Adoption of out-of-order completion
- Processor modes
  A supervisor mode and a user mode are supported.
- Data arrangement
  Selectable as little endian or big endian

2.2 Register Set of the CPU

The RX CPU has sixteen general-purpose registers, eight control registers, and one accumulator used for DSP instructions.



Note 1. The stack pointer (SP) can be the interrupt stack pointer (ISP) or user stack pointer (USP), according to the value of the U bit in the PSW register.

Figure 2.1 Register Set of the CPU

2.2.1 General-Purpose Registers (R0 to R15)

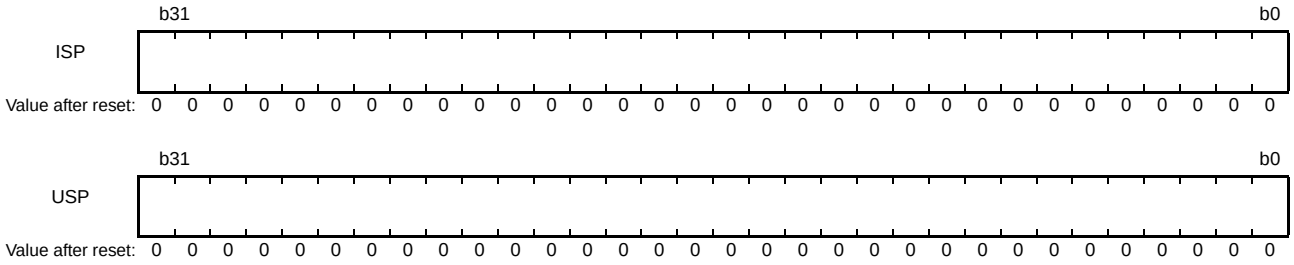
This CPU has sixteen general-purpose registers (R0 to R15). R1 to R15 can be used as data registers or address registers. R0, a general-purpose register, also functions as the stack pointer (SP). The stack pointer is switched to operate as the interrupt stack pointer (ISP) or user stack pointer (USP) by the value of the stack pointer select bit (U) in the processor status word (PSW).

2.2.2 Control Registers

This CPU has the following eight control registers.

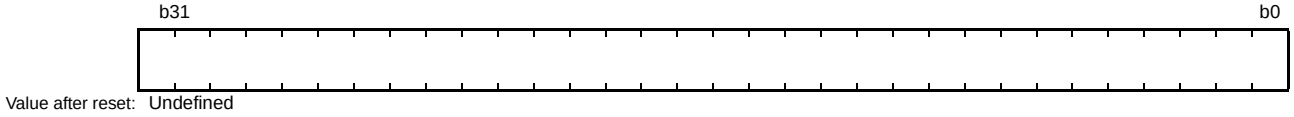
- Interrupt stack pointer (ISP)
- User stack pointer (USP)
- Interrupt table register (INTB)
- Program counter (PC)
- Processor status word (PSW)
- Backup PC (BPC)
- Backup PSW (BPSW)
- Fast interrupt vector register (FINTV)

2.2.2.1 Interrupt Stack Pointer (ISP)/User Stack Pointer (USP)



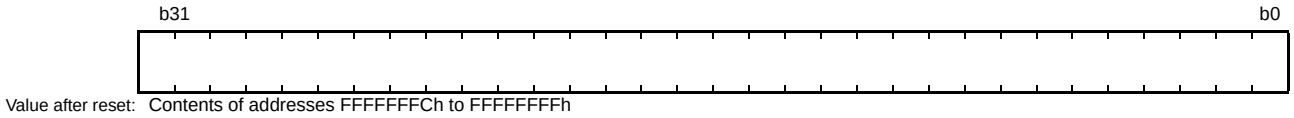
The stack pointer (SP) can be either of two types, the interrupt stack pointer (ISP) or the user stack pointer (USP). Whether the stack pointer operates as the ISP or USP depends on the value of the stack pointer select bit (U) in the processor status word (PSW).
Set the ISP or USP to a multiple of four, as this reduces the numbers of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

2.2.2.2 Interrupt Table Register (INTB)



The interrupt table register (INTB) specifies the address where the relocatable vector table starts.

2.2.2.3 Program Counter (PC)



The program counter (PC) indicates the address of the instruction being executed.

2.2.2.4 Processor Status Word (PSW)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	IPL[3:0]				—	—	—	PM	—	—	U	I
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	O	S	Z	C
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	C	Carry Flag	0: No carry has occurred. 1: A carry has occurred.	R/W
b1	Z	Zero Flag	0: Result is non-zero. 1: Result is 0.	R/W
b2	S	Sign Flag	0: Result is a positive value or 0. 1: Result is a negative value.	R/W
b3	O	Overflow Flag	0: No overflow has occurred. 1: An overflow has occurred.	R/W
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b16	I*1	Interrupt Enable	0: Interrupt disabled. 1: Interrupt enabled.	R/W
b17	U*1	Stack Pointer Select	0: Interrupt stack pointer (ISP) is selected. 1: User stack pointer (USP) is selected.	R/W
b19, b18	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b20	PM*1,*2,*3	Processor Mode Select	0: Supervisor mode is selected. 1: User mode is selected.	R/W
b23 to b21	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b27 to b24	IPL[3:0]*1	Processor Interrupt Priority Level	b27 b24 0 0 0 0: Priority level 0 (lowest) 0 0 0 1: Priority level 1 0 0 1 0: Priority level 2 0 0 1 1: Priority level 3 0 1 0 0: Priority level 4 0 1 0 1: Priority level 5 0 1 1 0: Priority level 6 0 1 1 1: Priority level 7 1 0 0 0: Priority level 8 1 0 0 1: Priority level 9 1 0 1 0: Priority level 10 1 0 1 1: Priority level 11 1 1 0 0: Priority level 12 1 1 0 1: Priority level 13 1 1 1 0: Priority level 14 1 1 1 1: Priority level 15 (highest)	R/W
b31 to b28	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. In user mode, writing to the IPL[3:0], PM, U, and I bits by an MVTC or a POPC instruction is ignored. Writing to the IPL[3:0] bits by an MVTIPL instruction generates a privileged instruction exception.
Note 2. In supervisor mode, writing to the PM bit by an MVTC or a POPC instruction is ignored, but writing to the other bits is possible.
Note 3. Switching from supervisor mode to user mode requires execution of an RTE instruction after having set the PSW.PM bit saved on the stack to 1 or executing an RTFI instruction after having set the BPSW.PM bit to 1.

The processor status word (PSW) indicates the results of instruction execution or the state of the CPU.

C Flag (Carry Flag)

This flag indicates whether a carry, borrow, or shift-out has occurred as the result of an operation.

Z Flag (Zero Flag)

This flag indicates that the result of an operation was 0.

S Flag (Sign Flag)

This flag indicates that the result of an operation was negative.

O Flag (Overflow Flag)

This flag indicates that an overflow occurred during an operation.

I Bit (Interrupt Enable)

This bit enables interrupt requests. When an exception is accepted, the value of this bit becomes 0.

U Bit (Stack Pointer Select)

This bit specifies the stack pointer as either the ISP or USP. When an exception request is accepted, this bit is set to 0. When the processor mode is switched from supervisor mode to user mode, this bit is set to 1.

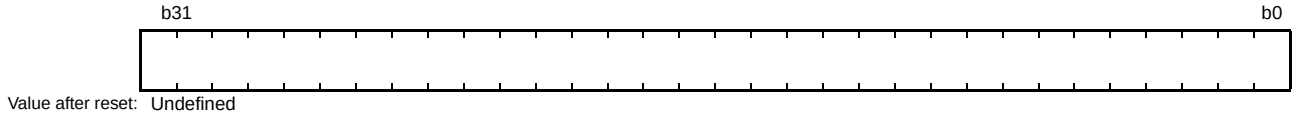
PM Bit (Processor Mode Select)

This bit specifies the processor mode. When an exception is accepted, the value of this bit becomes 0.

IPL[3:0] Bits (Processor Interrupt Priority Level)

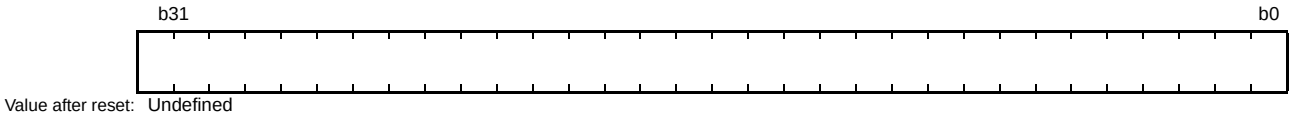
The IPL[3:0] bits specify the processor interrupt priority level as one of sixteen levels from zero to fifteen, wherein priority level zero is the lowest and priority level fifteen the highest. When the priority level of a requested interrupt is higher than the processor interrupt priority level, the interrupt is enabled. Setting the IPL[3:0] bits to level fifteen (Fh) disables all interrupt requests. The IPL[3:0] bits are set to level fifteen (Fh) when a non-maskable interrupt is generated. When interrupts in general are generated, the bits are set to the priority levels of accepted interrupts.

2.2.2.5 Backup PC (BPC)



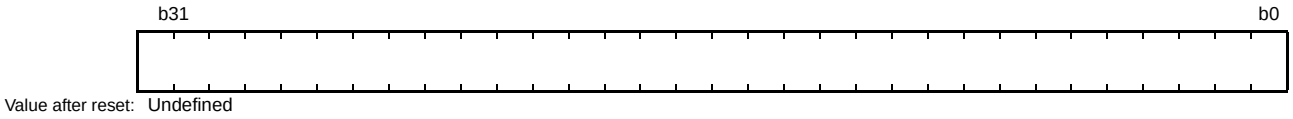
The backup PC (BPC) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the program counter (PC) are saved in the BPC register.

2.2.2.6 Backup PSW (BPSW)



The backup PSW (BPSW) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the processor status word (PSW) are saved in the BPSW. The allocation of bits in the BPSW corresponds to that in the PSW.

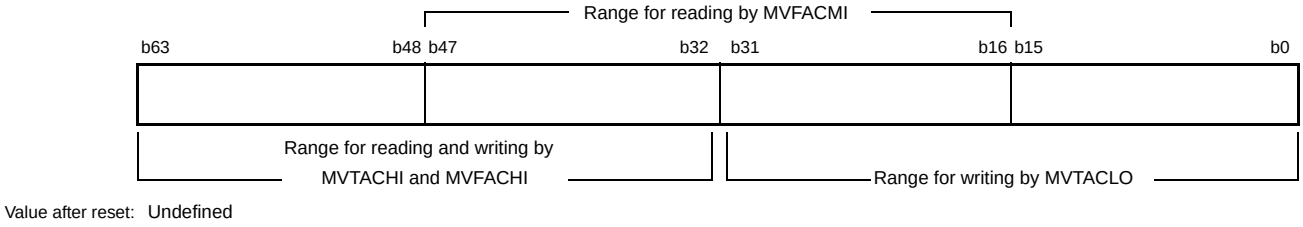
2.2.2.7 Fast Interrupt Vector Register (FINTV)



The fast interrupt vector register (FINTV) is provided to speed up response to interrupts.
The FINTV register specifies a branch destination address when a fast interrupt has been generated.

2.2.3 Register Associated with DSP Instructions

2.2.3.1 Accumulator (ACC)



The accumulator (ACC) is a 64-bit register used for DSP instructions. The accumulator is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, MUL, and RMPA, in which case the prior value in the accumulator is modified by execution of the instruction.
Use the MVTACHI and MVTACLO instructions for writing to the accumulator. The MVTACHI and MVTACLO instructions write data to the higher-order 32 bits (bits 63 to 32) and the lower-order 32 bits (bits 31 to 0), respectively.
Use the MVFACHI and MVFACMI instructions for reading data from the accumulator. The MVFACHI and MVFACMI instructions read data from the higher-order 32 bits (bits 63 to 32) and the middle 32 bits (bits 47 to 16), respectively.

2.3 Processor Mode

The RX CPU supports two processor modes, supervisor and user. These processor modes enable the realization of a hierarchical CPU resource protection.
Each processor mode imposes a level on rights of access to the CPU resources and the instructions that can be executed. Supervisor mode carries greater rights than those of user mode.
The initial state after a reset is supervisor mode.

2.3.1 Supervisor Mode

In supervisor mode, all CPU resources are accessible and all instructions are available. However, writing to the processor mode select bit (PM) in the processor status word (PSW) by executing an MVTC or a POPC instruction will be ignored. For details on how to write to the PM bit, refer to section 2.2.2.4, Processor Status Word (PSW).

2.3.2 User Mode

In user mode, write access to the CPU resources listed below is restricted. The restriction applies to any instruction capable of write access.

- Some bits (bits IPL[3:0], PM, U, and I) in the processor status word (PSW)
- Interrupt stack pointer (ISP)
- Interrupt table register (INTB)
- Backup PSW (BPSW)
- Backup PC (BPC)
- Fast interrupt vector register (FINTV)

2.3.3 Privileged Instruction

Privileged instructions can only be executed in supervisor mode. Executing a privileged instruction in user mode produces a privileged instruction exception. Privileged instructions include the RTFI, MVTIPL, RTE, and WAIT instructions.

2.3.4 Switching Between Processor Modes

Manipulating the processor mode select bit (PM) in the processor status word (PSW) switches the processor mode. However, rewriting to the PM bit by executing an MVTC or a POPC instruction is prohibited. Switch the processor mode by following the procedures described below.

(1) Switching from user mode to supervisor mode

After an exception has been generated, the PSW.PM bit is set to 0 and the CPU switches to supervisor mode. The hardware pre-processing is executed in supervisor mode. The state of the processor mode before the exception was generated is retained in the copy of PSW.PM bit is saved on the stack.

(2) Switching from supervisor mode to user mode

Executing an RTE instruction when the value of the copy of the PSW.PM bit that has been preserved on the stack is 1 or an RTFI instruction when the value of the copy of the PSW.PM bit that has been preserved in the backup PSW (BPSW) is 1 causes a transition to user mode. In the transition to user mode, the value of the stack pointer designation bit (the U bit in the PSW) becomes 1.

2.4 Data Types

The RX CPU can handle three types of data: integer, bit, and string.

2.4.1 Integer

An integer can be signed or unsigned. For signed integers, negative values are represented by two's complements.

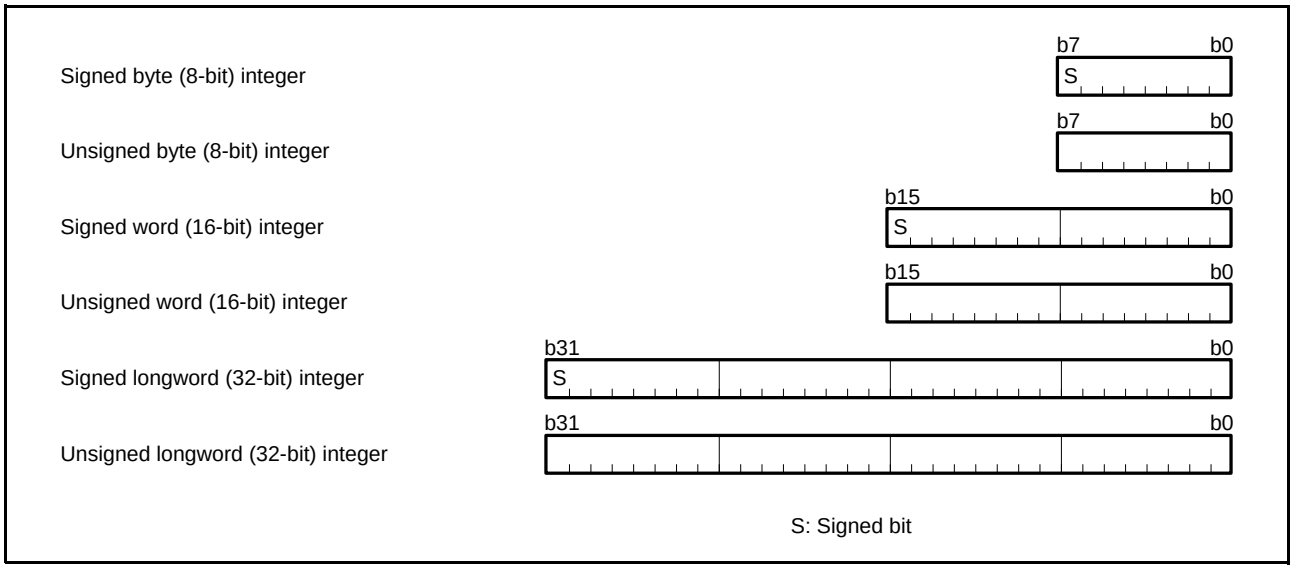


Figure 2.2 Integer

2.4.2 Bit wise Operations

Five bit-manipulation instructions are provided for bitwise operations: BCLR, BMCnd, BNOT, BSET, and BTST.
A bit in a register is specified as the destination register and a bit number in the range from 31 to 0.
A bit in memory is specified as the destination address and a bit number from 7 to 0. The addressing modes available to specify addresses are register indirect and register relative.

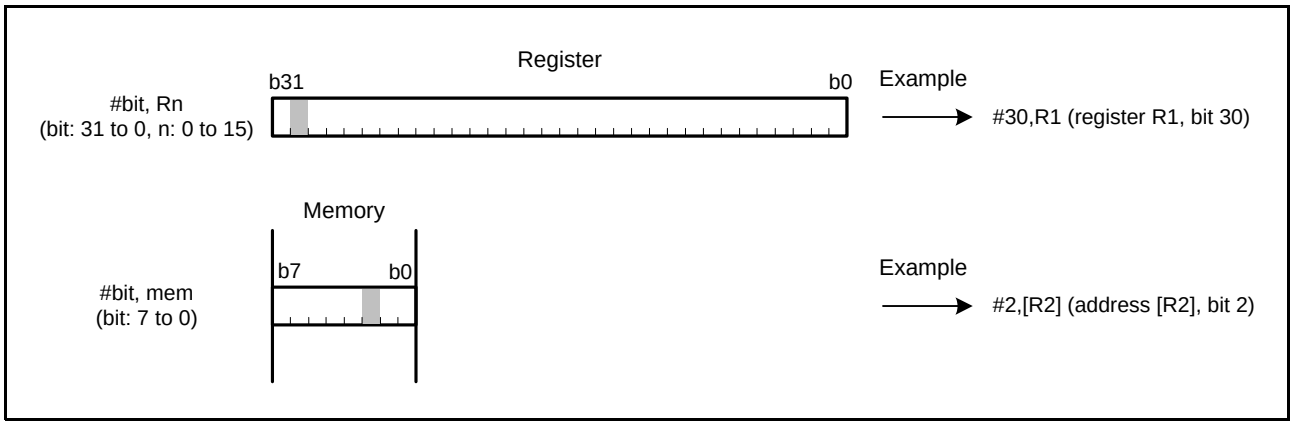


Figure 2.3 Bit

2.4.3 Strings

The string data type consists of an arbitrary number of consecutive byte (8-bit), word (16-bit), or longword (32-bit) units.
Seven string manipulation instructions are provided for use with strings: SCMPU, SMOVB, SMOVF, SMOVU, SSTR, SUNTIL, and SWHILE.

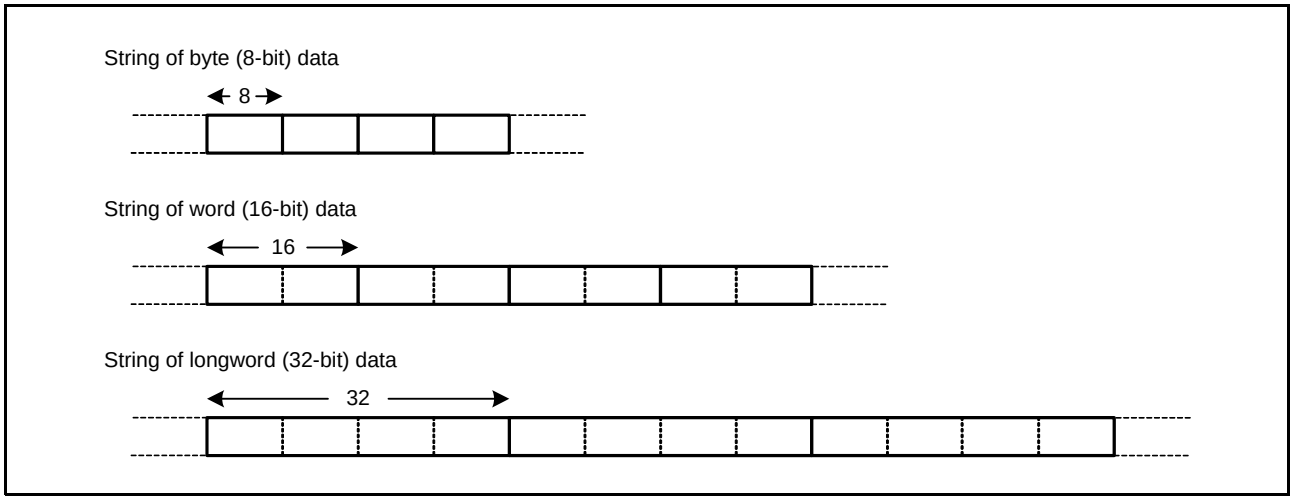


Figure 2.4 String

2.5 Endian

For the RX CPU, instructions are little endian, but the treatment of data is selectable as little or big endian.

2.5.1 Switching the Endian

As arrangements of bytes, the RX210 Group supports both big endian, where the higher-order byte (MSB) is at location 0, and little endian, where the lower-order byte (LSB) is at location 0.
For details on the endian setting, see section 3, Operating Modes.
Operations for access differ according to the endian setting and, depending on the instruction, whether 8-, 16- or 32-bit access has been selected. Operations for access in the various possible cases are described in Table 2.1 to Table 2.12.
In the tables,

LL indicates bits D7 to D0 of the general-purpose register,
LH indicates bits D15 to D8 of the general-purpose register,
HL indicates bits D23 to D16 of the general-purpose register, and
HH indicates bits D31 to D24 of the general-purpose register.

	D31 to D24	D23 to D16	D15 to D8	D7 to D0
General purpose register: Rm	HH	HL	LH	LL

Table 2.1 32-Bit Read Operations when Little Endian has been Selected

Operation / Address of src	Reading a 32-bit unit from address 0	Reading a 32-bit unit from address 1	Reading a 32-bit unit from address 2	Reading a 32-bit unit from address 3	Reading a 32-bit unit from address 4
Address 0	Transfer to LL	—	—	—	—
Address 1	Transfer to LH	Transfer to LL	—	—	—
Address 2	Transfer to HL	Transfer to LH	Transfer to LL	—	—
Address 3	Transfer to HH	Transfer to HL	Transfer to LH	Transfer to LL	—
Address 4	—	Transfer to HH	Transfer to HL	Transfer to LH	Transfer to LL
Address 5	—	—	Transfer to HH	Transfer to HL	Transfer to LH
Address 6	—	—	—	Transfer to HH	Transfer to HL
Address 7	—	—	—	—	Transfer to HH

Table 2.2 32-Bit Read Operations when Big Endian has been Selected

Operation / Address of src	Reading a 32-bit unit from address 0	Reading a 32-bit unit from address 1	Reading a 32-bit unit from address 2	Reading a 32-bit unit from address 3	Reading a 32-bit unit from address 4
Address 0	Transfer to HH	—	—	—	—
Address 1	Transfer to HL	Transfer to HH	—	—	—
Address 2	Transfer to LH	Transfer to HL	Transfer to HH	—	—
Address 3	Transfer to LL	Transfer to LH	Transfer to HL	Transfer to HH	—
Address 4	—	Transfer to LL	Transfer to LH	Transfer to HL	Transfer to HH
Address 5	—	—	Transfer to LL	Transfer to LH	Transfer to HL
Address 6	—	—	—	Transfer to LL	Transfer to LH
Address 7	—	—	—	—	Transfer to LL

Table 2.3 32-Bit Write Operations when Little Endian has been Selected

Operation / Address of dest	Writing a 32-bit unit to address 0	Writing a 32-bit unit to address 1	Writing a 32-bit unit to address 2	Writing a 32-bit unit to address 3	Writing a 32-bit unit to address 4
Address 0	Transfer from LL	—	—	—	—
Address 1	Transfer from LH	Transfer from LL	—	—	—
Address 2	Transfer from HL	Transfer from LH	Transfer from LL	—	—
Address 3	Transfer from HH	Transfer from HL	Transfer from LH	Transfer from LL	—
Address 4	—	Transfer from HH	Transfer from HL	Transfer from LH	Transfer from LL
Address 5	—	—	Transfer from HH	Transfer from HL	Transfer from LH
Address 6	—	—	—	Transfer from HH	Transfer from HL
Address 7	—	—	—	—	Transfer from HH

Table 2.4 32-Bit Write Operations when Big Endian has been Selected

Operation / Address of dest	Writing a 32-bit unit to address 0	Writing a 32-bit unit to address 1	Writing a 32-bit unit to address 2	Writing a 32-bit unit to address 3	Writing a 32-bit unit to address 4
Address 0	Transfer from HH	—	—	—	—
Address 1	Transfer from HL	Transfer from HH	—	—	—
Address 2	Transfer from LH	Transfer from HL	Transfer from HH	—	—
Address 3	Transfer from LL	Transfer from LH	Transfer from HL	Transfer from HH	—
Address 4	—	Transfer from LL	Transfer from LH	Transfer from HL	Transfer from HH
Address 5	—	—	Transfer from LL	Transfer from LH	Transfer from HL
Address 6	—	—	—	Transfer from LL	Transfer from LH
Address 7	—	—	—	—	Transfer from LL

Table 2.5 16-Bit Read Operations when Little Endian has been Selected

Operation / Address of src	Reading a 16-bit unit from address 0	Reading a 16-bit unit from address 1	Reading a 16-bit unit from address 2	Reading a 16-bit unit from address 3	Reading a 16-bit unit from address 4	Reading a 16-bit unit from address 5	Reading a 16-bit unit from address 6
Address 0	Transfer to LL	—	—	—	—	—	—
Address 1	Transfer to LH	Transfer to LL	—	—	—	—	—
Address 2	—	Transfer to LH	Transfer to LL	—	—	—	—
Address 3	—	—	Transfer to LH	Transfer to LL	—	—	—
Address 4	—	—	—	Transfer to LH	Transfer to LL	—	—
Address 5	—	—	—	—	Transfer to LH	Transfer to LL	—
Address 6	—	—	—	—	—	Transfer to LH	Transfer to LL
Address 7	—	—	—	—	—	—	Transfer to LH

Table 2.6 16-Bit Read Operations when Big Endian has been Selected

Operation / Address of src	Reading a 16-bit unit from address 0	Reading a 16-bit unit from address 1	Reading a 16-bit unit from address 2	Reading a 16-bit unit from address 3	Reading a 16-bit unit from address 4	Reading a 16-bit unit from address 5	Reading a 16-bit unit from address 6
Address 0	Transfer to LH	—	—	—	—	—	—
Address 1	Transfer to LL	Transfer to LH	—	—	—	—	—
Address 2	—	Transfer to LL	Transfer to LH	—	—	—	—
Address 3	—	—	Transfer to LL	Transfer to LH	—	—	—
Address 4	—	—	—	Transfer to LL	Transfer to LH	—	—
Address 5	—	—	—	—	Transfer to LL	Transfer to LH	—
Address 6	—	—	—	—	—	Transfer to LL	Transfer to LH
Address 7	—	—	—	—	—	—	Transfer to LL

Table 2.7 16-Bit Write Operations when Little Endian has been Selected

Operation / Address of dest	Writing a 16-bit unit to address 0	Writing a 16-bit unit to address 1	Writing a 16-bit unit to address 2	Writing a 16-bit unit to address 3	Writing a 16-bit unit to address 4	Writing a 16-bit unit to address 5	Writing a 16-bit unit to address 6
Address 0	Transfer from LL	—	—	—	—	—	—
Address 1	Transfer from LH	Transfer from LL	—	—	—	—	—
Address 2	—	Transfer from LH	Transfer from LL	—	—	—	—
Address 3	—	—	Transfer from LH	Transfer from LL	—	—	—
Address 4	—	—	—	Transfer from LH	Transfer from LL	—	—
Address 5	—	—	—	—	Transfer from LH	Transfer from LL	—
Address 6	—	—	—	—	—	Transfer from LH	Transfer from LL
Address 7	—	—	—	—	—	—	Transfer from LH

Table 2.8 16-Bit Write Operations when Big Endian has been Selected

Operation / Address of dest	Writing a 16-bit unit to address 0	Writing a 16-bit unit to address 1	Writing a 16-bit unit to address 2	Writing a 16-bit unit to address 3	Writing a 16-bit unit to address 4	Writing a 16-bit unit to address 5	Writing a 16-bit unit to address 6
Address 0	Transfer from LL	—	—	—	—	—	—
Address 1	Transfer from LH	Transfer from LL	—	—	—	—	—
Address 2	—	Transfer from LH	Transfer from LL	—	—	—	—
Address 3	—	—	Transfer from LH	Transfer from LL	—	—	—
Address 4	—	—	—	Transfer from LH	Transfer from LL	—	—
Address 5	—	—	—	—	Transfer from LH	Transfer from LL	—
Address 6	—	—	—	—	—	Transfer from LH	Transfer from LL
Address 7	—	—	—	—	—	—	Transfer from LH

Table 2.9 8-Bit Read Operations when Little Endian has been Selected

Operation / Address of src	Reading an 8-bit unit from address 0	Reading an 8-bit unit from address 1	Reading an 8-bit unit from address 2	Reading an 8-bit unit from address 3
Address 0	Transfer to LL	—	—	—
Address 1	—	Transfer to LL	—	—
Address 2	—	—	Transfer to LL	—
Address 3	—	—	—	Transfer to LL

Table 2.10 8-Bit Read Operations when Big Endian has been Selected

Operation / Address of src	Reading an 8-bit unit from address 0	Reading an 8-bit unit from address 1	Reading an 8-bit unit from address 2	Reading an 8-bit unit from address 3
Address 0	Transfer to LL	—	—	—
Address 1	—	Transfer to LL	—	—
Address 2	—	—	Transfer to LL	—
Address 3	—	—	—	Transfer to LL

Table 2.11 8-Bit Write Operations when Little Endian has been Selected

Operation / Address of dest	Writing an 8-bit unit to address 0	Writing an 8-bit unit to address 1	Writing an 8-bit unit to address 2	Writing an 8-bit unit to address 3
Address 0	Transfer from LL	—	—	—
Address 1	—	Transfer from LL	—	—
Address 2	—	—	Transfer from LL	—
Address 3	—	—	—	Transfer from LL

Table 2.12 8-Bit Write Operations when Big Endian has been Selected

Operation / Address of dest	Writing an 8-bit unit to address 0	Writing an 8-bit unit to address 1	Writing an 8-bit unit to address 2	Writing an 8-bit unit to address 3
Address 0	Transfer from LL	—	—	—
Address 1	—	Transfer from LL	—	—
Address 2	—	—	Transfer from LL	—
Address 3	—	—	—	Transfer from LL

2.5.2 Access to I/O Registers

The addresses of I/O registers are fixed, and this is regardless of whether the setting is for little endian or big endian. Accordingly, changes to the endian do not affect access to I/O registers. For the arrangements of I/O registers, refer to the descriptions of registers in the relevant sections.

2.5.3 Notes on Access to I/O Registers

Ensure that access to I/O registers is in accord with the following rules.

- With I/O registers for which a bus width of eight bits is indicated, use instructions having operands of the same width (eight bits). That is, access these registers by using instructions with .B as the size specifier (.size), or with .B or .UB as the size-extension specifier (.memex).
- With I/O registers for which a bus width of 16 bits is indicated, use instructions having operands of the same width (16 bits). That is, access these registers by using instructions with .W as the size specifier (.size), or with .W or .UW as the size-extension specifier (.memex).
- With I/O registers for which a bus width of 32 bits is indicated, use instructions having operands of the same width (32 bits). That is, access these registers by using instructions with .L as the size specifier (.size), or with .L size-extension specifier (.memex).

2.5.4 Data Arrangement

2.5.4.1 Data Arrangement in Registers

Figure 2.5 shows the relation between the sizes of registers and bit numbers.

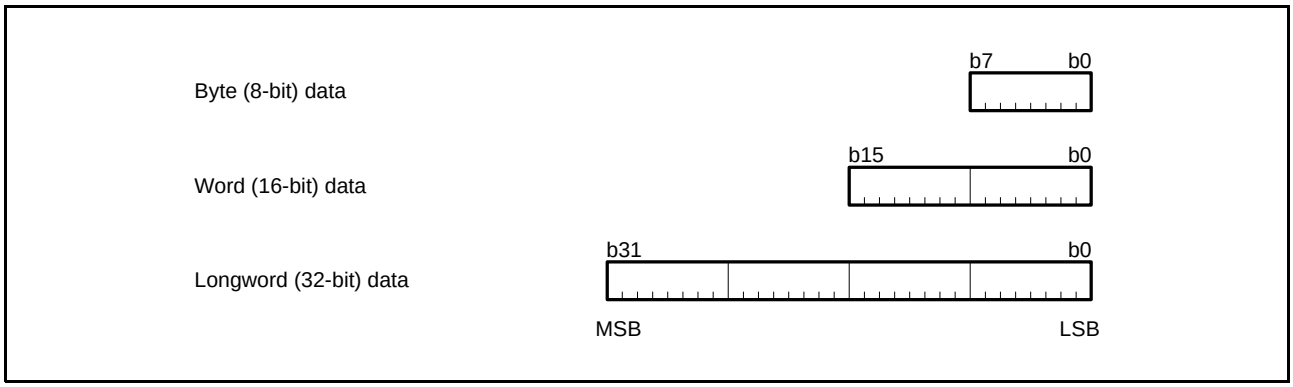


Figure 2.5 Data Arrangement in Registers

2.5.4.2 Data Arrangement in Memory

Data in memory have three sizes: byte (8-bit), word (16-bit), and longword (32-bit). The data arrangement is selectable as little endian or big endian. Figure 2.6 shows the arrangement of data in memory.

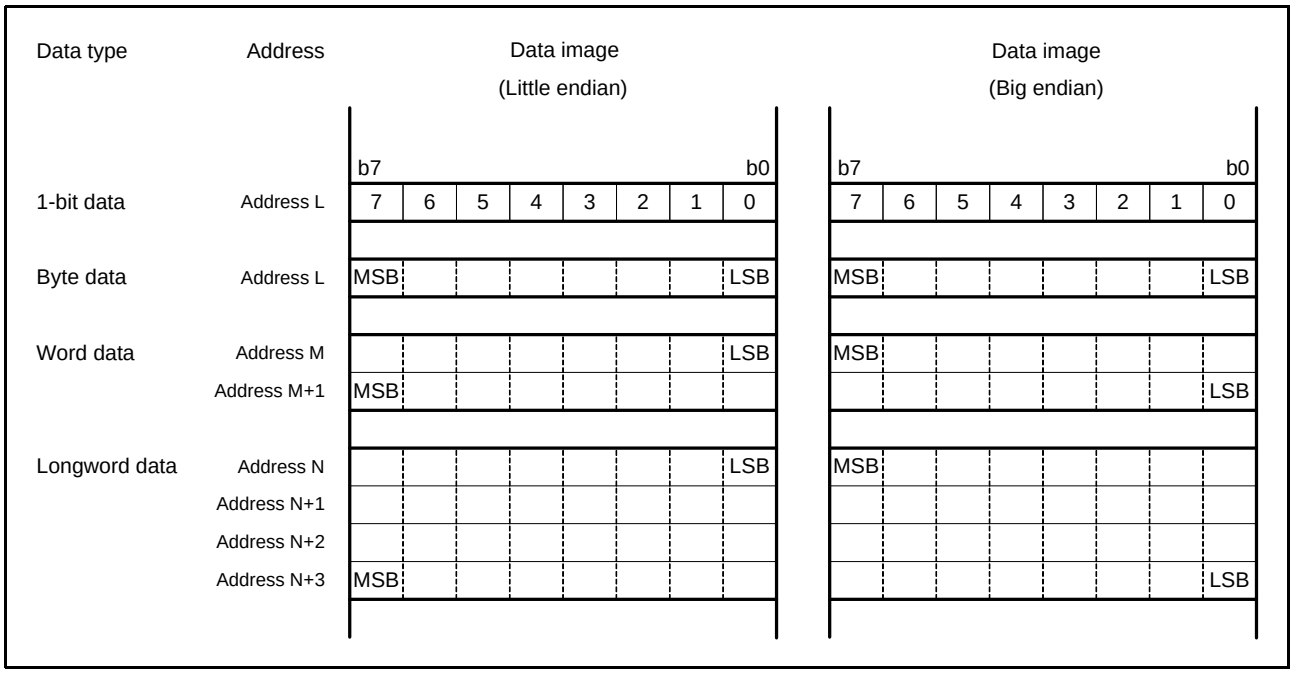


Figure 2.6 Data Arrangement in Memory

2.5.5 Notes on the Allocation of Instruction Codes

The allocation of instruction codes to an external space where the endian differs from that of the chip is prohibited. If the instruction codes are allocated to the external space, they must be allocated to areas where the endian setting is the same as that for the chip.

2.6 Vector Table

There are two types of vector table: fixed and relocatable. Each vector in the vector table consists of four bytes and specifies the address where the corresponding exception handling routine starts.

2.6.1 Fixed Vector Table

The fixed vector table is allocated to a fixed address range. The individual vectors for the privileged instruction exception, undefined instruction exception, non-maskable interrupt, and reset are allocated to addresses in the range from FFFFFF80h to FFFFFFFFh. Figure 2.7 shows the fixed vector table.

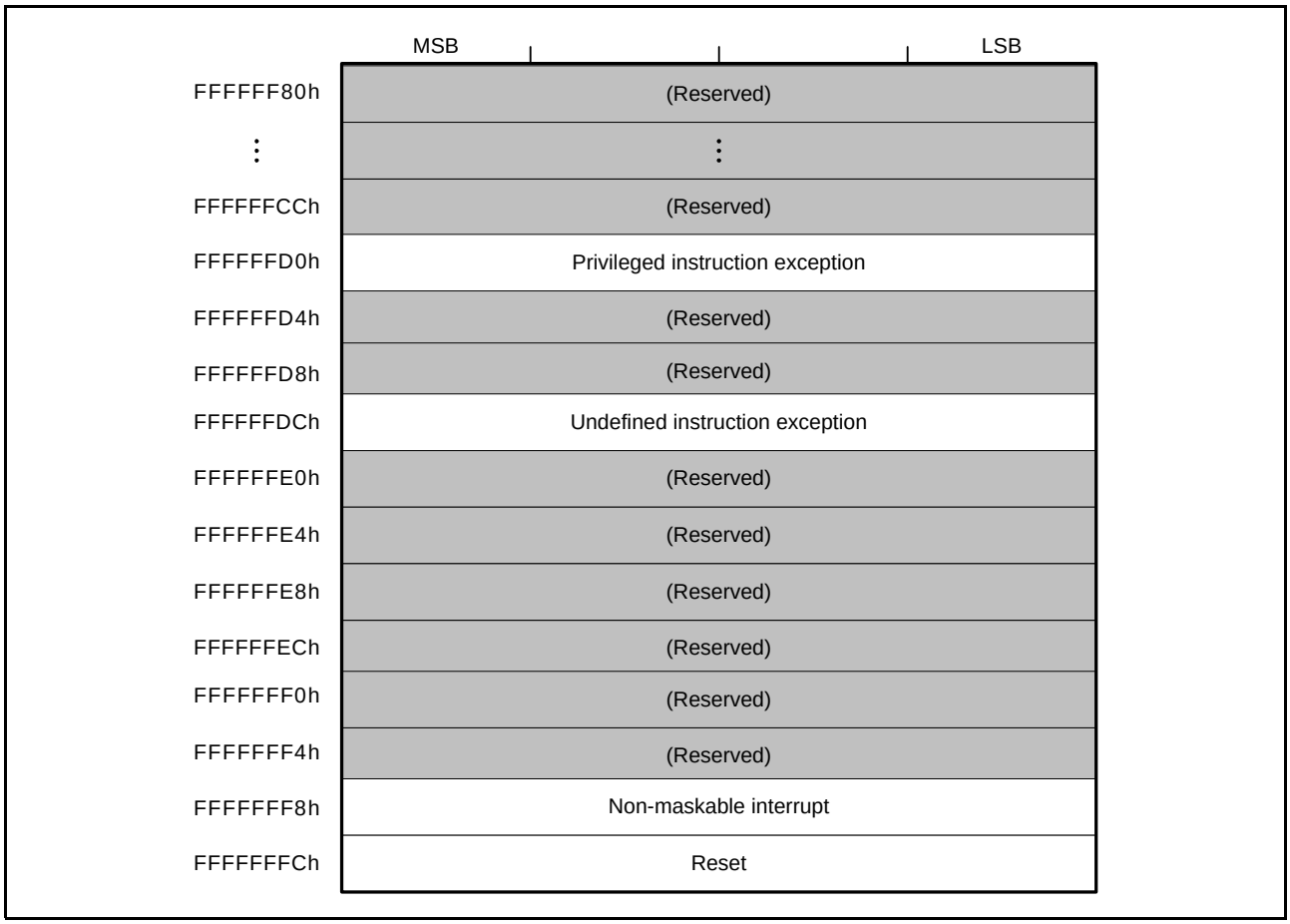


Figure 2.7 Fixed Vector Table

2.6.2 Relocatable Vector Table

The address where the relocatable vector table is placed can be adjusted. The table is a 1,024-byte region that contains all vectors for unconditional traps and interrupts and starts at the address (IntBase) specified in the interrupt table register (INTB). Figure 2.8 shows the relocatable vector table.
Each vector in the relocatable vector table has a vector number from 0 to 255. Each of the INT instructions, which act as the sources of unconditional traps, is allocated to the vector that has the same number as is specified as the operand of the instruction itself (from 0 to 255). The BRK instruction is allocated to the vector with number 0. Furthermore, vector numbers (from 0 to 255) are allocated to interrupt requests in a fixed way for each product. For more on interrupt vector numbers, see section 14.3.1, Interrupt Vector Table.

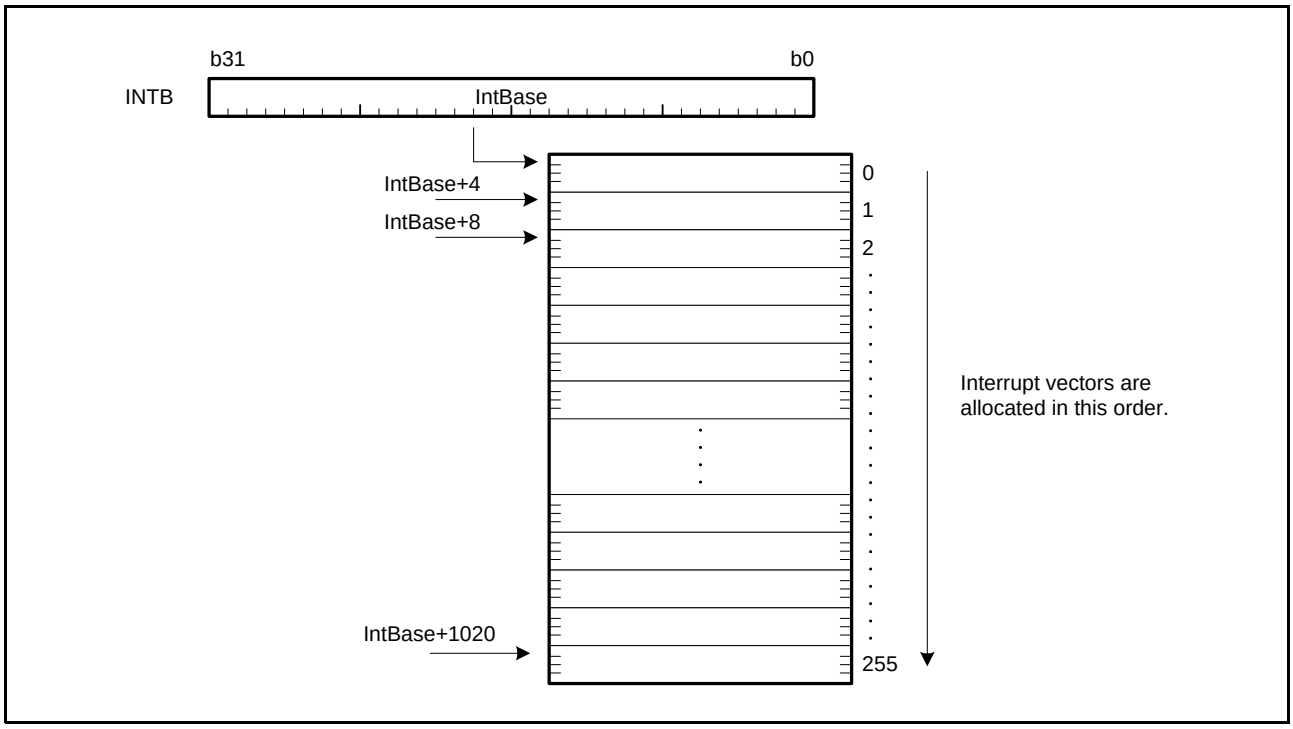


Figure 2.8 Relocatable Vector Table

2.7 Operation of Instructions

2.7.1 Data Prefetching by the RMPA Instruction and the String-Manipulation Instructions

The RMPA instruction and the string-manipulation instructions except the SSTR instruction (that is, SCMPU, SMOVB, SMOVF, SMOVU, SUNTIL, and SWHILE instructions) may prefetch data from the memory to speed up the read processing. Data is prefetched from the prefetching start position with three bytes as the upper limit. The prefetching start positions of each operation are shown below.

- RMPA instruction: The multiplicand address specified by R1, and the multiplier address specified by R2
- SCMPU instruction: The source address specified by R1 for comparison, and the destination address specified by R2 for comparison
- SUNTIL and SWHILE instructions: The destination address specified by R1 for comparison
- SMOVB, SMOVF, and SMOVU instructions: The source address specified by R2 for transfer

2.8 Pipeline

2.8.1 Overview

The RX CPU has 5-stage pipeline structure. The RX CPU instruction is converted into one or more micro-operations, which are then executed in pipeline processing. In the pipeline stage, the IF stage is executed in the unit of instructions, while the D and subsequent stages are executed in the unit of micro-operations.
The operation of pipeline and respective stages is described below.

(1) IF stage (instruction fetch stage)

In the IF stage, the CPU fetches instructions from the memory. As the RX CPU has four 4-byte instruction queues, it fetches instructions until the instruction queue is full, regardless of the completion of decoding in the D (decoding) stage.

(2) D stage (decoding stage)

The CPU decodes instructions in the D stage and converts them into micro-operations. The CPU reads the register information (RF) in this stage and executes a bypass process (BYP) if the result of the preceding instruction will be used in a subsequent instruction. The write of operation result to the register (RW) can be executed with the register reference by using the bypass process.

(3) E stage (execution stage)

Operations and address calculations (OP) are processed in the E stage.

(4) M stage (memory access stage)

Operand memory accesses (OA1, OA2) are processed in the M stage. This stage is used only when the memory is accessed, and is divided into two sub-stages, M1 and M2. The RX CPU enables respective memory accesses for M1 and M2.

- M1 stage (memory-access stage 1)
  Operand memory access (OA1) is processed.
  Store operation: The pipeline processing ends when a write request is received via the bus.
  Load operation: The operation proceeds to the M2 stage when a read request is received via the bus. If a request and load data are received at the same timing (no-wait memory access), the operation proceeds to the WB stage.
- M2 stage (memory-access stage 2)
  Operand memory access (OA2) is processed. The CPU waits for the load data in the M2 stage. When the load data is received, the operation proceeds to the WB stage.

(5) WB stage (write-back stage)

The operation result and the data read from memory are written to the register (RW) in the WB stage. The data read from memory and the other type of data, such as the operation result, can be written to the register in the same clock cycles.

Figure 2.9 shows the pipeline configuration and its operation.

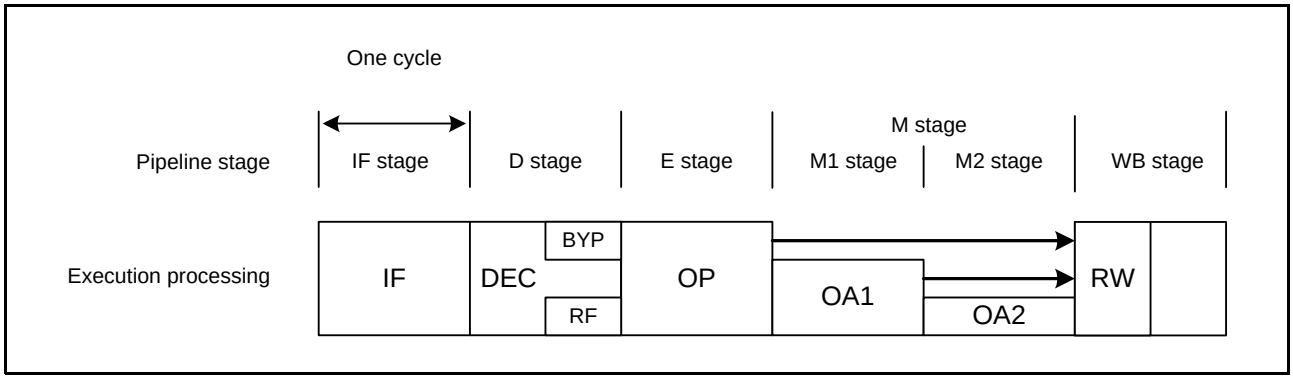


Figure 2.9 Pipeline Configuration and its Operation

2.8.2 Instructions and Pipeline Processing

The operands in the table below indicate the following meaning.

#IMM: Immediate

Rs, Rs2, Rd, Rd2, Ri, Rb: General-purpose register, CR: Control register

dsp: dsp5, dsp8, dsp16, dsp24

pcdsp: pcdsp3, pcdsp8, pcdsp16, pcdsp24

2.8.2.1 Instructions Converted into Single Micro-Operation and Pipeline Processing

The table below lists the instructions that are converted into a single micro-operation. The number of cycles in the table indicates the number of cycles during no-wait memory access.

Table 2.13 Instructions that are Converted into a Single Micro-Operation

Instruction	Mnemonic (indicates the common operation when the size is omitted)	Reference Figure	Number of Cycles
Arithmetic/logic instructions (register-register, immediate-register) Except EMUL, EMULU, RMPA, DIV, DIVU and SATR	• {ABS, ADC, ADD, AND, CMP, MAX, MIN, MUL, NEG, NOP, NOT, OR, ROLC, RORC, ROTL, ROTR, SAT, SBB, SHAR, SHLL, SHLR, SUB, TST, XOR} “#IMM, Rd”/“Rd”/ “Rs, Rd”/“Rs, Rs2, Rd”	Figure 2.10	1
Arithmetic/logic instructions (division)	• DIV “#IMM, Rd”/“Rs, Rd”	Figure 2.10	3 to 20*1
	• DIVU “#IMM, Rd”/“Rs, Rd”	Figure 2.10	2 to 18*1
Data transfer instructions (register-register, immediate-register)	• {MOV, MOVU, REVL, REVW} “#IMM, Rd”/“Rs, Rd” • SC*Cnd* “Rd” • {STNZ, STZ} “#IMM, Rd”	Figure 2.10	1
Transfer instructions (load operation)	• {MOV, MOVU} “[Rs], Rd”/“dsp[Rs], Rd”/“[Rs+], Rd”/ “[–Rs], Rd”/“Rs, [Ri, Rb]” • POP “Rd”	Figure 2.11	Throughput: 1 Latency: 2*2
Transfer instructions (store operation)	• MOV “Rs, [Rd]”/“Rs, dsp[Rd]”/“Rs, [Rd+]”/“Rs, [–Rd]”/ “Rs, [Ri, Rb]” • PUSH “Rs” • PUSHC “CR”	Figure 2.12	1
Bit manipulation instructions (register)	• {BCLR, BNOT, BSET, BTST} “#IMM, Rd”/“Rs, Rd” • BM*Cnd* “#IMM, Rd”	Figure 2.10	1
Branch instructions	• B*Cnd* “pcdsp” • {BRA, BSR} “pcdsp”/“Rs” • {JMP, JSR} “Rs”	Figure 2.20	Branch taken: 3 Branch not taken: 1
System manipulation instructions	• CLRPSW, SETPSW “#IMM” • MVTC “#IMM, CR”/“Rs, CR” • MVFC “CR, Rd” • MVTIPL“#IMM”	—	1
DSP instructions	• {MACHI, MACLO, MULHI, MULLO} “Rs, Rs2” • {MVFACHI, MVFACMI} “Rd” • {MVTACHI, MVTACLO} “Rs” • RACW“#IMM”	Figure 2.10	1

Note 1. The number of cycles for the dividing instruction varies according to the divisor and dividend.
Note 2. For the number of cycles for throughput and latency, see section 2.8.3, Calculation of the Instruction Processing Time.

Figure 2.10 to Figure 2.12 show the operation of instructions that are converted into a basic single micro-operation.

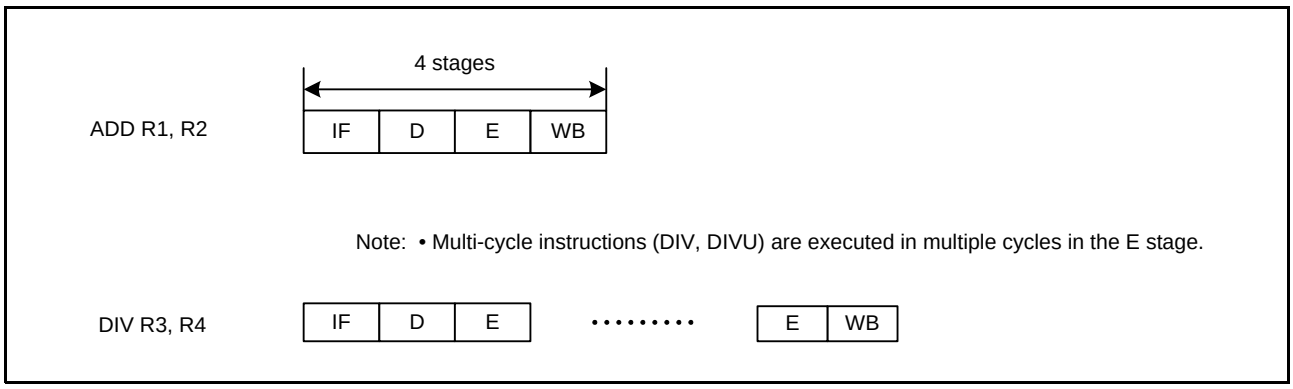


Figure 2.10 Operation for Register-Register, Immediate-Register

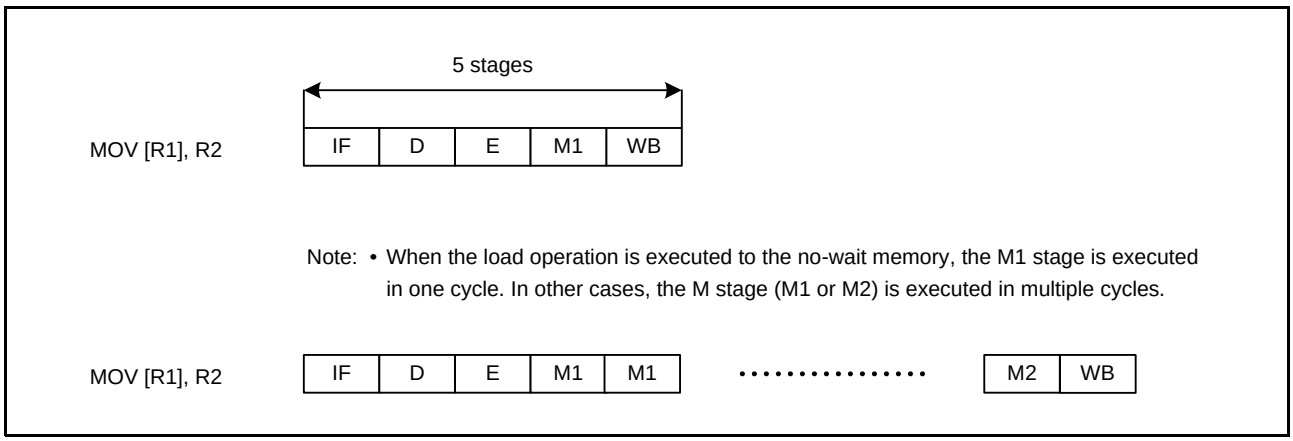


Figure 2.11 Load Operation

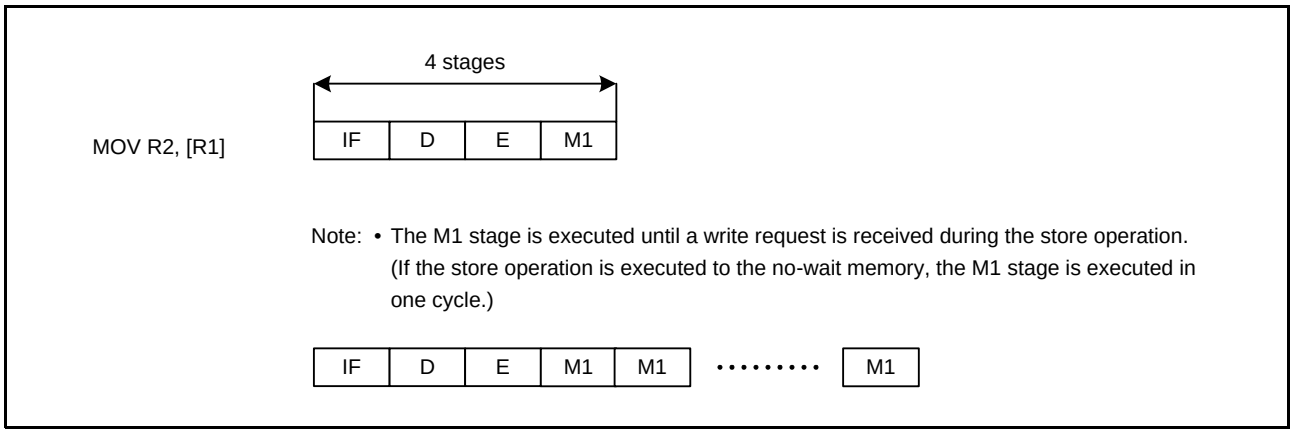


Figure 2.12 Store Operation

2.8.2.2 Instructions Converted into Multiple Micro-Operations and Pipeline Processing

The table below lists the instructions that are converted into multiple micro-operations. The number of cycles in the table indicates the number of cycles during no-wait memory access.

Table 2.14 Instructions that are Converted into Multiple Micro-Operations (1/2)

Instruction	Mnemonic (indicates the common operation when the size is omitted)	Reference Figure	Number of Cycles
Arithmetic/logic instructions (memory source operand)	• {ADC, ADD, AND, CMP, MAX, MIN, MUL, OR, SBB, SUB, TST, XOR} “[Rs], Rd”/“dsp[Rs], Rd”	Figure 2.13	3
Arithmetic/logic instructions (division)	• DIV “[Rs],Rd / dsp[Rs],Rd”	—	5 to 22
	• DIVU“[Rs],Rd / dsp[Rs],Rd”	—	4 to 20
Arithmetic/logic instructions (multiplier: 32 × 32 → 64 bits) (register-register, register-immediate)	• {EMUL, EMULU} “#IMM, Rd”/“Rs, Rd”	Figure 2.15	2
Arithmetic/logic instructions (multiplier: 32 × 32 → 64 bits) (memory source operand)	• {EMUL, EMULU} “[Rs], Rd”/“dsp[Rs], Rd”	—	4
Arithmetic/logic instructions (multiply-and-accumulate operation)	• RMPA.B	—	6+7×floor(n/4)+4×(n%4) n: Number of processing bytes*1
	• RMPA.W	—	6+5×floor(n/2)+4×(n%2) n: Number of processing words*1
	• RMPA.L	—	6+4n n: Number of processing longwords*1
Arithmetic/logic instructions (64-bit signed saturation processing for the RMPA instruction)	• SATR	—	3
Data transfer instructions (memory-memory transfer)	• MOV “[Rs], [Rd]”/“dsp[Rs], [Rd]”/“[Rs], dsp[Rd]”/ “dsp[Rs], [Rd]” • PUSH “[Rs]”/“dsp[Rs]”	Figure 2.14	3
Bit manipulation instructions (memory source operand)	• {BCLR, BNOT, BSET, BTST} “#IMM, [Rd]”/ “#IMM, dsp[Rd]” • BM*Cnd* “#IMM, [Rd]”/“#IMM, dsp[Rd]”	Figure 2.14	3
Transfer instructions (load operation)	• POPC “CR”	—	Throughput: 3 Latency: 4*2
Transfer instructions (save operation of multiple registers)	• PUSHM “Rs-Rs2”	—	n n: Number of registers*3
Transfer instructions (restore operation of multiple registers)	• POPM “Rs-Rs2”	—	Throughput: n Latency: n + 1 n: Number of registers*2,*4
Transfer instructions (register-register)	• XCHG “Rs, Rd”	Figure 2.16	2
Transfer instructions (memory-register)	• XCHG “[Rs], Rd”/“dsp[Rs], Rd”	Figure 2.17	2
Branch instructions	• RTS	—	5
	• RTSD “#IMM”	—	5
	• RTSD “#IMM, Rd-Rd2”	—	Throughput: n<5?5:1+n Latency: n<4?5:2+n n: Number of registers*2

Table 2.14 Instructions that are Converted into Multiple Micro-Operations (2/2)

Instruction	Mnemonic (indicates the common operation when the size is omitted)	Reference Figure	Number of Cycles
String manipulation instructions*5	• SCMPU	—	2+4×floor(n/4)+4×(n%4) n: Number of comparison bytes*1
	• SMOVB	—	n>3? 6+3×floor(n/4)+3×(n%4): 2+3n n: Number of transfer bytes*1
	• SMOVF, SMOVU	—	2+3×floor(n/4)+3×(n%4) n: Number of transfer bytes*1
	• SSTR.B	—	2+floor(n/4)+n%4 n: Number of transfer bytes*1
	• SSTR.W	—	2+floor(n/2)+n%2 n: Number of transfer words*1
	• SSTR.L	—	2+n n: Number of transfer longwords
	• SUNTIL.B, SWHILE.B	—	3+3×floor(n/4)+3×(n%4) n: Number of comparison bytes*1
	• SUNTIL.W, SWHILE.W	—	3+3×floor(n/2)+3×(n%2) n: Number of comparison words*1
	• SUNTIL.L, SWHILE.L	—	3+3×n n: Number of comparison longwords
System manipulation instructions	• RTE	—	6
	• RTFI	—	3

?: Conditional operator

Note 1. floor(x): Max. integer that is smaller than x
Note 2. For the number of cycles for throughput and latency, see section 2.8.3, Calculation of the Instruction Processing Time.
Note 3. The PUSHM instruction is converted into multiple store operations. The pipeline processing is the same as the one for the store operations of the MOV instruction, where the operation is repeated for the number of specified registers.
Note 4. The POPM instruction is converted into multiple load operations. The pipeline processing is the same as the one for the load operations of the MOV instruction, where the operation is repeated for the number of specified registers.
Note 5. Each of the SCMPU, SMOVU, SWHILE, and SUNTIL instructions ends the execution regardless of the specified cycles, if the end condition is satisfied during execution.

Figure 2.13 to Figure 2.19 show the operation of instructions that are converted into basic multiple micro-operations.
Note: • mop: Micro-operation, stall: Pipeline stall

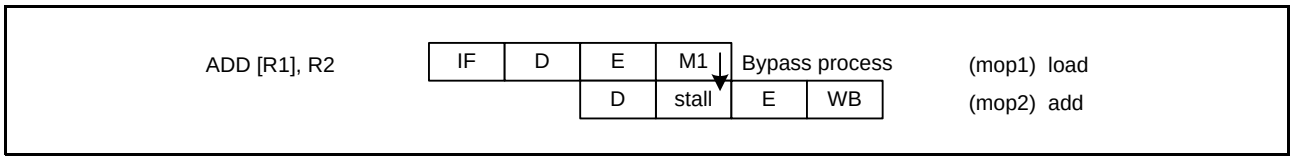


Figure 2.13 Arithmetic/Logic Instruction (Memory Source Operand)

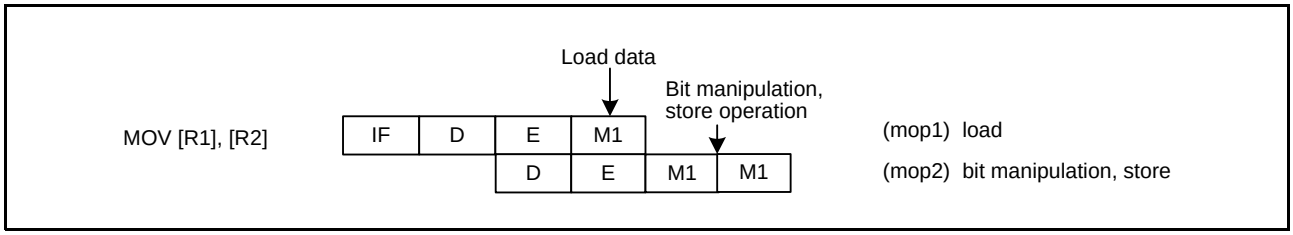


Figure 2.14 MOV Instruction (Memory-Memory), Bit Manipulation Instruction (Memory Source Operand)

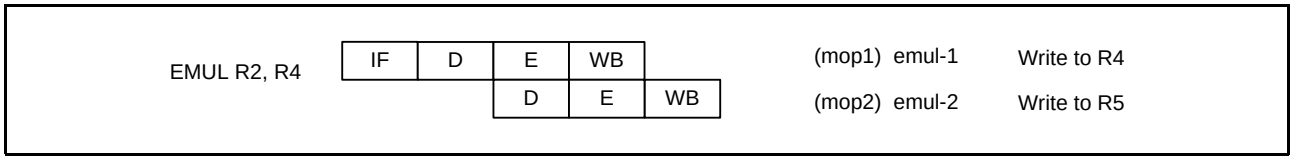


Figure 2.15 EMUL, EMULU Instructions (Register- Register, Register-Immediate)

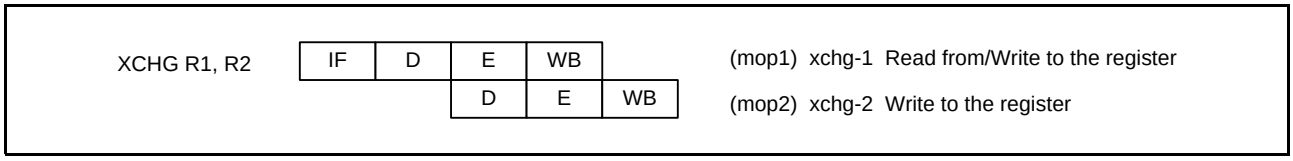


Figure 2.16 XCHG Instruction (Registers)

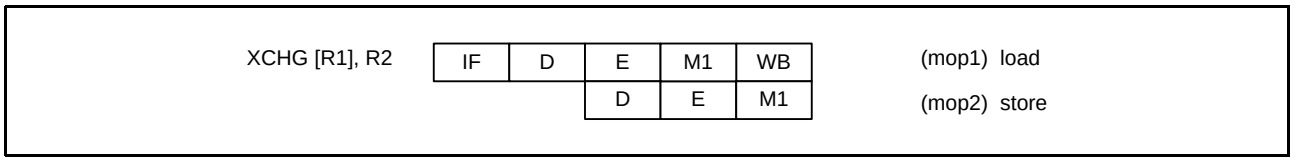


Figure 2.17 XCHG Instruction (Memory Source Operand)

2.8.2.3 Pipeline Basic Operation

In the ideal pipeline processing, each stage is executed in one cycle, though all instructions may not be pipelined in due to the processing in each stage and the branch execution.
The CPU controls the pipeline stage with the IF stage in the unit of instructions, while the D and subsequent stages in the unit of micro-operations.
The figures below show the pipeline processing of typical cases.
Note: • mop: Micro-operation, stall: Pipeline stall

(1) Pipeline Flow with Stalls

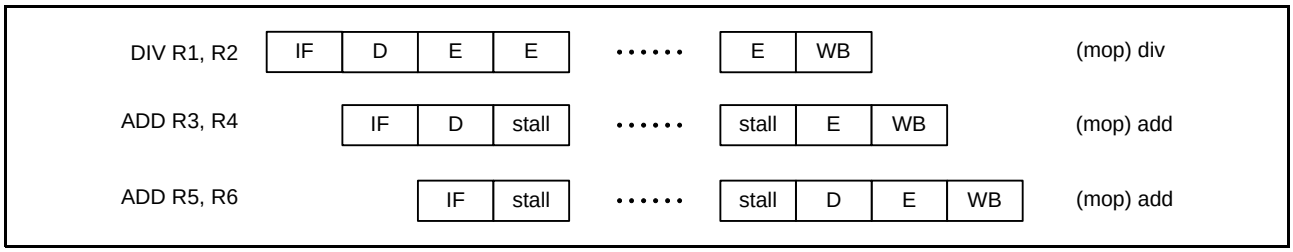


Figure 2.18 When an Instruction which Requires Multiple Cycles is Executed in the E Stage

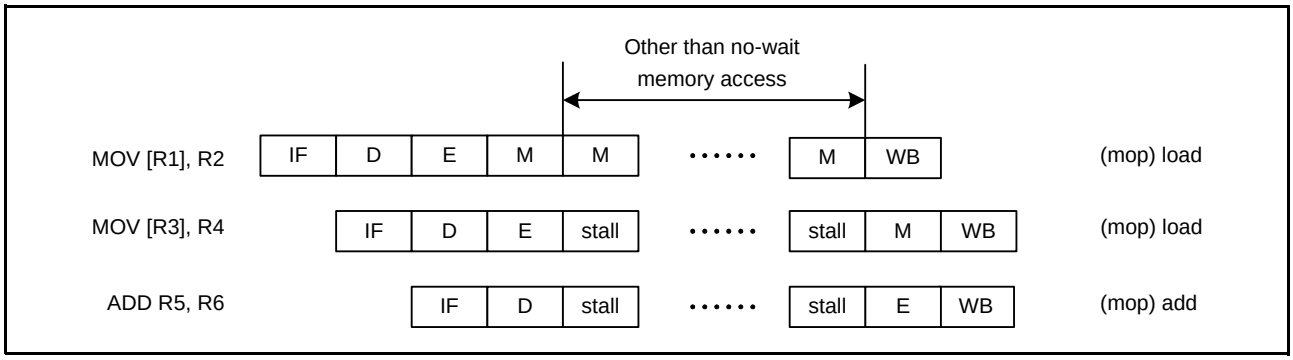


Figure 2.19 When an Instruction which Requires more than One Cycle for its Operand Access is Executed

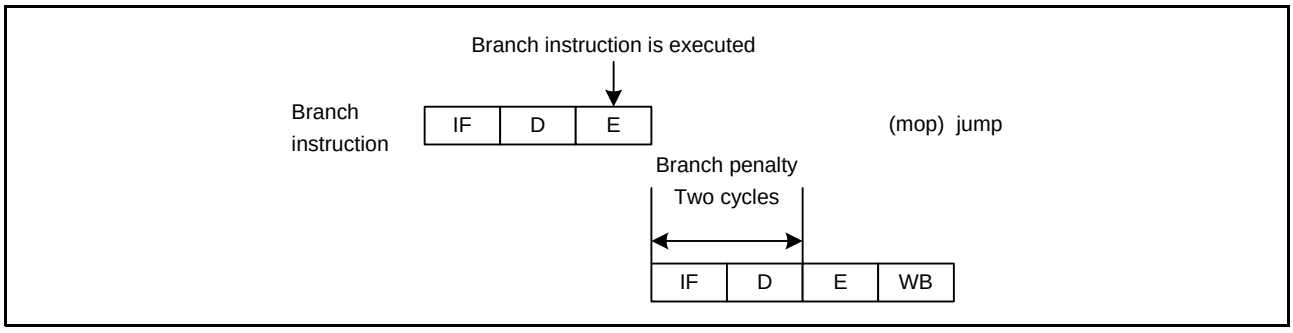


Figure 2.20 When a Branch Instruction is Executed (an Unconditional Branch Instruction is Executed or the Condition is Satisfied for a Conditional Branch Instruction)

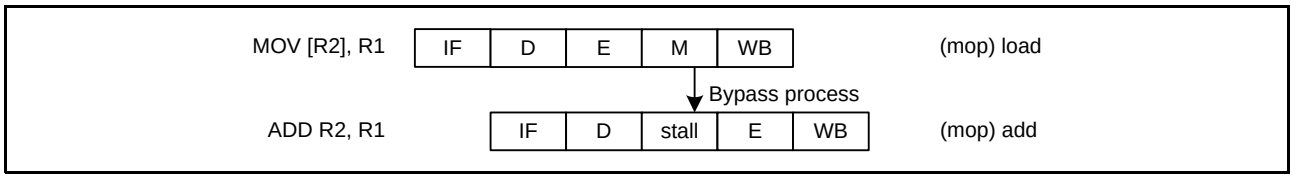


Figure 2.21 When the Subsequent Instruction Uses an Operand Read from the Memory

(2) Pipeline Flow with no Stall

(a) Bypass process

Even when the result of the preceding instruction will be used in a subsequent instruction, the operation processing between registers is pipelined in by the bypass process.

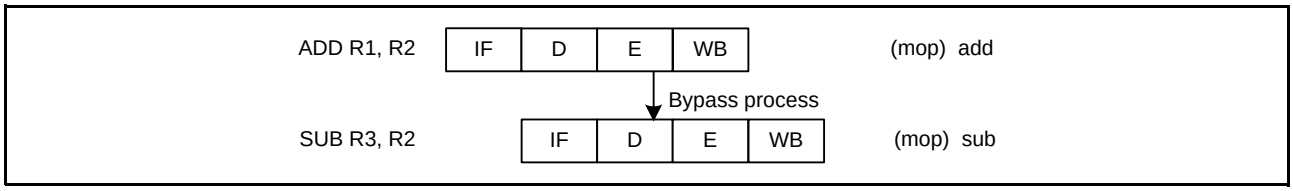


Figure 2.22 Bypass Process

(b) When WB stages for the memory load and for the operation are overlapped

Even when the WB stages for the memory load and for the operation are overlapped, the operation processing is pipelined in, because the load data and the operation result can be written to the register at the same timing.

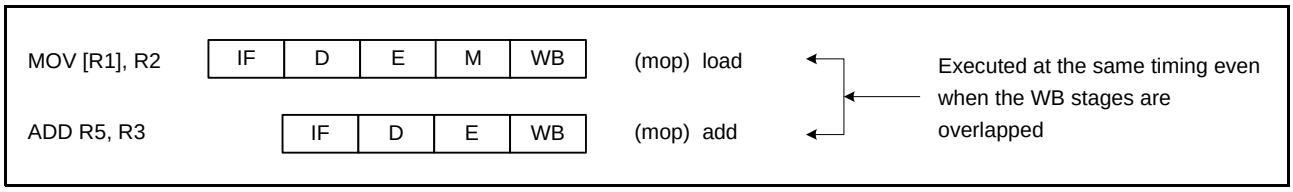


Figure 2.23 When WB Stages for the Memory Load and for the Operation are Overlapped

(c) When subsequent instruction writes to the same register before the end of memory load

Even when the subsequent instruction writes to the same register before the end of memory load, the operation processing is pipelined in, because the WB stage for the memory load is canceled.

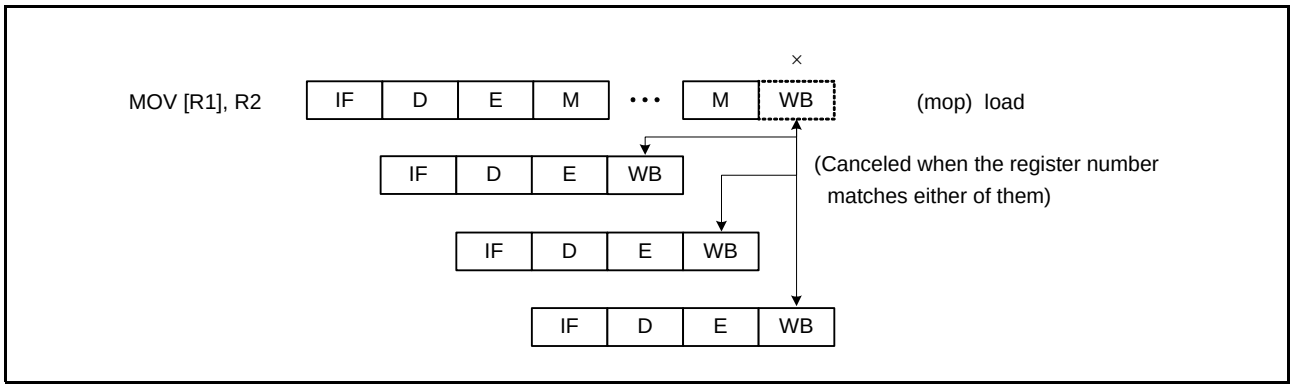


Figure 2.24 When Subsequent Instruction Writes to the Same Register before the End of Memory Load

(d) When the load data is not used by the subsequent instruction

When the load data is not used by the subsequent instruction, the subsequent operations are in fact executed earlier and the operation processing ends (out-of-order completion).

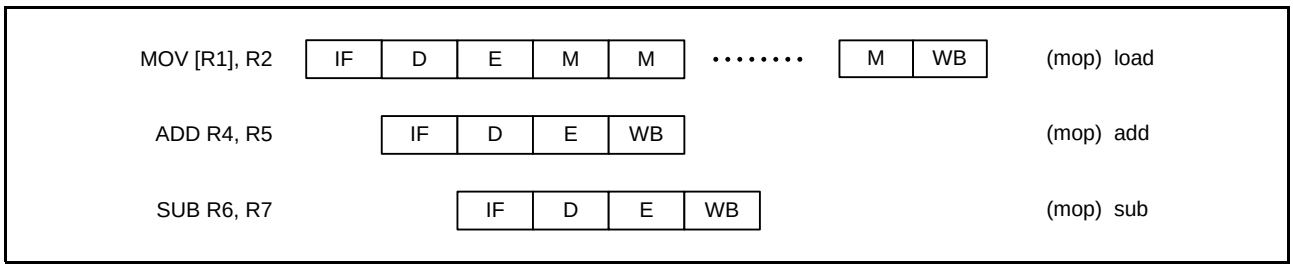


Figure 2.25 When Load Data is not Used by the Subsequent Instruction

2.8.3 Calculation of the Instruction Processing Time

Though the instruction processing time of the CPU varies according to the pipeline processing, the approximate time can be calculated in the following methods.

- Count the number of cycles (see Table 2.13 and Table 2.14)
- When the load data is used by the subsequent instruction, the number of cycles described as “latency” is counted as the number of cycles for the memory load instruction. For the cycles other than the memory load instruction, the number of cycles described as “throughput” is counted.
- If the instruction fetch stall is generated, the number of cycles increments.
- Depending on the system configuration, multiple cycles are required for the memory access.

2.8.4 Numbers of Cycles for Response to Interrupts

Table 2.15 lists numbers of cycles taken by processing for response to interrupts.

Table 2.15 Numbers of Cycles for Response to Interrupts

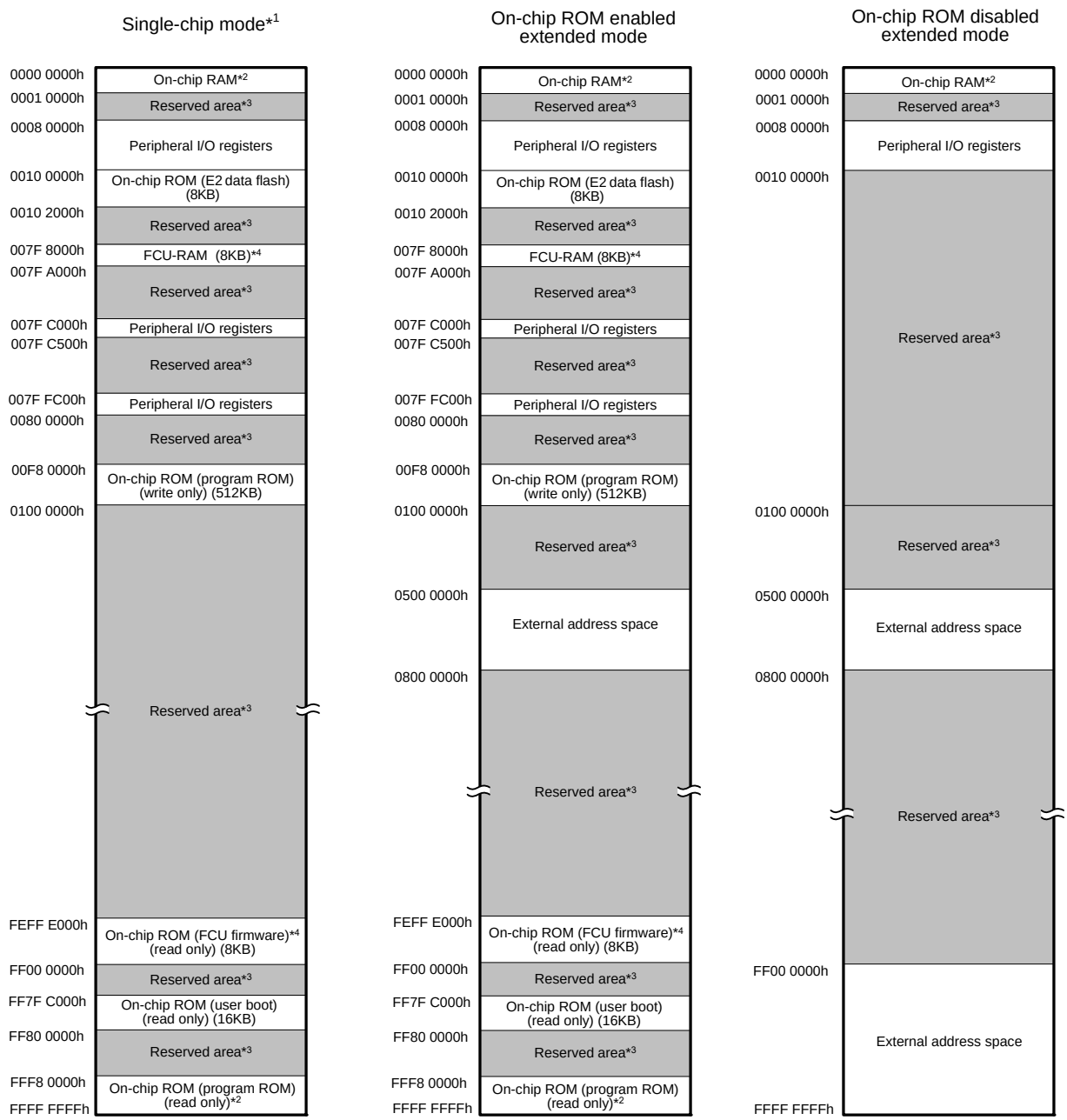
Type of Interrupt Request/Details of Processing	Fast Interrupt	Other Interrupts
ICUA Judgment of priority order	2 cycles	
CPU Number of cycles from notification to acceptance of the interrupt request	N cycles (varies with the instruction being executed at the time the interrupt was received)	
CPU Pre-processing by hardware Saving the current PC and PSW values in RAM (or in control registers in the case of the fast interrupt) Reading of the vector Branching to the start of the exception handling routine	4 cycles	6 cycles

Times calculated from the values in Table 2.15 will be applicable when access to memory from the CPU is processed with no waiting. The on-chip RAM and ROM in products of the RX210 Groups allow such access. Numbers of cycles for response to interrupts can be minimized by placing program code (and vectors) in on-chip ROM and the stack in on-chip RAM. Furthermore, place the addresses where the exception handling routine start on eight-byte boundaries.
For information on the number of cycles from notification to acceptance of the interrupt request, indicated by N in the table above, see Table 2.13, Instructions that are Converted into a Single Micro-Operation, and Table 2.14, Instructions that are Converted into Multiple Micro-Operations.
The timing of interrupt acceptance depends on the state of the pipelines. For more information on this, see section 13.3.1, Acceptance Timing and Saved PC Value.

3. Address Space

3.1 Address Space

This LSI has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas.
Figure 3.1 shows the memory maps in the respective operating modes. Accessible areas will differ according to the operating mode and states of control bits.



Note 1. The address space in boot mode and user boot mode is the same as the address space in single-chip mode.
Note 2. The capacity of ROM/RAM differs depending on the products.

ROM (byt)		RAM (byt)	
Capacity	**Address**	**Capacity**	**Address**
512 Kbytes	FFF8 0000h to FFFF FFFFh	64 Kbytes	0000 0000h to 0000 FFFFh
384 Kbytes	FFFA 0000h to FFFF FFFFh		
256 Kbytes	FFFC 0000h to FFFF FFFFh	32 Kbytes	0000 0000h to 0000 7FFFh
128 Kbytes	FFFE 0000h to FFFF FFFFh	20 Kbytes	0000 0000h to 0000 4FFFh

Note:•See Table 1.3, List of Products, for the product type name.

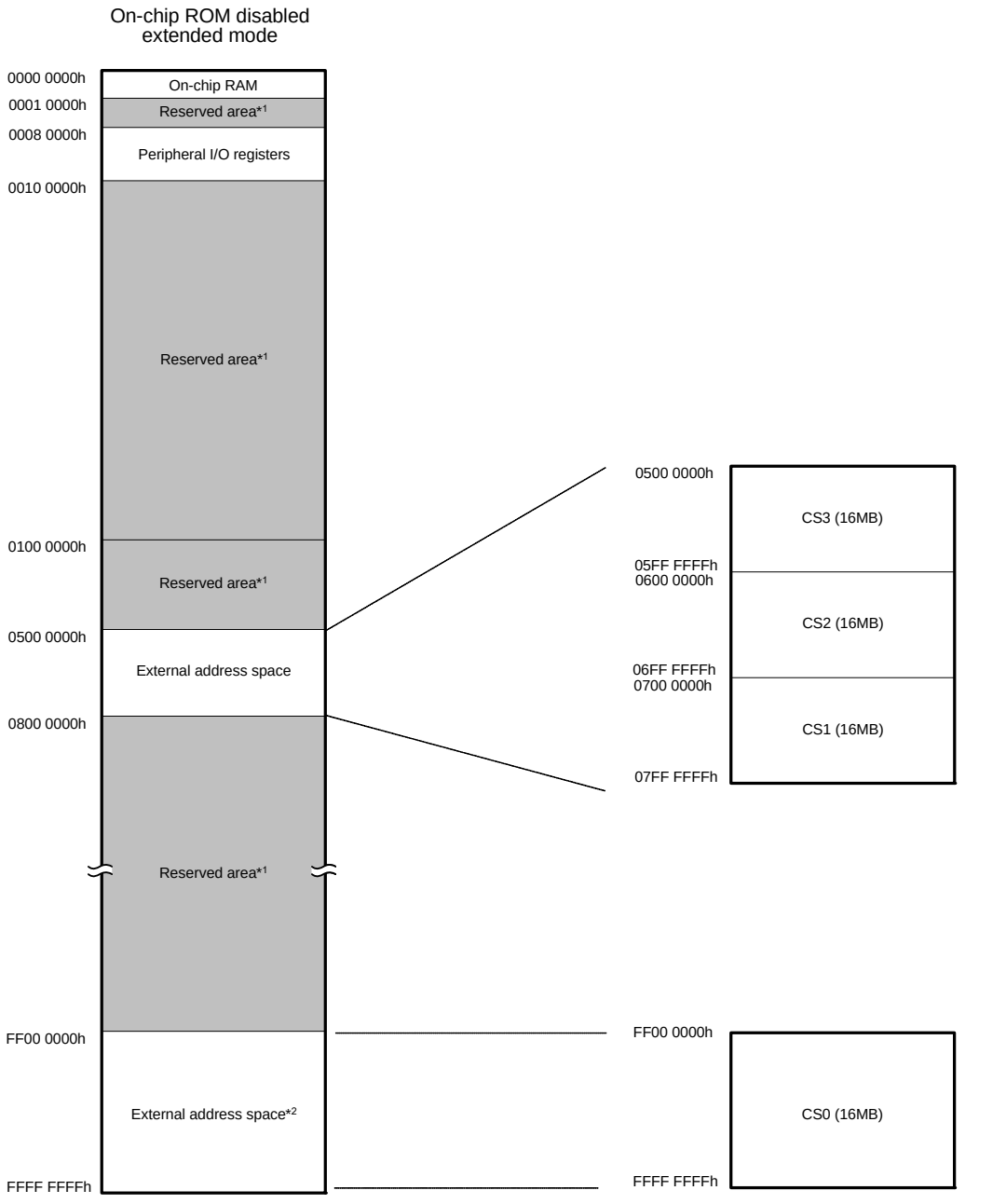
Note 3. Reserved areas should not be accessed.
Note 4. For details on the FCU, see section 39, ROM (Flash Memory for Code Storage) and section 40, E2 DataFlash Memory (Flash Memory for Data Storage).

Figure 3.1 Memory Map in Each Operating Mode

3.2 External Address Space

The external address space is divided into up to four CS areas (CS0 to CS3), each corresponding to the CSn# signal output from a CSn# (n = 0 to 3) pin.

Figure 3.2 shows the address ranges corresponding to the individual CS areas (CS0 to CS3) in on-chip ROM disabled extended mode.



Note 1. Reserved areas should not be accessed.
Note 2. The CS0 area is disabled in on-chip ROM enabled extended mode. In this mode, the address space for addresses above 0800 0000h is as shown in figure on this section “Memory Map in Each Operating Mode”.

Figure 3.2 Correspondence between External Address Spaces and CS Areas (In On-Chip ROM Disabled Extended Mode)

4. I/O Registers

This section gives information on the on-chip I/O register addresses and bit configuration. The information is given as shown below. Notes on writing to registers are also given at the end.

(1) I/O register addresses (address order)

- Registers are listed from the lower allocation addresses.
- Registers are classified according to module symbols.
- Numbers of cycles for access indicate numbers of cycles of the given base clock.
- Among the internal I/O register area, addresses not listed in the list of registers are reserved. Reserved addresses must not be accessed. Do not access these addresses; otherwise, the operation when accessing these bits and subsequent operations cannot be guaranteed.

(2) Notes on writing to I/O registers

When writing to an I/O register, the CPU starts executing the subsequent instruction before completing I/O register write. This may cause the subsequent instruction to be executed before the post-update I/O register value is reflected on the operation.
As described in the following examples, special care is required for the cases in which the subsequent instruction must be executed after the post-update I/O register value is actually reflected.

[Examples of cases requiring special care]

- The subsequent instruction must be executed while an interrupt request is disabled with the IENj bit in IERn of the ICU (interrupt request enable bit) cleared to 0.
- A WAIT instruction is executed immediately after the preprocessing for causing a transition to the low power consumption state.

In the above cases, after writing to an I/O register, wait until the write operation is completed using the following procedure and then execute the subsequent instruction.

(a) Write to an I/O register.
(b) Read the value from the I/O register to a general register.
(c) Execute the operation using the value read.
(d) Execute the subsequent instruction.

[Instruction examples]

- Byte-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.B  #SFR_DATA, [R1]
CMP    [R1].UB, R1
;; Next process
```

- Word-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.W  #SFR_DATA, [R1]
CMP    [R1].W, R1
;; Next process
```

- Longword-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.L  #SFR_DATA, [R1]
CMP    [R1].L, R1
;; Next process
```

If multiple registers are written to and a subsequent instruction should be executed after the write operations are entirely completed, only read the I/O register that was last written to and execute the operation using the value; it is not necessary to read or execute operation for all the registers that were written to.

(3) Number of Access Cycles to I/O Registers

For numbers of clock cycles for access to I/O registers, see Table 4.1, List of I/O Registers (Address Order).
The number of access cycles to I/O registers is obtained by following equation.*1

Number of access cycles to I/O registers = Number of bus cycles for internal main bus 1 +
Number of divided clock synchronization cycles +
Number of bus cycles for internal peripheral bus 1 to 6

The number of bus cycles of internal peripheral bus 1 to 6 differs according to the register to be accessed.
When peripheral functions connected to internal peripheral bus 2 to 6 or registers for the external bus control unit (except for bus error related registers) are accessed, the number of divided clock synchronization cycles is added.
The number of divided clock synchronization cycles differs depending on the frequency ratio between ICLK and PCLK (or FCLK, BCLK) or bus access timing.
In the peripheral function unit, when the frequency ratio of ICLK is equal to or greater than that of PCLK (or FCLK), the sum of the number of bus cycles for internal main bus 1 and the number of the divided clock synchronization cycles will be one cycle of PCLK (or FCLK) at a maximum. Therefore, one PCLK (or FCLK) has been added to the number of access cycles shown in Table 4.1.
When the frequency ratio of ICLK is lower than that of PCLK (or FCLK), the subsequent bus access is started from the ICLK cycle following the completion of the access to the peripheral functions. Therefore, the access cycles are described on an ICLK basis.
In the external bus control unit, the sum of the number of bus cycles for internal main bus 1 and the number of divided clock synchronization cycles will be one cycle of BCLK at a maximum. Therefore, one BCLK is added to the number of access cycles shown in Table 4.1.

Note 1. This applies to the number of cycles when the access from the CPU does not conflict with the instruction fetching to the external memory or bus access from the different bus master (DMACA or DTC).

Table 4.1 List of I/O Registers (Address Order) (1 / 22)

100-pin	80-pin	64-pin	Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States	
									ICLK ≥ PCLK	ICLK < PCLK
○	○	○	0008 0000h	SYSTEM	Mode monitor register	MDMONR	16	16	3 ICLK	
○	○	○	0008 0002h	SYSTEM	Mode status register	MDSR	16	16	3 ICLK	
○	○	○	0008 0006h	SYSTEM	System control register 0	SYSCR0	16	16	3 ICLK	
○	○	○	0008 0008h	SYSTEM	System control register 1	SYSCR1	16	16	3 ICLK	
○	○	○	0008 000Ch	SYSTEM	Standby control register	SBYCR	16	16	3 ICLK	
○	○	○	0008 0010h	SYSTEM	Module stop control register A	MSTPCRA	32	32	3 ICLK	
○	○	○	0008 0014h	SYSTEM	Module stop control register B	MSTPCRB	32	32	3 ICLK	
○	○	○	0008 0018h	SYSTEM	Module stop control register C	MSTPCRC	32	32	3 ICLK	
○	○	○	0008 0020h	SYSTEM	System clock control register	SCKCR	32	32	3 ICLK	
○	○	○	0008 0026h	SYSTEM	System clock control register 3	SCKCR3	16	16	3 ICLK	
○	○	○	0008 0028h	SYSTEM	PLL control register	PLLCR	16	16	3 ICLK	
○	○	○	0008 002Ah	SYSTEM	PLL control register 2	PLLCR2	8	8	3 ICLK	
○	○	○	0008 0030h	SYSTEM	External bus clock control register	BCKCR	8	8	3 ICLK	
○	○	○	0008 0032h	SYSTEM	Main clock oscillator control register	MOSCCR	8	8	3 ICLK	
○	○	○	0008 0033h	SYSTEM	Sub-clock oscillator control register	SOSCCR	8	8	3 ICLK	
○	○	○	0008 0034h	SYSTEM	Low-speed clock oscillator control register	LOCOCR	8	8	3 ICLK	
○	○	○	0008 0035h	SYSTEM	IWDT-dedicated low-speed clock oscillator control register	ILOCOCR	8	8	3 ICLK	
○	○	○	0008 0036h	SYSTEM	High-speed clock oscillator control register	HOCOCR	8	8	3 ICLK	
○	○	○	0008 0037h	SYSTEM	High-speed clock oscillator control register	HOCOCR2	8	8	3 ICLK	
○	○	○	0008 0040h	SYSTEM	Oscillation stop detection control register	OSTDCR	8	8	3 ICLK	
○	○	○	0008 0041h	SYSTEM	Oscillation stop detection status register	OSTDSR	8	8	3 ICLK	
○	○	○	0008 00A0h	SYSTEM	Operating power control register	OPCCR	8	8	3 ICLK	
○	○	○	0008 00A1h	SYSTEM	Sleep mode return clock source switching register	RSTCKCR	8	8	3 ICLK	
○	○	○	0008 00A2h	SYSTEM	Main clock oscillator wait control register	MOSCWTCR	8	8	3 ICLK	
○	○	○	0008 00A3h	SYSTEM	Sub-clock oscillator wait control register	SOSCWTCR	8	8	3 ICLK	
○	○	○	0008 00A6h	SYSTEM	PLL wait control register	PLLWTCR	8	8	3 ICLK	
○	○	○	0008 00A8h	SYSTEM	LOCO wait control register 2	LOCOWTCR2	8	8	3 ICLK	
○	○	○	0008 00A9h	SYSTEM	HOCO wait control register 2	HOCOWTCR2	8	8	3 ICLK	
○	○	○	0008 00C0h	SYSTEM	Reset status register 2	RSTSR2	8	8	3 ICLK	
○	○	○	0008 00C2h	SYSTEM	Software reset register	SWRR	16	16	3 ICLK	
○	○	○	0008 00E0h	SYSTEM	Voltage monitoring 1 circuit/comparator A1 control register 1	LVD1CR1	8	8	3 ICLK	
○	○	○	0008 00E1h	SYSTEM	Voltage monitoring 1 circuit/comparator A1 status register	LVD1SR	8	8	3 ICLK	
○	○	○	0008 00E2h	SYSTEM	Voltage monitoring 2 circuit/comparator A2 control register 1	LVD2CR1	8	8	3 ICLK	
○	○	○	0008 00E3h	SYSTEM	Voltage monitoring 2 circuit/comparator A2 status register	LVD2SR	8	8	3 ICLK	
○	○	○	0008 03FEh	SYSTEM	Protect register	PRCR	16	16	3 ICLK	
○	○	○	0008 1300h	BSC	Bus error status clear register	BERCLR	8	8	2 ICLK	
○	○	○	0008 1304h	BSC	Bus error monitoring enable register	BEREN	8	8	2 ICLK	
○	○	○	0008 1308h	BSC	Bus error status register 1	BERSR1	8	8	2 ICLK	
○	○	○	0008 130Ah	BSC	Bus error status register 2	BERSR2	16	16	2 ICLK	
○	○	○	0008 1310h	BSC	Bus priority control register	BUSPRI	16	16	2 ICLK	
○	○	○	0008 2000h	DMAC0	DMA source address register	DMSAR	32	32	2 ICLK	
○	○	○	0008 2004h	DMAC0	DMA destination address register	DMDAR	32	32	2 ICLK	
○	○	○	0008 2008h	DMAC0	DMA transfer count register	DMCRA	32	32	2 ICLK	
○	○	○	0008 200Ch	DMAC0	DMA block transfer count register	DMCRB	16	16	2 ICLK	
○	○	○	0008 2010h	DMAC0	DMA transfer mode register	DMTMD	16	16	2 ICLK	
○	○	○	0008 2013h	DMAC0	DMA interrupt setting register	DMINT	8	8	2 ICLK	
○	○	○	0008 2014h	DMAC0	DMA address mode register	DMAMD	16	16	2 ICLK	
○	○	○	0008 2018h	DMAC0	DMA offset register	DMOFR	32	32	2 ICLK	
○	○	○	0008 201Ch	DMAC0	DMA transfer enable register	DMCNT	8	8	2 ICLK	
○	○	○	0008 201Dh	DMAC0	DMA software start register	DMREQ	8	8	2 ICLK	
○	○	○	0008 201Eh	DMAC0	DMA status register	DMSTS	8	8	2 ICLK	
○	○	○	0008 201Fh	DMAC0	DMA activation source flag control register	DMCSL	8	8	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (2 / 22)

100-pin	80-pin	64-pin	Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States	
									ICLK ≥ PCLK	ICLK < PCLK
○	○	○	0008 2040h	DMAC1	DMA source address register	DMSAR	32	32	2 ICLK	
○	○	○	0008 2044h	DMAC1	DMA destination address register	DMDAR	32	32	2 ICLK	
○	○	○	0008 2048h	DMAC1	DMA transfer count register	DMCRA	32	32	2 ICLK	
○	○	○	0008 204Ch	DMAC1	DMA block transfer count register	DMCRB	16	16	2 ICLK	
○	○	○	0008 2050h	DMAC1	DMA transfer mode register	DMTMD	16	16	2 ICLK	
○	○	○	0008 2053h	DMAC1	DMA interrupt setting register	DMINT	8	8	2 ICLK	
○	○	○	0008 2054h	DMAC1	DMA address mode register	DMAMD	16	16	2 ICLK	
○	○	○	0008 205Ch	DMAC1	DMA transfer enable register	DMCNT	8	8	2 ICLK	
○	○	○	0008 205Dh	DMAC1	DMA software start register	DMREQ	8	8	2 ICLK	
○	○	○	0008 205Eh	DMAC1	DMA status register	DMSTS	8	8	2 ICLK	
○	○	○	0008 205Fh	DMAC1	DMA activation source flag control register	DMCSL	8	8	2 ICLK	
○	○	○	0008 2080h	DMAC2	DMA source address register	DMSAR	32	32	2 ICLK	
○	○	○	0008 2084h	DMAC2	DMA destination address register	DMDAR	32	32	2 ICLK	
○	○	○	0008 2088h	DMAC2	DMA transfer count register	DMCRA	32	32	2 ICLK	
○	○	○	0008 208Ch	DMAC2	DMA block transfer count register	DMCRB	16	16	2 ICLK	
○	○	○	0008 2090h	DMAC2	DMA transfer mode register	DMTMD	16	16	2 ICLK	
○	○	○	0008 2093h	DMAC2	DMA interrupt setting register	DMINT	8	8	2 ICLK	
○	○	○	0008 2094h	DMAC2	DMA address mode register	DMAMD	16	16	2 ICLK	
○	○	○	0008 209Ch	DMAC2	DMA transfer enable register	DMCNT	8	8	2 ICLK	
○	○	○	0008 209Dh	DMAC2	DMA software start register	DMREQ	8	8	2 ICLK	
○	○	○	0008 209Eh	DMAC2	DMA status register	DMSTS	8	8	2 ICLK	
○	○	○	0008 209Fh	DMAC2	DMA activation source flag control register	DMCSL	8	8	2 ICLK	
○	○	○	0008 20C0h	DMAC3	DMA source address register	DMSAR	32	32	2 ICLK	
○	○	○	0008 20C4h	DMAC3	DMA destination address register	DMDAR	32	32	2 ICLK	
○	○	○	0008 20C8h	DMAC3	DMA transfer count register	DMCRA	32	32	2 ICLK	
○	○	○	0008 20CCh	DMAC3	DMA block transfer count register	DMCRB	16	16	2 ICLK	
○	○	○	0008 20D0h	DMAC3	DMA transfer mode register	DMTMD	16	16	2 ICLK	
○	○	○	0008 20D3h	DMAC3	DMA interrupt setting register	DMINT	8	8	2 ICLK	
○	○	○	0008 20D4h	DMAC3	DMA address mode register	DMAMD	16	16	2 ICLK	
○	○	○	0008 20DCh	DMAC3	DMA transfer enable register	DMCNT	8	8	2 ICLK	
○	○	○	0008 20DDh	DMAC3	DMA software start register	DMREQ	8	8	2 ICLK	
○	○	○	0008 20DEh	DMAC3	DMA status register	DMSTS	8	8	2 ICLK	
○	○	○	0008 20DFh	DMAC3	DMA activation source flag control register	DMCSL	8	8	2 ICLK	
○	○	○	0008 2200h	DMAC	DMACA module activation register	DMAST	8	8	2 ICLK	
○	○	○	0008 2400h	DTC	DTC control register	DTCCR	8	8	2 ICLK	
○	○	○	0008 2404h	DTC	DTC vector base register	DTCVBR	32	32	2 ICLK	
○	○	○	0008 2408h	DTC	DTC address mode register	DTCADMOD	8	8	2 ICLK	
○	○	○	0008 240Ch	DTC	DTC module start register	DTCST	8	8	2 ICLK	
○	○	○	0008 240Eh	DTC	DTC status register	DTCSTS	16	16	2 ICLK	
○	—	—	0008 3002h	BSC	CS0 mode register	CS0MOD	16	16	1, 2 BCLK	
○	—	—	0008 3004h	BSC	CS0 wait control register 1	CS0WCR1	32	32	1, 2 BCLK	
○	—	—	0008 3008h	BSC	CS0 wait control register 2	CS0WCR2	32	32	1, 2 BCLK	
○	—	—	0008 3012h	BSC	CS1 mode register	CS1MOD	16	16	1, 2 BCLK	
○	—	—	0008 3014h	BSC	CS1 wait control register 1	CS1WCR1	32	32	1, 2 BCLK	
○	—	—	0008 3018h	BSC	CS1 wait control register 2	CS1WCR2	32	32	1, 2 BCLK	
○	—	—	0008 3022h	BSC	CS2 mode register	CS2MOD	16	16	1, 2 BCLK	
○	—	—	0008 3024h	BSC	CS2 wait control register 1	CS2WCR1	32	32	1, 2 BCLK	
○	—	—	0008 3028h	BSC	CS2 wait control register 2	CS2WCR2	32	32	1, 2 BCLK	
○	—	—	0008 3032h	BSC	CS3 mode register	CS3MOD	16	16	1, 2 BCLK	
○	—	—	0008 3034h	BSC	CS3 wait control register 1	CS3WCR1	32	32	1, 2 BCLK	
○	—	—	0008 3038h	BSC	CS3 wait control register 2	CS3WCR2	32	32	1, 2 BCLK	
○	—	—	0008 3802h	BSC	CS0 control register	CS0CR	16	16	1, 2 BCLK	

Table 4.1 List of I/O Registers (Address Order) (3 / 22)

100-pin	80-pin	64-pin	Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States	
									ICLK ≥ PCLK	ICLK < PCLK
○	—	—	0008 380Ah	BSC	CS0 recovery cycle register	CS0REC	16	16	1, 2 BCLK	
○	—	—	0008 3812h	BSC	CS1 control register	CS1CR	16	16	1, 2 BCLK	
○	—	—	0008 381Ah	BSC	CS1 recovery cycle register	CS1REC	16	16	1, 2 BCLK	
○	—	—	0008 3822h	BSC	CS2 control register	CS2CR	16	16	1, 2 BCLK	
○	—	—	0008 382Ah	BSC	CS2 recovery cycle register	CS2REC	16	16	1, 2 BCLK	
○	—	—	0008 3832h	BSC	CS3 control register	CS3CR	16	16	1, 2 BCLK	
○	—	—	0008 383Ah	BSC	CS3 recovery cycle register	CS3REC	16	16	1, 2 BCLK	
○	—	—	0008 3880h	BSC	CS recovery cycle insertion enable register	CSRECEN	16	16	1, 2 BCLK	
○	○	○	0008 7010h	ICU	Interrupt request register 016	IR016	8	8	2 ICLK	
○	○	○	0008 7015h	ICU	Interrupt request register 021	IR021	8	8	2 ICLK	
○	○	○	0008 7017h	ICU	Interrupt request register 023	IR023	8	8	2 ICLK	
○	○	○	0008 701Bh	ICU	Interrupt request register 027	IR027	8	8	2 ICLK	
○	○	○	0008 701Ch	ICU	Interrupt request register 028	IR028	8	8	2 ICLK	
○	○	○	0008 701Dh	ICU	Interrupt request register 029	IR029	8	8	2 ICLK	
○	○	○	0008 701Eh	ICU	Interrupt request register 030	IR030	8	8	2 ICLK	
○	○	○	0008 701Fh	ICU	Interrupt request register 031	IR031	8	8	2 ICLK	
○	○	○	0008 7020h	ICU	Interrupt request register 032	IR032	8	8	2 ICLK	
○	○	○	0008 7021h	ICU	Interrupt request register 033	IR033	8	8	2 ICLK	
○	○	○	0008 7022h	ICU	Interrupt request register 034	IR034	8	8	2 ICLK	
○	○	○	0008 702Ch	ICU	Interrupt request register 044	IR044	8	8	2 ICLK	
○	○	○	0008 702Dh	ICU	Interrupt request register 045	IR045	8	8	2 ICLK	
○	○	○	0008 702Eh	ICU	Interrupt request register 046	IR046	8	8	2 ICLK	
○	○	○	0008 702Fh	ICU	Interrupt request register 047	IR047	8	8	2 ICLK	
○	○	○	0008 7039h	ICU	Interrupt request register 057	IR057	8	8	2 ICLK	
○	○	○	0008 703Ah	ICU	Interrupt request register 058	IR058	8	8	2 ICLK	
○	○	○	0008 703Bh	ICU	Interrupt request register 059	IR059	8	8	2 ICLK	
○	○	○	0008 703Fh	ICU	Interrupt request register 063	IR063	8	8	2 ICLK	
○	○	○	0008 7040h	ICU	Interrupt request register 064	IR064	8	8	2 ICLK	
○	○	○	0008 7041h	ICU	Interrupt request register 065	IR065	8	8	2 ICLK	
○	○	○	0008 7042h	ICU	Interrupt request register 066	IR066	8	8	2 ICLK	
○	○	○	0008 7043h	ICU	Interrupt request register 067	IR067	8	8	2 ICLK	
○	○	○	0008 7044h	ICU	Interrupt request register 068	IR068	8	8	2 ICLK	
○	○	○	0008 7045h	ICU	Interrupt request register 069	IR069	8	8	2 ICLK	
○	○	○	0008 7046h	ICU	Interrupt request register 070	IR070	8	8	2 ICLK	
○	○	○	0008 7047h	ICU	Interrupt request register 071	IR071	8	8	2 ICLK	
○	○	○	0008 7058h	ICU	Interrupt request register 088	IR088	8	8	2 ICLK	
○	○	○	0008 7059h	ICU	Interrupt request register 089	IR089	8	8	2 ICLK	
○	○	○	0008 705Ch	ICU	Interrupt request register 092	IR092	8	8	2 ICLK	
○	○	○	0008 705Dh	ICU	Interrupt request register 093	IR093	8	8	2 ICLK	
○	○	○	0008 7066h	ICU	Interrupt request register 102	IR102	8	8	2 ICLK	
○	○	○	0008 7067h	ICU	Interrupt request register 103	IR103	8	8	2 ICLK	
○	○	○	0008 706Ah	ICU	Interrupt request register 106	IR106	8	8	2 ICLK	
○	○	○	0008 706Bh	ICU	Interrupt request register 107	IR107	8	8	2 ICLK	
○	○	○	0008 7072h	ICU	Interrupt request register 114	IR114	8	8	2 ICLK	
○	○	○	0008 7073h	ICU	Interrupt request register 115	IR115	8	8	2 ICLK	
○	○	○	0008 7074h	ICU	Interrupt request register 116	IR116	8	8	2 ICLK	
○	○	○	0008 7075h	ICU	Interrupt request register 117	IR117	8	8	2 ICLK	
○	○	○	0008 7076h	ICU	Interrupt request register 118	IR118	8	8	2 ICLK	
○	○	○	0008 7077h	ICU	Interrupt request register 119	IR119	8	8	2 ICLK	
○	○	○	0008 7078h	ICU	Interrupt request register 120	IR120	8	8	2 ICLK	
○	○	○	0008 7079h	ICU	Interrupt request register 121	IR121	8	8	2 ICLK	
○	○	○	0008 707Ah	ICU	Interrupt request register 122	IR122	8	8	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (4 / 22)

100-pin	80-pin	64-pin	Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States	
									ICLK ≥ PCLK	ICLK < PCLK
○	○	○	0008 707Bh	ICU	Interrupt request register 123	IR123	8	8	2 ICLK	
○	○	○	0008 707Ch	ICU	Interrupt request register 124	IR124	8	8	2 ICLK	
○	○	○	0008 707Dh	ICU	Interrupt request register 125	IR125	8	8	2 ICLK	
○	○	○	0008 707Eh	ICU	Interrupt request register 126	IR126	8	8	2 ICLK	
○	○	○	0008 707Fh	ICU	Interrupt request register 127	IR127	8	8	2 ICLK	
○	○	○	0008 7080h	ICU	Interrupt request register 128	IR128	8	8	2 ICLK	
○	○	○	0008 7081h	ICU	Interrupt request register 129	IR129	8	8	2 ICLK	
○	○	○	0008 7082h	ICU	Interrupt request register 130	IR130	8	8	2 ICLK	
○	○	○	0008 7083h	ICU	Interrupt request register 131	IR131	8	8	2 ICLK	
○	○	○	0008 7084h	ICU	Interrupt request register 132	IR132	8	8	2 ICLK	
○	○	○	0008 7085h	ICU	Interrupt request register 133	IR133	8	8	2 ICLK	
○	○	○	0008 7086h	ICU	Interrupt request register 134	IR134	8	8	2 ICLK	
○	○	○	0008 7087h	ICU	Interrupt request register 135	IR135	8	8	2 ICLK	
○	○	○	0008 7088h	ICU	Interrupt request register 136	IR136	8	8	2 ICLK	
○	○	○	0008 7089h	ICU	Interrupt request register 137	IR137	8	8	2 ICLK	
○	○	○	0008 708Ah	ICU	Interrupt request register 138	IR138	8	8	2 ICLK	
○	○	○	0008 708Bh	ICU	Interrupt request register 139	IR139	8	8	2 ICLK	
○	○	○	0008 708Ch	ICU	Interrupt request register 140	IR140	8	8	2 ICLK	
○	○	○	0008 708Dh	ICU	Interrupt request register 141	IR141	8	8	2 ICLK	
○	○	○	0008 70AAh	ICU	Interrupt request register 170	IR170	8	8	2 ICLK	
○	○	○	0008 70ABh	ICU	Interrupt request register 171	IR171	8	8	2 ICLK	
○	○	○	0008 70AEh	ICU	Interrupt request register 174	IR174	8	8	2 ICLK	
○	○	○	0008 70AFh	ICU	Interrupt request register 175	IR175	8	8	2 ICLK	
○	○	○	0008 70B0h	ICU	Interrupt request register 176	IR176	8	8	2 ICLK	
○	○	○	0008 70B1h	ICU	Interrupt request register 177	IR177	8	8	2 ICLK	
○	○	○	0008 70B2h	ICU	Interrupt request register 178	IR178	8	8	2 ICLK	
○	○	○	0008 70B3h	ICU	Interrupt request register 179	IR179	8	8	2 ICLK	
○	○	○	0008 70B4h	ICU	Interrupt request register 180	IR180	8	8	2 ICLK	
○	○	○	0008 70B5h	ICU	Interrupt request register 181	IR181	8	8	2 ICLK	
○	○	○	0008 70B6h	ICU	Interrupt request register 182	IR182	8	8	2 ICLK	
○	○	○	0008 70B7h	ICU	Interrupt request register 183	IR183	8	8	2 ICLK	
○	○	○	0008 70B8h	ICU	Interrupt request register 184	IR184	8	8	2 ICLK	
○	○	○	0008 70B9h	ICU	Interrupt request register 185	IR185	8	8	2 ICLK	
○	○	○	0008 70C6h	ICU	Interrupt request register 198	IR198	8	8	2 ICLK	
○	○	○	0008 70C7h	ICU	Interrupt request register 199	IR199	8	8	2 ICLK	
○	○	○	0008 70C8h	ICU	Interrupt request register 200	IR200	8	8	2 ICLK	
○	○	○	0008 70C9h	ICU	Interrupt request register 201	IR201	8	8	2 ICLK	
○	○	—	0008 70D6h	ICU	Interrupt request register 214	IR214	8	8	2 ICLK	
○	○	—	0008 70D7h	ICU	Interrupt request register 215	IR215	8	8	2 ICLK	
○	○	—	0008 70D8h	ICU	Interrupt request register 216	IR216	8	8	2 ICLK	
○	○	—	0008 70D9h	ICU	Interrupt request register 217	IR217	8	8	2 ICLK	
○	○	○	0008 70DAh	ICU	Interrupt request register 218	IR218	8	8	2 ICLK	
○	○	○	0008 70DBh	ICU	Interrupt request register 219	IR219	8	8	2 ICLK	
○	○	○	0008 70DCh	ICU	Interrupt request register 220	IR220	8	8	2 ICLK	
○	○	○	0008 70DDh	ICU	Interrupt request register 221	IR221	8	8	2 ICLK	
○	○	○	0008 70DEh	ICU	Interrupt request register 222	IR222	8	8	2 ICLK	
○	○	○	0008 70DFh	ICU	Interrupt request register 223	IR223	8	8	2 ICLK	
○	○	○	0008 70E0h	ICU	Interrupt request register 224	IR224	8	8	2 ICLK	
○	○	○	0008 70E1h	ICU	Interrupt request register 225	IR225	8	8	2 ICLK	
○	○	○	0008 70E2h	ICU	Interrupt request register 226	IR226	8	8	2 ICLK	
○	○	○	0008 70E3h	ICU	Interrupt request register 227	IR227	8	8	2 ICLK	
○	○	○	0008 70E4h	ICU	Interrupt request register 228	IR228	8	8	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (5 / 22)

100-pin	80-pin	64-pin	Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States	
									ICLK ≥ PCLK	ICLK < PCLK
○	○	○	0008 70E5h	ICU	Interrupt request register 229	IR229	8	8	2 ICLK	
○	○	○	0008 70E6h	ICU	Interrupt request register 230	IR230	8	8	2 ICLK	
○	○	○	0008 70E7h	ICU	Interrupt request register 231	IR231	8	8	2 ICLK	
○	○	○	0008 70E8h	ICU	Interrupt request register 232	IR232	8	8	2 ICLK	
○	○	○	0008 70E9h	ICU	Interrupt request register 233	IR233	8	8	2 ICLK	
○	○	○	0008 70EAh	ICU	Interrupt request register 234	IR234	8	8	2 ICLK	
○	○	○	0008 70EBh	ICU	Interrupt request register 235	IR235	8	8	2 ICLK	
○	○	○	0008 70ECh	ICU	Interrupt request register 236	IR236	8	8	2 ICLK	
○	○	○	0008 70EDh	ICU	Interrupt request register 237	IR237	8	8	2 ICLK	
○	○	○	0008 70EEh	ICU	Interrupt request register 238	IR238	8	8	2 ICLK	
○	○	○	0008 70EFh	ICU	Interrupt request register 239	IR239	8	8	2 ICLK	
○	○	○	0008 70F0h	ICU	Interrupt request register 240	IR240	8	8	2 ICLK	
○	○	○	0008 70F1h	ICU	Interrupt request register 241	IR241	8	8	2 ICLK	
○	○	○	0008 70F2h	ICU	Interrupt request register 242	IR242	8	8	2 ICLK	
○	○	○	0008 70F3h	ICU	Interrupt request register 243	IR243	8	8	2 ICLK	
○	○	○	0008 70F4h	ICU	Interrupt request register 244	IR244	8	8	2 ICLK	
○	○	○	0008 70F5h	ICU	Interrupt request register 245	IR245	8	8	2 ICLK	
○	○	○	0008 70F6h	ICU	Interrupt request register 246	IR246	8	8	2 ICLK	
○	○	○	0008 70F7h	ICU	Interrupt request register 247	IR247	8	8	2 ICLK	
○	○	○	0008 70F8h	ICU	Interrupt request register 248	IR248	8	8	2 ICLK	
○	○	○	0008 70F9h	ICU	Interrupt request register 249	IR249	8	8	2 ICLK	
○	○	○	0008 711Bh	ICU	DTC activation enable register027	DTCER027	8	8	2 ICLK	
○	○	○	0008 711Ch	ICU	DTC activation enable register028	DTCER028	8	8	2 ICLK	
○	○	○	0008 711Dh	ICU	DTC activation enable register029	DTCER029	8	8	2 ICLK	
○	○	○	0008 711Eh	ICU	DTC activation enable register030	DTCER030	8	8	2 ICLK	
○	○	○	0008 711Fh	ICU	DTC activation enable register031	DTCER031	8	8	2 ICLK	
○	○	○	0008 712Dh	ICU	DTC activation enable register045	DTCER045	8	8	2 ICLK	
○	○	○	0008 712Eh	ICU	DTC activation enable register046	DTCER046	8	8	2 ICLK	
○	○	○	0008 713Ah	ICU	DTC activation enable register058	DTCER058	8	8	2 ICLK	
○	○	○	0008 713Bh	ICU	DTC activation enable register059	DTCER059	8	8	2 ICLK	
○	○	○	0008 7140h	ICU	DTC activation enable register064	DTCER064	8	8	2 ICLK	
○	○	○	0008 7141h	ICU	DTC activation enable register065	DTCER065	8	8	2 ICLK	
○	○	○	0008 7142h	ICU	DTC activation enable register066	DTCER066	8	8	2 ICLK	
○	○	○	0008 7143h	ICU	DTC activation enable register067	DTCER067	8	8	2 ICLK	
○	○	○	0008 7144h	ICU	DTC activation enable register068	DTCER068	8	8	2 ICLK	
○	○	○	0008 7145h	ICU	DTC activation enable register069	DTCER069	8	8	2 ICLK	
○	○	○	0008 7146h	ICU	DTC activation enable register070	DTCER070	8	8	2 ICLK	
○	○	○	0008 7147h	ICU	DTC activation enable register071	DTCER071	8	8	2 ICLK	
○	○	○	0008 7166h	ICU	DTC activation enable register102	DTCER102	8	8	2 ICLK	
○	○	○	0008 7167h	ICU	DTC activation enable register103	DTCER103	8	8	2 ICLK	
○	○	○	0008 716Ah	ICU	DTC activation enable register106	DTCER106	8	8	2 ICLK	
○	○	○	0008 716Bh	ICU	DTC activation enable register107	DTCER107	8	8	2 ICLK	
○	○	○	0008 7172h	ICU	DTC activation enable register114	DTCER114	8	8	2 ICLK	
○	○	○	0008 7173h	ICU	DTC activation enable register115	DTCER115	8	8	2 ICLK	
○	○	○	0008 7174h	ICU	DTC activation enable register116	DTCER116	8	8	2 ICLK	
○	○	○	0008 7175h	ICU	DTC activation enable register117	DTCER117	8	8	2 ICLK	
○	○	○	0008 7179h	ICU	DTC activation enable register121	DTCER121	8	8	2 ICLK	
○	○	○	0008 717Ah	ICU	DTC activation enable register122	DTCER122	8	8	2 ICLK	
○	○	○	0008 717Dh	ICU	DTC activation enable register125	DTCER125	8	8	2 ICLK	
○	○	○	0008 717Eh	ICU	DTC activation enable register126	DTCER126	8	8	2 ICLK	
○	○	○	0008 7181h	ICU	DTC activation enable register129	DTCER129	8	8	2 ICLK	
○	○	○	0008 7182h	ICU	DTC activation enable register130	DTCER130	8	8	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (6 / 22)

100-pin	80-pin	64-pin	Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States	
									ICLK ≥ PCLK	ICLK < PCLK
○	○	○	0008 7183h	ICU	DTC activation enable register131	DTCER131	8	8	2 ICLK	
○	○	○	0008 7184h	ICU	DTC activation enable register132	DTCER132	8	8	2 ICLK	
○	○	○	0008 7186h	ICU	DTC activation enable register134	DTCER134	8	8	2 ICLK	
○	○	○	0008 7187h	ICU	DTC activation enable register135	DTCER135	8	8	2 ICLK	
○	○	○	0008 7188h	ICU	DTC activation enable register136	DTCER136	8	8	2 ICLK	
○	○	○	0008 7189h	ICU	DTC activation enable register137	DTCER137	8	8	2 ICLK	
○	○	○	0008 718Ah	ICU	DTC activation enable register138	DTCER138	8	8	2 ICLK	
○	○	○	0008 718Bh	ICU	DTC activation enable register139	DTCER139	8	8	2 ICLK	
○	○	○	0008 718Ch	ICU	DTC activation enable register140	DTCER140	8	8	2 ICLK	
○	○	○	0008 718Dh	ICU	DTC activation enable register141	DTCER141	8	8	2 ICLK	
○	○	○	0008 71AEh	ICU	DTC activation enable register174	DTCER174	8	8	2 ICLK	
○	○	○	0008 71AFh	ICU	DTC activation enable register175	DTCER175	8	8	2 ICLK	
○	○	○	0008 71B1h	ICU	DTC activation enable register177	DTCER177	8	8	2 ICLK	
○	○	○	0008 71B2h	ICU	DTC activation enable register178	DTCER178	8	8	2 ICLK	
○	○	○	0008 71B4h	ICU	DTC activation enable register180	DTCER180	8	8	2 ICLK	
○	○	○	0008 71B5h	ICU	DTC activation enable register181	DTCER181	8	8	2 ICLK	
○	○	○	0008 71B7h	ICU	DTC activation enable register183	DTCER183	8	8	2 ICLK	
○	○	○	0008 71B8h	ICU	DTC activation enable register184	DTCER184	8	8	2 ICLK	
○	○	○	0008 71C6h	ICU	DTC activation enable register198	DTCER198	8	8	2 ICLK	
○	○	○	0008 71C7h	ICU	DTC activation enable register199	DTCER199	8	8	2 ICLK	
○	○	○	0008 71C8h	ICU	DTC activation enable register200	DTCER200	8	8	2 ICLK	
○	○	○	0008 71C9h	ICU	DTC activation enable register201	DTCER201	8	8	2 ICLK	
○	○	○	0008 71D7h	ICU	DTC activation enable register215	DTCER215	8	8	2 ICLK	
○	○	○	0008 71D8h	ICU	DTC activation enable register216	DTCER216	8	8	2 ICLK	
○	○	○	0008 71DBh	ICU	DTC activation enable register219	DTCER219	8	8	2 ICLK	
○	○	○	0008 71DCh	ICU	DTC activation enable register220	DTCER220	8	8	2 ICLK	
○	○	○	0008 71DFh	ICU	DTC activation enable register223	DTCER223	8	8	2 ICLK	
○	○	○	0008 71E0h	ICU	DTC activation enable register224	DTCER224	8	8	2 ICLK	
○	○	○	0008 71E3h	ICU	DTC activation enable register227	DTCER227	8	8	2 ICLK	
○	○	○	0008 71E4h	ICU	DTC activation enable register228	DTCER228	8	8	2 ICLK	
○	○	○	0008 71E7h	ICU	DTC activation enable register231	DTCER231	8	8	2 ICLK	
○	○	○	0008 71E8h	ICU	DTC activation enable register232	DTCER232	8	8	2 ICLK	
○	○	○	0008 71EBh	ICU	DTC activation enable register235	DTCER235	8	8	2 ICLK	
○	○	○	0008 71ECh	ICU	DTC activation enable register236	DTCER236	8	8	2 ICLK	
○	○	○	0008 71EFh	ICU	DTC activation enable register239	DTCER239	8	8	2 ICLK	
○	○	○	0008 71F0h	ICU	DTC activation enable register240	DTCER240	8	8	2 ICLK	
○	○	○	0008 71F7h	ICU	DTC activation enable register247	DTCER247	8	8	2 ICLK	
○	○	○	0008 71F8h	ICU	DTC activation enable register248	DTCER248	8	8	2 ICLK	
○	○	○	0008 7202h	ICU	Interrupt request enable register 02	IER02	8	8	2 ICLK	
○	○	○	0008 7203h	ICU	Interrupt request enable register 03	IER03	8	8	2 ICLK	
○	○	○	0008 7204h	ICU	Interrupt request enable register 04	IER04	8	8	2 ICLK	
○	○	○	0008 7205h	ICU	Interrupt request enable register 05	IER05	8	8	2 ICLK	
○	○	○	0008 7207h	ICU	Interrupt request enable register 07	IER07	8	8	2 ICLK	
○	○	○	0008 7208h	ICU	Interrupt request enable register 08	IER08	8	8	2 ICLK	
○	○	○	0008 720Bh	ICU	Interrupt request enable register 0B	IER0B	8	8	2 ICLK	
○	○	○	0008 720Ch	ICU	Interrupt request enable register 0C	IER0C	8	8	2 ICLK	
○	○	○	0008 720Dh	ICU	Interrupt request enable register 0D	IER0D	8	8	2 ICLK	
○	○	○	0008 720Eh	ICU	Interrupt request enable register 0E	IER0E	8	8	2 ICLK	
○	○	○	0008 720Fh	ICU	Interrupt request enable register 0F	IER0F	8	8	2 ICLK	
○	○	○	0008 7210h	ICU	Interrupt request enable register 10	IER10	8	8	2 ICLK	
○	○	○	0008 7211h	ICU	Interrupt request enable register 11	IER11	8	8	2 ICLK	
○	○	○	0008 7215h	ICU	Interrupt request enable register 15	IER15	8	8	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (7 / 22)

100-pin	80-pin	64-pin	Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States	
									ICLK ≥ PCLK	ICLK < PCLK
○	○	○	0008 7216h	ICU	Interrupt request enable register 16	IER16	8	8	2 ICLK	
○	○	○	0008 7217h	ICU	Interrupt request enable register 17	IER17	8	8	2 ICLK	
○	○	○	0008 7218h	ICU	Interrupt request enable register 18	IER18	8	8	2 ICLK	
○	○	○	0008 7219h	ICU	Interrupt request enable register 19	IER19	8	8	2 ICLK	
○	○	○	0008 721Ah	ICU	Interrupt request enable register 1A	IER1A	8	8	2 ICLK	
○	○	○	0008 721Bh	ICU	Interrupt request enable register 1B	IER1B	8	8	2 ICLK	
○	○	○	0008 721Ch	ICU	Interrupt request enable register 1C	IER1C	8	8	2 ICLK	
○	○	○	0008 721Dh	ICU	Interrupt request enable register 1D	IER1D	8	8	2 ICLK	
○	○	○	0008 721Eh	ICU	Interrupt request enable register 1E	IER1E	8	8	2 ICLK	
○	○	○	0008 721Fh	ICU	Interrupt request enable register 1F	IER1F	8	8	2 ICLK	
○	○	○	0008 72E0h	ICU	Software interrupt activation register	SWINTR	8	8	2 ICLK	
○	○	○	0008 72F0h	ICU	Fast interrupt set register	FIR	16	16	2 ICLK	
○	○	○	0008 7300h	ICU	Interrupt source priority register 000	IPR000	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 7301h	ICU	Interrupt source priority register 001	IPR001	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 7302h	ICU	Interrupt source priority register 002	IPR002	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 7303h	ICU	Interrupt source priority register 003	IPR003	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 7304h	ICU	Interrupt source priority register 004	IPR004	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 7305h	ICU	Interrupt source priority register 005	IPR005	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 7306h	ICU	Interrupt source priority register 006	IPR006	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 7307h	ICU	Interrupt source priority register 007	IPR007	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 7320h	ICU	Interrupt source priority register 032	IPR032	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 7321h	ICU	Interrupt source priority register 033	IPR033	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 7322h	ICU	Interrupt source priority register 034	IPR034	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 732Ch	ICU	Interrupt source priority register 044	IPR044	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 7339h	ICU	Interrupt source priority register 057	IPR057	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 733Ah	ICU	Interrupt source priority register 058	IPR058	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 733Bh	ICU	Interrupt source priority register 059	IPR059	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 733Fh	ICU	Interrupt source priority register 063	IPR063	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 7340h	ICU	Interrupt source priority register 064	IPR064	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 7341h	ICU	Interrupt source priority register 065	IPR065	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 7342h	ICU	Interrupt source priority register 066	IPR066	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 7343h	ICU	Interrupt source priority register 067	IPR067	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 7344h	ICU	Interrupt source priority register 068	IPR068	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 7345h	ICU	Interrupt source priority register 069	IPR069	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 7346h	ICU	Interrupt source priority register 070	IPR070	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 7347h	ICU	Interrupt source priority register 071	IPR071	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 7358h	ICU	Interrupt source priority register 088	IPR088	8	8	3 ICLK for reading, 2 ICLK for writing	

Table 4.1 List of I/O Registers (Address Order) (8 / 22)

100-pin	80-pin	64-pin	Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States	
									ICLK ≥ PCLK	ICLK < PCLK
○	○	○	0008 7359h	ICU	Interrupt source priority register 089	IPR089	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 735Ch	ICU	Interrupt source priority register 092	IPR092	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 735Dh	ICU	Interrupt source priority register 093	IPR093	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 7366h	ICU	Interrupt source priority register 102	IPR102	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 7367h	ICU	Interrupt source priority register 103	IPR103	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 736Ah	ICU	Interrupt source priority register 106	IPR106	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 736Bh	ICU	Interrupt source priority register 107	IPR107	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 7372h	ICU	Interrupt source priority register 114	IPR114	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 7376h	ICU	Interrupt source priority register 118	IPR118	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 7379h	ICU	Interrupt source priority register 121	IPR121	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 737Bh	ICU	Interrupt source priority register 123	IPR123	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 737Dh	ICU	Interrupt source priority register 125	IPR125	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 737Fh	ICU	Interrupt source priority register 127	IPR127	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 7381h	ICU	Interrupt source priority register 129	IPR129	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 7385h	ICU	Interrupt source priority register 133	IPR133	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 7386h	ICU	Interrupt source priority register 134	IPR134	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 738Ah	ICU	Interrupt source priority register 138	IPR138	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 738Bh	ICU	Interrupt source priority register 139	IPR139	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 73AAh	ICU	Interrupt source priority register 170	IPR170	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 73ABh	ICU	Interrupt source priority register 171	IPR171	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 73AEh	ICU	Interrupt source priority register 174	IPR174	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 73B1h	ICU	Interrupt source priority register 177	IPR177	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 73B4h	ICU	Interrupt source priority register 180	IPR180	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 73B7h	ICU	Interrupt source priority register 183	IPR183	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 73C6h	ICU	Interrupt source priority register 198	IPR198	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 73C7h	ICU	Interrupt source priority register 199	IPR199	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 73C8h	ICU	Interrupt source priority register 200	IPR200	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 73C9h	ICU	Interrupt source priority register 201	IPR201	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 73D6h	ICU	Interrupt source priority register 214	IPR214	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 73DAh	ICU	Interrupt source priority register 218	IPR218	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 73DEh	ICU	Interrupt source priority register 222	IPR222	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 73E2h	ICU	Interrupt source priority register 226	IPR226	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 73E6h	ICU	Interrupt source priority register 230	IPR230	8	8	3 ICLK for reading, 2 ICLK for writing	

Table 4.1 List of I/O Registers (Address Order) (9 / 22)

100-pin	80-pin	64-pin	Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States	
									ICLK ≥ PCLK	ICLK < PCLK
○	○	○	0008 73EAh	ICU	Interrupt source priority register 234	IPR234	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 73EEh	ICU	Interrupt source priority register 238	IPR238	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 73F2h	ICU	Interrupt source priority register 242	IPR242	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 73F3h	ICU	Interrupt source priority register 243	IPR243	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 73F4h	ICU	Interrupt source priority register 244	IPR244	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 73F5h	ICU	Interrupt source priority register 245	IPR245	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 73F6h	ICU	Interrupt source priority register 246	IPR246	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 73F7h	ICU	Interrupt source priority register 247	IPR247	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 73F8h	ICU	Interrupt source priority register 248	IPR248	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 73F9h	ICU	Interrupt source priority register 249	IPR249	8	8	3 ICLK for reading, 2 ICLK for writing	
○	○	○	0008 7400h	ICU	DMACA activation request select register 0	DMRSR0	8	8	2 ICLK	
○	○	○	0008 7404h	ICU	DMACA activation request select register 1	DMRSR1	8	8	2 ICLK	
○	○	○	0008 7408h	ICU	DMACA activation request select register 2	DMRSR2	8	8	2 ICLK	
○	○	○	0008 740Ch	ICU	DMACA activation request select register 3	DMRSR3	8	8	2 ICLK	
○	○	○	0008 7500h	ICU	IRQ control register 0	IRQCR0	8	8	2 ICLK	
○	○	○	0008 7501h	ICU	IRQ control register 1	IRQCR1	8	8	2 ICLK	
○	○	○	0008 7502h	ICU	IRQ control register 2	IRQCR2	8	8	2 ICLK	
○	○	○	0008 7503h	ICU	IRQ control register 3	IRQCR3	8	8	2 ICLK	
○	○	○	0008 7504h	ICU	IRQ control register 4	IRQCR4	8	8	2 ICLK	
○	○	○	0008 7505h	ICU	IRQ control register 5	IRQCR5	8	8	2 ICLK	
○	○	○	0008 7506h	ICU	IRQ control register 6	IRQCR6	8	8	2 ICLK	
○	○	○	0008 7507h	ICU	IRQ control register 7	IRQCR7	8	8	2 ICLK	
○	○	○	0008 7510h	ICU	IRQ pin digital filter enable register 0	IRQFLTE0	8	8	2 ICLK	
○	○	○	0008 7514h	ICU	IRQ pin digital filter setting registerr 0	IRQFLTC0	16	16	2 ICLK	
○	○	○	0008 7580h	ICU	Non-maskable interrupt status register	NMISR	8	8	2 ICLK	
○	○	○	0008 7581h	ICU	Non-maskable interrupt enable register	NMIER	8	8	2 ICLK	
○	○	○	0008 7582h	ICU	Non-maskable interrupt clear register	NMICLR	8	8	2 ICLK	
○	○	○	0008 7583h	ICU	NMI pin interrupt control register	NMICR	8	8	2 ICLK	
○	○	○	0008 7590h	ICU	NMI pin digital filter enable register	NMIFLTE	8	8	2 ICLK	
○	○	○	0008 7594h	ICU	NMI pin digital filter setting register	NMIFLTC	8	8	2 ICLK	
○	○	○	0008 8000h	CMT	Compare match timer start register 0	CMSTR0	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8002h	CMT0	Compare match timer control register	CMCR	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8004h	CMT0	Compare match timer counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8006h	CMT0	Compare match timer constant register	CMCOR	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8008h	CMT1	Compare match timer control register	CMCR	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 800Ah	CMT1	Compare match timer counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 800Ch	CMT1	Compare match timer constant register	CMCOR	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8010h	CMT	Compare match timer start register 1	CMSTR1	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8012h	CMT2	Compare match timer control register	CMCR	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8014h	CMT2	Compare match timer counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8016h	CMT2	Compare match timer constant register	CMCOR	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8018h	CMT3	Compare match timer control register	CMCR	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 801Ah	CMT3	Compare match timer counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 801Ch	CMT3	Compare match timer constant register	CMCOR	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8020h	WDT	WDT refresh register	WDTRR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8022h	WDT	WDT control register	WDTCR	16	16	2, 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (10 / 22)

100-pin	80-pin	64-pin	Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States	
									ICLK ≥ PCLK	ICLK < PCLK
○	○	○	0008 8024h	WDT	WDT status register	WDTSR	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8026h	WDT	WDT reset control register	WDTRCR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8030h	IWDT	IWDT refresh register	IWDTRR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8032h	IWDT	IWDT control register	IWDTCR	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8034h	IWDT	IWDT status register	IWDTSR	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8036h	IWDT	IWDT reset control register	IWDTRCR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8038h	IWDT	IWDT count stop control register	IWDTCSTPR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 80C0h	DA	D/A data register 0	DADR0	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 80C2h	DA	D/A data register 1	DADR1	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 80C4h	DA	D/A control register	DACR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 80C5h	DA	DADRm format select register	DADPR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8200h	TMR0	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8201h	TMR1	Timer counter control register	TCR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8202h	TMR0	Timer control/status register	TCSR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8203h	TMR1	Timer control/status register	TCSR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8204h	TMR0	Time constant register A	TCORA	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8205h	TMR1	Time constant register A	TCORA	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8206h	TMR0	Time constant register B	TCORB	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8207h	TMR1	Time constant register B	TCORB	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8208h	TMR0	Timer counter	TCNT	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8209h	TMR1	Timer counter	TCNT	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 820Ah	TMR0	Timer counter control register	TCCR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 820Bh	TMR1	Timer counter control register	TCCR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 820Ch	TMR0	Time count start register	TCSTR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8210h	TMR2	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8211h	TMR3	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8212h	TMR2	Timer control/status registe	TCSR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8213h	TMR3	Timer control/status registe	TCSR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8214h	TMR2	Time constant register A	TCORA	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8215h	TMR3	Time constant register A	TCORA	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8216h	TMR2	Time constant register B	TCORB	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8217h	TMR3	Time constant register B	TCORB	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8218h	TMR2	Timer counter	TCNT	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8219h	TMR3	Timer counter	TCNT	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 821Ah	TMR2	Timer counter control register	TCCR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 821Bh	TMR3	Timer counter control register	TCCR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 821Ch	TMR2	Time count start register	TCSTR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8280h	CRC	CRC control register	CRCCR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8281h	CRC	CRC data input register	CRCDIR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8282h	CRC	CRC data output register	CRCDOR	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8300h	RIIC0	I^2C bus control register 1	ICCR1	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8301h	RIIC0	I^2C bus control register 2	ICCR2	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8302h	RIIC0	I^2C bus mode register 1	ICMR1	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8303h	RIIC0	I^2C bus mode register 2	ICMR2	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8304h	RIIC0	I^2C bus mode register 3	ICMR3	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8305h	RIIC0	I^2C bus function enable register	ICFER	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8306h	RIIC0	I^2C bus status enable register	ICSER	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8307h	RIIC0	I^2C bus interrupt enable register	ICIER	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8308h	RIIC0	I^2C bus status register 1	ICSR1	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8309h	RIIC0	I^2C bus status register 2	ICSR2	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 830Ah	RIIC0	Slave address register L0	SARL0	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 830Bh	RIIC0	Slave address register U0	SARU0	8	8	2, 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (11 / 22)

100-pin	80-pin	64-pin	Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States	
									ICLK ≥ PCLK	ICLK < PCLK
○	○	○	0008 830Ch	RIIC0	Slave address register L1	SARL1	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 830Dh	RIIC0	Slave address register U1	SARU1	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 830Eh	RIIC0	Slave address register L2	SARL2	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 830Fh	RIIC0	Slave address register U2	SARU2	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8310h	RIIC0	I^2C bus bit rate low-level register	ICBRL	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8311h	RIIC0	I^2C bus bit rate high-level register	ICBRH	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8312h	RIIC0	I^2C bus transmit data register	ICDRT	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8313h	RIIC0	I^2C bus receive data register	ICDRR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8380h	RSPI0	RSPI control register	SPCR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8381h	RSPI0	RSPI slave select polarity register	SSLP	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8382h	RSPI0	RSPI pin control register	SPPCR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8383h	RSPI0	RSPI status register	SPSR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8384h	RSPI0	RSPI data register	SPDR	32	16, 32	2, 3 PCLKB	2 ICLK
○	○	○	0008 8388h	RSPI0	RSPI sequence control register	SPSCR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8389h	RSPI0	RSPI sequence status register	SPSSR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 838Ah	RSPI0	RSPI bit rate register	SPBR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 838Bh	RSPI0	RSPI data control register	SPDCR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 838Ch	RSPI0	RSPI clock delay register	SPCKD	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 838Dh	RSPI0	RSPI slave select negation delay register	SSLND	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 838Eh	RSPI0	RSPI next-access delay register	SPND	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 838Fh	RSPI0	RSPI control register 2	SPCR2	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8390h	RSPI0	RSPI command register 0	SPCMD0	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8392h	RSPI0	RSPI command register 1	SPCMD1	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8394h	RSPI0	RSPI command register 2	SPCMD2	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8396h	RSPI0	RSPI command register 3	SPCMD3	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8398h	RSPI0	RSPI command register 4	SPCMD4	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 839Ah	RSPI0	RSPI command register 5	SPCMD5	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 839Ch	RSPI0	RSPI command register 6	SPCMD6	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 839Eh	RSPI0	RSPI command register 7	SPCMD7	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8600h	MTU3	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8601h	MTU4	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8602h	MTU3	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8603h	MTU4	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8604h	MTU3	Timer I/O control register H	TIORH	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8605h	MTU3	Timer I/O control register L	TIORL	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8606h	MTU4	Timer I/O control register H	TIORH	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8607h	MTU4	Timer I/O control register L	TIORL	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8608h	MTU3	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8609h	MTU4	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 860Ah	MTU	Timer output master enable register	TOER	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 860Dh	MTU	Timer gate control register	TGCR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 860Eh	MTU	Timer output control register 1	TOCR1	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 860Fh	MTU	Timer output control register 2	TOCR2	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8610h	MTU3	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8612h	MTU4	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8614h	MTU	Timer cycle data register	TCDR	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8616h	MTU	Timer dead time data register	TDDR	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8618h	MTU3	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 861Ah	MTU3	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 861Ch	MTU4	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 861Eh	MTU4	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8620h	MTU	Timer subcounter	TCNTS	16	16	2, 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (12 / 22)

100-pin	80-pin	64-pin	Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States	
									ICLK ≥ PCLK	ICLK < PCLK
○	○	○	0008 8622h	MTU	Timer cycle buffer register	TCBR	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8624h	MTU3	Timer general register C	TGRC	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8626h	MTU3	Timer general register D	TGRD	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8628h	MTU4	Timer general register C	TGRC	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 862Ah	MTU4	Timer general register D	TGRD	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 862Ch	MTU3	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 862Dh	MTU4	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8630h	MTU	Timer interrupt skipping set register	TITCR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8631h	MTU	Timer interrupt skipping counter	TITCNT	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8632h	MTU	Timer buffer transfer set register	TBTER	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8634h	MTU	Timer dead time enable register	TDER	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8636h	MTU	Timer output level buffer register	TOLBR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8638h	MTU3	Timer buffer operation transfer mode register	TBTM	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8639h	MTU4	Timer buffer operation transfer mode register	TBTM	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8640h	MTU4	Timer A/D converter start request control register	TADCR	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8644h	MTU4	Timer A/D converter start request cycle set register A	TADCORA	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8646h	MTU4	Timer A/D converter start request cycle set register B	TADCORB	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8648h	MTU4	Timer A/D converter start request cycle set buffer register A	TADCOBRA	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 864Ah	MTU4	Timer A/D converter start request cycle set buffer register B	TADCOBRB	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8660h	MTU	Timer waveform control register	TWCR	8	8, 16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8680h	MTU	Timer start register	TSTR	8	8, 16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8681h	MTU	Timer synchronous register	TSYR	8	8, 16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8684h	MTU	Timer read/write enable register	TRWER	8	8, 16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8690h	MTU0	Noise filter control register	NFCR	8	8, 16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8691h	MTU1	Noise filter control register	NFCR	8	8, 16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8692h	MTU2	Noise filter control register	NFCR	8	8, 16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8693h	MTU3	Noise filter control register	NFCR	8	8, 16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8694h	MTU4	Noise filter control register	NFCR	8	8, 16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8695h	MTU5	Noise filter control register	NFCR	8	8, 16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8700h	MTU0	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8701h	MTU0	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8702h	MTU0	Timer I/O control register H	TIORH	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8703h	MTU0	Timer I/O control register L	TIORL	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8704h	MTU0	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8705h	MTU0	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8706h	MTU0	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8708h	MTU0	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 870Ah	MTU0	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 870Ch	MTU0	Timer general register C	TGRC	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 870Eh	MTU0	Timer general register D	TGRD	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8720h	MTU0	Timer general register E	TGRE	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8722h	MTU0	Timer general register F	TGRF	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8724h	MTU0	Timer interrupt enable register 2	TIER2	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8726h	MTU0	Timer buffer operation transfer mode register	TBTM	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8780h	MTU1	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8781h	MTU1	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8782h	MTU1	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8784h	MTU1	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8785h	MTU1	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8786h	MTU1	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8788h	MTU1	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 878Ah	MTU1	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (13 / 22)

100-pin	80-pin	64-pin	Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States	
									ICLK ≥ PCLK	ICLK < PCLK
○	○	○	0008 8790h	MTU1	Timer input capture control register	TICCR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8800h	MTU2	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8801h	MTU2	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8802h	MTU2	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8804h	MTU2	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8805h	MTU2	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8806h	MTU2	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8808h	MTU2	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 880Ah	MTU2	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8880h	MTU5	Timer counter U	TCNTU	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8882h	MTU5	Timer general register U	TGRU	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8884h	MTU5	Timer control register U	TCRU	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8886h	MTU5	Timer I/O control register U	TIORU	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8890h	MTU5	Timer counter V	TCNTV	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8892h	MTU5	Timer general register V	TGRV	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8894h	MTU5	Timer control register V	TCRV	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8896h	MTU5	Timer I/O control register V	TIORV	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 88A0h	MTU5	Timer counter W	TCNTW	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 88A2h	MTU5	Timer general register W	TGRW	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 88A4h	MTU5	Timer control register W	TCRW	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 88A6h	MTU5	Timer I/O control register W	TIORW	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 88B2h	MTU5	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 88B4h	MTU5	Timer start registe	TSTR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 88B6h	MTU5	Timer compare match clear registe	TCNTCMPCLR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 8900h	POE	Input level control/status register 1	ICSR1	16	8, 16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8902h	POE	Output level control/status register 1	OCSR1	16	8, 16	2, 3 PCLKB	2 ICLK
○	○	○	0008 8908h	POE	Input level control/status register 2	ICSR2	16	8, 16	2, 3 PCLKB	2 ICLK
○	○	○	0008 890Ah	POE	Software port output enable register	SPOER	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 890Bh	POE	Port output enable control register 1	POECR1	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 890Ch	POE	Port output enable control register 2	POECR2	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 890Eh	POE	Input level control/status register 3	ICSR3	16	8, 16	2, 3 PCLKB	2 ICLK
○	○	○	0008 9000h	S12AD	A/D control register	ADCSR	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 9004h	S12AD	A/D channel select register A	ADANSA	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 9008h	S12AD	A/D-converted value addition mode select register	ADADS	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 900Ch	S12AD	A/D-converted value addition count select register	ADADC	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 900Eh	S12AD	A/D control extended register	ADCER	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 9010h	S12AD	A/D start trigger select register	ADSTRGR	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 9012h	S12AD	A/D-converted extended input control register	ADEXICR	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 9014h	S12AD	A/D channel select register B	ADANSB	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 9018h	S12AD	A/D double register	ADDBLDR	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 901Ah	S12AD	A/D temperature sensor data register	ADTSDR	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 901Ch	S12AD	A/D internal reference voltage data register	ADOCDR	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 901Eh	S12AD	A/D self-diagnosis data register	ADRD	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 9020h	S12AD	A/D data register 0	ADDR0	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 9022h	S12AD	A/D data register 1	ADDR1	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 9024h	S12AD	A/D data register 2	ADDR2	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 9026h	S12AD	A/D data register 3	ADDR3	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 9028h	S12AD	A/D data register 4	ADDR4	16	16	2, 3 PCLKB	2 ICLK
○	○	—	0008 902Ah	S12AD	A/D data register 5	ADDR5	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 902Ch	S12AD	A/D data register 6	ADDR6	16	16	2, 3 PCLKB	2 ICLK
○	○	—	0008 902Eh	S12AD	A/D data register 7	ADDR7	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 9030h	S12AD	A/D data register 8	ADDR8	16	16	2, 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (14 / 22)

100-pin	80-pin	64-pin	Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States	
									ICLK ≥ PCLK	ICLK < PCLK
○	○	○	0008 9032h	S12AD	A/D data register 9	ADDR9	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 9034h	S12AD	A/D data register 10	ADDR10	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 9036h	S12AD	A/D data register 11	ADDR11	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 9038h	S12AD	A/D data register 12	ADDR12	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 903Ah	S12AD	A/D data register 13	ADDR13	16	16	2, 3 PCLKB	2 ICLK
○	—	—	0008 903Ch	S12AD	A/D data register 14	ADDR14	16	16	2, 3 PCLKB	2 ICLK
○	—	—	0008 903Eh	S12AD	A/D data register 15	ADDR15	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 9060h	S12AD	A/D sampling state register 0	ADSSTR0	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 9061h	S12AD	A/D sampling state register L	ADSSTRL	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 9066h	S12AD	A/D sample and hold circuit register	ADSHCR	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 9070h	S12AD	A/D sampling state register T	ADSSTRT	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 9071h	S12AD	A/D sampling state register O	ADSSTRO	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 9073h	S12AD	A/D sampling state register 1	ADSSTR1	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 9074h	S12AD	A/D sampling state register 2	ADSSTR2	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 9075h	S12AD	A/D sampling state register 3	ADSSTR3	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 9076h	S12AD	A/D sampling state register 4	ADSSTR4	8	8	2, 3 PCLKB	2 ICLK
○	○	—	0008 9077h	S12AD	A/D sampling state register 5	ADSSTR5	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 9078h	S12AD	A/D sampling state register 6	ADSSTR6	8	8	2, 3 PCLKB	2 ICLK
○	○	—	0008 9079h	S12AD	A/D sampling state register 7	ADSSTR7	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 907Ah	S12AD	A/D disconnecting detection control register	ADDISCR	8	8	2, 3 PCLKB	2 ICLK
○	○	—	0008 A000h	SCI0	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
○	○	—	0008 A001h	SCI0	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
○	○	—	0008 A002h	SCI0	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
○	○	—	0008 A003h	SCI0	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
○	○	—	0008 A004h	SCI0	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
○	○	—	0008 A005h	SCI0	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
○	○	—	0008 A006h	SCI0	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
○	○	—	0008 A007h	SCI0	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
○	○	—	0008 A008h	SCI0	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
○	○	—	0008 A009h	SCI0	I^2C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
○	○	—	0008 A00Ah	SCI0	I^2C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
○	○	—	0008 A00Bh	SCI0	I^2C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
○	○	—	0008 A00Ch	SCI0	I^2C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
○	○	—	0008 A00Dh	SCI0	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A020h	SCI1	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A021h	SCI1	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A022h	SCI1	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A023h	SCI1	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A024h	SCI1	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A025h	SCI1	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A026h	SCI1	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A027h	SCI1	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A028h	SCI1	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A029h	SCI1	I^2C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A02Ah	SCI1	I^2C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A02Bh	SCI1	I^2C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A02Ch	SCI1	I^2C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A02Dh	SCI1	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A0A0h	SCI5	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A0A1h	SCI5	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A0A2h	SCI5	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A0A3h	SCI5	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (15 / 22)

100-pin	80-pin	64-pin	Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States	
									ICLK ≥ PCLK	ICLK < PCLK
○	○	○	0008 A0A4h	SCI5	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A0A5h	SCI5	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A0A6h	SCI5	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A0A7h	SCI5	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A0A8h	SCI5	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A0A9h	SCI5	I^2C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A0AAh	SCI5	I^2C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A0ABh	SCI5	I^2C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A0ACh	SCI5	I^2C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A0ADh	SCI5	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A0C0h	SCI6	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A0C1h	SCI6	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A0C2h	SCI6	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A0C3h	SCI6	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A0C4h	SCI6	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A0C5h	SCI6	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A0C6h	SCI6	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A0C7h	SCI6	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A0C8h	SCI6	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A0C9h	SCI6	I^2C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A0CAh	SCI6	I^2C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A0CBh	SCI6	I^2C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A0CCh	SCI6	I^2C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A0CDh	SCI6	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A100h	SCI8	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A101h	SCI8	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A102h	SCI8	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A103h	SCI8	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A104h	SCI8	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A105h	SCI8	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A106h	SCI8	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A107h	SCI8	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A108h	SCI8	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A109h	SCI8	I^2C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A10Ah	SCI8	I^2C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A10Bh	SCI8	I^2C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A10Ch	SCI8	I^2C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A10Dh	SCI8	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A120h	SCI9	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A121h	SCI9	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A122h	SCI9	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A123h	SCI9	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A124h	SCI9	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A125h	SCI9	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A126h	SCI9	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A127h	SCI9	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A128h	SCI9	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A129h	SCI9	I^2C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A12Ah	SCI9	I^2C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A12Bh	SCI9	I^2C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A12Ch	SCI9	I^2C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 A12Dh	SCI9	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (16 / 22)

100-pin	80-pin	64-pin	Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States	
									ICLK ≥ PCLK	ICLK < PCLK
○	○	○	0008 B000h	CAC	CAC control register 0	CACR0	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B001h	CAC	CAC control register 1	CACR1	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B002h	CAC	CAC control register 2	CACR2	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B003h	CAC	CAC interrupt control register	CAICR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B004h	CAC	CAC status register	CASTR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B006h	CAC	CAC upper-limit value setting register	CAULVR	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 B008h	CAC	CAC lower-limit value setting register	CALLVR	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 B00Ah	CAC	CAC counter buffer register	CACNTBR	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 B080h	DOC	DOC control register	DOCR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B082h	DOC	DOC data input register	DODIR	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 B084h	DOC	DOC data setting register	DODSR	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 B100h	ELC	Event link control register	ELCR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B102h	ELC	Event link setting register 1	ELSR1	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B103h	ELC	Event link setting register 2	ELSR2	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B104h	ELC	Event link setting register 3	ELSR3	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B105h	ELC	Event link setting register 4	ELSR4	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B108h	ELC	Event link setting register 7	ELSR7	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B10Bh	ELC	Event link setting register 10	ELSR10	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B10Dh	ELC	Event link setting register 12	ELSR12	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B110h	ELC	Event link setting register 15	ELSR15	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B111h	ELC	Event link setting register 16	ELSR16	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B113h	ELC	Event link setting register 18	ELSR18	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B114h	ELC	Event link setting register 19	ELSR19	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B115h	ELC	Event link setting register 20	ELSR20	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B116h	ELC	Event link setting register 21	ELSR21	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B117h	ELC	Event link setting register 22	ELSR22	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B118h	ELC	Event link setting register 23	ELSR23	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B119h	ELC	Event link setting register 24	ELSR24	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B11Ah	ELC	Event link setting register 25	ELSR25	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B11Bh	ELC	Event link setting register 26	ELSR26	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B11Ch	ELC	Event link setting register 27	ELSR27	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B11Dh	ELC	Event link setting register 28	ELSR28	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B11Eh	ELC	Event link setting register 29	ELSR29	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B11Fh	ELC	Event link option setting register A	ELOPA	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B120h	ELC	Event link option setting register B	ELOPB	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B121h	ELC	Event link option setting register C	ELOPC	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B122h	ELC	Event link option setting register D	ELOPD	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B123h	ELC	Port group setting register 1	PGR1	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B124h	ELC	Port group setting register 2	PGR2	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B125h	ELC	Port group control register 1	PGC1	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B126h	ELC	Port group control register 2	PGC2	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B127h	ELC	Port buffer register 1	PDBF1	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B128h	ELC	Port buffer register 2	PDBF2	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B129h	ELC	Event link port setting register 0	PEL0	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B12Ah	ELC	Event link port setting register 1	PEL1	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B12Bh	ELC	Event link port setting register 2	PEL2	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B12Ch	ELC	Event link port setting register 3	PEL3	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B12Dh	ELC	Event link software event generation register	ELSEGR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B300h	SCI12	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B301h	SCI12	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B302h	SCI12	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B303h	SCI12	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (17 / 22)

100-pin	80-pin	64-pin	Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States	
									ICLK ≥ PCLK	ICLK < PCLK
○	○	○	0008 B304h	SCI12	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B305h	SCI12	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B306h	SCI12	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B307h	SCI12	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B308h	SCI12	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B309h	SCI12	I^2C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B30Ah	SCI12	I^2C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B30Bh	SCI12	I^2C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B30Ch	SCI12	I^2C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B30Dh	SCI12	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B320h	SCI12	Extended serial mode enable register	ESMER	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B321h	SCI12	Control register 0	CR0	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B322h	SCI12	Control register 1	CR1	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B323h	SCI12	Control register 2	CR2	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B324h	SCI12	Control register 3	CR3	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B325h	SCI12	Port control register	PCR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B326h	SCI12	Interrupt control register	ICR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B327h	SCI12	status register	STR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B328h	SCI12	Status clear register	STCR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B329h	SCI12	Control Field 0 data register	CF0DR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B32Ah	SCI12	Control Field 0 compare enable register	CF0CR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B32Bh	SCI12	Control Field 0 receive data register	CF0RR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B32Ch	SCI12	Primary control field 1 data register	PCF1DR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B32Dh	SCI12	Secondary control field 1 data register	SCF1DR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B32Eh	SCI12	Control field 1 compare enable register	CF1CR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B32Fh	SCI12	Control field 1 receive data register	CF1RR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B330h	SCI12	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B331h	SCI12	Timer mode register	TMR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B332h	SCI12	Timer prescaler register	TPRE	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 B333h	SCI12	Timer count register	TCNT	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C000h	PORT0	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C001h	PORT1	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C002h	PORT2	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C003h	PORT3	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C004h	PORT4	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C005h	PORT5	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C00Ah	PORTA	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C00Bh	PORTB	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C00Ch	PORTC	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK
○	○	—	0008 C00Dh	PORTD	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C00Eh	PORTE	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C011h	PORTH	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK
○	○	—	0008 C012h	PORTJ	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C020h	PORT0	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C021h	PORT1	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C022h	PORT2	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C023h	PORT3	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C024h	PORT4	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C025h	PORT5	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C02Ah	PORTA	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C02Bh	PORTB	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C02Ch	PORTC	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (18 / 22)

100-pin	80-pin	64-pin	Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States	
									ICLK ≥ PCLK	ICLK < PCLK
○	○	—	0008 C02Dh	PORTD	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C02Eh	PORTE	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C031h	PORTH	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK
○	○	—	0008 C032h	PORTJ	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C040h	PORT0	Port input register	PIDR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C041h	PORT1	Port input register	PIDR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C042h	PORT2	Port input register	PIDR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C043h	PORT3	Port input register	PIDR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C044h	PORT4	Port input register	PIDR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C045h	PORT5	Port input register	PIDR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C04Ah	PORTA	Port input register	PIDR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C04Bh	PORTB	Port input register	PIDR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C04Ch	PORTC	Port input register	PIDR	8	8	2, 3 PCLKB	2 ICLK
○	○	—	0008 C04Dh	PORTD	Port input register	PIDR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C04Eh	PORTE	Port input register	PIDR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C051h	PORTH	Port input register	PIDR	8	8	2, 3 PCLKB	2 ICLK
○	○	—	0008 C052h	PORTJ	Port input register	PIDR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C060h	PORT0	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C061h	PORT1	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C062h	PORT2	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C063h	PORT3	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C064h	PORT4	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C065h	PORT5	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C06Ah	PORTA	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C06Bh	PORTB	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C06Ch	PORTC	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
○	○	—	0008 C06Dh	PORTD	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C06Eh	PORTE	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C071h	PORTH	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
○	○	—	0008 C072h	PORTJ	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C082h	PORT1	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK
○	○	○	0008 C083h	PORT1	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK
○	○	○	0008 C084h	PORT2	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK
○	○	○	0008 C085h	PORT2	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK
○	○	○	0008 C086h	PORT3	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK
○	○	○	0008 C087h	PORT3	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK
○	○	○	0008 C094h	PORTA	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK
○	○	○	0008 C095h	PORTA	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK
○	○	○	0008 C096h	PORTB	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK
○	○	○	0008 C097h	PORTB	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK
○	○	○	0008 C098h	PORTC	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK
○	○	○	0008 C099h	PORTC	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK
○	○	○	0008 C09Ch	PORTE	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK
○	○	○	0008 C09Dh	PORTE	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK
○	○	○	0008 C0C0h	PORT0	Pull-up resistor control register	PCR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C0C1h	PORT1	Pull-up resistor control register	PCR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C0C2h	PORT2	Pull-up resistor control register	PCR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C0C3h	PORT3	Pull-up resistor control register	PCR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C0C4h	PORT4	Pull-up resistor control register	PCR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C0C5h	PORT5	Pull-up resistor control register	PCR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C0CAh	PORTA	Pull-up resistor control register	PCR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C0CBh	PORTB	Pull-up resistor control register	PCR	8	8	2, 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (19 / 22)

100-pin	80-pin	64-pin	Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States	
									ICLK ≥ PCLK	ICLK < PCLK
○	○	○	0008 C0CCh	PORTC	Pull-up resistor control register	PCR	8	8	2, 3 PCLKB	2 ICLK
○	○	—	0008 C0CDh	PORTD	Pull-up resistor control register	PCR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C0CEh	PORTE	Pull-up resistor control register	PCR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C0D1h	PORTH	Pull-up resistor control register	PCR	8	8	2, 3 PCLKB	2 ICLK
○	○	—	0008 C0D2h	PORTJ	Pull-up resistor control register	PCR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C0E1h	PORT1	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C0E2h	PORT2	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C0E3h	PORT3	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C0E5h	PORT5	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C0EAh	PORTA	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C0EBh	PORTB	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C0ECh	PORTC	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
○	○	—	0008 C0EDh	PORTD	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C0EEh	PORTE	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C0F1h	PORTH	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
○	○	—	0008 C0F2h	PORTJ	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
○	—	—	0008 C100h	MPC	CS output enable register	PFCSE	8	8	2, 3 PCLKB	2 ICLK
○	—	—	0008 C104h	MPC	Address output enable register 0	PFAOE0	8	8, 16	2, 3 PCLKB	2 ICLK
○	—	—	0008 C105h	MPC	Address output enable register 1	PFAOE1	8	8, 16	2, 3 PCLKB	2 ICLK
○	—	—	0008 C106h	MPC	External bus control register 0	PFBCR0	8	8, 16	2, 3 PCLKB	2 ICLK
○	—	—	0008 C107h	MPC	External bus control register 1	PFBCR1	8	8, 16	2, 3 PCLKB	2 ICLK
○	—	—	0008 C11Fh	MPC	Write-protect register	PWPR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C143h	MPC	Port 03 pin control select register	P03PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C145h	MPC	Port 05 pin control select register	P05PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	—	0008 C147h	MPC	Port 07 pin control select register	P07PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	—	0008 C14Ah	MPC	Port 12 pin control select register	P12PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	—	0008 C14Bh	MPC	Port 13 pin control select register	P13PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C14Ch	MPC	Port 14 pin control select register	P14PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C14Dh	MPC	Port 15 pin control select register	P15PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C14Eh	MPC	Port 16 pin control select register	P16PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C14Fh	MPC	Port 17 pin control select register	P17PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	—	0008 C150h	MPC	Port 20 pin control select register	P20PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	—	0008 C151h	MPC	Port 21 pin control select register	P21PFS	8	8	2, 3 PCLKB	2 ICLK
○	—	—	0008 C152h	MPC	Port 22 pin control select register	P22PFS	8	8	2, 3 PCLKB	2 ICLK
○	—	—	0008 C153h	MPC	Port 23 pin control select register	P23PFS	8	8	2, 3 PCLKB	2 ICLK
○	—	—	0008 C154h	MPC	Port 24 pin control select register	P24PFS	8	8	2, 3 PCLKB	2 ICLK
○	—	—	0008 C155h	MPC	Port 25 pin control select register	P25PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C156h	MPC	Port 26 pin control select register	P26PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C157h	MPC	Port 27 pin control select register	P27PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C158h	MPC	Port 30 pin control select register	P30PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C159h	MPC	Port 31 pin control select register	P31PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C15Ah	MPC	Port 32 pin control select register	P32PFS	8	8	2, 3 PCLKB	2 ICLK
○	—	—	0008 C15Bh	MPC	Port 33 pin control select register	P33PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	—	0008 C15Ch	MPC	Port 34 pin control select register	P34PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C160h	MPC	Port 40 pin control select register	P40PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C161h	MPC	Port 41 pin control select register	P41PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C162h	MPC	Port 42 pin control select register	P42PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C163h	MPC	Port 43 pin control select register	P43PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C164h	MPC	Port 44 pin control select register	P44PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	—	0008 C165h	MPC	Port 45 pin control select register	P45PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C166h	MPC	Port 46 pin control select register	P46PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	—	0008 C167h	MPC	Port 47 pin control select register	P47PFS	8	8	2, 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (20 / 22)

100-pin	80-pin	64-pin	Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States	
									ICLK ≥ PCLK	ICLK < PCLK
○	○	○	0008 C16Ch	MPC	Port 54 pin control select register	P54PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C16Dh	MPC	Port 55 pin control select register	P55PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C190h	MPC	Port A0 pin control select register	PA0PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C191h	MPC	Port A1 pin control select register	PA1PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	—	0008 C192h	MPC	Port A2 pin control select register	PA2PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C193h	MPC	Port A3 pin control select register	PA3PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C194h	MPC	Port A4 pin control select register	PA4PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	—	0008 C195h	MPC	Port A5 pin control select register	PA5PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C196h	MPC	Port A6 pin control select register	PA6PFS	8	8	2, 3 PCLKB	2 ICLK
○	—	—	0008 C197h	MPC	Port A7 pin control select register	PA7PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C198h	MPC	Port B0 pin control select register	PB0PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C199h	MPC	Port B1 pin control select register	PB1PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	—	0008 C19Ah	MPC	Port B2 pin control select register	PB2PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C19Bh	MPC	Port B3 pin control select register	PB3PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	—	0008 C19Ch	MPC	Port B4 pin control select register	PB4PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C19Dh	MPC	Port B5 pin control select register	PB5PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C19Eh	MPC	Port B6 pin control select register	PB6PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C19Fh	MPC	Port B7 pin control select register	PB7PFS	8	8	2, 3 PCLKB	2 ICLK
○	—	—	0008 C1A0h	MPC	Port C0 pin control select register	PC0PFS	8	8	2, 3 PCLKB	2 ICLK
○	—	—	0008 C1A1h	MPC	Port C1 pin control select register	PC1PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C1A2h	MPC	Port C2 pin control select register	PC2PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C1A3h	MPC	Port C3 pin control select register	PC3PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C1A4h	MPC	Port C4 pin control select register	PC4PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C1A5h	MPC	Port C5 pin control select register	PC5PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C1A6h	MPC	Port C6 pin control select register	PC6PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C1A7h	MPC	Port C7 pin control select register	PC7PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	—	0008 C1A8h	MPC	Port D0 pin control select register	PD0PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	—	0008 C1A9h	MPC	Port D1 pin control select register	PD1PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	—	0008 C1AAh	MPC	Port D2 pin control select register	PD2PFS	8	8	2, 3 PCLKB	2 ICLK
○	—	—	0008 C1ABh	MPC	Port D3 pin control select register	PD3PFS	8	8	2, 3 PCLKB	2 ICLK
○	—	—	0008 C1ACh	MPC	Port D4 pin control select register	PD4PFS	8	8	2, 3 PCLKB	2 ICLK
○	—	—	0008 C1ADh	MPC	Port D5 pin control select register	PD5PFS	8	8	2, 3 PCLKB	2 ICLK
○	—	—	0008 C1AEh	MPC	Port D6 pin control select register	PD6PFS	8	8	2, 3 PCLKB	2 ICLK
○	—	—	0008 C1AFh	MPC	Port D7 pin control select register	PD7PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C1B0h	MPC	Port E0 pin control select register	PE0PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C1B1h	MPC	Port E1 pin control select register	PE1PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C1B2h	MPC	Port E2 pin control select register	PE2PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C1B3h	MPC	Port E3 pin control select register	PE3PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C1B4h	MPC	Port E4 pin control select register	PE4PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C1B5h	MPC	Port E5 pin control select register	PE5PFS	8	8	2, 3 PCLKB	2 ICLK
○	—	—	0008 C1B6h	MPC	Port E6 pin control select register	PE6PFS	8	8	2, 3 PCLKB	2 ICLK
○	—	—	0008 C1B7h	MPC	Port E7 pin control select register	PE7PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C1C8h	MPC	Port H0 pin control select register	PH0PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C1C9h	MPC	Port H1 pin control select register	PH1PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C1CAh	MPC	Port H2 pin control select register	PH2PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C1CBh	MPC	Port H3 pin control select register	PH3PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	—	0008 C1D1h	MPC	Port J1 pin control select register	PJ1PFS	8	8	2, 3 PCLKB	2 ICLK
○	—	—	0008 C1D3h	MPC	Port J3 pin control select register	PJ3PFS	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C280h	SYSTEM	Deep standby control register	DPSBYCR	8	8	4, 5 PCLKB	2, 3 ICLK
○	○	○	0008 C282h	SYSTEM	Deep standby interrupt enable register 0	DPSIER0	8	8	4, 5 PCLKB	2, 3 ICLK
○	○	○	0008 C284h	SYSTEM	Deep standby interrupt enable register 2	DPSIER2	8	8	4, 5 PCLKB	2, 3 ICLK
○	○	○	0008 C286h	SYSTEM	Deep standby interrupt flag register 0	DPSIFR0	8	8	4, 5 PCLKB	2, 3 ICLK

Table 4.1 List of I/O Registers (Address Order) (21 / 22)

100-pin	80-pin	64-pin	Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States	
									ICLK ≥ PCLK	ICLK < PCLK
○	○	○	0008 C288h	SYSTEM	Deep standby interrupt flag register 2	DPSIFR2	8	8	4, 5 PCLKB	2, 3 ICLK
○	○	○	0008 C28Ah	SYSTEM	Deep standby interrupt edge register 0	DPSIEGR0	8	8	4, 5 PCLKB	2, 3 ICLK
○	○	○	0008 C28Ch	SYSTEM	Deep standby interrupt edge register 2	DPSIEGR2	8	8	4, 5 PCLKB	2, 3 ICLK
○	○	○	0008 C28Fh	SYSTEM	Flash HOCO software standy control register	FHSSBYCR	8	8	4, 5 PCLKB	2, 3 ICLK
○	○	○	0008 C290h	SYSTEM	Reset status register 0	RSTSR0	8	8	4, 5 PCLKB	2, 3 ICLK
○	○	○	0008 C291h	SYSTEM	Reset status register 1	RSTSR1	8	8	4, 5 PCLKB	2, 3 ICLK
○	○	○	0008 C293h	SYSTEM	Main clock oscillator forced oscillation control register	MOFCR	8	8	4, 5 PCLKB	2, 3 ICLK
○	○	○	0008 C294h	SYSTEM	High-speed clock oscillator power supply control register	HOCOPCR	8	8	4, 5 PCLKB	2, 3 ICLK
○	○	○	0008 C296h	FLASH	Flash write erase protection register	FWEPROR	8	8	4, 5 PCLKB	2, 3 ICLK
○	○	○	0008 C297h	SYSTEM	Voltage monitoring circuit/comparator A control register	LVCMPCR	8	8	4, 5 PCLKB	2, 3 ICLK
○	○	○	0008 C298h	SYSTEM	Voltage detection level select register	LVDLVLR	8	8	4, 5 PCLKB	2, 3 ICLK
○	○	○	0008 C29Ah	SYSTEM	Voltage monitoring 1 circuit/comparator A1 control register 0	LVD1CR0	8	8	4, 5 PCLKB	2, 3 ICLK
○	○	○	0008 C29Bh	SYSTEM	Voltage monitoring 2 circuit/comparator A2 control register 0	LVD2CR0	8	8	4, 5 PCLKB	2, 3 ICLK
○	○	○	0008 C2A0h to 0008 C2BFh	SYSTEM	Deep standby backup register 0 to 31	DPSBKR0 to DPSBKR31	8	8	4, 5 PCLKB	2, 3 ICLK
○	○	○	0008 C400h	RTC	64-Hz counter	R64CNT	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C402h	RTC	Second counter	RSECCNT	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C404h	RTC	Minute counter	RMINCNT	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C406h	RTC	Hour counter	RHRCNT	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C408h	RTC	Day-of-week counter	RWKCNT	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C40Ah	RTC	Date counter	RDAYCNT	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C40Ch	RTC	Month counter	RMONCNT	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C40Eh	RTC	Year counter	RYRCNT	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 C410h	RTC	Second alarm register	RSECAR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C412h	RTC	Minute alarm register	RMINAR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C414h	RTC	Hour alarm register	RHRAR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C416h	RTC	Day-of-week alarm register	RWKAR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C418h	RTC	Date alarm register	RDAYAR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C41Ah	RTC	Month alarm register	RMONAR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C41Ch	RTC	Year alarm register	RYRAR	16	16	2, 3 PCLKB	2 ICLK
○	○	○	0008 C41Eh	RTC	Year alarm enable register	RYRAREN	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C422h	RTC	RTC control register 1	RCR1	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C424h	RTC	RTC control register 2	RCR2	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C426h	RTC	RTC control register 3	RCR3	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C42Eh	RTC	Time error adjustment register	RADJ	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C440h	RTC	Time capture control register 0	RTCCR0	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C442h	RTC	Time capture control register 1	RTCCR1	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C444h	RTC	Time capture control register 2	RTCCR2	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C452h	RTC	Second capture register 0	RSECCP0	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C454h	RTC	Minute capture register 0	RMINCP0	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C456h	RTC	Hour capture register 0	RHRCP0	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C45Ah	RTC	Date capture register 0	RDAYCP0	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C45Ch	RTC	Month capture register 0	RMONCP0	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C462h	RTC	Second capture register 1	RSECCP1	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C464h	RTC	Minute capture register 1	RMINCP1	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C466h	RTC	Hour capture register 1	RHRCP1	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C46Ah	RTC	Date capture register 1	RDAYCP1	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C46Ch	RTC	Month capture register 1	RMONCP1	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C472h	RTC	Second capture register 2	RSECCP2	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C474h	RTC	Minute capture register 2	RMINCP2	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C476h	RTC	Hour capture register 2	RHRCP2	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C47Ah	RTC	Date capture register 2	RDAYCP2	8	8	2, 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (22 / 22)

100-pin	80-pin	64-pin	Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States	
									ICLK ≥ PCLK	ICLK < PCLK
○	○	○	0008 C47Ch	RTC	Month capture register 2	RMONCP2	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C500h	TEMPS	Temperature sensor control register	TSCR	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C580h	CMPB	Comparator B control register 1	CPBCNT1	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C582h	CMPB	Comparator B flag register	CPBFLG	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C583h	CMPB	Comparator B interrupt control register	CPBINT	8	8	2, 3 PCLKB	2 ICLK
○	○	○	0008 C584h	CMPB	Comparator B filter select register	CPBF	8	8	2, 3 PCLKB	2 ICLK
○	○	○	007F C402h	FLASH	Flash mode register	FMODR	8	8	2, 3 FCLK	2 ICLK
○	○	○	007F C410h	FLASH	Flash access status register	FASTAT	8	8	2, 3 FCLK	2 ICLK
○	○	○	007F C411h	FLASH	Flash access error interrupt enable register	FAEINT	8	8	2, 3 FCLK	2 ICLK
○	○	○	007F C412h	FLASH	Flash ready interrupt enable register	FRDYIE	8	8	2, 3 FCLK	2 ICLK
○	○	○	007F C440h	FLASH	E2 data flash read enable register 0	DFLRE0	16	16	2, 3 FCLK	2 ICLK
○	○	○	007F C450h	FLASH	E2 data flash programming/erasure enable register 0	DFLWE0	16	16	2, 3 FCLK	2 ICLK
○	○	○	007F C454h	FLASH	FCU RAM enable register	FCURAME	16	16	2, 3 FCLK	2 ICLK
○	○	○	007F FFB0h	FLASH	Flash status register 0	FSTATR0	8	8	2, 3 FCLK	2 ICLK
○	○	○	007F FFB1h	FLASH	Flash status register 1	FSTATR1	8	8	2, 3 FCLK	2 ICLK
○	○	○	007F FFB2h	FLASH	Flash P/E mode entry register	FENTRYR	16	16	2, 3 FCLK	2 ICLK
○	○	○	007F FFB4h	FLASH	Flash protection register	FPROTR	16	16	2, 3 FCLK	2 ICLK
○	○	○	007F FFB6h	FLASH	Flash reset register	FRESETR	16	16	2, 3 FCLK	2 ICLK
○	○	○	007F FFBAh	FLASH	FCU command register	FCMDR	16	16	2, 3 FCLK	2 ICLK
○	○	○	007F FFC8h	FLASH	FCU processing switching register	FCPSR	16	16	2, 3 FCLK	2 ICLK
○	○	○	007F FFCAh	FLASH	E2 data flash blank check control register	DFLBCCNT	16	16	2, 3 FCLK	2 ICLK
○	○	○	007F FFCCh	FLASH	Flash P/E status register	FPESTAT	16	16	2, 3 FCLK	2 ICLK
○	○	○	007F FFCEh	FLASH	E2 data flash blank check status register	DFLBCSTAT	16	16	2, 3 FCLK	2 ICLK
○	○	○	007F FFE8h	FLASH	Peripheral clock notification register	PCKAR	16	16	2, 3 FCLK	2 ICLK

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

Conditions: VSS = AVSS0 = VREFL = VREFL0 = 0V

Item	Symbol	Value	Unit
Power supply voltage	VCC	–0.3 to +6.5	V
Input voltage (except for ports for 5 V tolerant*1)	V_{in}	–0.3 to VCC + 0.3	V
Input voltage (ports for 5 V tolerant*1)	V_{in}	–0.3 to +6.5	V
Reference power supply voltage	VREFH, VREFH0	–0.3 to VCC + 0.3	V
Analog power supply voltage	AVCC0*2	–0.3 to +6.5	V
Analog input voltage	V_{AN}	–0.3 to VCC + 0.3	V
Operating temperature	T_{opr}	–40 to +85	°C
Storage temperature	T_{stg}	–55 to +125	°C

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Note 1. Ports12, 13, 16 and 17 are 5 V tolerant.

Note 2. Connect AVCC0 to VCC. When neither the A/D converter nor the D/A converter is in use, do not leave the AVCC0, REFH/VREFH0, AVSS0, and VREFL/VREFL0 pins open. Connect the AVCC0 and VREFH/VREFH0 pins to VCC, and the AVSS0 and VREFL/VREFL0 pins to VSS, respectively.

5.2 DC Characteristics

Table 5.2 DC Characteristics (1)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH = VREFH0 = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0V
T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	IRQ input pin*1 MTU input pin*1 TMR input pin*1 SCI input pin*1 ADTRG0# input pin*1 RES#, NMI	V_{IH}	VCC × 0.8	—	VCC + 0.3	V	
		V_{IL}	–0.3	—	VCC × 0.2		
		ΔV_T	VCC × 0.1	—	—		
	RIIC input pin (except for SMBus)	V_{IH}	VCC × 0.7	—	5.8		
		V_{IL}	–0.3	—	VCC × 0.3		
		ΔV_T	VCC × 0.05	—	—		
	Ports for 5 V tolerant*2	V_{IH}	VCC × 0.8	—	5.8		
		V_{IL}	–0.3	—	VCC × 0.2		
	Other input pins excluding ports for 5 V tolerant	V_{IH}	VCC × 0.8	—	VCC + 0.3		
		V_{IL}	–0.3	—	VCC × 0.2		
Input high voltage (except for Schmitt trigger input pin)	MD pin	V_{IH}	VCC × 0.9	—	VCC + 0.3	V	
	EXTAL, RSPI, WAIT#, TCK		VCC × 0.8	—	VCC + 0.3		
	XCIN		VCC × 0.8	—	VCC + 0.3		
	D0 to D15		VCC × 0.7	—	VCC + 0.3		
	RIIC (SMBus)		2.1	—	VCC + 0.3		
Input low voltage (except for Schmitt trigger input pin)	MD pin, EMLE	V_{IL}	–0.3	—	VCC × 0.1	V	
	EXTAL, RSPI, WAIT#, TCK		–0.3	—	VCC × 0.2		
	XCIN		–0.3	—	VCC × 0.2		
	D0 to D15		–0.3	—	VCC × 0.3		
	RIIC (SMBus)		–0.3	—	0.8		

Note 1. This does not include the pins which are multiplexed as ports for 5 V tolerant.
Note 2. Pins 12, 13, 16 and 17 are for 5 V tolerant.

Table 5.3 DC Characteristics (2)

Conditions: VCC = AVCC0 = 1.62 to 2.7 V, VREFH = VREFH0 = 1.62 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V
T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	IRQ input pin*1 MTU input pin*1 TMR input pin*1 SCI input pin*1 ADTRG0# input pin*1 RES#, NMI	V_{IH}	VCC × 0.8	—	VCC + 0.3	V	
		V_{IL}	–0.3	—	VCC × 0.2		
	Ports for 5 V tolerant*2	V_{IH}	VCC × 0.8	—	5.8		
		V_{IL}	–0.3	—	VCC × 0.2		
	Other input pins excluding ports for 5 V tolerant	V_{IH}	VCC × 0.8	—	VCC + 0.3		
		V_{IL}	–0.3	—	VCC × 0.2		
Input high voltage (except for Schmitt trigger input pin)	MD pin	V_{IH}	VCC × 0.9	—	VCC + 0.3	V	
	EXTAL, RSPI, WAIT#, TCK		VCC × 0.8	—	VCC + 0.3		
	XCIN		VCC × 0.8	—	VCC + 0.3		
	D0 to D15		VCC × 0.7	—	VCC + 0.3		
Input low voltage (except for Schmitt trigger input pin)	MD pin	V_{IL}	–0.3	—	VCC × 0.1	V	
	EXTAL, RSPI, WAIT#, TCK		–0.3	—	VCC × 0.2		
	XCIN		–0.3	—	VCC × 0.2		
	D0 to D15		–0.3	—	VCC × 0.3		

Note 1. This does not include the pins which are multiplexed as ports for 5 V tolerant.
Note 2. Pins 12, 13, 16 and 17 are for 5 V tolerant.

Table 5.4 DC Characteristics (3)

Conditions: VCC = AVCC0 = 1.62 to 2.7 V, VREFH = VREFH0 = 1.62 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V
T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input leakage current	RES#, MD pin, NMI	$\lvert I_{in} \rvert$	—	—	1.0	µA	V_{in} = 0 V, V_{in} = VCC
Three - state leakage current (off-state)	Other than ports for 5 V tolerant	$\lvert I_{TSI} \rvert$	—	—	0.2	µA	V_{in} = 0 V, V_{in} = VCC
	Ports for 5 V tolerant		—	—	T.B.D		V_{in} = 0 V, 5.8V
Input capacitance	All input pins (except for ports 12, 13, 16, 17, port 4, and port E)	C_{in}	—	—	15	pF	V_{in} = 0 V, f = 1 MHz, T_a = 25°C
	Ports 12, 13, 16, 17, port 4, and port E		—	—	T.B.D		

Table 5.5 DC Characteristics (4)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VREFH = VREFH0 = 1.62 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V
T_a = –40 to +85°C

Item		Symbol	VCC.			Unit	Test Conditions
			1.62 to 2.7 V	2.7 to 4.0 V	4.0 to 5.5 V		
Input pull-up MOS current	All ports (except for port 35)	$-I_p$	5 to 150	10 to 200	50 to 400	µA	V_{in} = 0 V

Table 5.6 DC Characteristics (5)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +85°C

Item				Symbol	Typ.*6	Max.	Unit	Test Conditions
Current drawn*1	High-speed operating mode	Max. operation*2		I_{CC}	—	T.B.D	mA	ICLK = 50 MHz PCLKB = 25 MHz FCLK = 25 MHz BCLK = 25 MHz
		Normal operation*3			T.B.D	—		
	Medium-speed operating modes A and B	Max. operation*2			—	T.B.D		ICLK = 32 MHz PCLKB = 32 MHz FCLK = 32 MHz BCLK = 16 MHz
		Normal operation*3			T.B.D	—		
		Sleep mode			T.B.D	T.B.D		
		All module clock stop mode*4			T.B.D	T.B.D		
		Increase during BGO*5	Medium-speed operating mode A		T.B.D	—		
			Medium-speed operating mode B		T.B.D	—		
	Low-speed operating mode 1	Max. operation*2			—	T.B.D		ICLK = 1 MHz
		Normal operation*3			T.B.D	—		
	Low-speed operating mode 2	Max. operation*2			—	T.B.D		ICLK = 32 kHz
		Normal operation*3			T.B.D	—		
	Sotware standby	RTC stop			T.B.D	T.B.D	µA	
		RTC operation			T.B.D	T.B.D		
	Deep software standby	RTC stop			T.B.D	T.B.D		
		RTC operation			T.B.D	T.B.D		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.
Note 3. Measured with clocks not supplied to the peripheral functions. This does not include the BGO operation.
Note 4. The values are for reference.
Note 5. This is the increase in current drawn if data are written to or erased from the ROM or the flash memory for data storage during program execution.
Note 6. This is the value when VCC = 3.3 V

Table 5.7 DC Characteristics (6)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Analog power supply current*1	During A/D conversion	AI_{CC}	—	T.B.D	T.B.D	mA	
	During D/A conversion (per channel)		—	T.B.D	T.B.D		
	Temperature sensor		—	T.B.D	T.B.D	µA	
	Waiting for A/D, D/A conversion (all units)		—	T.B.D	T.B.D		
	A/D, D/A converter in standby mode (all units)		—	T.B.D	T.B.D		
Reference power supply current	During A/D conversion	I_{REFH}, I_{REFH0}	—	T.B.D	T.B.D	mA	
	During D/A conversion (per channel)		—	T.B.D	T.B.D		
	Waiting for A/D, D/A conversion (all units)		—	T.B.D	T.B.D	µA	
	A/D, D/A converter in standby mode (all units)		—	T.B.D	T.B.D		

Note 1. The reference power supply current is included in the power supply current value for D/A conversion.

Table 5.8 DC Characteristics (7)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VREFH = VREFH0 = 1.62 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V
T_a = –40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit
VCC rising gradient	SrVCC	0.02	—	20	ms/V
VCC falling gradient	SfVCC	0.02	—	20	ms/V

Table 5.9 Permissible Output Currents

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VREFH = VREFH0 = 1.62 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V
T_a = –40 to +85°C

Item			Symbol	Max.	Unit
Permissible output low current (average value per pin)	All output pins	When the driving ability is low	I_{OL}	4.0	mA
		When the driving ability is high		8.0	
Permissible output low current (max. value per pin)	All output pins	When the driving ability is low		4.0	mA
		When the driving ability is high		8.0	
Permissible output low current (total)	Total of all output pins		ΣI_{OL}	80	mA
Permissible output high current (average value per pin)	All output pins	When the driving ability is low	$-I_{OH}$	4.0	mA
		When the driving ability is high		8.0	
Permissible output high current (max. value per pin)	All output pins	When the driving ability is low		4.0	mA
		When the driving ability is high		8.0	
Permissible output high current (total)	Total of all output pins		$\Sigma -I_{OH}$	80	mA

Table 5.10 Output values of current and voltage

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VREFH = VREFH0 = 1.62 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V
T_a = –40 to +85°C

Item			Symbol	VCC.			Unit
				1.62 to 2.7 V	2.7 to 4.0 V	4.0 to 5.5 V	
Output low	All output pins (except for RIIC pins)	When the driving ability is low	I_{OL}/V_{OL}	0.5 mA/0.4 V	3.0 mA/1.0 V	4.0 mA/1.0 V	mA/V
		When the driving ability is high		1.0 mA/0.4 V	5.0 mA/1.0 V	8.0 mA/1.0 V	
	RIIC pins	Standard, Fm		—	3.0 mA/0.4 V	3.0 mA/0.4 V	
		Fm		—	6.0 mA/0.6 V	6.0 mA/0.6 V	
Output high	All output pins	When the driving ability is low	$-I_{OH}/V_{OH}$	0.5 mA/Vcc–0.4 V	3.0 mA/Vcc–1.0 V	4.0 mA/Vcc–1.0 V	mA/V
		When the driving ability is high		1.0 mA/Vcc–0.4 V	5.0 mA/Vcc–1.0 V	8.0 mA/Vcc–1.0 V	

5.3 AC Characteristics

Table 5.11 Operation Frequency Value (High-Speed Operating Mode)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH = VREFH0 = 1.62 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V
T_a = –40 to +85°C

Item		Symbol	VCC.	Unit
			2.7 to 4.0 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	50	MHz
	FlashIF clock (FCLK)*1		32	
	Peripheral module clock (PCLKB)		32	
	Peripheral module clock (PCLK)		50	
	External bus clock (BCLK)		25	
	BCLK pin output		12.5	

Note 1. The FCLK must be running at a frequency of at least 4 MHz during programming or erasing of the flash memory.

Table 5.12 Operation Frequency Value (Medium-Speed Operating Mode A)

Conditions: VCC = AVCC0 = 1.62 to 5.5V, VREFH = VREFH0 = 1.62 v to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V
T_a = –40 to +85°C

Item		Symbol	VCC.			Unit
			1.62 to 1.8 V	1.8 to 2.7 V	2.7 to 5.5 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	20	32	32	MHz
	FlashIF clock (FCLK)*1		20	32	32	
	Peripheral module clock (PCLKB)		20	32	32	
	Peripheral module clock (PCLK)		20	32	32	
	External bus clock (BCLK)		12	16	16	
	BCLK pin output		6	8	8	

Note 1. The VCC is 2.7 to 5.5 V and the FCLK must be running at a frequency of at least 4 MHz during programming or erasing of the flash memory.

Table 5.13 Operation Frequency Value (Medium-Speed Operating Mode B)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VREFH = VREFH0 = 1.62 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V
T_a = –40 to +85°C

Item		Symbol	VCC.			Unit
			1.62 to 1.8 V	1.8 to 2.7 V	2.7 to 5.5 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	20	32	32	MHz
	FlashIF clock (FCLK)*1		20	32	32	
	Peripheral module clock (PCLKB)		20	32	32	
	Peripheral module clock (PCLK)		20	32	32	
	External bus clock (BCLK)		12	16	16	
	BCLK pin output		6	8	8	

Note 1. The VCC is 1.62 to 3.6 V and the FCLK must be running at a frequency of at least 4 MHz during programming or erasing of the flash memory.

Table 5.14 Operation Frequency Value (Low-Speed Operating Mode 1)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VREFH = VREFH0 = 1.62 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V
T_a = –40 to +85°C

Item		Symbol	VCC.			Unit
			1.62 to 1.8 V	1.8 to 2.7 V	2.7 to 5.5 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	1	1	1	MHz
	FlashIF clock (FCLK)*1		1	1	1	
	Peripheral module clock (PCLKB)		1	1	1	
	Peripheral module clock (PCLK)		1	1	1	
	External bus clock (BCLK)		1	1	1	
	BCLK pin output		1	1	1	

Note 1. Programming and erasing the flash memory is impossible.

Table 5.15 Operation Frequency Value (Low-Speed Operating Mode 2)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VREFH = VREFH0 = 1.62 V to AVCC0, VSS = AVSS0 = VREFL=VREFL0 = 0V
T_a = –40 to +85°C

Item		Symbol	VCC.			Unit
			1.62 to 1.8 V	1.8 to 2.7 V	2.7 to 5.5 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	32	32	32	MHz
	FlashIF clock (FCLK)*1		32	32	32	
	Peripheral module clock (PCLKB)		32	32	32	
	Peripheral module clock (PCLK)*2		32	32	32	
	External bus clock (BCLK)		32	32	32	
	BCLK pin output		32	32	32	

Note 1. Programming and erasing the flash memory is impossible.
Note 2. Accuracy of A/D conversion is not guaranteed.

5.4 Clock Timing

Table 5.16 Clock Timing (1)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH = VREFH0 = 1.8 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V
BCLK = up to 25 MHz (BCLK output = up to 12.5 MHz), T_a = –40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BCLK pin output cycle time	t_{Bcyc}	80	—	—	ns	Figure 5.1
BCLK pin output high pulse width	t_{CH}	20	—	—	ns	
BCLK pin output low pulse width	t_{CL}	20	—	—	ns	
BCLK pin output rising time	t_{Cr}	—	—	15	ns	
BCLK pin output falling time	t_{Cr}	—	—	15	ns	

Table 5.17 Clock Timing (2)

Conditions: VCC = AVCC0 = 1.8 to 2.7 V, VREFH=VREFH0 = 1.8 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V
BCLK = up to 16 MHz (BCLK output = up to 8 MHz), T_a = –40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BCLK pin output cycle time	t_{Bcyc}	125	—	—	ns	Figure 5.1
BCLK pin output high pulse width	t_{CH}	30	—	—	ns	
BCLK pin output low pulse width	t_{CL}	30	—	—	ns	
BCLK pin output rising time	t_{Cr}	—	—	25	ns	
BCLK pin output falling time	t_{Cr}	—	—	25	ns	

Table 5.18 Clock Timing (3)

Conditions: VCC = AVCC0 = 1.62 to 1.8 V, VREFH = VREFH0 = 1.62 V to AVCC0, VSS = AVSS0 = VREFL=VREFL0 = 0 V
BCLK = up to 12 MHz (BCLK output = up to 6 MHz), T_a = –40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BCLK pin output cycle time	t_{Bcyc}	167	—	—	ns	Figure 5.1
BCLK pin output high pulse width	t_{CH}	42	—	—	ns	
BCLK pin output low pulse width	t_{CL}	42	—	—	ns	
BCLK pin output rising time	t_{Cr}	—	—	35	ns	
BCLK pin output falling time	t_{Cr}	—	—	35	ns	

Note: • Set high driving ability for the output port pin to be used for the BCLK pin function.

Table 5.19 Clock Timing (4)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VREFH = VREFH0 = 1.62 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V
T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
EXTAL external clock input cycle time		t_{EXcyc}	50	—	—	ns	Figure 5.2
EXTAL external clock input high pulse width		t_{EXH}	20	—	—	ns	
EXTAL external clock input low pulse width		t_{EXL}	20	—	—	ns	
EXTAL external clock rising time		t_{EXr}	—	—	5	ns	
EXTAL external clock falling time		t_{EXf}	—	—	5	ns	
EXTAL external clock input wait time		t_{EXWT}	1	—	—	ms	
Main clock oscillator oscillation frequency		f_{MAIN}	1	—	20	MHz	
Main clock oscillation settling time (crystal)		$t_{MAINOSC}$	T.B.D	—	—	ms	Figure 5.3
Main clock oscillation settling wait time (crystal)		$t_{MAINOSCWT}$	T.B.D	—	—	ms	
Low-speed clock cycle time		t_{cyc}	8.89	8	7.27	µs	
Low-speed clock oscillator oscillation frequency		f_{LOCO}	112.5	125	137.5	kHz	
Low-speed clock oscillation settling wait time		t_{LOCOWT}	—	—	20	µs	Figure 5.4
High-speed clock oscillator oscillation frequency		f_{HOCO}	T.B.D	32	T.B.D	MHz	HCFRQ = 00b
			T.B.D	36.864	T.B.D		HCFRQ = 01b
			T.B.D	40	T.B.D		HCFRQ = 10b
			T.B.D	50	T.B.D		HCFRQ = 11b
High-speed clock oscillation settling wait time 1		$t_{HOCOWT1}$	—	—	T.B.D	ms	Figure 5.5
High-speed clock oscillation settling wait time 2		$t_{HOCOWT2}$	—	—	T.B.D	ms	Figure 5.6
High-speed clock power supply settling time		t_{HOCOP}	—	—	T.B.D	ms	Figure 5.7
PLL input frequency		f_{PLLIN}	4	—	12.5	MHz	Figure 5.8
PLL circuit oscillation frequency		f_{PLL}	50	—	100	MHz	
PLL clock oscillation settling time	PLL operation started after main clock oscillation has settled	t_{PLL1}	—	—	500	µs	Figure 5.9
PLL clock oscillation settling wait time		t_{PLLWT1}	1.5	—	—	ms	
PLL clock oscillation settling time	PLL operation started before main clock oscillation has settled	t_{PLL2}	10	—	—	ms	Figure 5.10
PLL clock oscillation settling wait time		t_{PLLWT2}	11	—	—	ms	
Sub-clock oscillator oscillation frequency		f_{SUB}	—	32.768	—	kHz	
Sub-clock oscillation settling time		t_{SUBOSC}	2	—	—	s	Figure 5.11
Sub-clock oscillation settling wait time		$t_{SUBOSCW}T$	4	—	—	s	

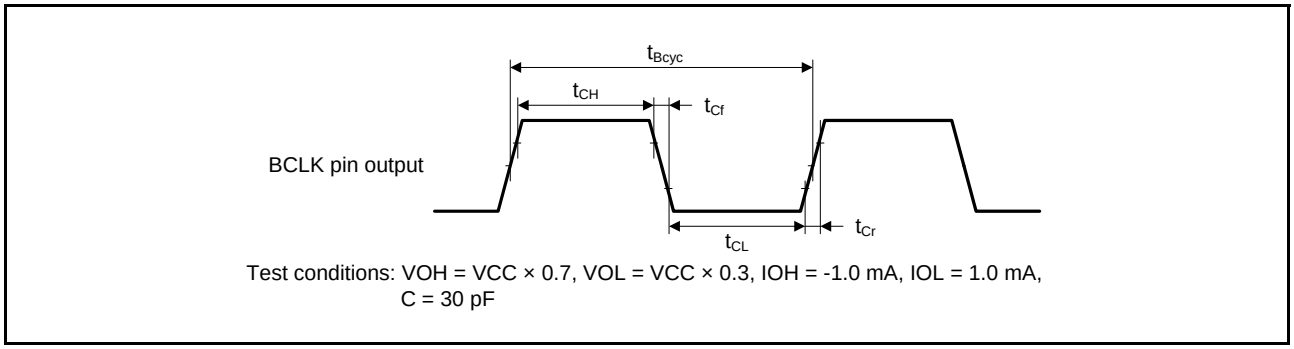


Figure 5.1 BCLK Pin Output, SDCLK Pin Output Timing

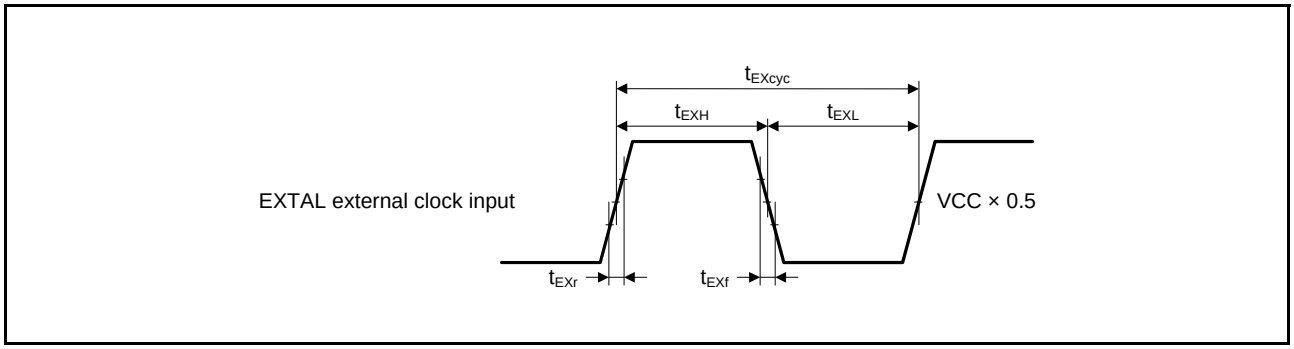


Figure 5.2 EXTAL External Clock Input Timing

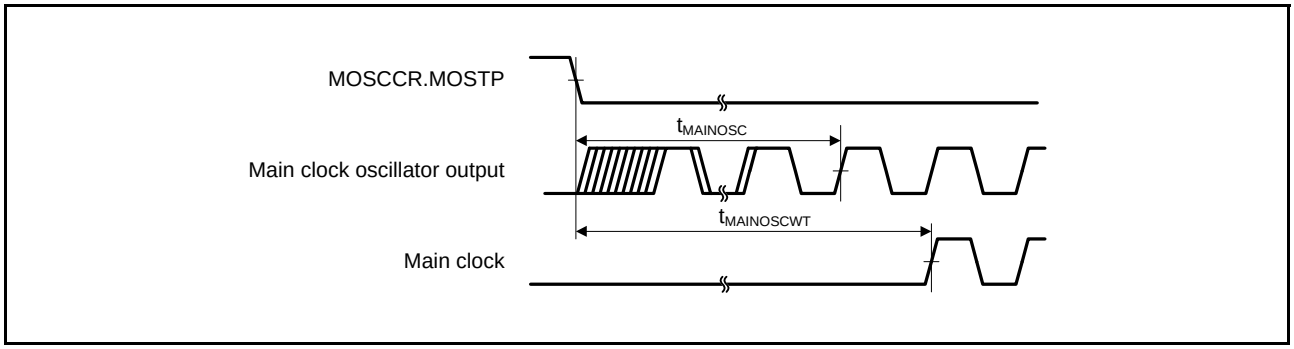


Figure 5.3 Main Clock Oscillation Start Timing

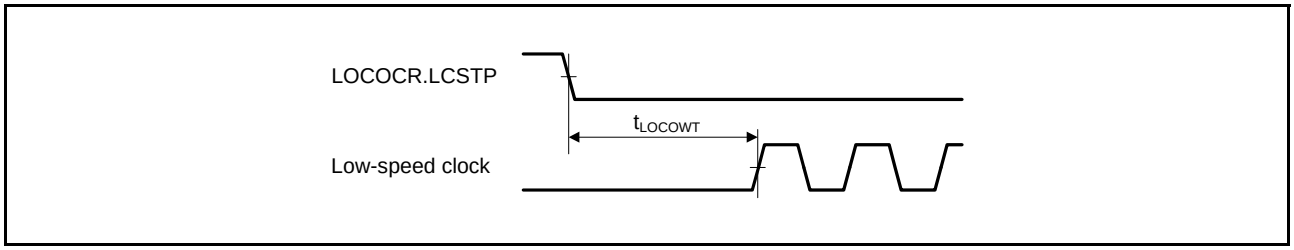


Figure 5.4 Low-Speed Clock Oscillation Start Timing

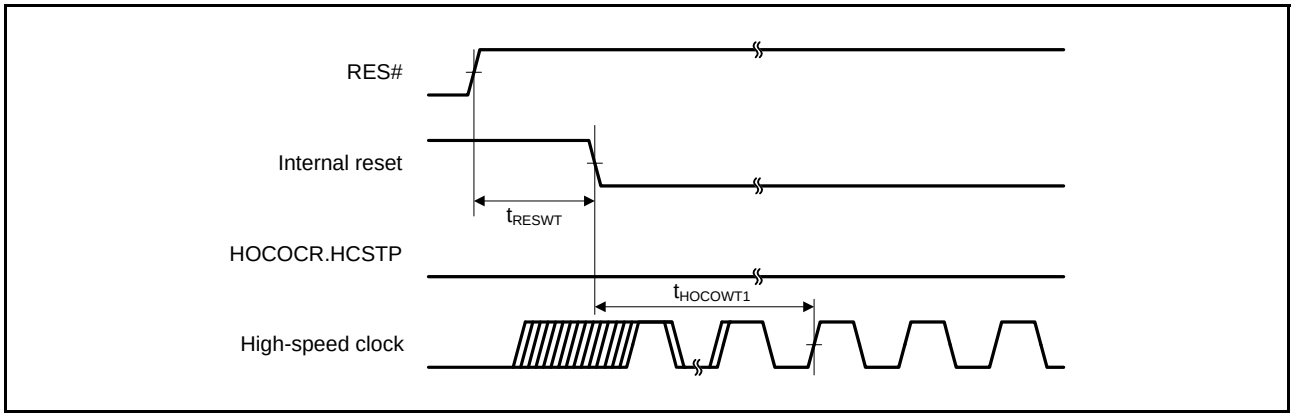


Figure 5.5 High-Speed Clock Oscillation Start Timing (After Reset is Canceled by Setting the OFS1.HOCOEN Bit to 0)

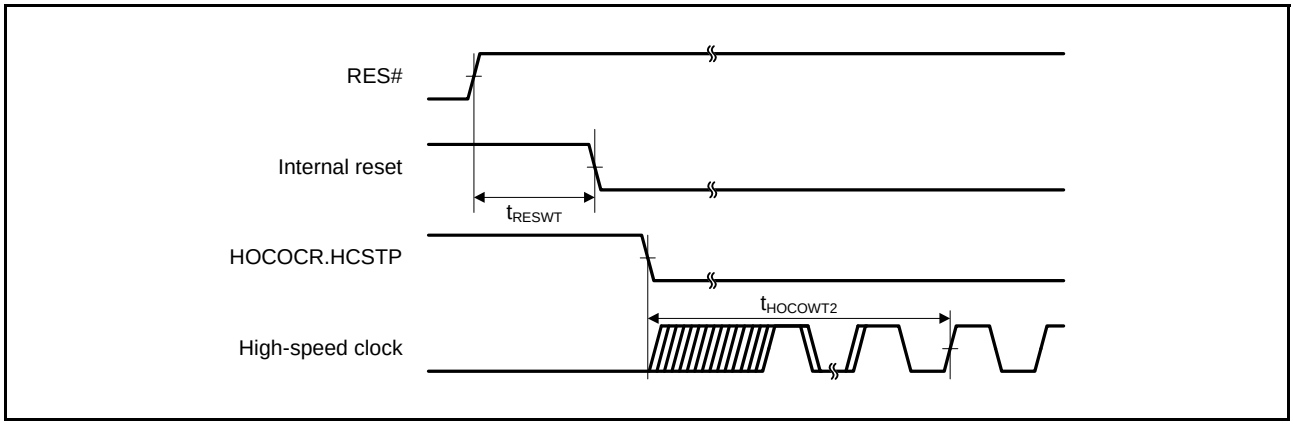


Figure 5.6 High-Speed Clock Oscillation Start Timing (Oscillation is Started by Setting the HOCOCR.HCSTP Bit)

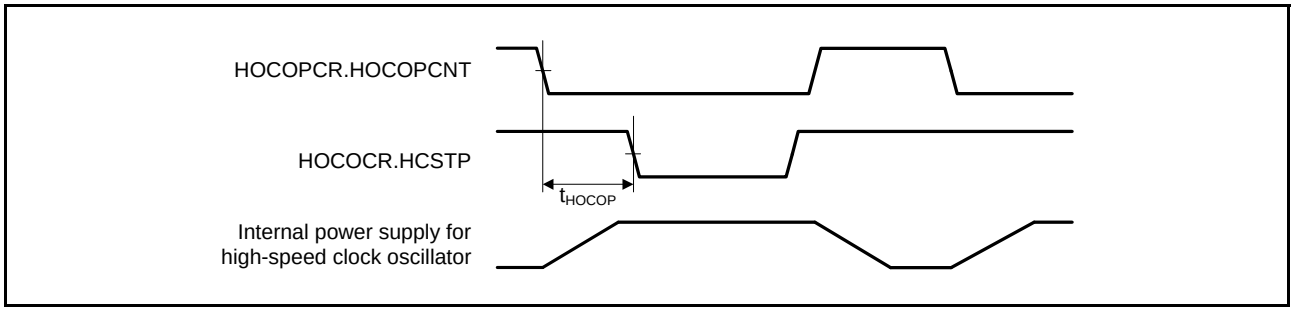


Figure 5.7 High-Speed Clock Oscillator Power Supply Control Timing

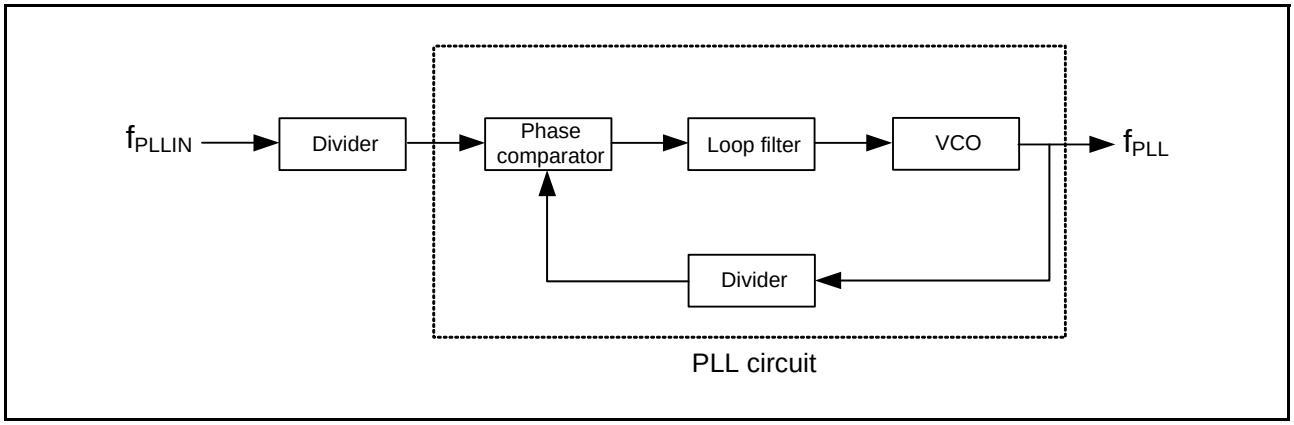


Figure 5.8 PLL Circuit Block

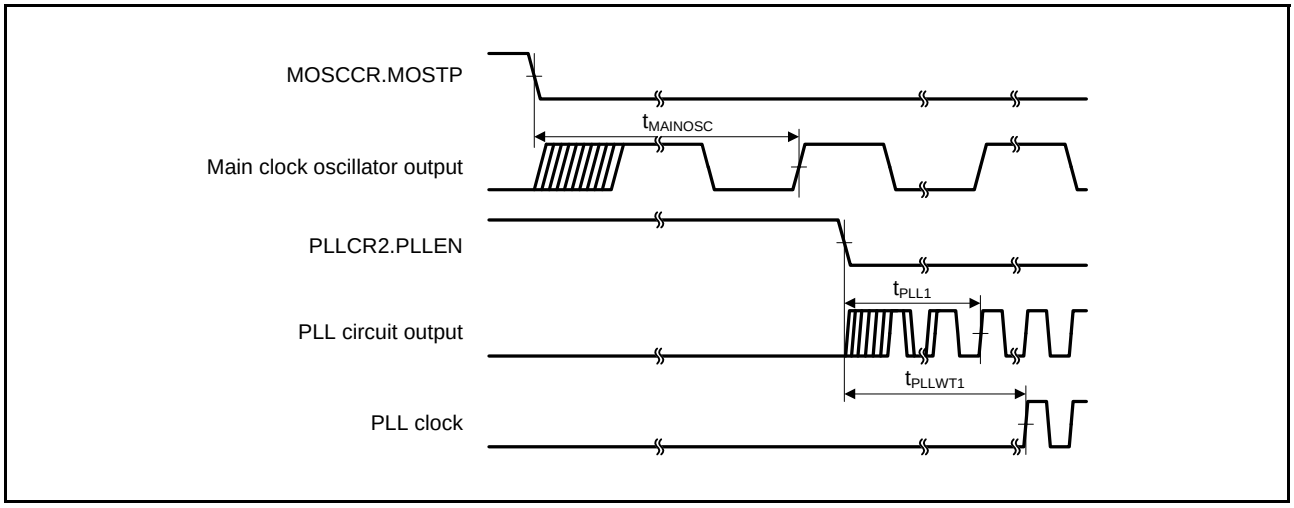


Figure 5.9 PLL Clock Oscillation Start Timing (PLL is Operated after Main Clock Oscillation Has Settled)

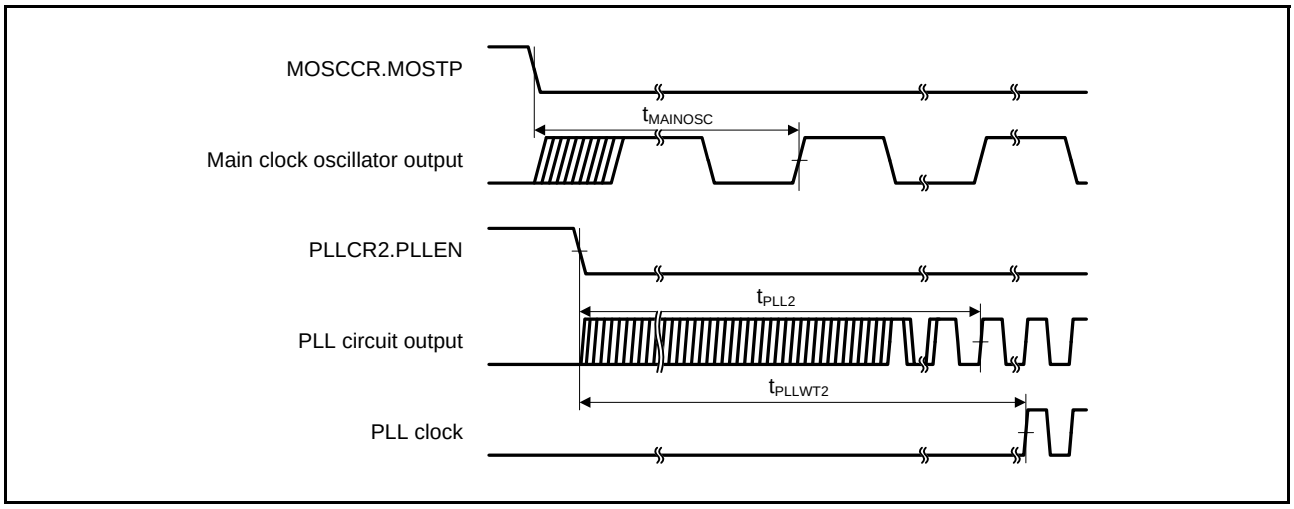


Figure 5.10 PLL Clock Oscillation Start Timing (PLL is Operated before Main Clock Oscillation Has Settled)

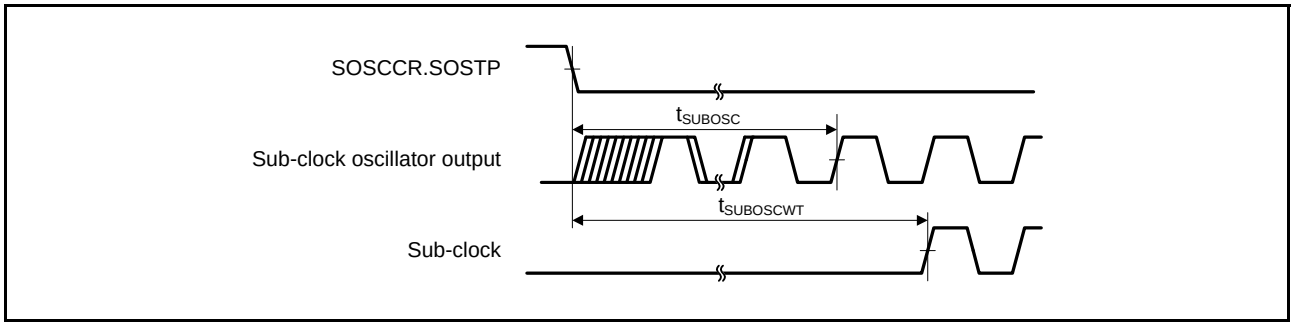


Figure 5.11 PLL Clock Oscillation Start Timing (PLL is Operated before Main Clock Oscillation Has Settled)

5.4.1 Reset Timing

Table 5.20 Reset Timing

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VREFH = VREFH0 = 1.62V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V
T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RES# pulse width	Power-on	t_{RESWP}	T.B.D	—	—	ms	Figure 5.12
	Deep software standby mode	t_{RESWD}	T.B.D	—	—	ms	Figure 5.13
	Software standby mode, low.speed operating mode 1, 2	t_{RESWS}	T.B.D	—	—	ms	
	Other than above (except for programming or erasure of the ROM or E^2 data-flash memory or blank checking of the E^2 data-flash memory)	t_{RESW}	T.B.D	—	—	µs	
Wait time after RES# cancellation		t_{RESWT}	T.B.D	—	T.B.D	t_{cyc}	Figure 5.12
Internal reset time (independent watchdog timer reset, watchdog timer reset, software reset)		t_{RESW2}	T.B.D	—	T.B.D	t_{cyc}	

Note: • Do not allow a reset by the signal on the RES# pin during programming or erasure of the ROM or E^2 data-flash memory or during blank checking of the E^2 data-flash memory. For details, see section 39.13, Usage Notes, in section 39, ROM (Flash Memory for Code Storage).

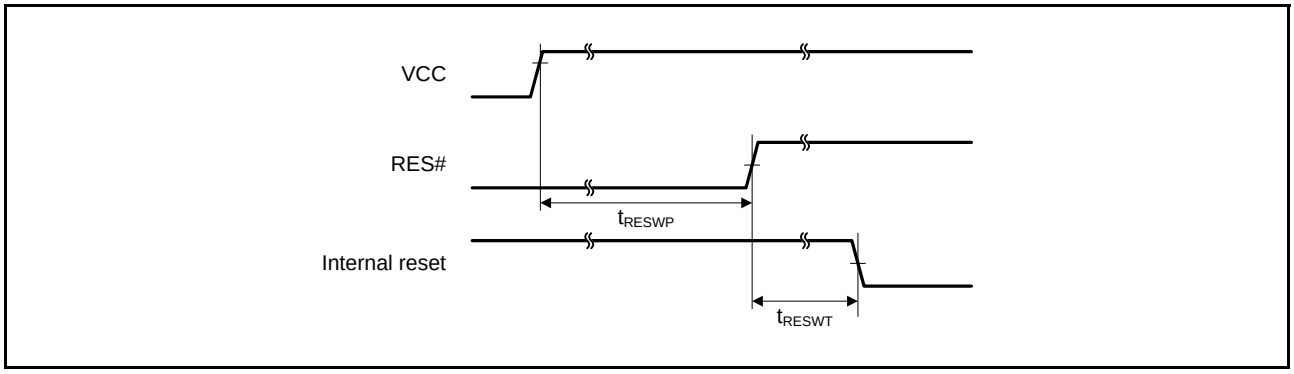


Figure 5.12 Reset Input Timing at Power-On

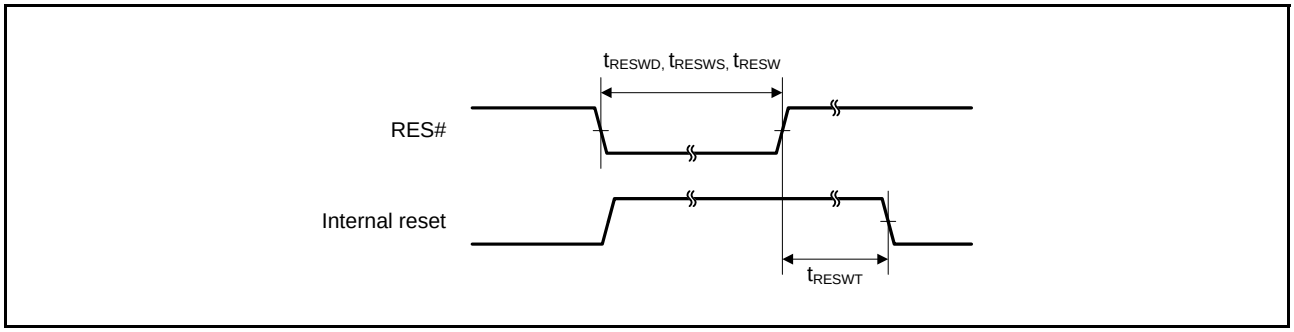


Figure 5.13 Reset Input Timing

5.4.2 Timing of Recovery from Low Power Consumption Modes

Table 5.21 Timing of Recovery from Low Power Consumption Modes

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VREFH = VREFH0 = 1.62 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, ICLK = up to 50 MHz, BCLK = up to 25 MHz (BCLK output = up to 12.5 MHz), T_a = –40 to +85°C

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time after cancellation of software standby mode	Crystal resonator connected to main clock oscillator	Main clock oscillator operating	t_{SBYMC}	T.B.D	—	—	ms	Figure 5.14
		Main clock oscillator and PLL circuit operating	t_{SBYPC}	T.B.D	—	—	ms	
	External clock input to main clock oscillator	Main clock oscillator operating	t_{SBYEX}	T.B.D	—	—	ms	
		Main clock oscillator and PLL circuit operating	t_{SBYPE}	T.B.D	—	—	ms	
	Sub-clock oscillator operating		t_{SBYSC}	T.B.D	—	—	s	
	High-speed clock oscillator operating		t_{SBYHO}	—	—	T.B.D	ms	
	Low-speed clock oscillator or IWDT-specific low-speed clock oscillator operating		t_{SBYLO}	—	—	T.B.D	µs	
Recovery time after cancellation of deep software standby mode			t_{DSBY}	—	—	T.B.D	ms	Figure 5.15
Wait time after cancellation of deep software standby mode			t_{DSBYWT}	T.B.D	—	T.B.D	t_{cyc}	

Note: • The wait time varies depending on the state in which each oscillator was when the WAIT instruction was executed. The recovery time when multiple oscillators are operating is the same period as that when the oscillator, which takes the longest time for recovery among the operating oscillators, is operating alone.

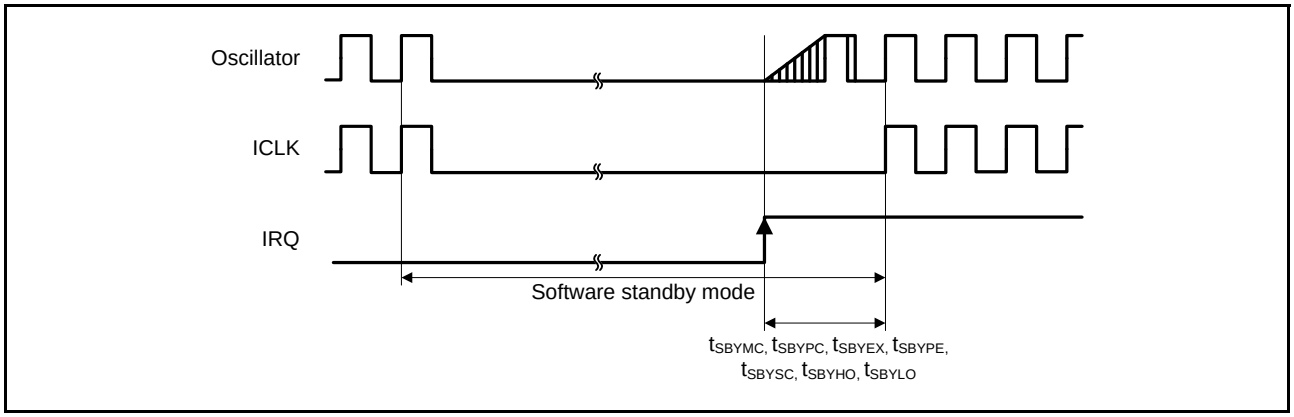


Figure 5.14 Software Standby Mode Cancellation Timing

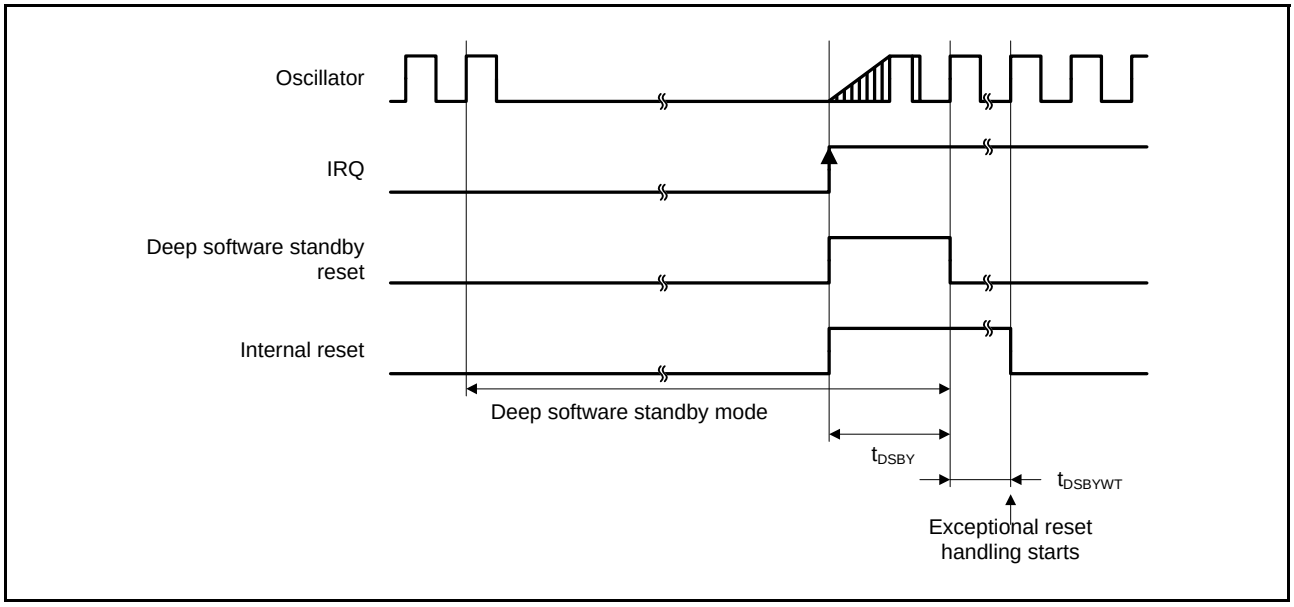


Figure 5.15 Deep Software Standby Mode Cancellation Timing

5.4.3 Control Signal Timing

Table 5.22 Control Signal Timing

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VREFH = VREFH0 = 1.62 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, ICLK = up to 50 MHz, BCLK = up to 25 MHz (BCLK output = up to 12.5 MHz), T_a = –40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
NMI pulse width	t_{NMIW}	T.B.D	—	—	ns	Figure 5.16
IRQ pulse width	t_{IRQW}	T.B.D	—	—	ns	Figure 5.17

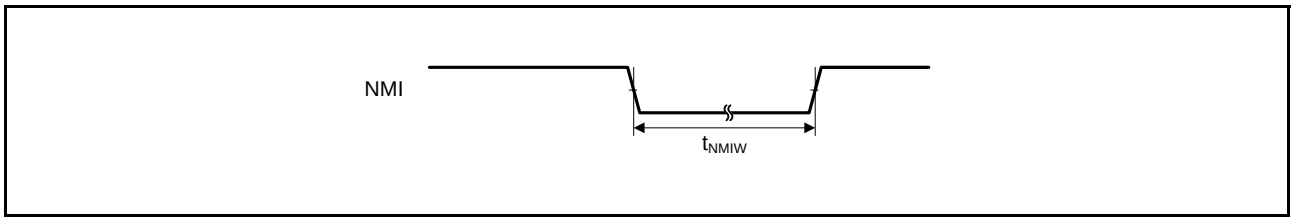


Figure 5.16 NMI Interrupt Input Timing

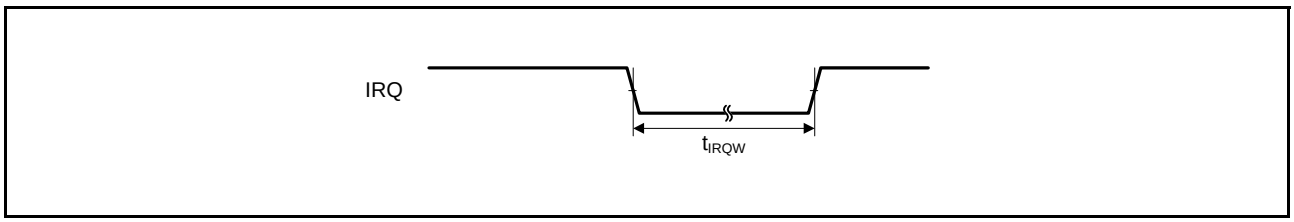


Figure 5.17 IRQ Interrupt Input Timing

5.4.4 Bus Timing

Table 5.23 Bus Timing (1)

Conditions: AVCC0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, (BCLK output = up to 12.5 MHz),
T_a = –40 to +85°C
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, I_{OH} = -1.0 mA, I_{OL} = 1.0 mA, C = 30 pF

Item	Symbol	Min.	Typ.	Max.	Unit
Address delay time	t_{AD}	—	60	ns	Figure 5.18 to Figure 5.21
Byte control delay time	t_{BCD}	—	60	ns	
CS# delay time	t_{CSD}	—	60	ns	
RD# delay time	t_{RSD}	—	60	ns	
Read data setup time	t_{RDS}	40	—	ns	
Read data hold time	t_{RDH}	0.0	—	ns	
WR# delay time	t_{WRD}	—	60	ns	
Write data delay time	t_{WDD}	—	60	ns	
Write data hold time	t_{WDH}	0.0	—	ns	
WAIT# setup time	t_{WTS}	40	—	ns	Figure 5.22
WAIT# hold time	t_{WTH}	0.0	—	ns	

Table 5.24 Bus Timing (2)

Conditions: AVCC0 = 1.8 to 2.7 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V (BCLK output = up to 8 MHz),
T_a = –40 to +85°C
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, I_{OH} = -1.0 mA, I_{OL} = 1.0 mA, C = 30 pF

Item	Symbol	Min.	Typ.	Max.	Unit
Address delay time	t_{AD}	—	90	ns	Figure 5.18 to Figure 5.21
Byte control delay time	t_{BCD}	—	90	ns	
CS# delay time	t_{CSD}	—	90	ns	
RD# delay time	t_{RSD}	—	90	ns	
Read data setup time	t_{RDS}	60	—	ns	
Read data hold time	t_{RDH}	0.0	—	ns	
WR# delay time	t_{WRD}	—	90	ns	
Write data delay time	t_{WDD}	—	90	ns	
Write data hold time	t_{WDH}	0.0	—	ns	
WAIT# setup time	t_{WTS}	60	—	ns	Figure 5.22
WAIT# hold time	t_{WTH}	0.0	—	ns	

Table 5.25 Bus Timing (3)

Conditions: AVCC0 = 1.62 to 1.8V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, (BCLK output = to 6 MHz),
T_a = –40 to +85°C
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, I_{OH} = -1.0 mA, I_{OL} = 1.0 mA, C = 30 pF

Item	Symbol	Min.	Typ.	Max.	Unit
Address delay time	t_{AD}	—	125	ns	Figure 5.18 to Figure 5.21
Byte control delay time	t_{BCD}	—	125	ns	
CS# delay time	t_{CSD}	—	125	ns	
RD# delay time	t_{RSD}	—	125	ns	
Read data setup time	t_{RDS}	85	—	ns	
Read data hold time	t_{RDH}	0.0	—	ns	
WR# delay time	t_{WRD}	—	125	ns	
Write data delay time	t_{WDD}	—	125	ns	
Write data hold time	t_{WDH}	0.0	—	ns	
WAIT# setup time	t_{WTS}	85	—	ns	Figure 5.22
WAIT# hold time	t_{WTH}	0.0	—	ns	

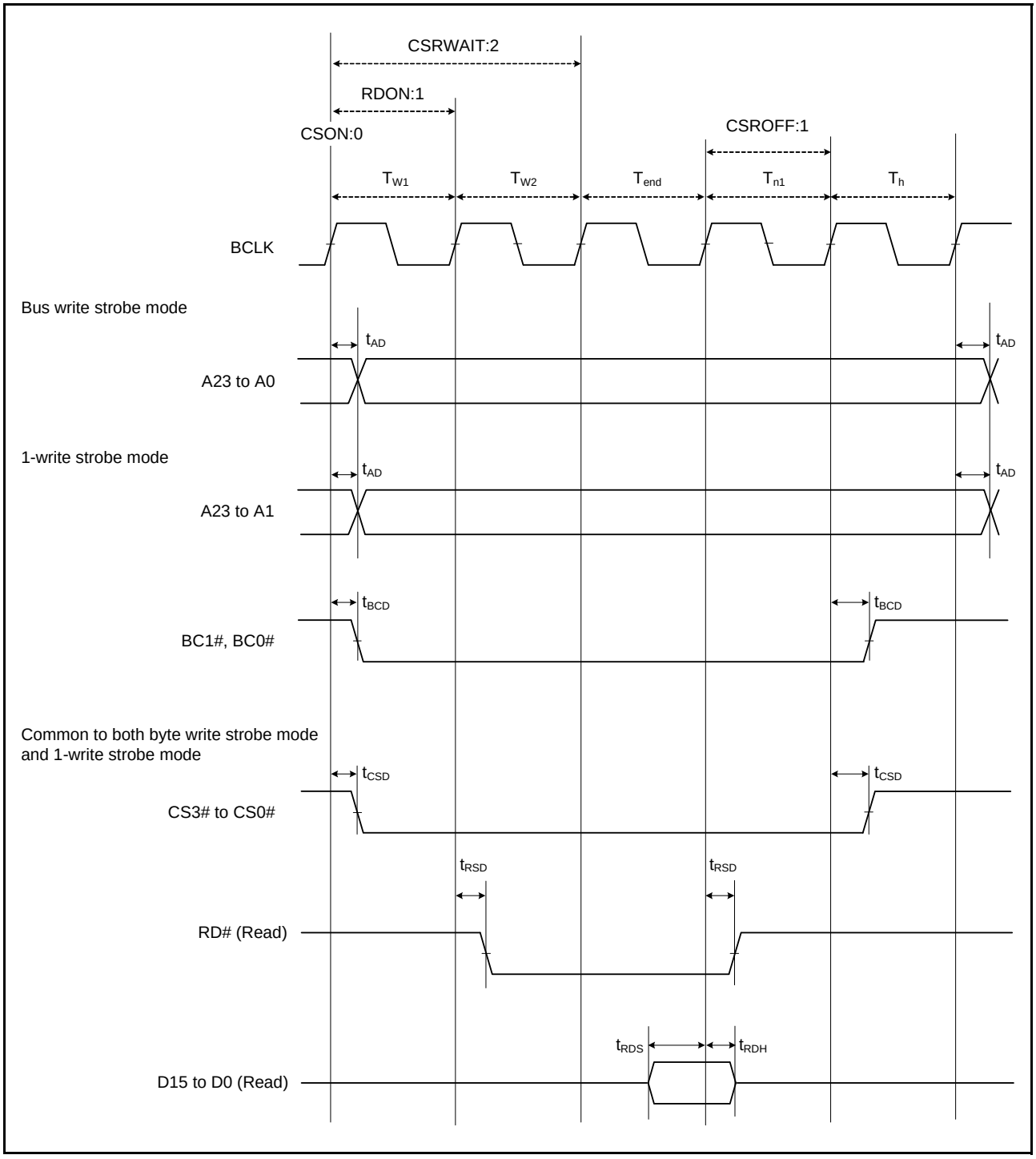
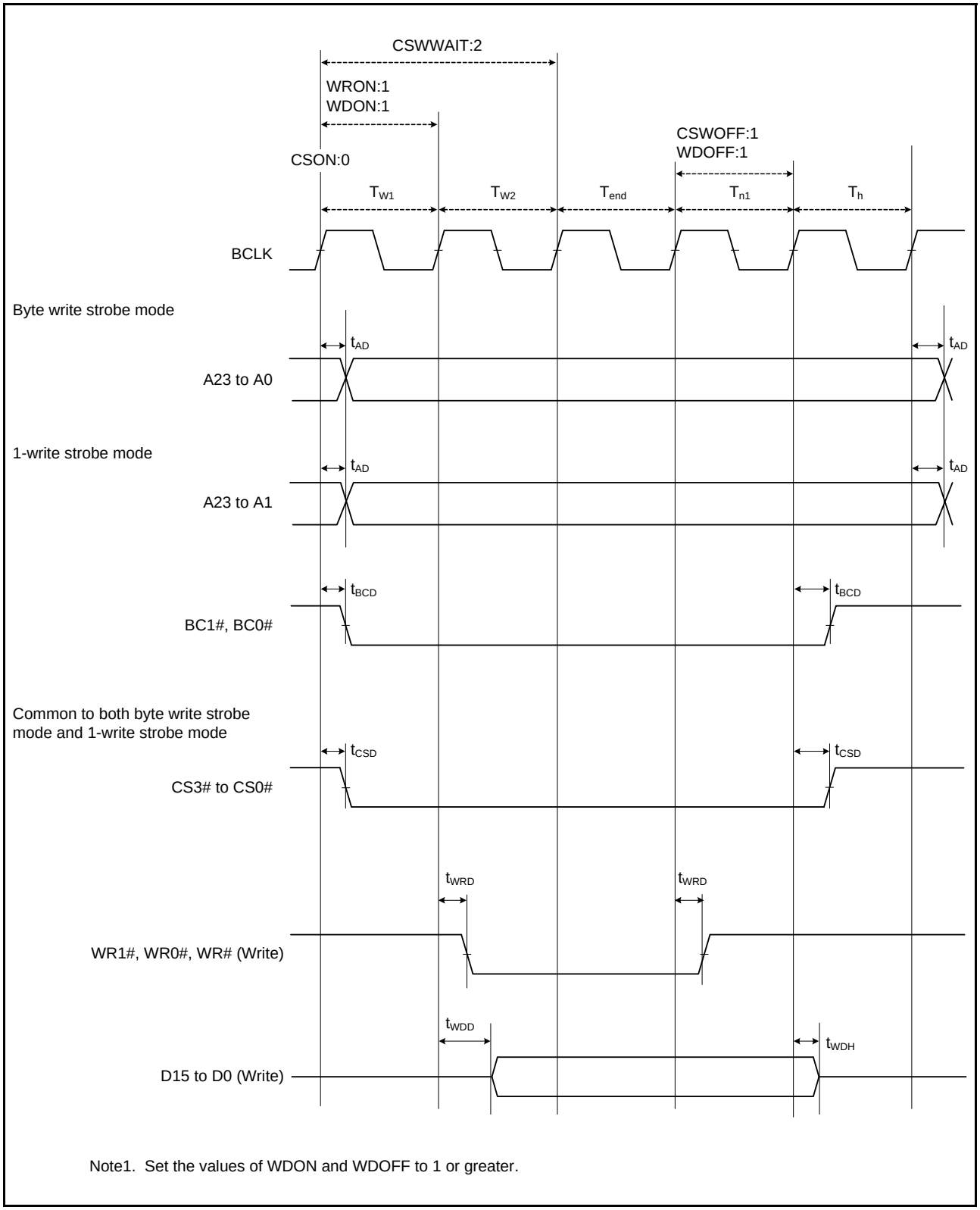


Figure 5.18 External Bus Timing/Normal Read Cycle (Bus Clock Synchronized)



Note1. Set the values of WDON and WDOFF to 1 or greater.

Figure 5.19 External Bus Timing/Normal Write Cycle (Bus Clock Synchronized)

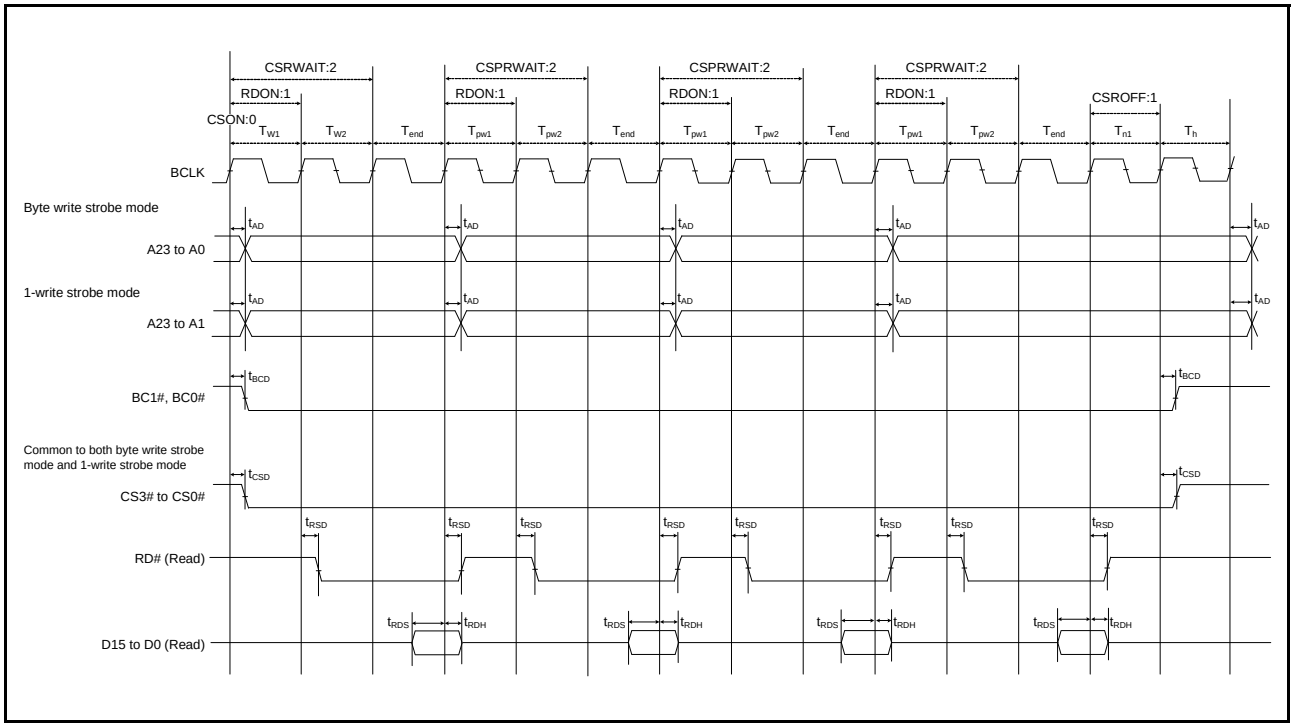
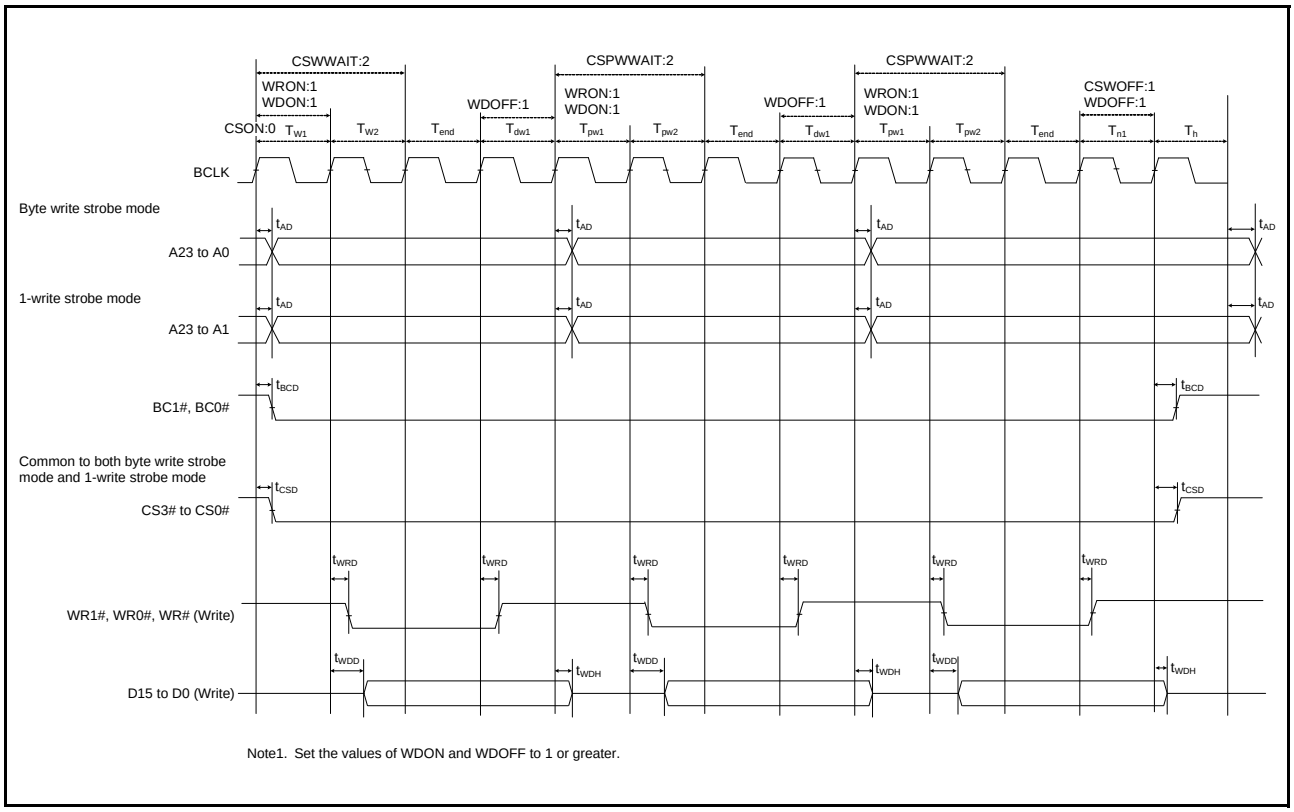


Figure 5.20 External Bus Timing/Page Read Cycle (Bus Clock Synchronized)



Note1. Set the values of WDON and WDOFF to 1 or greater.

Figure 5.21 External Bus Timing/Page Write Cycle (Bus Clock Synchronized)

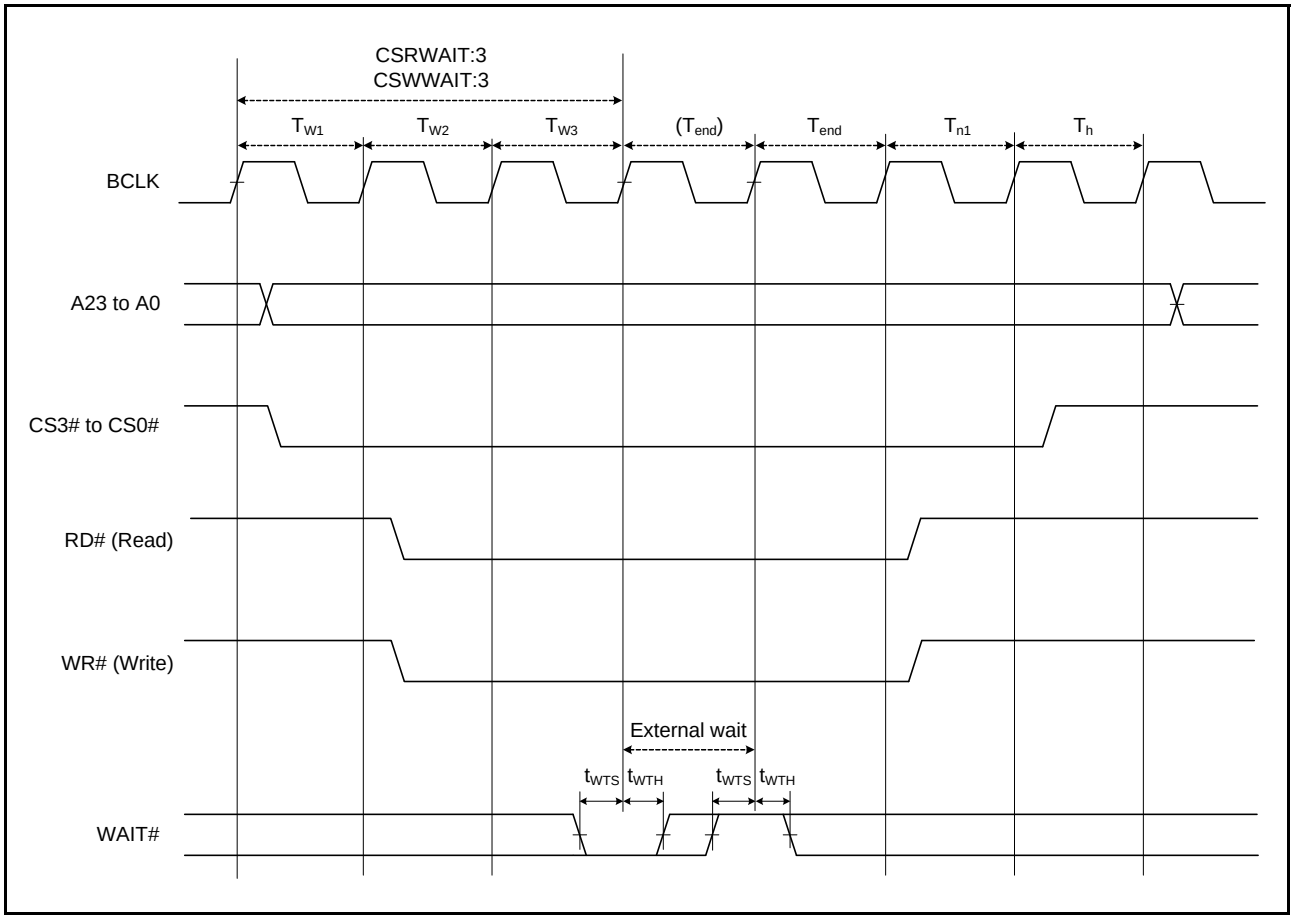


Figure 5.22 External Bus Timing/External Wait Control

Table 5.26 Bus Timing (Multiplexed Bus) (1)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, (BCLK output = up to 12.5 MHz),
T_a = –40 to +85°C
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, I_{OH} = -1.0 mA, I_{OL} = 1.0 mA, C = 30 pF

Item	Symbol	Min.	Typ.	Max.	Unit
Address delay time	t_{AD}	—	60	ns	Figure 5.18 to Figure 5.21
Byte control delay time	t_{BCD}	—	60	ns	
CS# delay time	t_{CSD}	—	60	ns	
RD# delay time	t_{RSD}	—	60	ns	
Read data setup time	t_{RDS}	40	—	ns	
Read data hold time	t_{RDH}	0.0	—	ns	
WR# delay time	t_{WRD}	—	60	ns	
Write data delay time	t_{WDD}	—	60	ns	
Write data hold time	t_{WDH}	0.0	—	ns	
WAIT# setup time	t_{WTS}	40	—	ns	Figure 5.22
WAIT# hold time	t_{WTH}	0.0	—	ns	
ALE output delay time (BCLK standard)	td(BCLK-ALE) →tALED	—	60	ns	Figure 5.23, Figure 5.24
ALE output delay time (address standard)	td(AD-ALE)	T.B.D	—	ns	
ALE output hold time (address standard)	th(ALE-AD)	T.B.D	—	ns	
RD signal output delay time after address setup	td(AD-RD)	0	—	ns	
WR signal output delay time after address setup	td(AD-WR)	0	—	ns	
Address output floating start time	tdZ(RD-AD)	—	60	ns	

Table 5.27 Bus Timing (Multiplexed Bus) (2)

Conditions: VCC = AVCC0 = 1.8 to 2.7 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, (BCLK output = up to 8 MHz),
T_a = –40 to +85°C
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, I_{OH} = -1.0 mA, I_{OL} = 1.0 mA, C = 30 pF

Item	Symbol	Min.	Typ.	Max.	Unit
Address delay time	t_{AD}	—	90	ns	Figure 5.18 to Figure 5.21
Byte control delay time	t_{BCD}	—	90	ns	
CS# delay time	t_{CSD}	—	90	ns	
RD# delay time	t_{RSD}	—	90	ns	
Read data setup time	t_{RDS}	60	—	ns	
Read data hold time	t_{RDH}	0.0	—	ns	
WR# delay time	t_{WRD}	—	90	ns	
Write data delay time	t_{WDD}	—	90	ns	
Write data hold time	t_{WDH}	0.0	—	ns	
WAIT# setup time	t_{WTS}	60	—	ns	Figure 5.22
WAIT# hold time	t_{WTH}	0.0	—	ns	
ALE output delay time (BCLK standard)	td(BCLK-ALE) →tALED	—	90	ns	Figure 5.23, Figure 5.24
ALE output delay time (address standard)	td(AD-ALE)	T.B.D	—	ns	
ALE output hold time (address standard)	th(ALE-AD)	T.B.D	—	ns	
RD signal output delay time after address setup	td(AD-RD)	0	—	ns	
WR signal output delay time after address setup	td(AD-WR)	0	—	ns	
Address output floating start time	tdZ(RD-AD)	—	90	ns	

Table 5.28 Bus Timing (Multiplexed Bus) (3)

Conditions: VCC = AVCC0 = 1.62 to 1.8 V, VSS = AVSS0 = VREFL = VREFL0 = 0V, (BCLK output = up to 6 MHz),
T_a = –40 to +85°C
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, I_{OH} = -1.0 mA, I_{OL} = 1.0 mA, C = 30 pF

Item	Symbol	Min.	Typ.	Max.	Unit
Address delay time	t_{AD}	—	125	ns	Figure 5.18 to Figure 5.21
Byte control delay time	t_{BCD}	—	125	ns	
CS# delay time	t_{CSD}	—	125	ns	
RD# delay time	t_{RSD}	—	125	ns	
Read data setup time	t_{RDS}	85	—	ns	
Read data hold time	t_{RDH}	0.0	—	ns	
WR# delay time	t_{WRD}	—	125	ns	
Write data delay time	t_{WDD}	—	125	ns	
Write data hold time	t_{WDH}	0.0	—	ns	
WAIT# setup time	t_{WTS}	85	—	ns	Figure 5.22
WAIT# hold time	t_{WTH}	0.0	—	ns	
ALE output delay time (BCLK standard)	td(BCLK-ALE) →tALED	—	125	ns	Figure 5.23, Figure 5.24
ALE output delay time (address standard)	td(AD-ALE)	T.B.D	—	ns	
ALE output hold time (address standard)	th(ALE-AD)	T.B.D	—	ns	
RD signal output delay time after address setup	td(AD-RD)	0	—	ns	
WR signal output delay time after address setup	td(AD-WR)	0	—	ns	
Address output floating start time	tdZ(RD-AD)	—	125	ns	

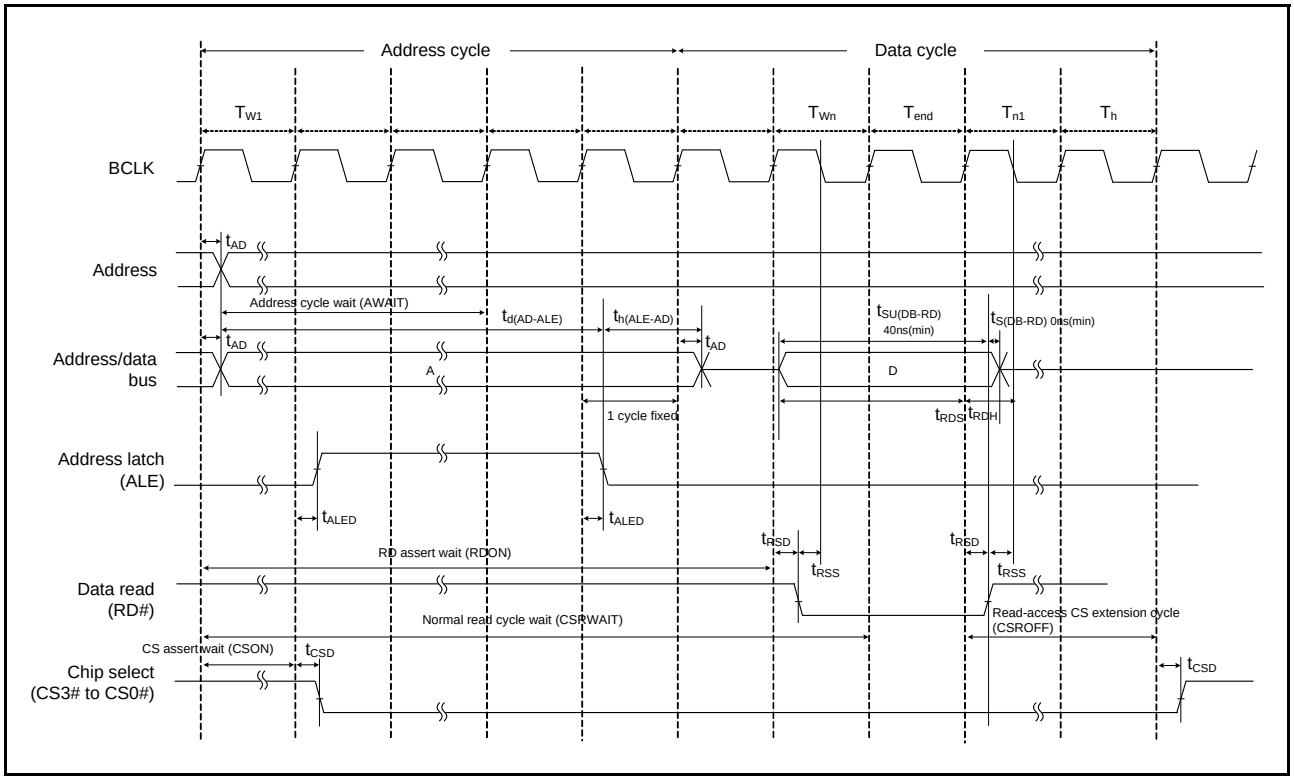


Figure 5.23 Example of Operation in Read Access over the External Bus (Multiplexed)

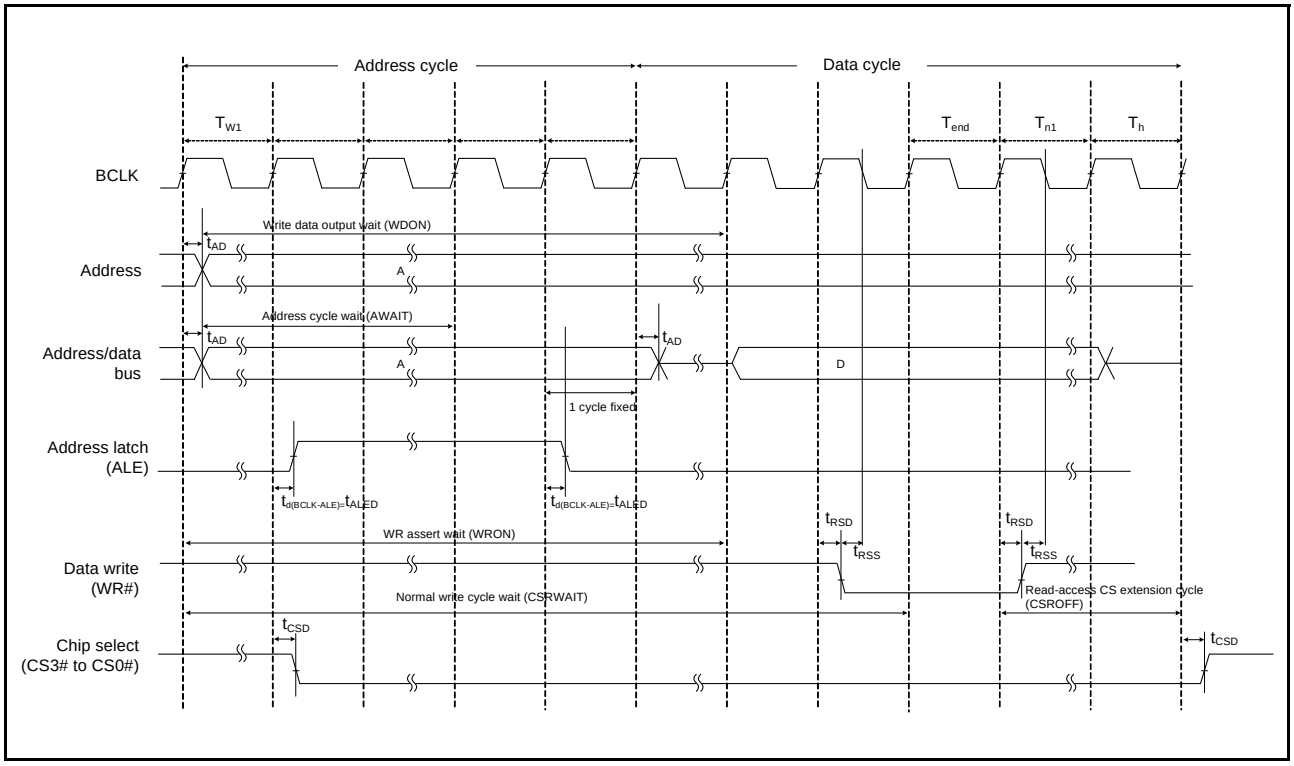


Figure 5.24 Example of Operation in Write Access over the External Bus (Multiplexed)

5.4.5 Timing of On-Chip Peripheral Modules

Table 5.29 Timing of On-Chip Peripheral Modules (1)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VREFH = VREFH0 = 1.8 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, I_{OH} = -1.0 mA, I_{OL} = 1.0 mA, C = 30 pF

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
I/O ports	Input data pulse width		t_{PRW}	1.5	—	t_{Pcyc}	Figure 5.25
MTU2A	Input capture input pulse width	Single-edge setting	t_{TICW}	1.5	—	t_{Pcyc}	Figure 5.26
		Both-edge setting		2.5	—		
	Timer clock pulse width	Single-edge setting	t_{TCKWH}, t_{TCKWL}	1.5	—	t_{Pcyc}	Figure 5.27
		Both-edge setting		2.5	—		
		Phase counting mode		2.5	—		
POE2	POE# input pulse width		t_{POEW}	1.5	—	t_{Pcyc}	Figure 5.28
8-bit timer	Timer clock pulse width	Single-edge setting	t_{TMCWH}, t_{TMCWL}	1.5	—	t_{Pcyc}	Figure 5.29
		Both-edge setting		2.5	—		
SCI	Input clock cycle	Asynchronous	t_{Scyc}	4	—	t_{Pcyc}	Figure 5.30
		Clock synchronous		6	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	T.B.D	ns	
	Input clock fall time		t_{SCKf}	—	T.B.D	ns	
	Output clock cycle	Asynchronous	t_{Scyc}	16	—	t_{Pcyc}	
		Clock synchronous		4	—		
	Output clock pulse width*2		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time*2		t_{SCKr}	—	T.B.D	ns	
	Output clock fall time*2		t_{SCKf}	—	T.B.D	ns	
	Transmit data delay time*3	Clock synchronous	t_{TXD}	—	T.B.D	ns	Figure 5.31
	Receive data setup time	Clock synchronous	t_{RXS}	T.B.D	—	ns	
	Receive data hold time	Clock synchronous	t_{RXH}	T.B.D	—	ns	
A/D converter	Trigger input pulse width		t_{TRGW}	1.5	—	t_{Pcyc}	Figure 5.32

Note 1. t_{Pcyc}: PCLK cycle
Note 2. Set high driving ability for the output port pin to be used for the clock.
Note 3. Set high driving ability for the output port pin to be used for the data.

Table 5.30 Timing of On-Chip Peripheral Modules (2)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VREFH = VREFH0 = 1.8 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0V,
T_a = –40 to +85°C
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, I_{OH} = -1.0 mA, I_{OL} = 1.0 mA, C = 30 pF

Item				Symbol	Min.	Max.	Unit*1	Test Conditions
RSPI	RSPCK clock cycle	Master		t_{SPcyc}	4	4096	t_{Pcyc}	Figure 5.33
		Slave			8	4096		
	RSPCK clock high pulse width*2	Master		t_{SPCKWH}	T.B.D	—	ns	
		Slave			T.B.D	—		
	RSPCK clock low pulse width*2	Master		t_{SPCKWL}	T.B.D	—	ns	
		Slave			T.B.D	—		
	RSPCK clock rise/fall time*2	Output		t_{SPCKr}, t_{SPCKf}	—	T.B.D	ns	
		Input			—	T.B.D	µs	
	Data input setup time	Master	VCC ≥ 3.0 V	t_{SU}	T.B.D	—	ns	Figure 5.34 to Figure 5.37
			VCC < 3.0 V		T.B.D	—		
		Slave			T.B.D	—		
	Data input hold time	Master		t_H	T.B.D	—	ns	
		Slave			T.B.D	—		
	SSL setup time	Master		t_{LEAD}	1	8	t_{SPcyc}	
		Slave			4	—	t_{Pcyc}	
	SSL hold time	Master		t_{LAG}	1	8	t_{SPcyc}	
		Slave			4	—	t_{Pcyc}	
	Data output delay time	Master		t_{OD}	—	T.B.D	ns	
		Slave			—	T.B.D		
	Data output hold time	Master		t_{OH}	T.B.D	—	ns	
		Slave			T.B.D	—		
	Successive transmission delay time	Master		t_{TD}	T.B.D	T.B.D	ns	
		Slave			T.B.D	—		
	MOSI and MISO rise/ fall time	Output		t_{Dr}, t_{Df}	—	T.B.D	ns	
		Input			—	T.B.D	µs	
	SSL rise/fall time	Output		t_{SSLr}, t_{SSLf}	—	T.B.D	ns	
		Input			—	T.B.D	µs	
	Slave access time			t_{SA}	—	4	t_{Pcyc}	Figure 5.36 and Figure 5.37
	Slave output release time			t_{REL}	—	3	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLK cycle
Note 2. Set high driving ability for the output port pin to be used for the clock.

Table 5.31 Timing of On-Chip Peripheral Modules (3)

Conditions: VVCC = AVCC0 = 1.62 to 5.5 V, VREFH = VREFH0 = 1.8 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0V,
T_a = –40 to +85°C
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, I_{OH} = -1.0 mA, I_{OL} = 1.0 mA, C = 30 pF

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)*2	t_{SPcyc}	4	65536	t_{Pcyc}	Figure 5.33
	SCK clock cycle input (slave)		8	65536		
	SCK clock high pulse width*2	t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width*2	t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time*2	t_{SPCKr}, t_{SPCKf}	—	T.B.D	ns	
	Data input setup time	t_{SU}	T.B.D	—	ns	Figure 5.34 to Figure 5.37
	Data input hold time	t_H	T.B.D	—	ns	
	SS input setup time	t_{LEAD}	1	—	t_{SPcyc}	
	SS input hold time	t_{LAG}	1	—	t_{SPcyc}	
	Data output delay time	t_{OD}	—	T.B.D	ns	
	Data output hold time	t_{OH}	T.B.D	—	ns	
	Data rise/fall time	t_{Dr}, t_{Df}	—	T.B.D	ns	
	SS input rise/fall time	t_{SSLr}, t_{SSLf}	—	T.B.D	ns	
	Save access time	t_{SA}	—	5	t_{Pcyc}	Figure 5.36 and Figure 5.37
	Slave output release time	t_{REL}	—	5	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLK cycle
Note 2. Set high driving ability for the output port pin to be used for the clock.

Table 5.32 Timing of On-Chip Peripheral Modules (4)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH = VREFH0 = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, PCLKB = up to 32 MHz, T_a = –40 to +85°C

Item		Symbol	Min.*1,*2	Max.	Unit	Test Conditions
RIIC (Standard-mode, SMBus) ICFER.FMPE = 0	SCL input cycle time	t_{SCL}	8(10) × (1/PCLK) + 1300	—	ns	Figure 5.38
	SCL input high pulse width	t_{SCLH}	3(5) × (1/PCLK) + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	5 × (1/PCLK) + 1000	—	ns	
	SCL, SDA input rise time	t_{Sr}	—	1000	ns	
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	4 × (1/PCLK)	ns	
	SDA input bus free time	t_{BUF}	5 × (1/PCLK) + 1000	—	ns	
	Start condition input hold time	t_{STAH}	3 (5) × (1/PCLK) + 300	—	ns	
	Restart condition input setup time	t_{STAS}	5 × (1/PCLK) + 1000	—	ns	
	Stop condition input setup time	t_{STOS}	3 (5) × (1/PCLK) + 300	—	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
RIIC (Fast-mode)	SCL input cycle time	t_{SCL}	8 (10) × (1/PCLK) + 600	—	ns	
	SCL input high pulse width	t_{SCLH}	3 (5) × (1/PCLK) + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	5 × (1/PCLK) + 300	—	ns	
	SCL, SDA input rise time	t_{Sr}	20 + 0.1C_b	300	ns	
	SCL, SDA input fall time	t_{Sf}	20 + 0.1C_b	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	4 × (1/PCLK)	ns	
	SDA input bus free time	t_{BUF}	5 × (1/PCLK) + 300	—	ns	
	Start condition input hold time	t_{STAH}	3 (5) × (1/PCLK) + 300	—	ns	
	Restart condition input setup time	t_{STAS}	5 × (1/PCLK) + 300	—	ns	
	Stop condition input setup time	t_{STOS}	3 (5) × (1/PCLK) + 300	—	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note 1. The value in parentheses is used when ICMR3.NF[1:0] are set to 11b while a digital filter is enabled with ICFER.FMPE = 1.
Note 2. C_b indicates the total capacity of the bus line.

Table 5.33 Timing of On-Chip Peripheral Modules (5)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH=VREFH0 = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, PCLKB = up to 32 MHz, T_a = –40 to +85°C

Item		Symbol	Min.*1,*2	Max.	Unit	Test Conditions
Simple IIC (Standard-mode)	SDA input rise time	t_{Sr}	—	1000	ns	Figure 5.38
	SDA input fall time	t_{Sf}	—	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × (1/PCLK)	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
Simple IIC (Fast-mode)	SCL, SDA input rise time	t_{Sr}	$20 + 0.1C_b$	300	ns	
	SCL, SDA input fall time	t_{Sf}	$20 + 0.1C_b$	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	4 × (1/PCLK)	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note 1. The value in parentheses is used when ICMR3.NF[1:0] are set to 11b while a digital filter is enabled with ICFER.NFE = 1.
Note 2. C_b indicates the total capacity of the bus line.

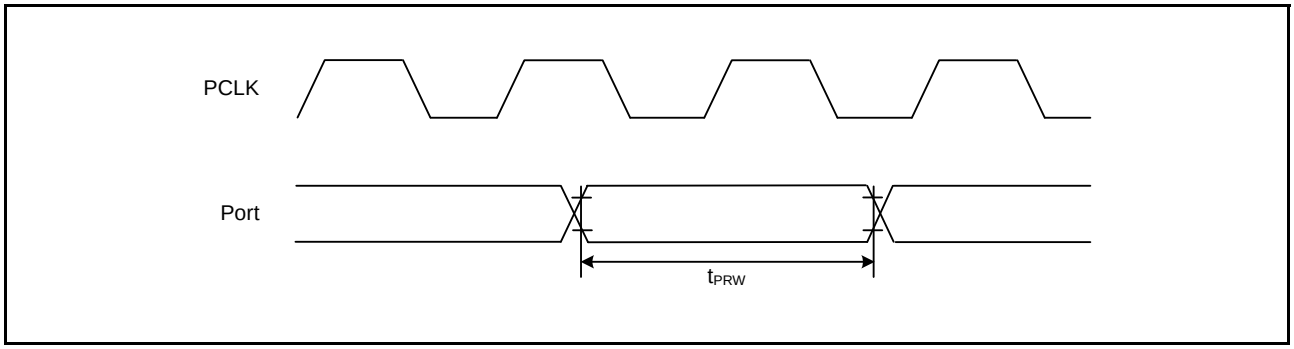


Figure 5.25 I/O Port Input Timing

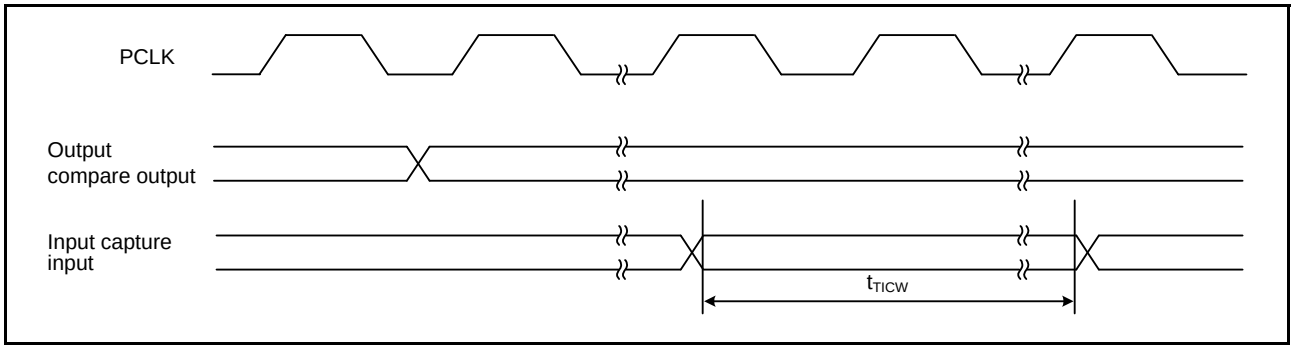


Figure 5.26 MTU2A Input/Output Timing

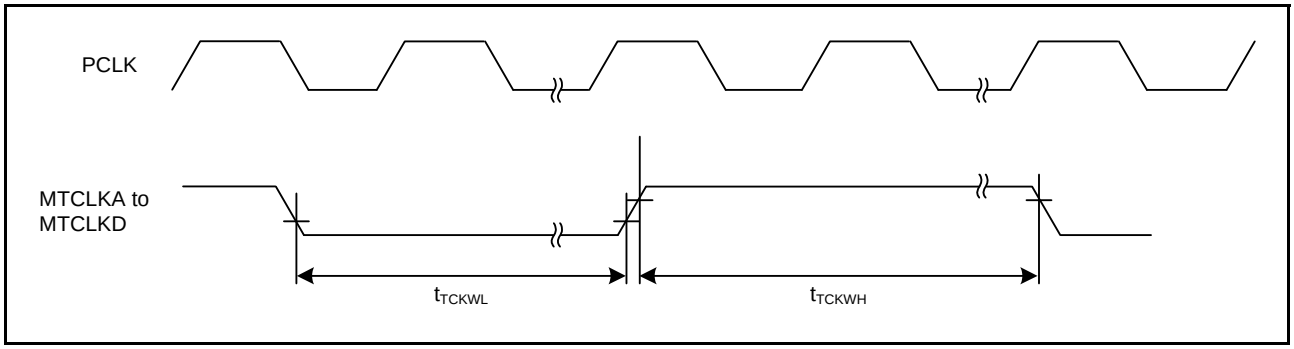


Figure 5.27 MTU2A Clock Input Timing

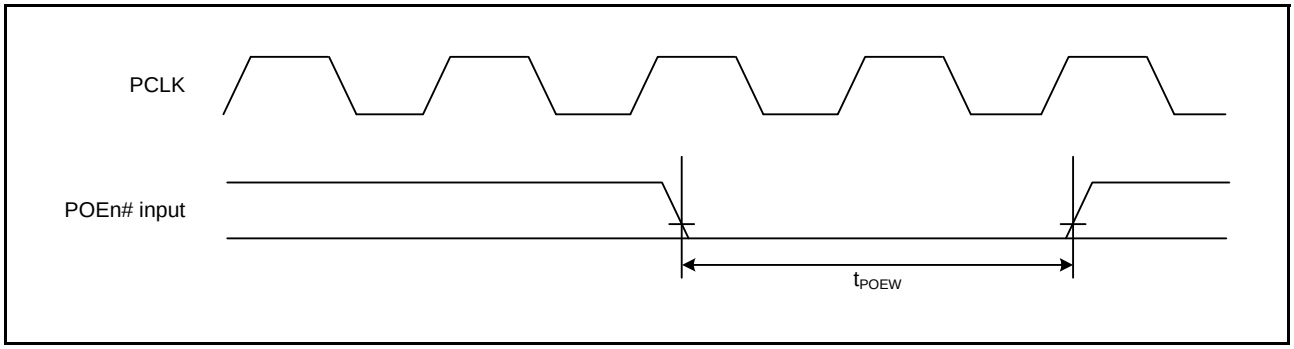


Figure 5.28 POE# Input Timing

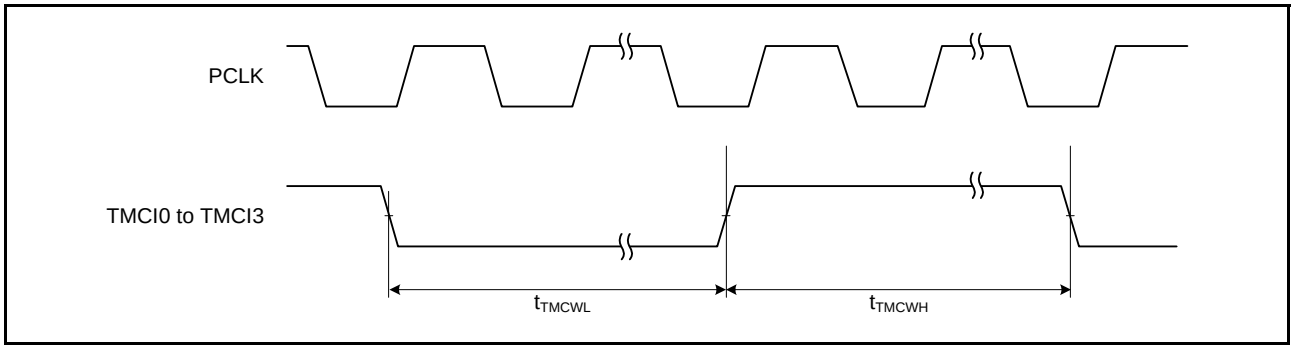


Figure 5.29 8-Bit Timer Clock Input Timing

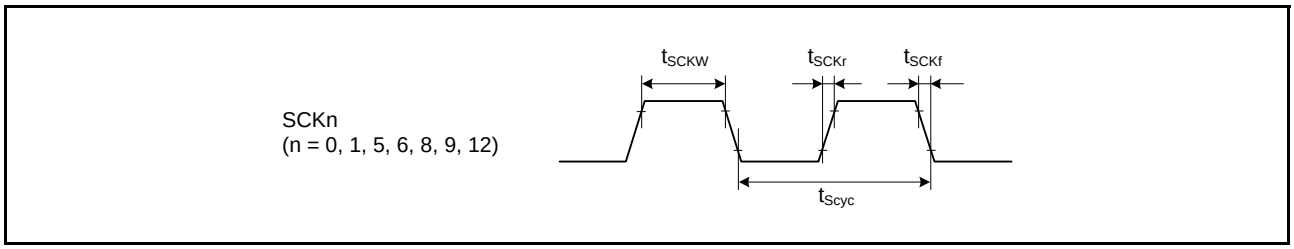


Figure 5.30 SCK Clock Input Timing

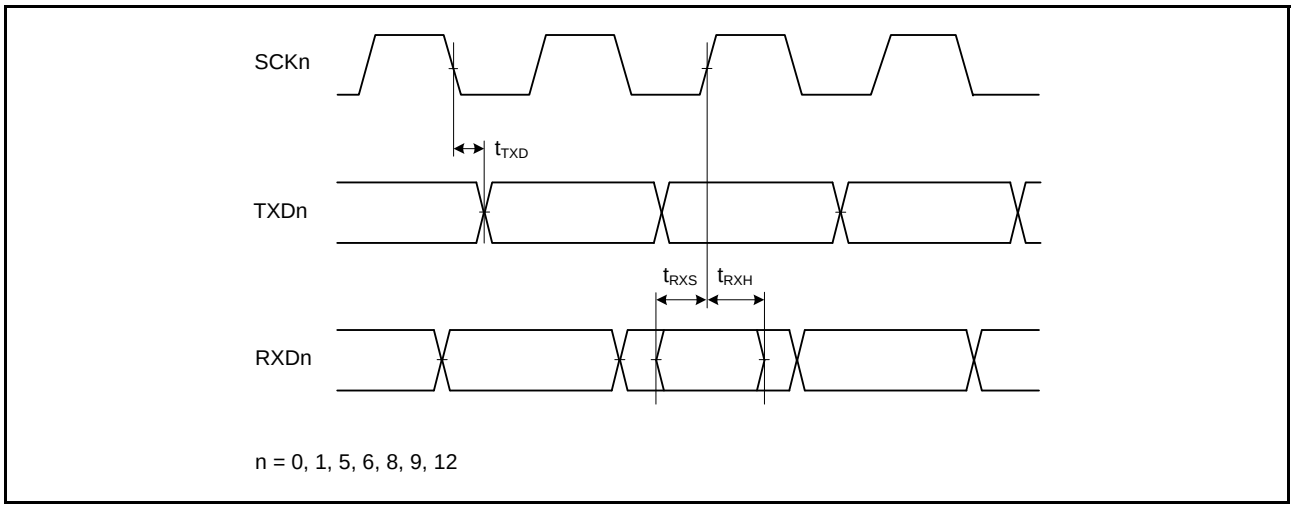


Figure 5.31 SCI Input/Output Timing: Clock Synchronous Mode

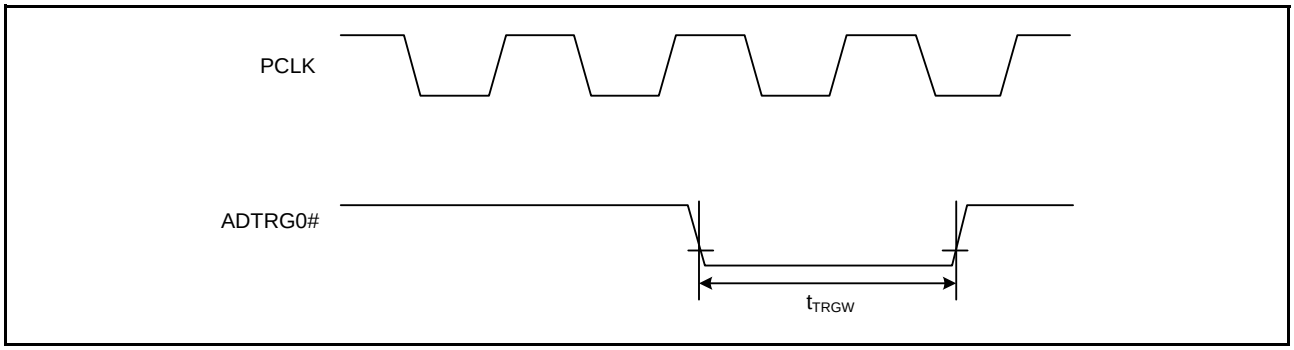


Figure 5.32 A/D Converter External Trigger Input Timing

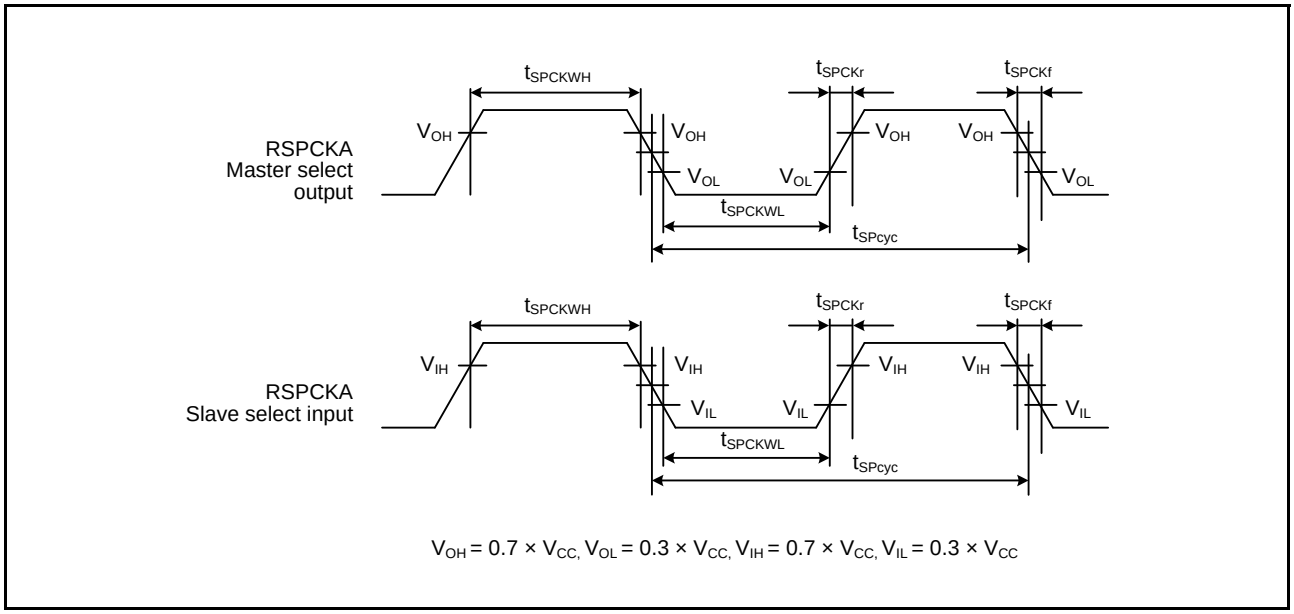


Figure 5.33 RSPI Clock Timing and Simple SPI Clock Timing

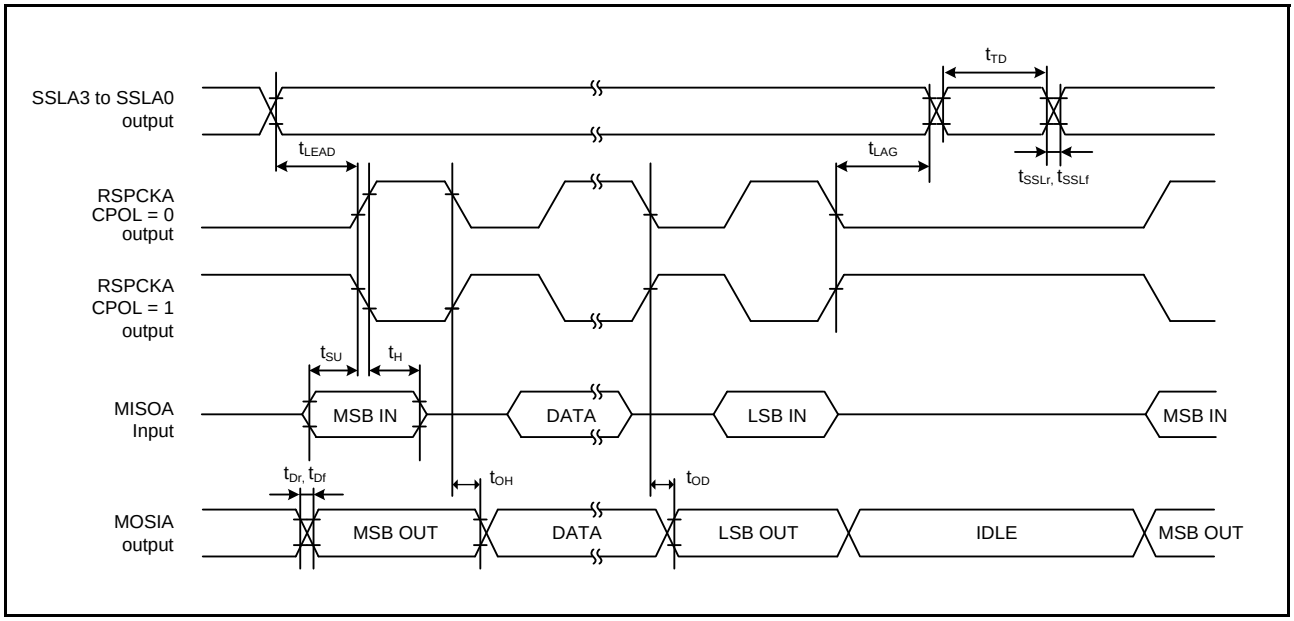


Figure 5.34 RSPI Timing (Master, CPHA = 0) and Simple SPI Timing (Master, CPHA = 0)

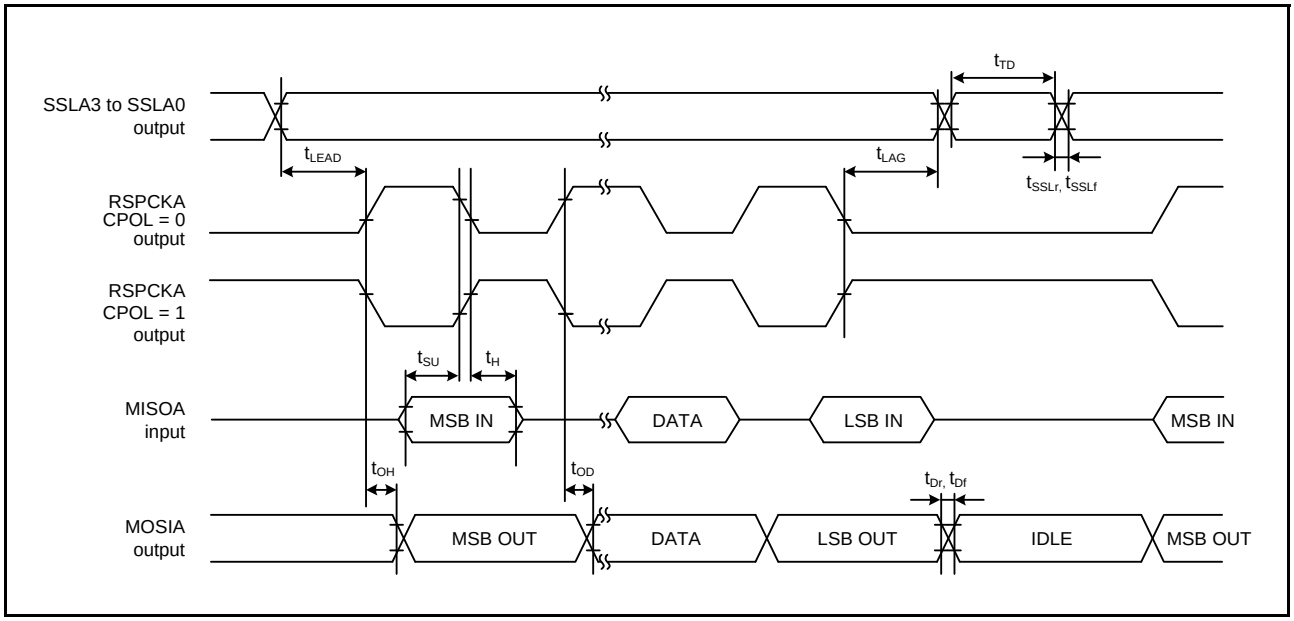


Figure 5.35 RSPI Timing (Master, CPHA = 1) and Simple SPI Timing (Master, CPHA = 1)

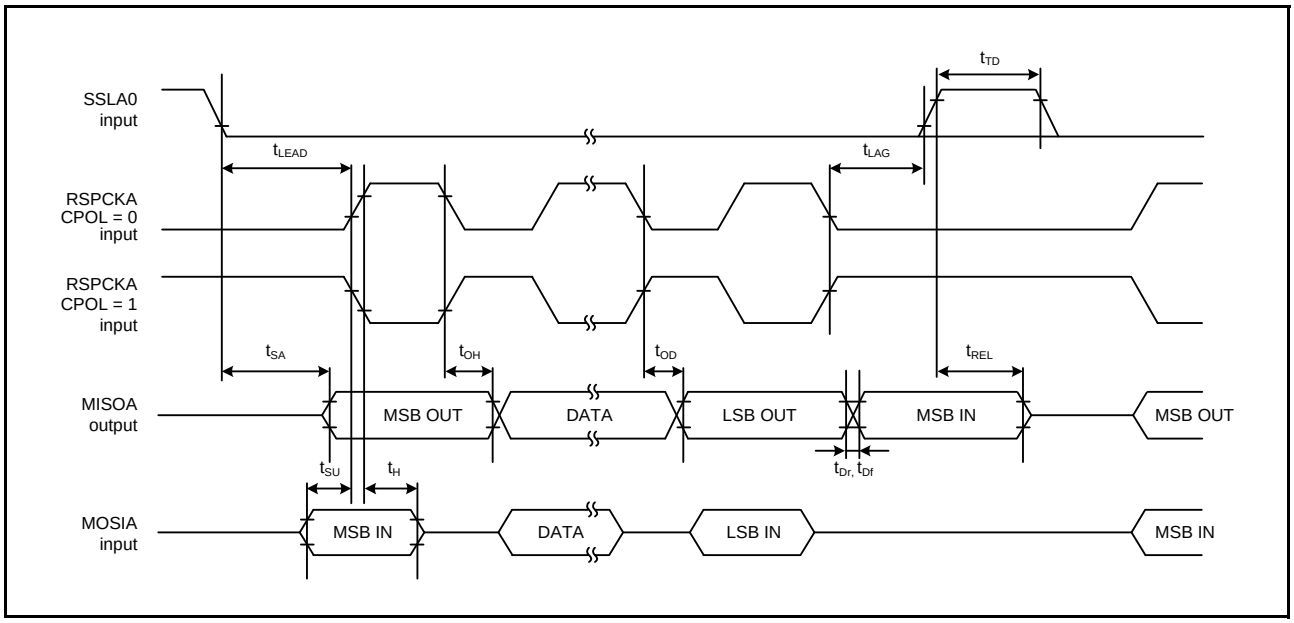


Figure 5.36 RSPI Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CPHA = 0)

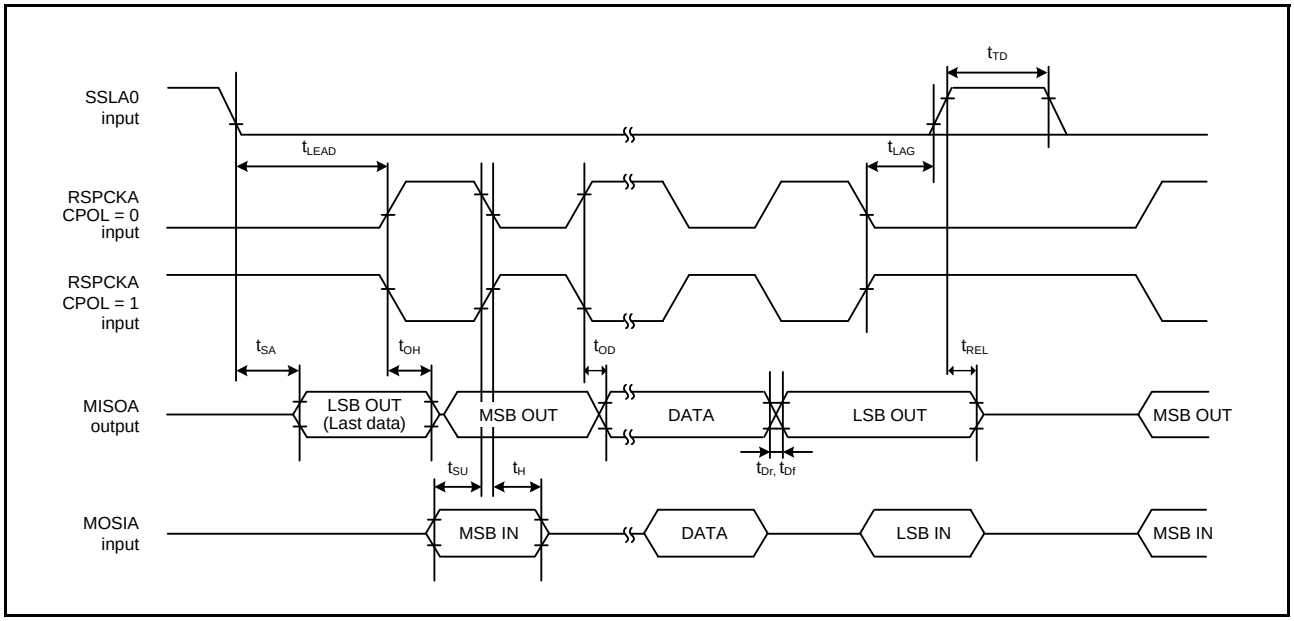
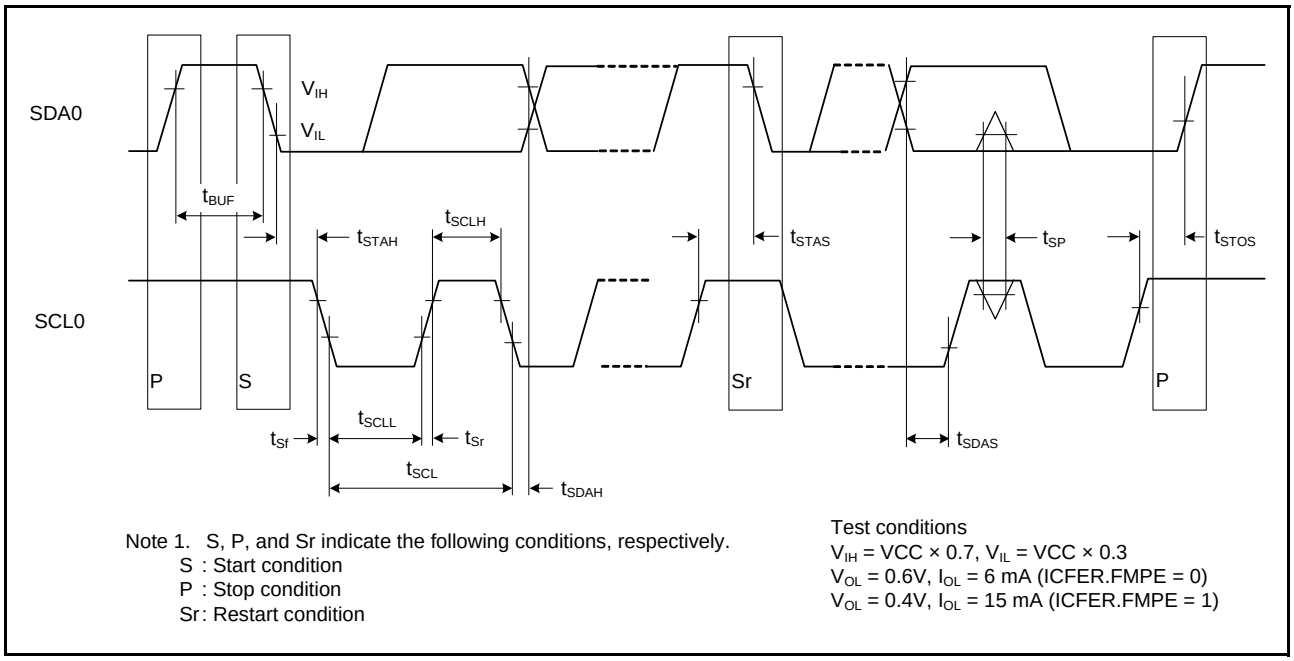


Figure 5.37 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CPHA = 1)



Note 1. S, P, and Sr indicate the following conditions, respectively.
S : Start condition
P : Stop condition
Sr: Restart condition

Test conditions
V_{IH} = VCC × 0.7, V_{IL} = VCC × 0.3
V_{OL} = 0.6V, I_{OL} = 6 mA (ICFER.FMPE = 0)
V_{OL} = 0.4V, I_{OL} = 15 mA (ICFER.FMPE = 1)

Figure 5.38 RIIC Bus Interface Input/Output Timing and Simple IIC Bus Interface Input/Output Timing

5.5 A/D Conversion Characteristics

Table 5.34 A/D Conversion Characteristics (1)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH = VREFH0 = (AVCC0 - 0.9 V) to AVCC0,
VSS = AVSS0 = VREFL = VREFL0 = 0 V, PCLKD = 1 to 50 MHz, T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit
Resolution		12	12	12	Bit	
Conversion time*1 (Operation at PCLK = 50 MHz)	Permissible signal source impedance (Max.) = 1 kΩ	T.B.D (T.B.D)*3	—	—	µs	Sampling in T.B.D states on a high-precision channel*4
	Permissible signal source impedance (Max.) = 1 kΩ	T.B.D (T.B.D)*3	—	—		Sampling in T.B.D states on a normal-precision channel*4
	Permissible signal source impedance (Max.) = 5 kΩ	T.B.D (T.B.D)*3	—	—		Sampling in T.B.D states on a high-precision channel*4
	Permissible signal source impedance (Max.) = 5 kΩ	T.B.D (T.B.D)*3	—	—		Sampling in T.B.D states on a normal-precision channel*4
Analog input capacitance		—	—	T.B.D	pF	
Offset error		—	T.B.D	T.B.D	LSB	
Full-scale error		—	T.B.D	T.B.D	LSB	
Quantization error		—	±0.5		LSB	
Absolute accuracy		—	T.B.D	±8*5	LSB	High-precision channel
		—	T.B.D	T.B.D*5	LSB	Normal-precision channel
DNL differential nonlinearity error		—	±2.0	T.B.D	LSB	
INL integral nonlinearity error		—	±2.0	T.B.D	LSB	

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.
Note 2. The scanning is not supported.
Note 3. The value in parentheses indicates the sampling time.
Note 4. Refer to the corresponding table for the types of channel.
Note 5. These are the characteristics when no pin function other than A/D converter input is in use.

Table 5.35 A/D Conversion Characteristics (2)

Conditions: VCC = AVCC0 = 1.8 to 2.7 V, VREFH = VREFH0 = (AVCC0 .0.9 V) to AVCC0,
VSS = AVSS0 = VREFL = VREFL0 = 0 V, PCLKD = 1 to 32 MHz, T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit
Resolution		12	12	12	Bit	
Conversion time*1 (Operation at PCLK = 32 MHz)	Permissible signal source impedance (Max.) = 1 kΩ	T.B.D (T.B.D)*3	—	—	µs	Sampling in T.B.D states on a high-precision channel*4
	Permissible signal source impedance (Max.) = 1 kΩ	T.B.D (T.B.D)*3	—	—		Sampling in T.B.D states on a normal-precision channel*4
	Permissible signal source impedance (Max.) = 5 kΩ	T.B.D (T.B.D)*3	—	—		Sampling in T.B.D states on a high-precision channel*4
	Permissible signal source impedance (Max.) = 5 kΩ	T.B.D (T.B.D)*3	—	—		Sampling in T.B.D states on a normal-precision channel*4
Analog input capacitance		—	—	T.B.D	pF	
Offset error		—	T.B.D	T.B.D	LSB	
Full-scale error		—	T.B.D	T.B.D	LSB	
Quantization error		—	±0.5		LSB	
Absolute accuracy		—	T.B.D	±8*5	LSB	High-precision channel
		—	T.B.D	T.B.D*5	LSB	Normal-precision channel
DNL differential nonlinearity error		—	±2.0	T.B.D	LSB	
INL integral nonlinearity error		—	T.B.D	T.B.D	LSB	

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.
Note 2. The scanning is not supported.
Note 3. The value in parentheses indicates the sampling time.
Note 4. Refer to the corresponding table for the types of channel.
Note 5. These are the characteristics when no pin function other than A/D converter input is in use.

Table 5.36 A/D Conversion Characteristics (3)

Conditions: VCC = AVCC0 = 1.62 to 1.8 V, VREFH = VREFH0 = (AVCC0 - T.B.D V) to AVCC0,
VSS = AVSS0 = VREFL = VREFL0 = 0 V, PCLKD = 1 to 16 MHz, T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit
Resolution		12	12	12	Bit	
Conversion time*1 (Operation at PCLK = 32 MHz)	Permissible signal source impedance (Max.) = 1 kΩ	T.B.D (T.B.D)*3	—	—	µs	Sampling in T.B.D states on a high-precision channel*4
	Permissible signal source impedance (Max.) = 1 kΩ	T.B.D (T.B.D)*3	—	—		Sampling in T.B.D states on a normal-precision channel*4
	Permissible signal source impedance (Max.) = 5 kΩ	T.B.D (T.B.D)*3	—	—		Sampling in T.B.D states on a high-precision channel*4
	Permissible signal source impedance (Max.) = 5 kΩ	T.B.D (T.B.D)*3	—	—		Sampling in T.B.D states on a normal-precision channel*4
Analog input capacitance		—	—	T.B.D	pF	
Offset error		—	T.B.D	T.B.D	LSB	
Full-scale error		—	T.B.D	T.B.D	LSB	
Quantization error		—	±0.5		LSB	
Absolute accuracy		—	T.B.D	±8*5	LSB	High-precision channel
		—	T.B.D	T.B.D*5	LSB	Normal-precision channel
DNL differential nonlinearity error		—	T.B.D	T.B.D	LSB	
INL integral nonlinearity error		—	±2.0	T.B.D	LSB	

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.
Note 2. The scanning is not supported.
Note 3. The value in parentheses indicates the sampling time.
Note 4. Refer to the corresponding table for the types of channel.
Note 5. These are the characteristics when no pin function other than A/D converter input is in use.

Table 5.37 Channel classification for A/D converter

Classification	Channel	Conditions
High-precision channel	AN003 to AN007	AVCC0 = 1.62 to 5.5 V
	AN000, AN001, AN002	AVCC0 = 2.7 to 5.5 V, when the sample and hold circuit is in use.
		AVCC0 = 1.62 to 5.5 V, when the sample and hold circuit is not in use.
Normal-precision channel	AN008 to AN015	AVCC0 = 1.62 to 5.5 V

5.6 D/A Conversion Characteristics

Table 5.38 D/A Conversion Characteristics (1)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH = VREFH0 = 2.7 V to AVCC0,
VSS = AVSS0 = VREFL = VREFL0 = 0 V, PCLKB = up to 32 MHz, T_a = –40 to +85°C

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	10	10	10	Bit	
Conversion time	—	—	3.0	µs	20-pF capacitive load
Absolute accuracy	—	T.B.D	±4.0	LSB	4-MΩ resistive load
	—	—	T.B.D	LSB	8-MΩ resistive load
RO output resistance	—	T.B.D	—	kΩ	

Table 5.39 D/A Conversion Characteristics (2)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH = VREFH0 = 1.8 V to AVCC0,
VSS = AVSS0 = VREFL = VREFL0 = 0 V, PCLKB = up to 32 MHz, T_a = –40 to +85°C

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	10	10	10	Bit	
Conversion time	—	—	10.0	µs	20-pF capacitive load
Absolute accuracy	—	T.B.D	±4.0	LSB	4-MΩ resistive load
	—	—	T.B.D	LSB	8-MΩ resistive load
RO output resistance	—	T.B.D	—	kΩ	

5.7 Temperature Sensor Characteristics

Table 5.40 Temperature Sensor Characteristics

Conditions: VVCC = AVCC0 = 1.8 to 5.5 V, VREFH = VREFH0 = (AVCC0 - 0.9 V) to AVCC0,
VSS = AVSS0 = VREFL = VREFL0 = 0V, T_a = –40 to +85°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
Relative accuracy		—	T.B.D	—	°C	
Temperature slope		—	T.B.D	—	mV/°C	
Output voltage (@25°C)	VCC = 3.6 to 5.5 V	—	T.B.D	—	V	
	VCC = 2.7 to 3.6 V	—	T.B.D	—		
	VCC = 1.8 to 2.7 V	—	T.B.D	—		
Temperature sensor start time		—	—	T.B.D	µs	
Sampling time		T.B.D	70	T.B.D	µs	

5.8 Comparator Characteristics

Table 5.41 Comparator Characteristics

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0V, PCLKB = up to 32 MHz,
T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Comparator A	External standard voltage input range	LVREF	1.4	—	VCC	V	
	External comparison voltage (CMPA1, CMPA2) input range	VI	–0.3	—	VCC + 0.3	V	
	Internal standard voltage	—	T.B.D	T.B.D	T.B.D	V	
	Offset	—	—	±50	T.B.D	mV	
	Comparator output delay time	—	—	3	—	µs	At falling edge VI = LVREF – 100 mV
			—	1.5	—	µs	At falling edge VI = LVREF < 1 V
			—	2	—	µs	At rising edge VI = LVREF + 100 mV
			—	0.5	—	µs	At rising edge VI > LVREF + 1 V
	Comparator operating currrent	ICMPA	—	0.5	—	µA	
Comparator B	Input standard voltage for CVREFB0, CVREFB1	VREF	0	—	VCC – 1.4	V	
	Input standard voltage for CMPB0, CMPB1	VI	–0.3	—	VCC + 0.3	V	
	Offset	—	—	—	±50	mV	
	Comparator output delay time	td	—	—	1	µs	VI = VREF + 100 mV
	Comparator operating current	ICMPB	—	75	150	µA	VCC = 5.0 V For total two channels

Note 1. When the digital filter is disabled.

5.9 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Table 5.42 Power-on Reset Circuit and Voltage Detection Circuit Characteristics(1)

Conditions: VCC = AVCC, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	Low power consumption function disabled	V_{POR}	T.B.D	T.B.D	T.B.D	V	Figure 5.39
		Low power consumption function enabled		T.B.D	T.B.D	T.B.D		
	Voltage detection circuit (LVD0)		V_{det0_0}	T.B.D	1.72	T.B.D	V	Figure 5.40
			V_{det0_1}	T.B.D	1.90	T.B.D		
			V_{det0_2}	T.B.D	2.85	T.B.D		
			V_{det0_3}	T.B.D	3.80	T.B.D		
	Voltage detection circuit (LVD1)		V_{det1_0}	T.B.D	4.15	T.B.D	V	Figure 5.41
			V_{det1_1}	T.B.D	4.00	T.B.D		
			V_{det1_2}	T.B.D	3.85	T.B.D		
			V_{det1_3}	T.B.D	3.70	T.B.D		
			V_{det1_4}	T.B.D	3.55	T.B.D		
			V_{det1_5}	T.B.D	3.40	T.B.D		
			V_{det1_6}	T.B.D	3.25	T.B.D		
			V_{det1_7}	T.B.D	3.10	T.B.D		
			V_{det1_8}	T.B.D	2.95	T.B.D		
			V_{det1_9}	T.B.D	2.80	T.B.D		
			V_{det1_A}	T.B.D	2.65	T.B.D		
			V_{det1_B}	T.B.D	2.50	T.B.D		
			V_{det1_C}	T.B.D	2.35	T.B.D		
			V_{det1_D}	T.B.D	2.20	T.B.D		
			V_{det1_E}	T.B.D	2.05	T.B.D		
			V_{det1_F}	T.B.D	1.90	T.B.D		

Table 5.43 Power-on Reset Circuit and Voltage Detection Circuit Characteristics (2)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, PCLKB = up to 32 MHz,
T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Voltage detection circuit (LVD2)	V_{det2_0}	T.B.D	4.15	T.B.D	V	Figure 5.42
		V_{det2_1}	T.B.D	4.00	T.B.D		
		V_{det2_2}	T.B.D	3.85	T.B.D		
		V_{det2_3}	T.B.D	3.70	T.B.D		
		V_{det2_4}	T.B.D	3.55	T.B.D		
		V_{det2_5}	T.B.D	3.40	T.B.D		
		V_{det2_6}	T.B.D	3.25	T.B.D		
		V_{det2_7}	T.B.D	3.10	T.B.D		
		V_{det2_8}	T.B.D	2.95	T.B.D		
		V_{det2_9}	T.B.D	2.80	T.B.D		
		V_{det2_A}	T.B.D	2.65	T.B.D		
		V_{det2_B}	T.B.D	2.50	T.B.D		
		V_{det2_C}	T.B.D	2.35	T.B.D		
		V_{det2_D}	T.B.D	2.20	T.B.D		
		V_{det2_E}	T.B.D	2.05	T.B.D		
		V_{det2_F}	T.B.D	1.90	T.B.D		
		V_{det2_EXT}	T.B.D	T.B.D	T.B.D		
Internal reset time	Power-on reset time	t_{POR}	—	T.B.D	—	ms	Figure 5.39
	LVD0 reset time	t_{LVD0}	—	T.B.D	—		Figure 5.40
	LVD1 reset time	t_{LVD1}	—	T.B.D	—		Figure 5.41
	LVD2 reset time	t_{LVD2}	—	T.B.D	—		Figure 5.42
Minimum VCC down time*1		t_{VOFF}	T.B.D	—	—	µs	Figure 5.39
Response delay time		t_{det}	—	—	150	µs	Figure 5.39
LVD operation stabilization time (after LVD is enabled)		$Td_{(E-A)}$	—	—	100	µs	Figure 5.41
Hysteresis width (LVD1 and LVD2)		V_{LVH}	—	100	—	mV	When selection is from among VdetX_0 to 5.
			—	70	—		When selection is from among VdetX_6 to F.

Note 1. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det1}, and V_{det2} for the POR/ LVD.

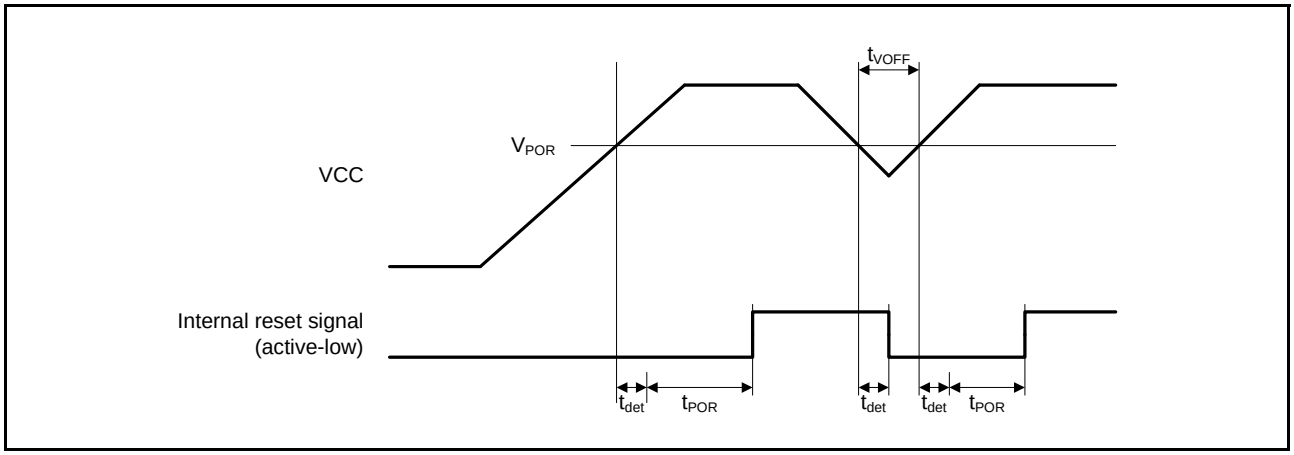


Figure 5.39 Power-on Reset Timing

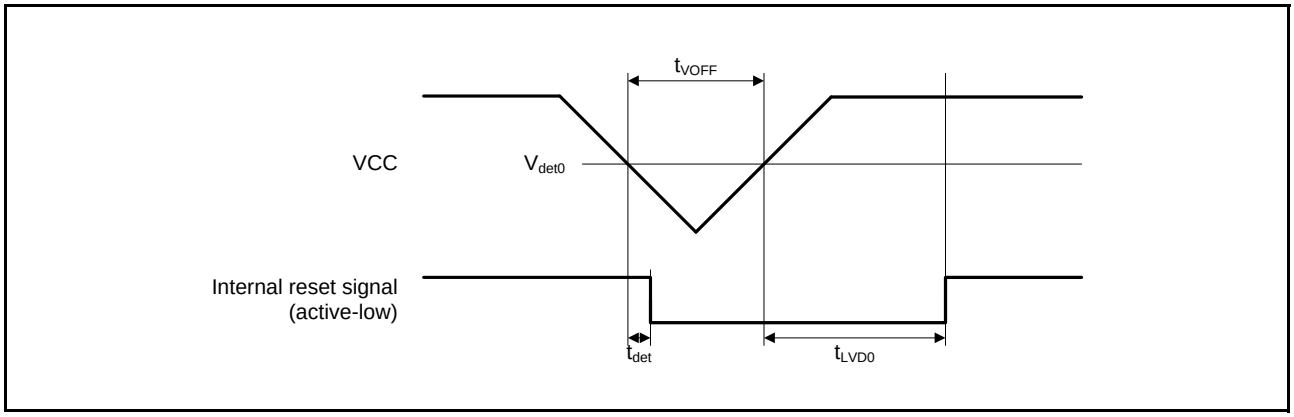


Figure 5.40 Voltage Detection Circuit Timing (V_{det0})

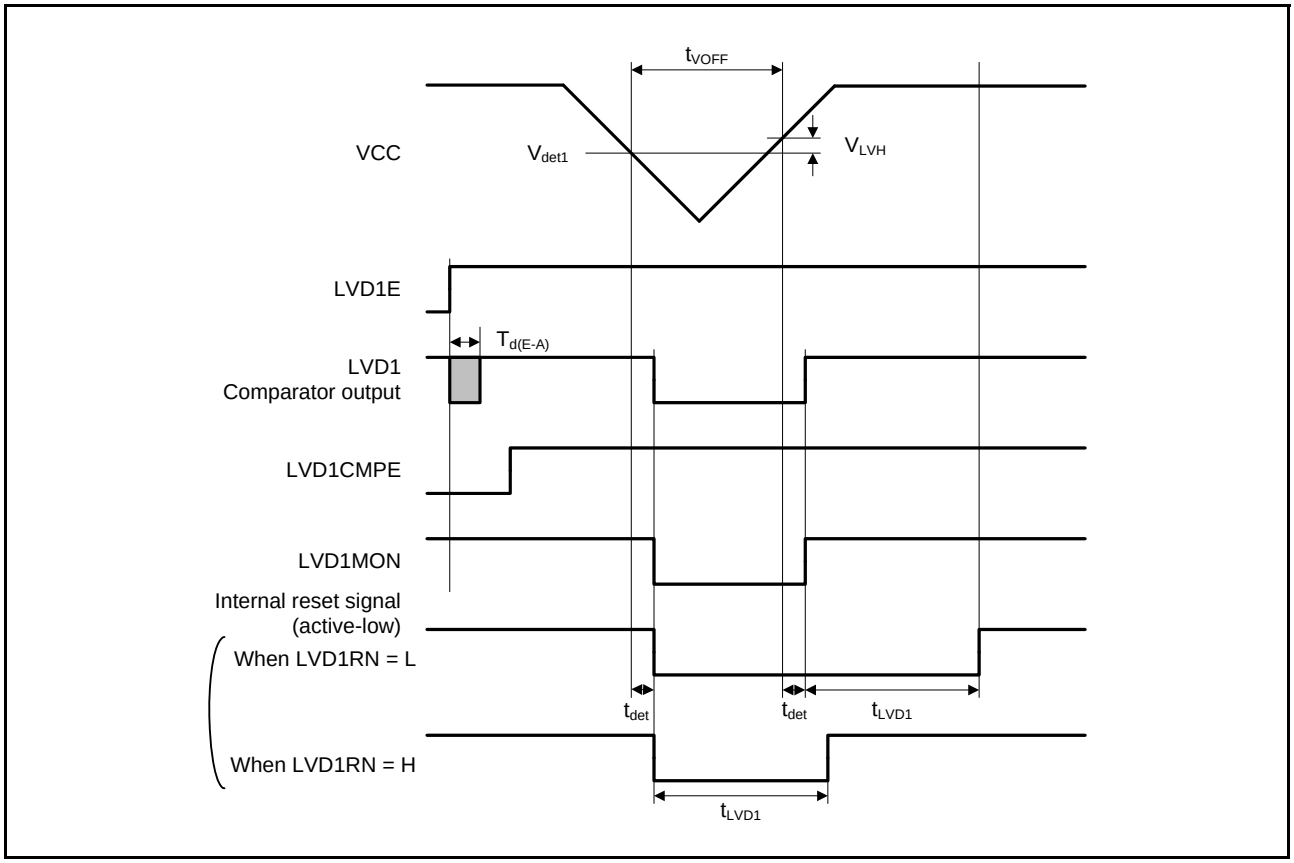


Figure 5.41 Voltage Detection Circuit Timing (V_{det1})

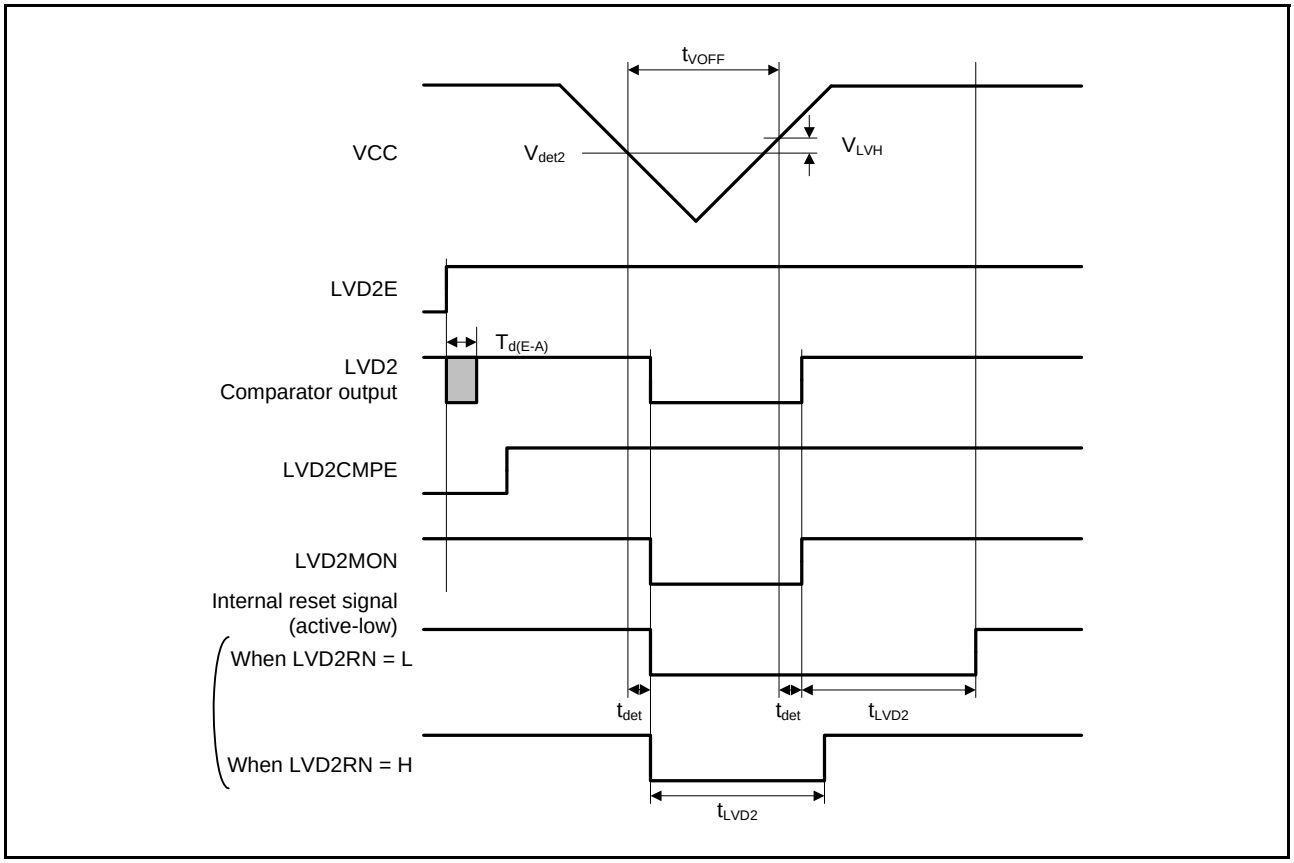


Figure 5.42 Voltage Detection Circuit Timing (V_{det2})

5.10 Oscillation Stop Detection Timing

Table 5.44 Oscillation Stop Detection Circuit Characteristics

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	T.B.D	ms	Figure 5.43

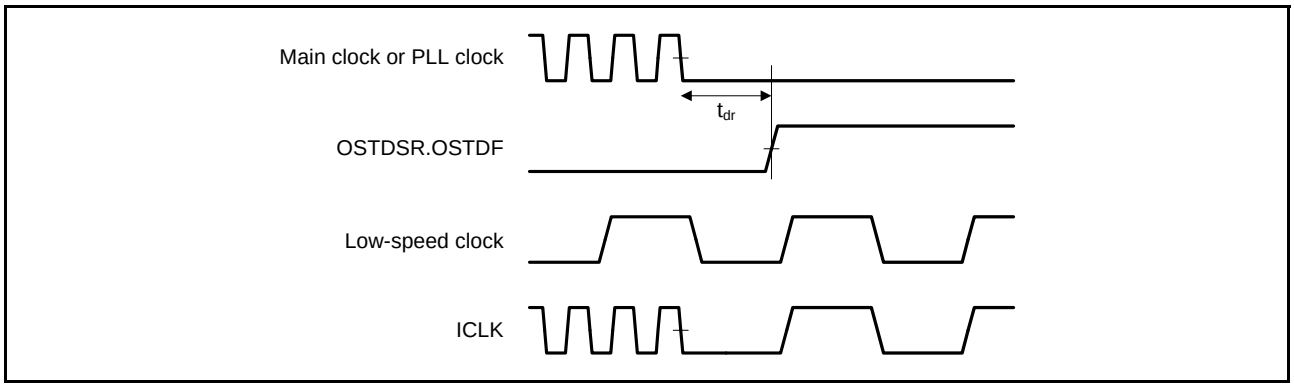


Figure 5.43 Oscillation Stop Detection Timing

5.11 ROM (Flash Memory for Code Storage) Characteristics

Table 5.45 ROM (Flash Memory for Code Storage) Characteristics (1)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Reprogramming/erasure cycle*1	N_{PEC}	1000	—	—	Times	
Data hold time*2	t_{DRP}	10	—	—	Year	
FCU reset time	t_{FCUR}	T.B.D	—	—	µs	

Note 1. Definition of reprogram/erase cycle: The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 128-byte programming is performed 16 times for different addresses in 2-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. This indicates the characteristic when reprogram is performed within the specification range including the minimum number.

Table 5.46 ROM (Flash Memory for Code Storage) Characteristics (2) : high-speed operating mode, medium-speed operating mode A

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH = VREFH0 = AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V
Temperature range for the programming/erasure operation: T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Programming time	2 bytes	t_{P2}	—	0.5	2.5	ms	FCLK = 32 MHz $N_{PEC} \leq 100$
	8 bytes	t_{P8}	—	0.5	2.5		
	128 bytes	t_{P128}	—	1.0	4.8		
	2 bytes	t_{P2}	—	T.B.D	3.0	ms	FCLK = 32 MHz $N_{PEC} > 100$
	8 bytes	t_{P8}	—	T.B.D	3.2		
	128 bytes	t_{P128}	—	T.B.D	6.0		
Erasure time	2 Kbytes	t_{E2K}	—	15	T.B.D	ms	FCLK = 32 MHz $N_{PEC} \leq 100$
	2 Kbytes	t_{E2K}	—	T.B.D	T.B.D	ms	FCLK = 32 MHz $N_{PEC} > 100$
Suspend delay time during programming (in programming/erasure priority mode)		t_{SPD}	—	—	0.8	ms	Figure 5.44 FCLK = 32 MHz
First suspend delay time during programming (in suspend priority mode)		t_{SPSD1}	—	—	120	µs	
Second suspend delay time during programming (in suspend priority mode)		t_{SPSD2}	—	—	0.8	ms	
Suspend delay time during erasing (in programming/erasure priority mode)		t_{SED}	—	—	0.8	ms	
First suspend delay time during erasing (in suspend priority mode)		t_{SESD1}	—	—	120	µs	
Second suspend delay time during erasing (in suspend priority mode)		t_{SESD2}	—	—	0.8	ms	

Table 5.47 ROM (Flash Memory for Code Storage) Characteristics (3) : medium-speed operating mode B

Conditions: VCC = AVCC0 = 1.62 to 3.6 V, VREFH = VREFH0 = AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V
Temperature range for the programming/erasure operation: T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Programming time*1	2 bytes	t_{P2}	—	0.8	3.5	ms	FCLK = 32 MHz $N_{PEC} \leq 100$
	8 bytes	t_{P8}	—	0.8	3.5		
	128 bytes	t_{P128}	—	1.6	8.3		
	2 bytes	t_{P2}	—	T.B.D	4.2	ms	FCLK = 32 MHz $N_{PEC} > 100$
	8 bytes	t_{P8}	—	T.B.D	4.5		
	128 bytes	t_{P128}	—	T.B.D	10		
Erasure time	2 bytes	t_{E2K}	—	32	T.B.D	ms	FCLK = 32 MHz $N_{PEC} \leq 100$
	2 bytes	t_{E2K}	—	T.B.D	T.B.D	ms	FCLK = 32 MHz $N_{PEC} > 100$
Suspend delay time during programming (in programming/erasure priority mode)		t_{SPD}	—	—	1.6	ms	Figure 5.44 FCLK = 32 MHz*1
First suspend delay time during programming (in suspend priority mode)		t_{SPSD1}	—	—	120	µs	
Second suspend delay time during programming (in suspend priority mode)		t_{SPSD2}	—	—	1.6	ms	
Suspend delay time during erasing (in programming/erasure priority mode)		t_{SED}	—	—	1.6	ms	
First suspend delay time during erasing (in suspend priority mode)		t_{SESD1}	—	—	120	µs	
Second suspend delay time during erasing (in suspend priority mode)		t_{SESD2}	—	—	1.6	ms	

Note 1. The operating frequency is 20 MHz (max.) when the voltage is in the range from 1.62 V to less than 1.8 V.

5.12 E^2 Flash Characteristics

Table 5.48 E^2 Data Flash Characteristics (1)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Reprogramming/erasure cycle	N_{DPEC}	100000	—	—	Times	
Data hold time	t_{DRP}	10	—	—	Year	

Note 1. The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 100000), erasing can be performed n times for each block. For instance, when 8-byte programming is performed 16 times for different addresses in 128-byte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).
Note 2. This indicates the characteristics when reprogram is performed within the specification range including the minimum number.

Table 5.49 E^2 Data Flash Characteristics (2) : high-speed operating mode, medium-speed operating mode A

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH = VREFH0 = AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0V
Temperature range for the programming/erasure operation: T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Programming time*1	2 bytes	t_{P2}	—	0.3	2.0	ms	FCLK = 32 MHz $N_{PEC} \leq 100$
	8 bytes	t_{P8}	—	0.4	2.2		
	2 bytes	t_{P2}	—	T.B.D	3.0	ms	FCLK = 32 MHz $N_{PEC} > 100$
	8 bytes	t_{P8}	—	T.B.D	3.2		
Erasure time	128 bytes	t_{E2K}	—	4.5	T.B.D	ms	FCLK = 32 MHz $N_{PEC} \leq 100$
	128 bytes	t_{E2K}	—	T.B.D	T.B.D	ms	FCLK = 32 MHz $N_{PEC} > 100$
Blank check time	2 bytes	t_{BC2}	—	—	35	µs	FCLK = 32 MHz
	2 Kbytes	t_{BC2K}	—	—	2.5	ms	
Suspend delay time during programming (in programming/erasure priority mode)		t_{SPD}	—	—	0.8	ms	Figure 5.44 FCLK = 32 MHz
First suspend delay time during programming (in suspend priority mode)		t_{SPSD1}	—	—	120	µs	
Second suspend delay time during programming (in suspend priority mode)		t_{SPSD2}	—	—	0.8	ms	
Suspend delay time during erasing (in programming/erasure priority mode)		t_{SED}	—	—	0.8	ms	
First suspend delay time during erasing (in suspend priority mode)		t_{SESD1}	—	—	120	µs	
Second suspend delay time during erasing (in suspend priority mode)		t_{SESD2}	—	—	0.8	ms	

Table 5.50 E^2 Data Flash Characteristics (3)
3): medium-speed operating mode B

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH = VREFH0 = AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0V
Temperature range for the programming/erasure operation: T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Programming time*1	2 bytes	t_{P2}	—	0.6	2.8	ms	FCLK = 32 MHz $N_{PEC} \leq 100$
	8 bytes	t_{P8}	—	0.6	3.2		
	2 bytes	t_{P2}	—	T.B.D	4.2	ms	FCLK = 32 MHz $N_{PEC} > 100$
	8 bytes	t_{P8}	—	T.B.D	4.5		
Erasure time	128 bytes	t_{E2K}	—	7	T.B.D	ms	FCLK = 32 MHz $N_{PEC} \leq 100$
	128 bytes	t_{E2K}	—	T.B.D	T.B.D	ms	FCLK = 32 MHz $N_{PEC} > 100$
Blank check time	2 bytes	t_{BC2}	—	—	40		FCLK = 32 MHz*1
	2 Kbytes	t_{BC2K}	—	—	2.6		
Suspend delay time during programming (in programming/erasure priority mode)		t_{SPD}	—	—	1.6	ms	Figure 5.44 FCLK = 32 MHz*1
First suspend delay time during programming (in suspend priority mode)		t_{SPSD1}	—	—	120	µs	
Second suspend delay time during programming (in suspend priority mode)		t_{SPSD2}	—	—	1.6	ms	
Suspend delay time during erasing (in programming/erasure priority mode)		t_{SED}	—	—	1.6	ms	
First suspend delay time during erasing (in suspend priority mode)		t_{SESD1}	—	—	12	µs	
Second suspend delay time during erasing (in suspend priority mode)		t_{SESD2}	—	—	1.6	ms	

Note 1. The operating frequency is 20 MHz (max.) when the voltage is in the range from 1.62 V to less than 1.8 V.

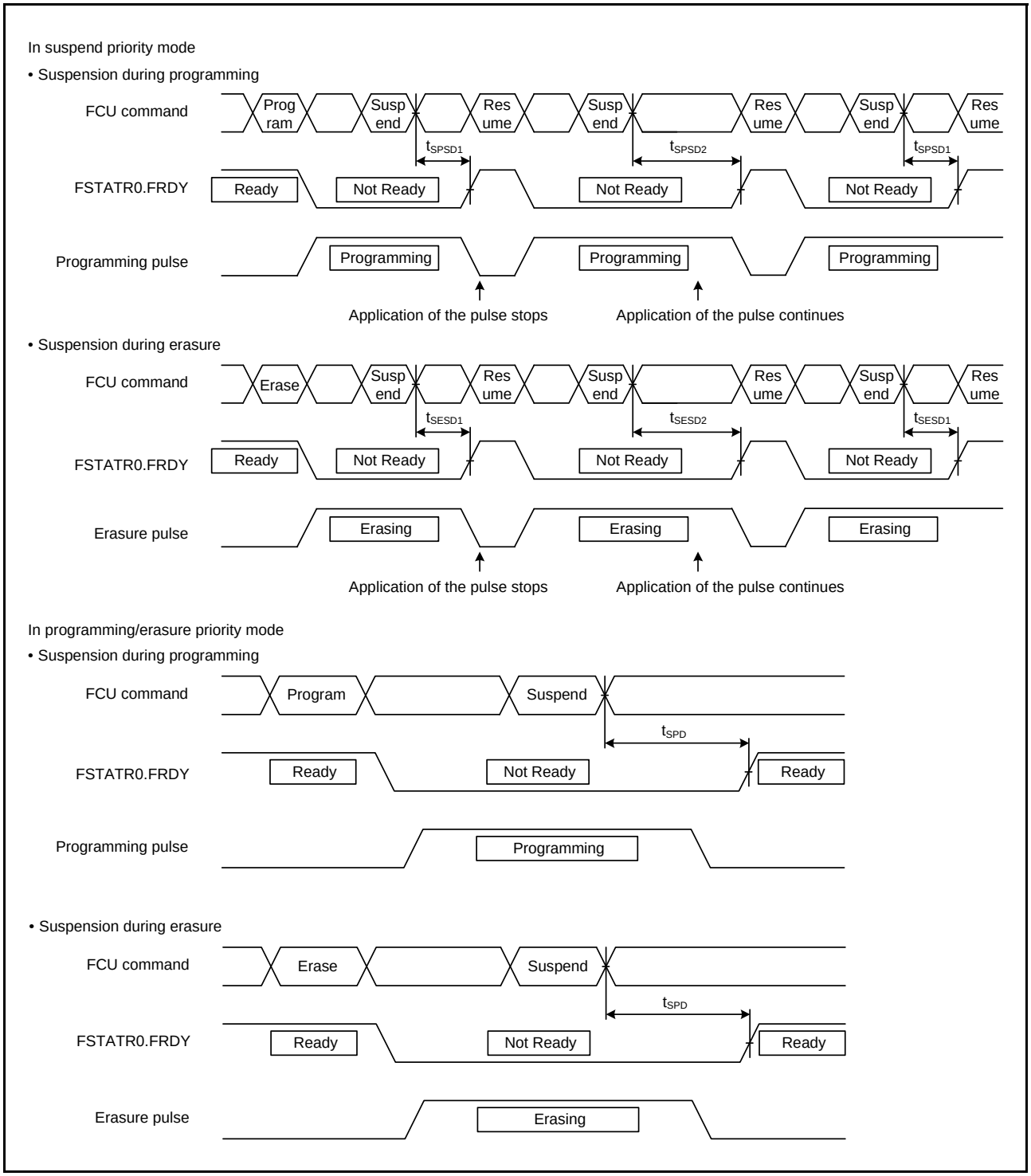
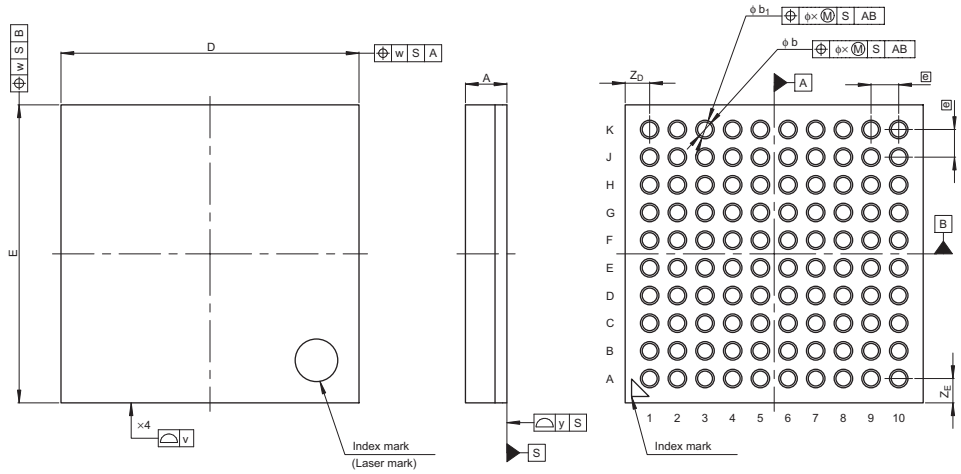


Figure 5.44 Flash Memory Program/Erase Suspend Timing

Appendix 1.Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation. website.

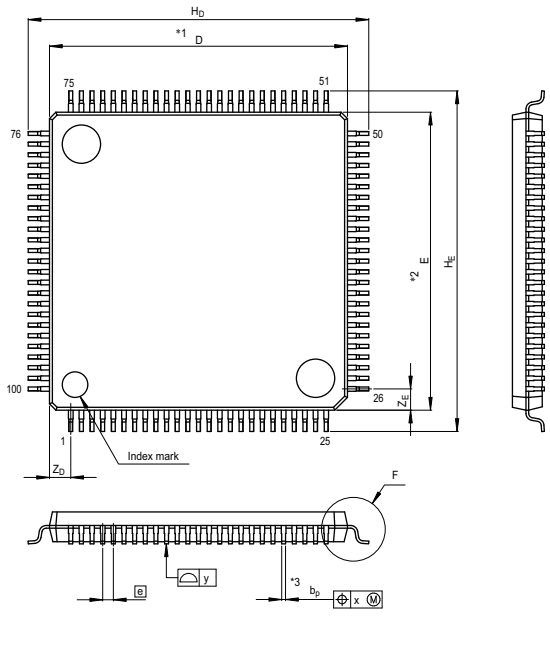
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TFLGA100-7x7-0.65	PTLG0100JA-A	100F0G	0.1g

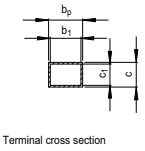


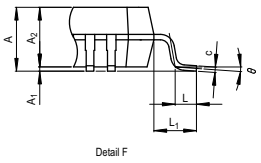
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	7.0	—
E	—	7.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.05
e	—	0.65	—
b	0.31	0.35	0.39
b_1	0.385	0.435	0.485
x	—	—	0.08
y	—	—	0.10
Z_D	—	0.575	—
Z_E	—	0.575	—

Figure A 100-Pin TFLGA (PTLG0100JA-A)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP100-14x14-0.50	PLQP0100KB-A	100P6Q-A / FP-100U / FP-100UV	0.6g





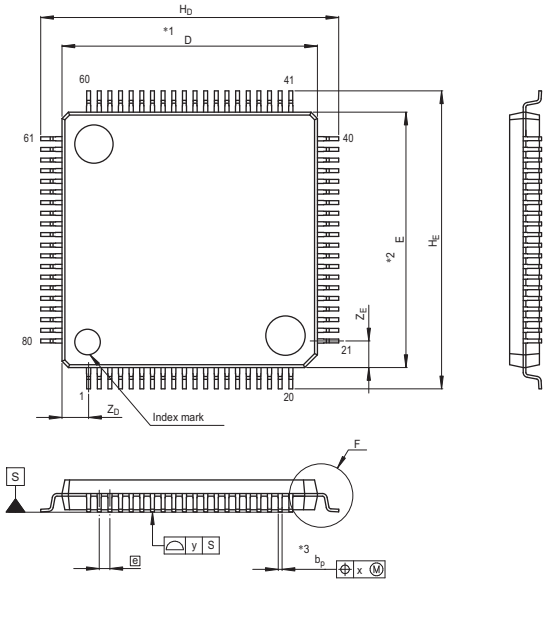


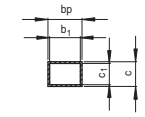
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.35	0.5	0.65
L_1	—	1.0	—

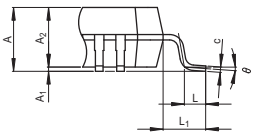
Figure B 100-Pin LQFP (PLQP0100KB-A)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP80-12x12-0.50	PLQP0080KB-A	80P6Q-A	0.5g





Terminal cross section



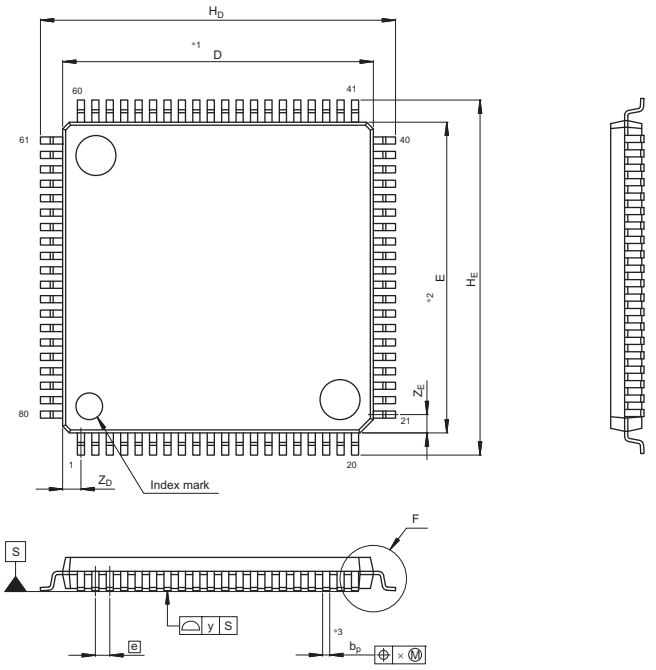
Detail F

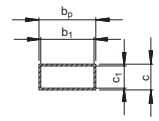
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	11.9	12.0	12.1
E	11.9	12.0	12.1
A_2	—	1.4	—
H_D	13.8	14.0	14.2
H_E	13.8	14.0	14.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	10°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.3	0.5	0.7
L_1	—	1.0	—

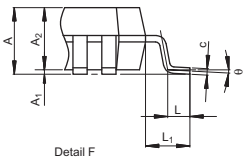
Figure C 80-Pin LQFP (PLQP0080KB-A)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP80-14x14-0.65	PLQP0080JA-A	FP-80W / FP-80WV	0.6g





Terminal cross section



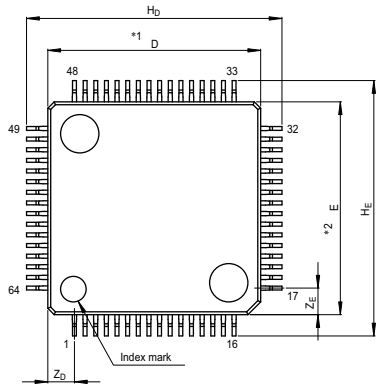
Detail F

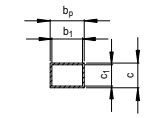
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.27	0.32	0.37
b_1	—	0.30	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z_D	—	0.825	—
Z_E	—	0.825	—
L	0.35	0.5	0.65
L_1	—	1.0	—

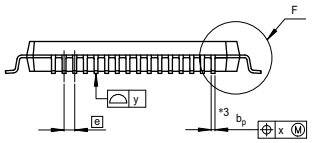
Figure D 80-Pin LQFP (PLQP0080JA-A)

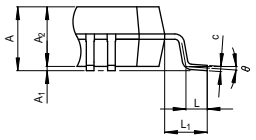
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP64-10x10-0.50	PLQP0064KB-A	64P6Q-A / FP-64K / FP-64KV	0.3g





Terminal cross section





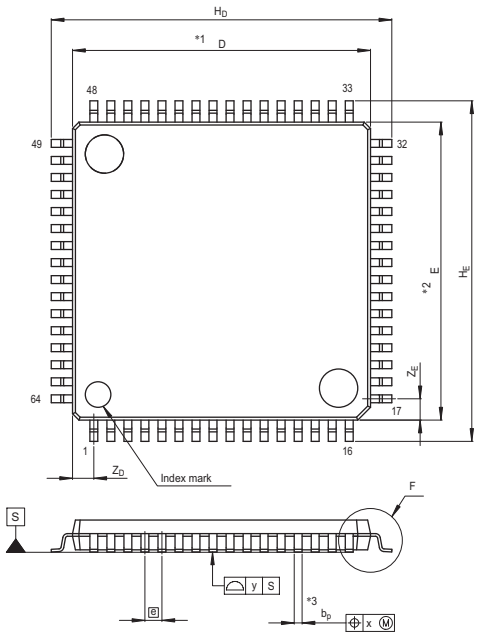
Detail F

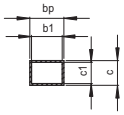
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

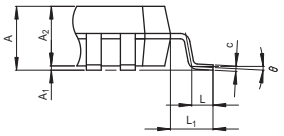
Figure E 64-Pin LQFP (PLQP0064KB-A)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP64-14x14-0.80	PLQP0064GA-A	64P6U-A/ —	0.7g





Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.32	0.37	0.42
b_1	—	0.35	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.8	—
x	—	—	0.20
y	—	—	0.10
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.3	0.5	0.7
L_1	—	1.0	—

Figure F 64-Pin LQFP (PLQP0064GA-A)

REVISION HISTORY	RX210 Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.50	Apr.15, 2011	—	First edition, issued
0.90	Aug.10, 2011	1. Overview	
		4	Table 1.1 Outline of Specifications: Power supply voltage/ Operating frequency, changed
		17, 21, 24, 26	Table 1.5 to Table 1.8 List of Pins and Pin Functions (Pin name: LVCMP2 → CMPA2), changed
		2. CPU	
		51	Table 2.14 Instructions that are Converted into Multiple Micro-Operations (multiplier: 32 × 32 → 64 bits), (memory source operand), added
		4. I/O Registers	
		63	Table 5.1 List of I/O Registers (Address Order), SOSCWTCR, LOCOWTCR2, HOCOWTCR2, added
		114 to 116	Table 5.1 List of I/O Registers (Address Order): Interrupt source priority register, changed
		5. Electrical Characteristics	
		85 to 137	Newly added

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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