REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update drawing to current requirements. Editorial changes throughout. - drw	04-01-27	Raymond Monnin

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

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REV STATUS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A	
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	

PMIC N/A

PREPARED BY
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Raymond Monnin

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
88-05-10

MICROCIRCUIT, LINEAR, CMOS, DUAL 12-BIT, DIGITAL-TO-ANALOG CONVERTER, MONOLITHIC SILICON

REVISION LEVEL	SIZE	CAGE CODE	
A	A	**67268**	**5962-87763**

SHEET 1 OF 13

DSCC FORM 2233
APR 97

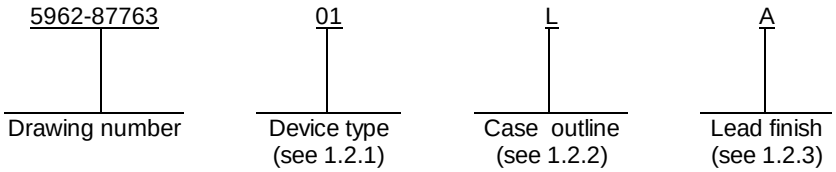
5962-E115-04

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device types. The device types identify the circuit function as follows:

Device type	Generic number	Circuit function
01	7537S	8 + 4 loading structure, dual 12-bit CMOS D/A converter, 11-bit linearity, ±6 LSB's of gain error
02	7537T	8 + 4 loading structure, dual 12-bit CMOS D/A converter, 12-bit linearity, ±3 LSB's of gain error
03	7537U	8 + 4 loading structure, dual 12-bit CMOS D/A converter, 12-bit linearity, ±2 LSB's of gain error

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
L	GDIP3-T24 or CDIP4-T24	24	Dual-in-line
3	CQCC1-N28	28	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

V_{DD} to DGND ..... -0.3 V, +17 V
V_{REFA}, V_{REFB} to AGNDA, AGNDB..... ±25 V
V_{RFBA}, V_{RFBB} to AGNDA, AGNDB..... ±25 V
Digital input voltage to DGND ..... -0.3 V, V_{DD} +0.3 V
V_{IOUTA}, V_{IOUTB} to DGND..... -0.3 V, V_{DD} +0.3 V
AGNDA, AGNDB to DGND ..... -0.3 V, V_{DD} +0.3 V
Power dissipation:
  Up to +75°C ..... 450 mW
  Derate above +75°C ..... 6 mW/°C
Lead temperature (soldering, 10 seconds)..... +300°C
Thermal resistance (θ_{JC}):
  Cases L and 3 ..... See MIL-STD-1835
Thermal resistance (θ_{JA}) ..... 120°C/W

1.4 Recommended operating conditions.

Ambient operating temperature range	-55°C to +125°C
Supply voltage range (V_{DD})	10.8 V dc to 16.5 V dc
Minimum high level input voltage	2.4 V dc
Maximum low level input voltage	0.8 V dc
V_{REFA}, V_{REFB}	10 V dc
V_{AGNDA}, V_{IOUTA}	0 V dc
V_{AGNDB}, V_{IOUTB}	0 V dc
Output amplifiers	AD644 or equivalent

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.2.4 Logic diagrams. The logic diagrams shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Resolution					12		Bits
Input low voltage	V_{IL}	V_{DD} = 10.8 V and 16.5 V	1, 2, 3	All		0.8	V
Input high voltage	V_{IH}	V_{DD} = 10.8 V and 16.5 V	1, 2, 3	All	2.4		V
Input current	I_{IN}	$V_{IN} = V_{DD}$ = 16.5 V	1	All		1.0	µA
			2, 3			10.0	
Supply current	I_{DD}	V_{DD} = 16.5 V	1, 2, 3	All		2.0	mA
Relative accuracy	RA	V_{DD} = 10.8 V and 16.5 V	1	All	-1.0	+1.0	LSB
			2, 3	01	-1.0	+1.0	
			2, 3	02, 03	-0.5	+0.5	
			12	02, 03	-0.5	+0.5	
Differential nonlinearity	DNL	All grades guaranteed monotonic to 12 bits over -55°C to +125°C range. V_{DD} = 10.8 V and 16.5 V	1, 2, 3	All	-1.0	+1.0	LSB
Gain error	A_E	Measured using R_{FA} and R_{FB}. Both DAC registers loaded with all 1's. V_{DD} = 10.8 V	1	All	-6.0	+6.0	LSB
			2, 3	01	-6.0	+6.0	
			2, 3	02	-3.0	+3.0	
			2, 3	03	-2.0	+2.0	
			12	02	-3.0	+3.0	
			12	03	-2.0	+2.0	
Gain temperature 2/ coefficient	TCA_E/dt		4	All	-5.0	+5.0	ppm/°C

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output leakage current	I_{OUTA}	DAC A register loaded with all 0's. V_{DD} = 16.5 V	1	All	-10	+10	nA
			2, 3		-250	+250	
Output leakage current	I_{OUTB}	DAC B register loaded with all 0's. V_{DD} = 16.5 V	1	All	-10	+10	nA
			2, 3		-250	+250	
Reference input resistance	R_I	V_{DD} = 10.8 V	1, 2, 3	All	9	20	kΩ
Reference input resistance match. V_{REFA}, V_{REFB}	R_{IN}	V_{DD} = 10.8 V	1	All	-3	+3	%
			2, 3	01, 02	-3	+3	
			2, 3	03	-1	+1	
			12	03	-1	+1	
Output current settling time 2/, 3/	t_{SL}		4	All		1.5	µs
AC feedthrough V_{REFA} to I_{OUTA} and V_{REFB} to I_{OUTB} 2/	FT	V_{REFA}, V_{REFB} = 20 V p-p, 10 kHz sinewave. DAC register loaded with all 0's	4	All		-65	dB
Power supply rejection ratio	PSRR	$V_{DD} = V_{DD}$ max – V_{DD} min V_{DD} = 10.8 V	1	All	-0.01	+0.01	%/%
			2, 3		-0.02	+0.02	
Output capacitance for DAC A and DAC B	C_{OUT}	DAC A, DAC B loaded with 0's	4	All		70	pF
		DAC A, DAC B loaded with 1's				140	
Functional test		See 4.3.1c	7	All			
Address valid to write setup time, t_1	t_{AWS}	See figure 4	9, 10, 11	All	30		ns
Address valid to write hold time, t_2	t_{AWH}	See figure 4	9, 10, 11	All	25		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Data setup time, t_3	t_{DS}	See figure 4	9, 10, 11	All	80		ns
Data hold time, t_4	t_{DH}	See figure 4	9, 10, 11	All	25		ns
Chip select or update to write setup time, t_5	t_{CWS}	See figure 4	9, 10, 11	All	0		ns
Chip select or update to write hold time, t_6	t_{CWH}	See figure 4	9, 10, 11	All	0		ns
Write pulse width, t_7	t_{WR}	See figure 4	9, 10, 11	All	100		ns
Clear pulse width, t_8	t_{CL}	See figure 4	9, 10, 11	All	100		ns

1/ V_{DD} = 10.8 V to 16.5 V except where otherwise specified; $V_{REFA} = V_{REFB}$ = 10 V (see 1.4). $V_{AGNDA} = V_{AGNDB}$ = 0 V, $V_{IOUTA} = V_{IOUTB}$ = 0 V.

2/ Guaranteed if not tested to the limits as specified on table I.

2/ To 0.01 percent of full-scale-range. I_{OUT} load = 100Ω; C_{EXT} = 13 pF. DAC output measured from rising edge of $\overline{WR}$.

Device types	01, 02, 03	
Case outlines	L	3
Terminal number	Terminal symbol	
1	AGNDA	NC
2	I_{OUTA}	AGNDA
3	R_{FBA}	I_{OUTA}
4	V_{REFA}	R_{FBA}
5	$\overline{CS}$	V_{REFA}
6	DB0	$\overline{CS}$
7	DB1	DB0
8	DB2	NC
9	DB3	DB1
10	DB4	DB2
11	DB5	DB3
12	DGND	DB4
13	DB6	DB5
14	DB7	DGND
15	A0	NC
16	A1	DB6
17	$\overline{CLR}$	DB7
18	$\overline{WR}$	A0
19	$\overline{UPD}$	A1
20	V_{DD}	$\overline{CLR}$
21	V_{REFB}	$\overline{WR}$
22	R_{FBB}	NC
23	I_{OUTB}	$\overline{UPD}$
24	AGNDB	V_{DD}
25	- - -	V_{REFB}
26	- - -	R_{FBB}
27	- - -	I_{OUTB}
28	- - -	AGNDB

Pin function description	
Mnemonic	Description
AGNDA	Analog ground for DAC A.
I_{OUTA}	Current output terminal of DAC A.
R_{FBA}	Feedback resistor for DAC A.
V_{REFA}	Reference input to DAC A.
$\overline{CS}$	Chip select input. Active low.
DB0-DB7	Eight data inputs, DB0-DB7
DGND	Digital ground
A0	Address line 0.
A1	Address line 1.
$\overline{CLR}$	Clear input. Active low. Clears all registers.
$\overline{WR}$	Write input. Active low.
$\overline{UPD}$	Updates DAC registers from input registers.
V_{DD}	Power supply input. Nominally +12 V to 15 V, with ±10 percent tolerance.
V_{REFB}	Reference input to DAC B.
R_{FBB}	Feedback resistor for DAC B.
I_{OUTB}	Current output terminal of DAC B.
AGNDB	Analog ground for DAC B.
NC	No connect.

FIGURE 1. Terminal connections and function descriptions.

$\overline{CLR}$	$\overline{UPD}$	$\overline{CS}$	$\overline{WR}$	A1	A0	Function
1	1	1	X	X	X	No data transfer
1	1	X	1	X	X	No data transfer
0	X	X	X	X	X	All registers cleared
1	1	0	0	0	0	DAC A LS input register loaded with DB7 – DB0
1	1	0	0	0	1	DAC A MS input register loaded with DB3 – DB0
1	1	0	0	1	0	DAC B LS input register loaded with DB7 – DB0
1	1	0	0	1	1	DAC B MS input register loaded with DB3 – DB0
1	0	1	0	X	X	DAC A, DAC B registers updated simultaneously from input registers
1	0	0	0	X	X	DAC A, DAC B registers are transparent

FIGURE 2. Truth table.

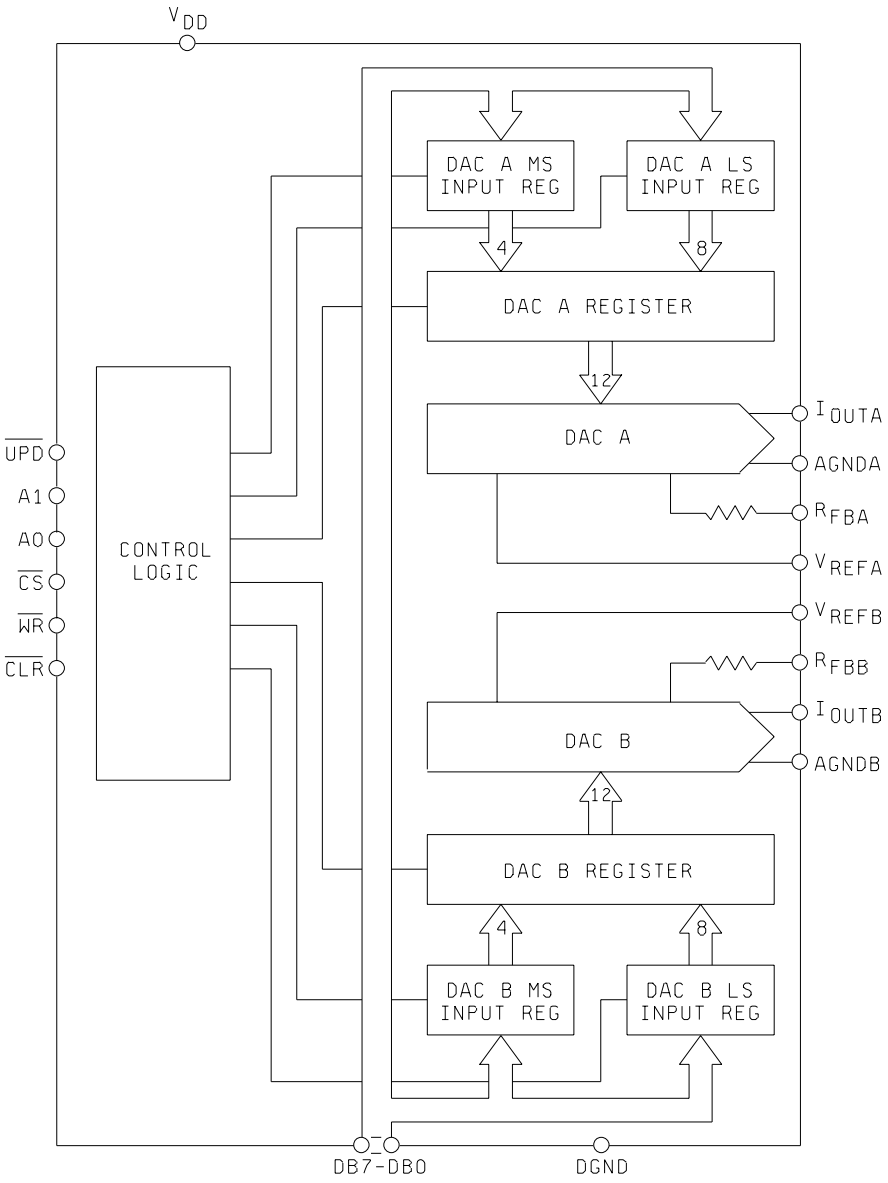
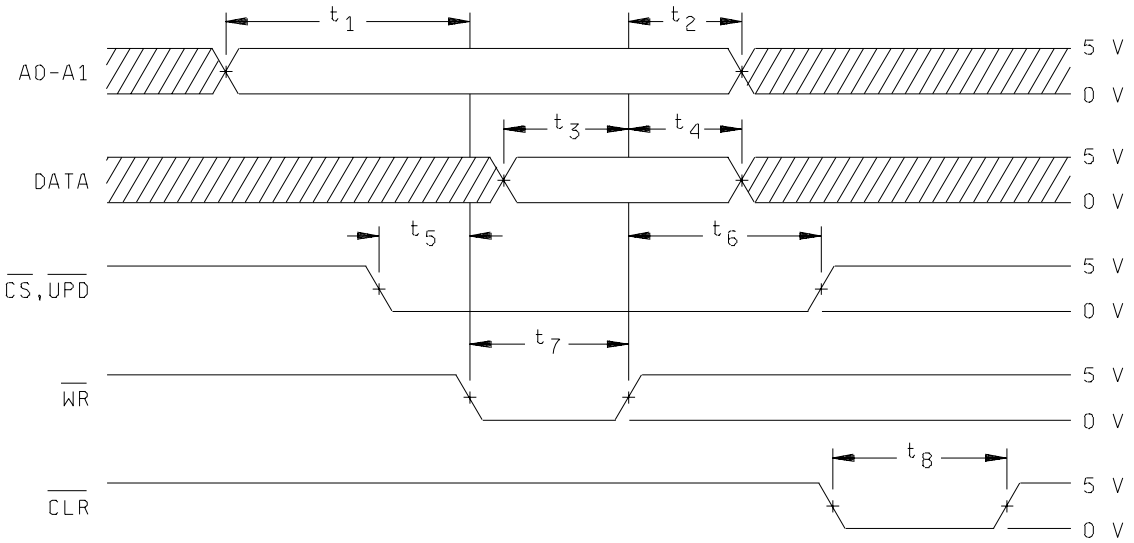


FIGURE 3. Logic diagram.



NOTES:
1. All input signal rise and fall times measured from 10 percent to 90 percent of +5 V, $t_r = t_f = 20$ ns.
2. Timing measurement reference level $\frac{V_{IH} + V_{IL}}{2}$.

FIGURE 4. Timing waveforms.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. Optional subgroup 12 is used for grading and part selection at +25°C, not included in PDA.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3, 4, 7, 12
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 9, 10**, 11**, 12
Groups C and D end-point electrical parameters (method 5005)	1, 12

* PDA applies to subgroup 1.
** Subgroups 10 and 11 shall be guaranteed if not tested.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5, 6, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 shall include verification of the truth table (see figure 2).

d. Optional subgroup 12 is used for grading and part selection at +25°C.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 04-01-27

Approved sources of supply for SMD 5962-87763 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-87763013A	3/	AD7537SE/883B
5962-87763013C	1ES66	MX7537SE/883B
5962-8776301LA	24335	AD7537SQ/883B
	1ES66	MX7537SQ/883B
5962-87763023A	3/	AD7537TE/883B
5962-87763023C	1ES66	MX7537TE/883B
5962-8776302LA	24335	AD7537TQ/883B
	1ES66	MX7537TQ/883B
5962-87763033A	3/	AD7537UE/883B
5962-87763033C	1ES66	MX7537UE/883B
5962-8776303LA	24335	AD7537UQ/883B
	1ES66	MX7537UQ/883B

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source.

Vendor CAGE number	Vendor name and address
24335	Analog Devices Rt 1 Industrial Park PO Box 9106 Norwood, MA 02062 Point of contact: Raheen Business Park Limerick, Ireland
1ES66	Maxim Integrated Products 120 San Gabriel Dr Sunnyvale, CA 94086-5125

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.