

Next-Generation NAND Flash Part Numbering System

Micron's part numbering system is available at www.micron.com/numbering

Next-Generation NAND Flash*

	MT	29F	2G	08	A	A	A	A	A	WP	-	xx	xx	x	ES	:	A																																																																																																																													
Micron Technology	<div style="display: flex; justify-content: space-between;"> <div style="width: 45%;"> <p>Single-Supply Flash 29F = NAND Flash 29E = Enterprise NAND Flash</p> <p>Density 1G = 1Gb 2G = 2Gb 4G = 4Gb 8G = 8Gb 16G = 16Gb 32G = 32Gb 64G = 64Gb 128G = 128Gb 256G = 256Gb</p> <p>Device Width 01 = 1 bit 08 = 8 bits 16 = 16 bits</p> <p>Level</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Mark</th> <th>Level</th> </tr> </thead> <tbody> <tr> <td>A</td> <td>SLC</td> </tr> <tr> <td>B</td> <td>Reserved</td> </tr> <tr> <td>C</td> <td>MLC-2</td> </tr> </tbody> </table> <p>Classification</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Mark</th> <th>Die</th> <th>nCE</th> <th>RnB</th> <th>IO Channels</th> </tr> </thead> <tbody> <tr><td>A</td><td>1</td><td>0</td><td>0</td><td>1</td></tr> <tr><td>B</td><td>1</td><td>1</td><td>1</td><td>1</td></tr> <tr><td>C</td><td>2</td><td>0</td><td>0</td><td>1</td></tr> <tr><td>D</td><td>2</td><td>1</td><td>1</td><td>1</td></tr> <tr><td>E</td><td>2</td><td>2</td><td>2</td><td>2</td></tr> <tr><td>F</td><td>2</td><td>2</td><td>2</td><td>1</td></tr> <tr><td>G</td><td></td><td></td><td></td><td></td></tr> <tr><td>H</td><td>4</td><td>1</td><td>1</td><td>1</td></tr> <tr><td>J</td><td>4</td><td>2</td><td>2</td><td>1</td></tr> <tr><td>K</td><td>4</td><td>2</td><td>2</td><td>2</td></tr> <tr><td>L</td><td>4</td><td>4</td><td>4</td><td>1</td></tr> <tr><td>M</td><td>4</td><td>4</td><td>4</td><td>2</td></tr> <tr><td>N</td><td>4 + 4</td><td>2 + 2</td><td>2 + 2</td><td>1</td></tr> <tr><td>P</td><td>8</td><td>1</td><td>1</td><td>1</td></tr> <tr><td>Q</td><td>8</td><td>2</td><td>2</td><td>1</td></tr> <tr><td>R</td><td>8</td><td>2</td><td>2</td><td>2</td></tr> <tr><td>T</td><td>8</td><td>4</td><td>4</td><td>1</td></tr> <tr><td>U</td><td>8</td><td>4</td><td>4</td><td>2</td></tr> <tr><td>V</td><td></td><td></td><td></td><td></td></tr> <tr><td>W</td><td></td><td></td><td></td><td></td></tr> <tr><td>Y</td><td></td><td></td><td></td><td></td></tr> </tbody> </table> </div> <div style="width: 45%;"> <p>Design Revision (shrink)</p> <p>Production Status Blank = Production ES = Engineering Samples QS = Qualification Samples MS = Mechanical Sample</p> <p>Reserved for Future use.</p> <p>Operating Temperature Range Blank = Commercial (0°C to +70°C) IT = Extended (-40°C to +85°C) (AKA ET) WT = Wireless Temp (-25°C to +85°C)</p> <p>Speed Grade (Synchronous) Blank if no speed grade defined 20 = 100MT/s 15 = 133MT/s 12 = 166MT/s</p> <p>Package Code WP = 48-pin TSOP I (CPL version) (Pb-free) WC = 48-pin TSOP I (OCPL version) (Pb-free) HC = 63-ball VFBGA, 10.5 x 13 x 1.0 C3 = 52-pad ULGA, 12 x 17 x 0.65 C4 = 52-pad VLGA, 12 x 17 x 1.0 (SDP/DDP/QDP) C5 = 52-pad VLGA, 14 x 18 x 1.0 (SDP/DDP/QDP) C6 = 52-pad LLGA, 14 x 18 x 1.47 (DDP/QDP/BDP) C7 = 48-pad LLGA, 12 x 20 x 1.47 (8DP) C8 = 52-pad WLGA, 14 x 18 x 0.75 (DDP/QDP) H1 = 100-ball VBGA (Pb-free), 12 x 18 x 1.0 H2 = 100-ball TBGA (Pb-free), 12 x 18 x 1.2 H3 = 100-ball LBGA, (Pb-free) 12 x 18 x 1.4 (DDP/QDP/BDP) H4 = 63-ball VFBGA, 9 x 11 x 1</p> <p>Interface</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Mark</th> <th>Interface</th> </tr> </thead> <tbody> <tr> <td>A</td> <td>Async only</td> </tr> <tr> <td>B</td> <td>Sync/Async</td> </tr> <tr> <td>D</td> <td>SPi</td> </tr> </tbody> </table> <p>Generation Feature Set A = 1st set of device features B = 2nd set of device features (rev only if different than 1st set) C = 3rd set of device features (rev only if different) D = 4th set of device features (rev only if different) etc.</p> <p>Operating Voltage Range A = 3.3V (2.70-3.60V) B = 1.8V (1.70-1.95V) C = 3.3V (2.70-3.60V), VccQ 1.8V (1.70-1.95V) D = 1.8V (1.65-3.6V) SIM</p> </div> </div>																Mark	Level	A	SLC	B	Reserved	C	MLC-2	Mark	Die	nCE	RnB	IO Channels	A	1	0	0	1	B	1	1	1	1	C	2	0	0	1	D	2	1	1	1	E	2	2	2	2	F	2	2	2	1	G					H	4	1	1	1	J	4	2	2	1	K	4	2	2	2	L	4	4	4	1	M	4	4	4	2	N	4 + 4	2 + 2	2 + 2	1	P	8	1	1	1	Q	8	2	2	1	R	8	2	2	2	T	8	4	4	1	U	8	4	4	2	V					W					Y					Mark	Interface	A	Async only	B	Sync/Async	D	SPi
Mark																	Level																																																																																																																													
A																	SLC																																																																																																																													
B																	Reserved																																																																																																																													
C																	MLC-2																																																																																																																													
Mark																	Die	nCE	RnB	IO Channels																																																																																																																										
A																	1	0	0	1																																																																																																																										
B																	1	1	1	1																																																																																																																										
C																	2	0	0	1																																																																																																																										
D																	2	1	1	1																																																																																																																										
E																	2	2	2	2																																																																																																																										
F																	2	2	2	1																																																																																																																										
G																																																																																																																																														
H																	4	1	1	1																																																																																																																										
J																	4	2	2	1																																																																																																																										
K																	4	2	2	2																																																																																																																										
L																	4	4	4	1																																																																																																																										
M	4	4	4	2																																																																																																																																										
N	4 + 4	2 + 2	2 + 2	1																																																																																																																																										
P	8	1	1	1																																																																																																																																										
Q	8	2	2	1																																																																																																																																										
R	8	2	2	2																																																																																																																																										
T	8	4	4	1																																																																																																																																										
U	8	4	4	2																																																																																																																																										
V																																																																																																																																														
W																																																																																																																																														
Y																																																																																																																																														
Mark	Interface																																																																																																																																													
A	Async only																																																																																																																																													
B	Sync/Async																																																																																																																																													
D	SPi																																																																																																																																													

*Contact Micron for help differentiating between standard and next-generation NAND offerings.

Rev. 8/19/09
© 2009 Micron Technology, Inc.
Micron and the Micron logo are trademarks of Micron Technology, Inc.
Products and specifications are subject to change without notice. Dates are estimates only.

