VNH2SP30-E

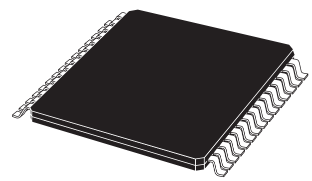
AUTOMOTIVE FULLY INTEGRATED H-BRIDGE MOTOR DRIVER

Table 1. General Features

Type	$R_{DS(on)}$	I_{out}	V_{ccmax}
VNH2SP30-E	19 mΩ max (per leg)	30 A	41 V

- OUTPUT CURRENT: 30A
- 5V LOGIC LEVEL COMPATIBLE INPUTS
- UNDERVOLTAGE AND OVERVOLTAGE SHUT-DOWN
- OVERVOLTAGE CLAMP
- THERMAL SHUT DOWN
- CROSS-CONDUCTION PROTECTION
- LINEAR CURRENT LIMITER
- VERY LOW STAND-BY POWER CONSUMPTION
- PWM OPERATION UP TO 20 KHz
- PROTECTION AGAINST: LOSS OF GROUND AND LOSS OF V_{CC}
- CURRENT SENSE OUTPUT PROPORTIONAL TO MOTOR CURRENT
- IN COMPLIANCE WITH THE 2002/95/EC EUROPEAN DIRECTIVE

Figure 1. Package



MultiPowerSO-30

DESCRIPTION

The VNH2SP30-E is a full bridge motor driver intended for a wide range of automotive applications. The device incorporates a dual monolithic High-Side drivers and two Low-Side switches. The High-Side driver switch is designed using STMicroelectronic's well known and proven proprietary VIPower™ M0 technology that allows to efficiently integrate on the same die a true Power MOSFET with an intelligent signal/ protection circuitry.

The Low-Side switches are vertical MOSFETs manufactured using STMicroelectronic's proprietary EHD ('STripFET™') process.The three dice are assembled in MultiPowerSO-30 package on electrically isolated leadframes. This package, specifically designed for the harsh automotive environment offers improved thermal performance thanks to exposed die pads. Moreover, its fully symmetrical mechanical design allows superior manufacturability at board level. The input signals IN_A and IN_B can directly interface to the microcontroller to select the motor direction and the brake condition. The $DIAG_A/EN_A$ or $DIAG_B/EN_B$, when connected to an external pull-up resistor, enable one leg of the bridge. They also provide a feedback digital diagnostic signal. The normal condition operation is explained in the truth table on page 14. The CS pin allows to monitor the motor current by delivering a current proportional to its value. The PWM, up to 20KHz, lets us to control the speed of the motor in all possible conditions. In all cases, a low level state on the PWM pin will turn off both the LS_A and LS_B switches. When PWM rises to a high level, LS_A or LS_B turn on again depending on the input pin state.

Table 2. Order Codes

Package	Tube	Tape and Reel
MultiPowerSO-30	VNH2SP30-E	VNH2SP30TR-E

Figure 2. Block Diagram

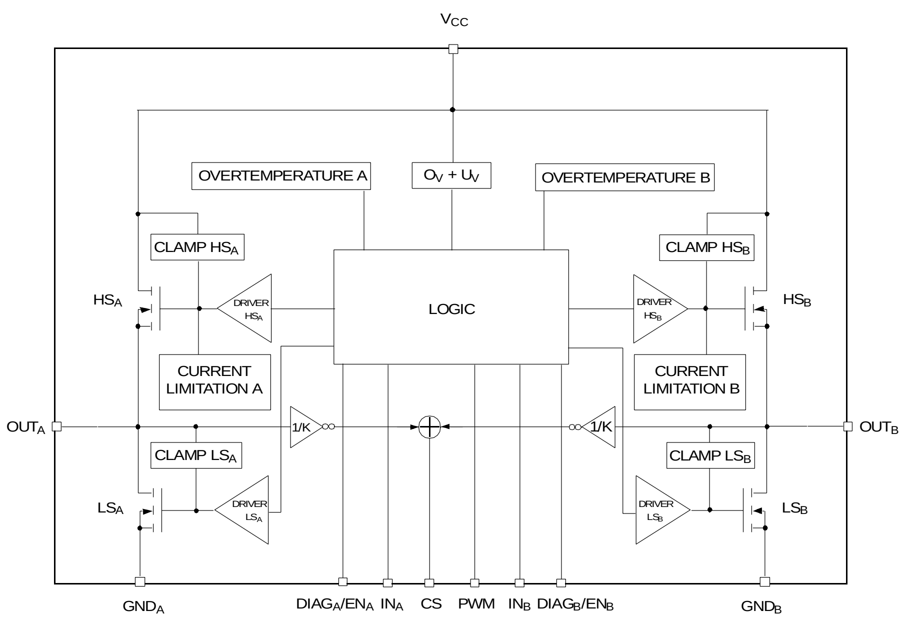


Figure 3. Configuration Diagram (Top View)

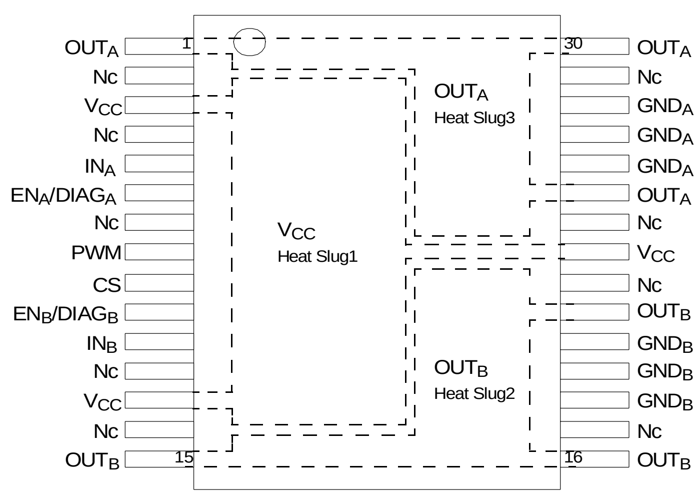


Table 3. Pin Definitions And Functions

Pin No	Symbol	Function
1, 25, 30	OUT_A, Heat Slug2	Source of High-Side Switch A / Drain of Low-Side Switch A
2,4,7,12,14,17, 22, 24,29	NC	Not connected
3, 13, 23	VCC, Heat Slug1	Drain of High-Side Switches and Power Supply Voltage
6	$EN_A/DIAG_A$	Status of High-Side and Low-Side Switches A; Open Drain Output
5	IN_A	Clockwise Input
8	PWM	PWM Input
9	CS	Output of Current sense
11	IN_B	Counter Clockwise Input
10	$EN_B/DIAG_B$	Status of High-Side and Low-Side Switches B; Open Drain Output
15, 16, 21	OUT_B, Heat Slug3	Source of High-Side Switch B / Drain of Low-Side Switch B
26, 27, 28	GND_A	Source of Low-Side Switch A (*)
18, 19, 20	GND_B	Source of Low-Side Switch B (*)

Note: (*) GND_A and GND_B must be externally connected together

Table 4. Pin Functions Description

Name	Description
V_{CC}	Battery connection.
GND_A GND_B	Power grounds, must always be externally connected together.
OUT_A OUT_B	Power connections to the motor.
IN_A IN_B	Voltage controlled input pins with hysteresis, CMOS compatible. These two pins control the state of the bridge in normal operation according to the truth table (brake to V_{CC}, Brake to GND, clockwise and counterclockwise).
PWM	Voltage controlled input pin with hysteresis, CMOS compatible.Gates of Low-Side FETS get modulated by the PWM signal during their ON phase allowing speed control of the motor
$EN_A/DIAG_A$ $EN_B/DIAG_B$	Open drain bidirectional logic pins.These pins must be connected to an external pull up resistor. When externally pulled low, they disable half-bridge A or B. In case of fault detection (thermal shutdown of a High-Side FET or excessive ON state voltage drop across a Low-Side FET), these pins are pulled low by the device (see truth table in fault condition).
CS	Analog current sense output. This output sources a current proportional to the motor current. The information can be read back as an analog voltage across an external resistor.

Table 5. Block Descriptions (see Block Diagram)

Name	Description
LOGIC CONTROL	Allows the turn-on and the turn-off of the High Side and the Low Side switches according to the truth table.
OVERVOLTAGE + UNDERVOLTAGE	Shut-down the device outside the range [5.5V..16V] for the battery voltage.
HIGH SIDE AND LOW SIDE CLAMP VOLTAGE	Protect the High Side and the Low Side switches from the high voltage on the battery line in all configuration for the motor.
HIGH SIDE AND LOW SIDE DRIVER	Drive the gate of the concerned switch to allow a proper $R_{DS(on)}$ for the leg of the bridge.
LINEAR CURRENT LIMITER	Limits the motor current, by reducing the High Side Switch gate-source voltage when short-circuit to ground occurs.
OVERTEMPERATURE PROTECTION	In case of short-circuit with the increase of the junction's temperature, shuts-down the concerned High Side to prevent its degradation and to protect the die.
FAULT DETECTION	Signalize an abnormal behavior of the switches in the half-bridge A or B by pulling low the concerned ENx/DIAGx pin.

Table 6. Absolute Maximum Rating

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	+ 41	V
I_{max}	Maximum Output Current (continuous)	30	A
I_R	Reverse Output Current (continuous)	-30	A
I_{IN}	Input Current (IN_A and IN_B pins)	+/- 10	mA
I_{EN}	Enable Input Current ($DIAG_A/EN_A$ and $DIAG_B/EN_B$ pins)	+/- 10	mA
I_{pw}	PWM Input Current	+/- 10	mA
V_{CS}	Current Sense Maximum Voltage	-3/+15	V
V_{ESD}	Electrostatic Discharge (R=1.5kΩ, C=100pF) - CS pin - logic pins - output pins: OUT_A, OUT_B, V_{CC}	 2 4 5	 kV kV kV
T_j	Junction Operating Temperature	Internally Limited	°C
T_c	Case Operating Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-55 to 150	°C

Figure 4. Current and Voltage Conventions

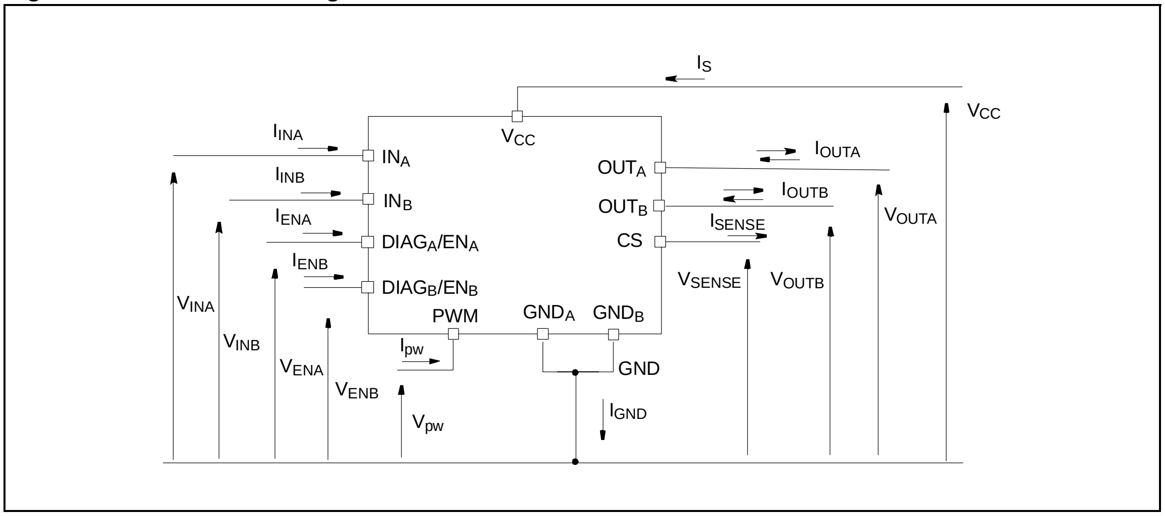


Table 7. Thermal Data

See MultiPowerSO-30 Thermal Data section (page)

ELECTRICAL CHARACTERISTICS

(V_{CC}=9V up to 16V; -40°C<T_j<150°C; unless otherwise specified)

Table 8. Power

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		5.5		16	V
I_S	Supply Current	Off state: IN_A=IN_B=PWM=0; T_j=25°C; V_{CC}=13V IN_A=IN_B=PWM=0		12	30 60	µA µA
		On state: IN_A or IN_B=5V, no PWM			10	mA
R_{ONHS}	Static High-Side resistance	I_{OUT}=15A; T_j=25°C I_{OUT}=15A; T_j= - 40 to 150°C			14 28	mΩ mΩ
R_{ONLS}	Static Low-Side resistance	I_{OUT}=15A; T_j=25°C I_{OUT}=15A; T_j= - 40 to 150°C			5 10	mΩ mΩ
V_f	High Side Free-wheeling Diode Forward Voltage	I_f=15A		0.8	1.1	V
$I_{L(off)}$	High Side Off State Output Current (per channel)	T_j=25°C; V_{OUTX}=EN_X=0V; V_{CC}=13V T_j=125°C; V_{OUTX}=EN_X=0V; V_{CC}=13V			3 5	µA µA
I_{RM}	Dynamic Cross-conduction Current	I_{OUT}=15A (see fig. 8)		0.7		A

Table 9. Logic Inputs (IN_A, IN_B, EN_A, EN_B)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Level Voltage	Normal operation ($DIAG_X$/EN_X pin acts as an input pin)			1.25	V
V_{IH}	Input High Level Voltage	Normal operation ($DIAG_X$/EN_X pin acts as an input pin)	3.25			V
V_{IHYST}	Input Hysteresis Voltage	Normal operation ($DIAG_X$/EN_X pin acts as an input pin)	0.5			V
V_{ICL}	Input Clamp Voltage	I_{IN}=1mA I_{IN}=-1mA	5.5 -1.0	6.3 -0.7	7.5 -0.3	V V
I_{INL}	Input Current	V_{IN}=1.25 V	1			µA
I_{INH}	Input Current	V_{IN}=3.25 V			10	µA
V_{DIAG}	Enable Output Low Level Voltage	Fault operation ($DIAG_X$/EN_X pin acts as an output pin); I_{EN}=1mA			0.4	V

ELECTRICAL CHARACTERISTICS (continued)

Table 10. PWM

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{pwl}	PWM Low Level Voltage				1.25	V
I_{pwl}	PWM Pin Current	V_{pw}=1.25V	1			µA
V_{pwh}	PWM High Level Voltage		3.25			V
I_{pwh}	PWM Pin Current	V_{pw}=3.25V			10	µA
$V_{pwhhyst}$	PWM Hysteresis Voltage		0.5			V
V_{pwcl}	PWM Clamp Voltage	I_{pw} = 1 mA I_{pw} = -1 mA	V_{CC}+0.3 -6.0	V_{CC}+0.7 -4.5	V_{CC}+1.0 -3.0	V V
C_{INPWM}	PWM Pin Input Capacitance	V_{IN} =2.5V			25	pF

Table 11. Switching (V_{CC}=13V, R_{LOAD}=0.87Ω)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
f	PWM Frequency		0		20	kHz
$t_{d(on)}$	Turn-on Delay Time	Input rise time < 1µs (see fig. 8)			250	µs
$t_{d(off)}$	Turn-off Delay Time	Input rise time < 1µs (see fig. 8)			250	µs
t_r	Rise Time	(see fig. 7)		1	1.6	µs
t_f	Fall Time	(see fig. 7)		1.2	2.4	µs
t_{DEL}	Delay Time During Change of Operating Mode	(see fig. 6)	300	600	1800	µs
t_{rr}	High Side Free Wheeling Diode Reverse Recovery Time	(see fig. 9)		110		ns
$t_{off(min)}$	PWM Minimum off time	9V<V_{CC}<16V; -40°C<T_j<150°C; I_{OUT}=15A			6	µs

Table 12. Protection And Diagnostic

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{USD}	Undervoltage Shut-down Undervoltage Reset			 4.7	5.5 	V V
V_{OV}	Overvoltage Shut-down		16	19	22	V
I_{LIM}	High-Side Current Limitation		30	50	70	A
V_{CLP}	Total Clamp Voltage (V_{CC} to GND)	I_{OUT}=15A	43	48	54	V
T_{TSD}	Thermal Shut-down Temperature	V_{IN} = 3.25 V	150	175	200	°C
T_{TR}	Thermal Reset Temperature		135			°C
T_{HYST}	Thermal Hysteresis		7	15		°C

ELECTRICAL CHARACTERISTICS (continued)

Table 13. Current Sense ($9V<V_{CC}<16V$)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
K_1	I_{OUT}/I_{SENSE}	I_{OUT}=30A; R_{SENSE}=1.5kΩ T_j= - 40 to 150°C	9665	11370	13075	
K_2	I_{OUT}/I_{SENSE}	I_{OUT}=8A; R_{SENSE}=1.5kΩ T_j= - 40 to 150°C	9096	11370	13644	
dK_1 / K_1 (*)	Analog sense current drift	I_{OUT}=30A; R_{SENSE}=1.5kΩ T_j= - 40 to 150°C	-8		+8	%
dK_2 / K_2 (*)	Analog sense current drift	I_{OUT} >8A; R_{SENSE}=1.5kΩ T_j= - 40 to 150°C	-10		+10	%
I_{SENSEO}	Analog Sense Leakage Current	I_{OUT}=0A; V_{SENSE}=0V; T_j= - 40 to 150°C	0		65	µA

Note:(*) Analog sense current drift is deviation of factor K for a given device over (-40°C to 150°C and $9V<V_{CC}<16V$) with respect to it's value measured at T_j=25°C, V_{CC}=13V.

WAVEFORMS AND TRUTH TABLE

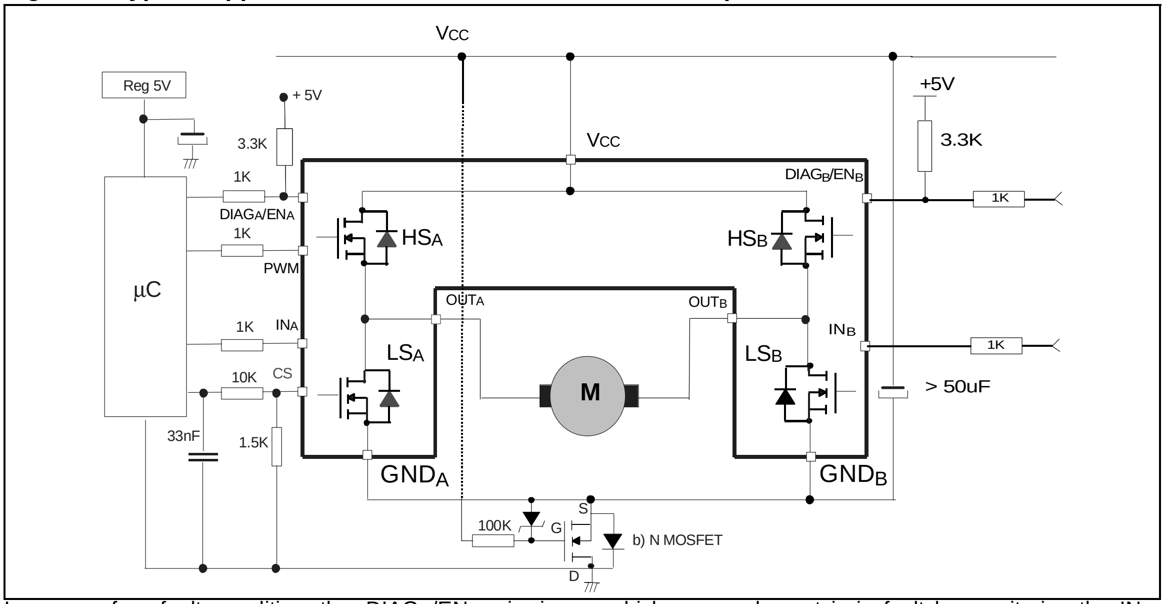
Table 14. Truth Table In Normal Operating Conditions

In normal operating conditions the $DIAG_X/EN_X$ pin is considered as an input pin by the device. This pin must be externally pulled high.

PWM pin usage: in all cases, a "0" on the PWM pin will turn-off both LS_A and LS_B switches. When PWM rises back to "1", LS_A or LS_B turn on again depending on the input pin state.

IN_A	IN_B	$DIAG_A/EN_A$	$DIAG_B/EN_B$	OUT_A	OUT_B	CS	Operating mode
1	1	1	1	H	H	High Imp.	Brake to V_{CC}
1	0	1	1	H	L	$I_{SENSE}=I_{OUT}/K$	Clockwise (CW)
0	1	1	1	L	H	$I_{SENSE}=I_{OUT}/K$	Counterclockwise (CCW)
0	0	1	1	L	L	High Imp.	Brake to GND

Figure 5. Typical Application Circuit For Dc To 20khz PWM OperationShort Circuit Protection



In case of a fault condition the $DIAG_X/EN_X$ pin is considered as an output pin by the device.

The fault conditions are:

- overtemperature on one or both high sides (for example if a short to ground occurs as it could be the case described in line 1 and 2 in the table below);
- short to battery condition on the output (saturation detection on the Low-Side Power MOSFET).

Possible origins of fault conditions may be:

OUT_A is shorted to ground ---> overtemperature detection on high side A.

OUT_A is shorted to V_{CC} ---> Low-Side Power MOSFET saturation detection.

When a fault condition is detected, the user can know which power element is in fault by monitoring the IN_A, IN_B, $DIAG_A/EN_A$ and $DIAG_B/EN_B$ pins.

In any case, when a fault is detected, the faulty leg of the bridge is latched off. To turn-on the respective output (OUT_X) again, the input signal must rise from low to high level.

Table 15. Truth Table In Fault Conditions (Detected On OUT_A)

IN_A	IN_B	$DIAG_A/EN_A$	$DIAG_B/EN_B$	OUT_A	OUT_B	CS
1	1	0	1	OPEN	H	High Imp.
1	0	0	1	OPEN	L	High Imp.
0	1	0	1	OPEN	H	I_{OUTB}/K
0	0	0	1	OPEN	L	High Imp.
X	X	0	0	OPEN	OPEN	High Imp.
X	1	0	1	OPEN	H	I_{OUTB}/K
X	0	0	1	OPEN	L	High Imp.

Fault Information (DIAGA/ENA, DIAGB/ENB) — Protection Action (OUTA, OUTB)

Table 16. Electrical Transient Requirements

ISO T/R 7637/1 Test Pulse	Test Level I	Test Level II	Test Level III	Test Level IV	Test Levels Delays and Impedance
1	-25V	-50V	-75V	-100V	2ms, 10Ω
2	+25V	+50V	+75V	+100V	0.2ms, 10Ω
3a	-25V	-50V	-100V	-150V	0.1µs, 50Ω
3b	+25V	+50V	+75V	+100V	0.1µs, 50Ω
4	-4V	-5V	-6V	-7V	100ms, 0.01Ω
5	+26.5V	+46.5V	+66.5V	+86.5V	400ms, 2Ω

ISO T/R 7637/1 Test Pulse	Test Levels Result I	Test Levels Result II	Test Levels Result III	Test Levels Result IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

Reverse Battery Protection

Three possible solutions can be thought of:

a) a Schottky diode D connected to V_{CC} pin

b) a N-channel MOSFET connected to the GND pin (see Typical Application Circuit on page 8)

c) a P-channel MOSFET connected to the V_{CC} pin

The device sustains no more than -30A in reverse battery conditions because of the two Body diodes of the Power MOSFETs. Additionally, in reverse battery condition the I/Os of VNH2SP30-E will be pulled down to the V_{CC} line (approximately -1.5V). Series resistor must be inserted to limit the current sunk from the microcontroller I/Os. If I_{Rmax} is the maximum target reverse current through µC I/Os, series resistor is:

$$R = \frac{V_{IOs} - V_{CC}}{I_{Rmax}}$$

Figure 6. Definition Of The Delay Times Measurement

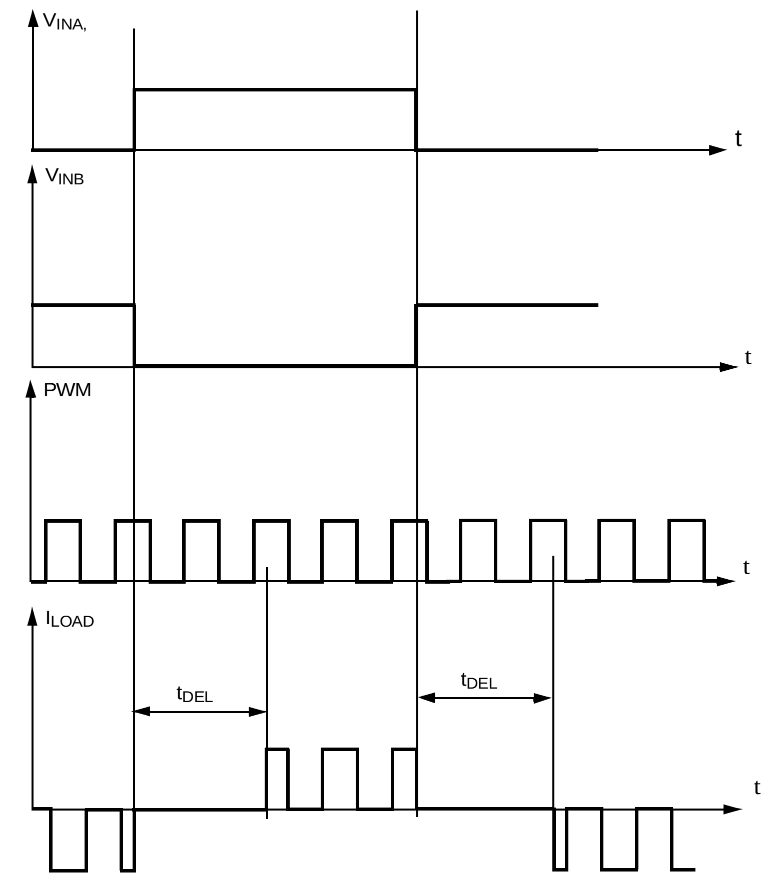


Figure 7. Definition Of The Low Side Switching Times

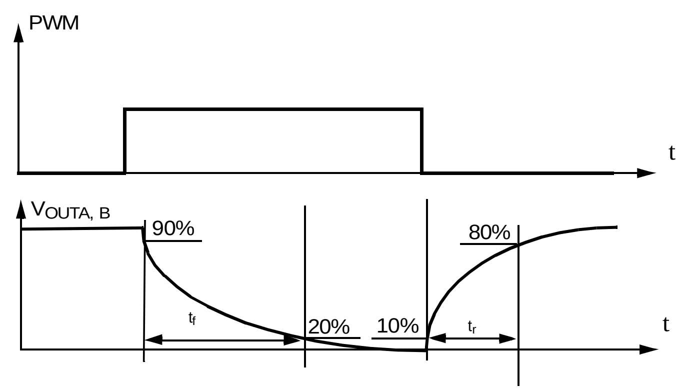


Figure 8. Definition Of The High Side Switching Times

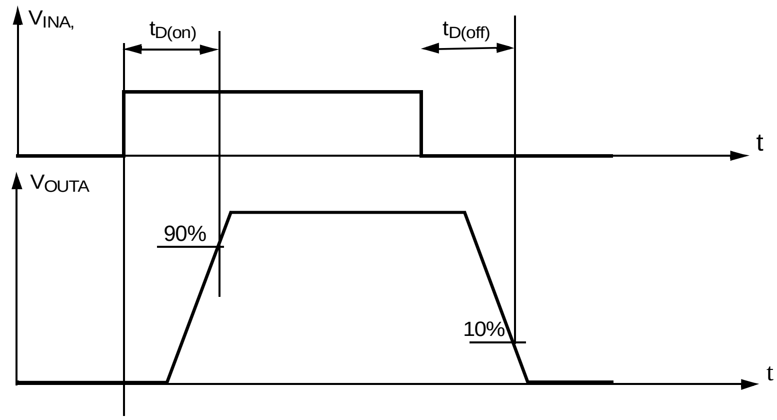


Figure 9. Definition Of Dynamic Cross Conduction Current During A Pwm Operation

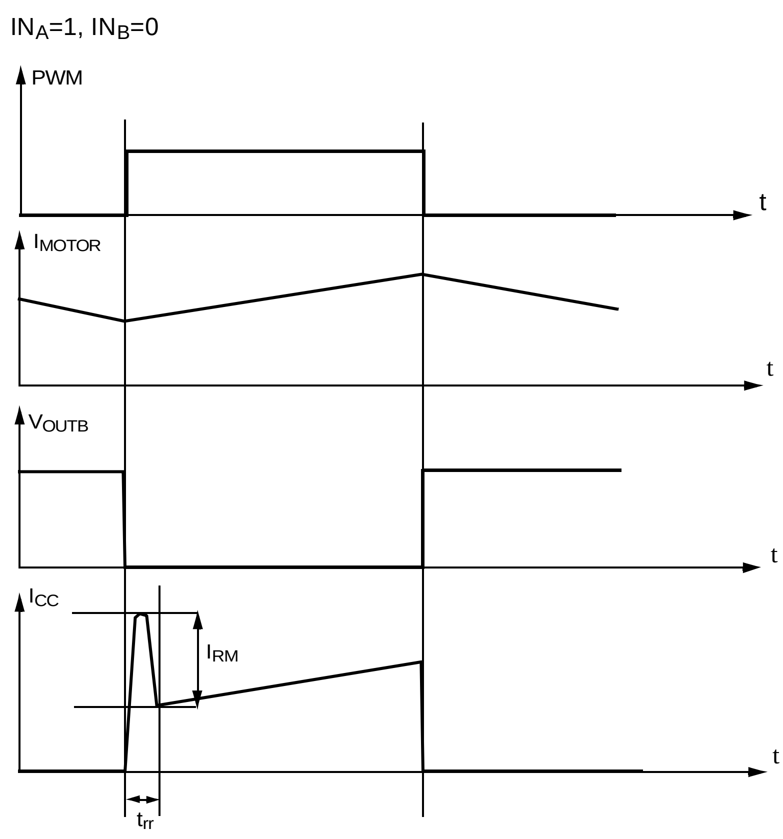


Figure 10. Waveforms in full bridge operation

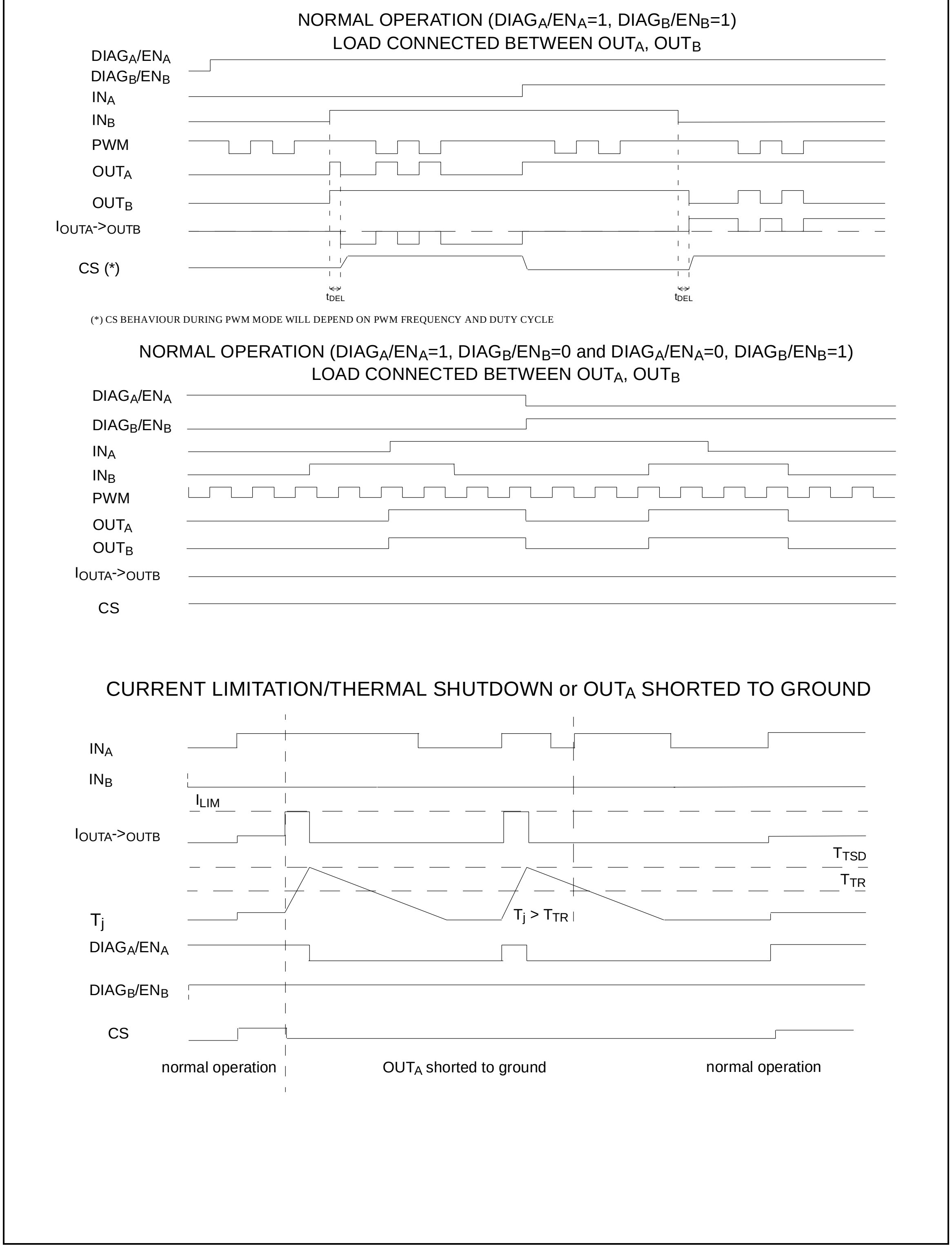


Figure 11. Waveforms In Full Bridge Operation (continued)

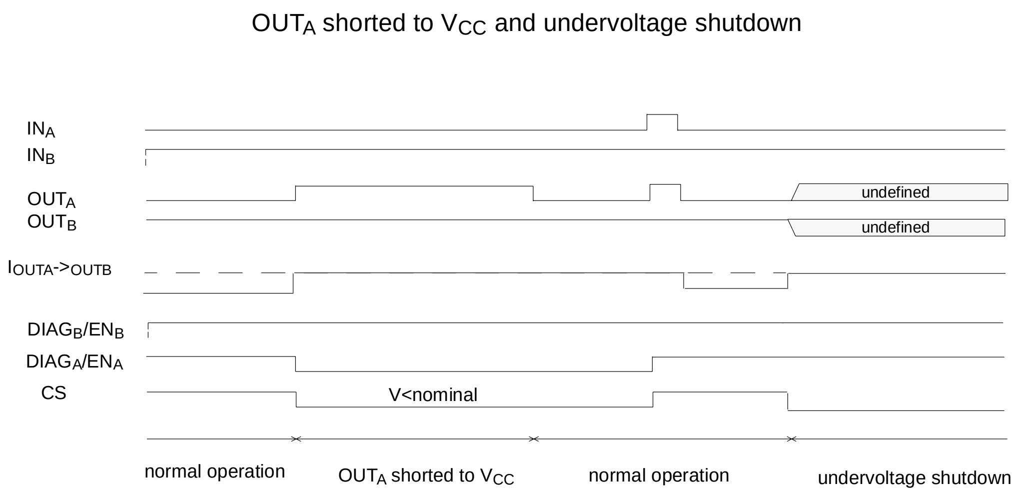


Figure 12. Half-bridge Configuration

The VNH2SP30-E can be used as a high power half-bridge driver achieving an On resistance per leg of 9.5mΩ. Suggested configuration is the following:

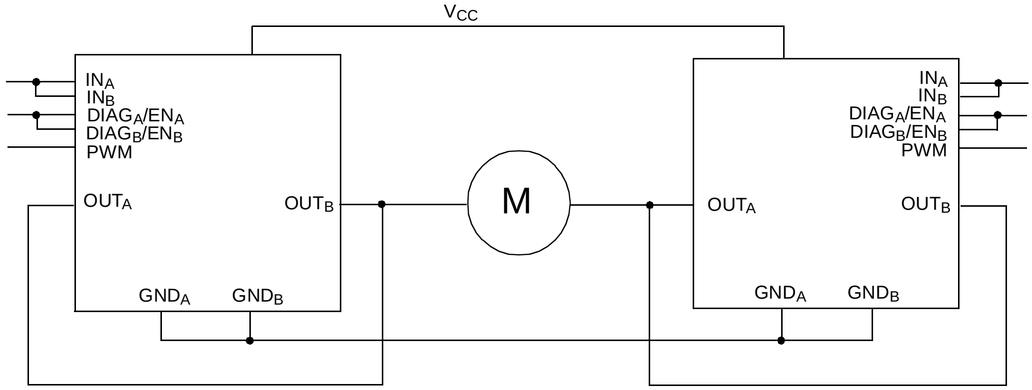


Figure 13. Multi-motors Configuration

The VNH2SP30-E can easily be designed in multi-motors driving applications such as seat positioning systems where only one motor must be driven at a time. $DIAG_X/EN_X$ pins allow to put unused half-bridges in high impedance. Suggested configuration is the following:

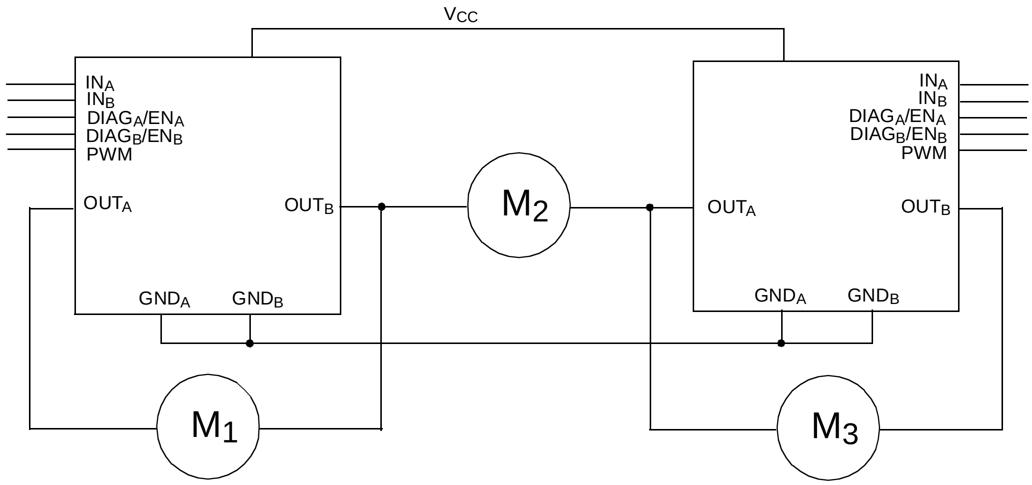


Figure 14. On State Supply Current

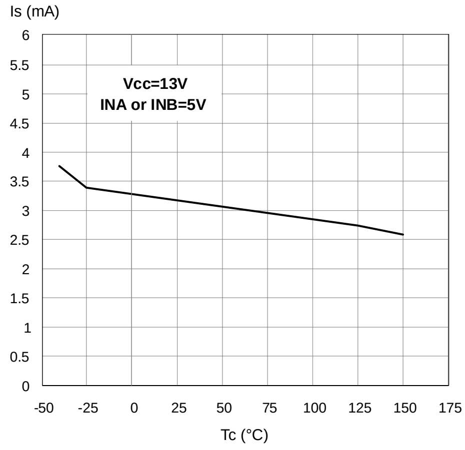


Figure 17. Off State Supply Current

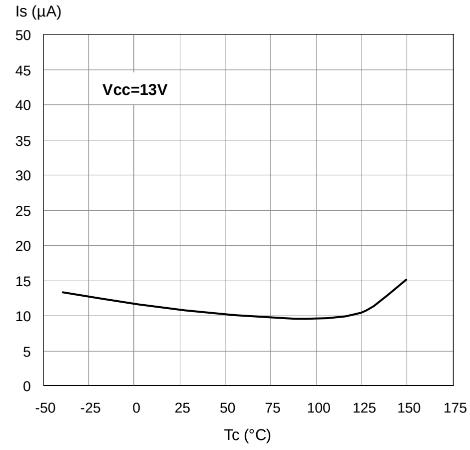


Figure 15. High Level Input Current

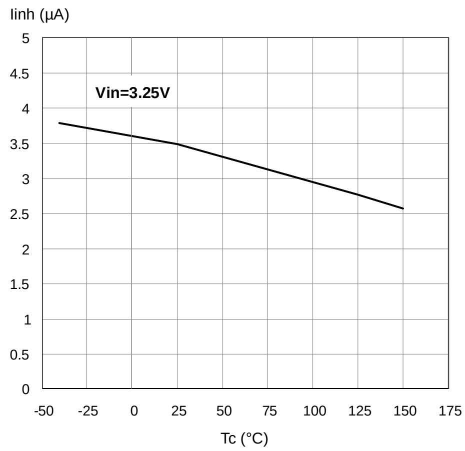


Figure 18. Input Clamp Voltage

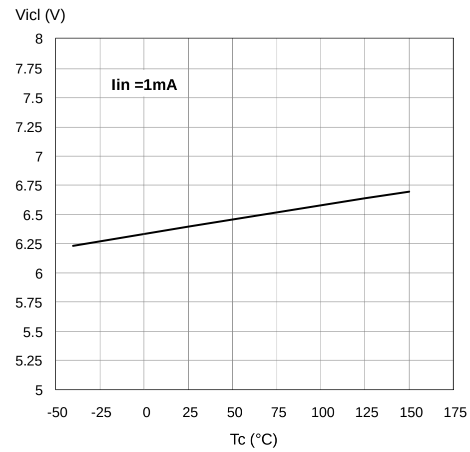


Figure 16. Input High Level Voltage

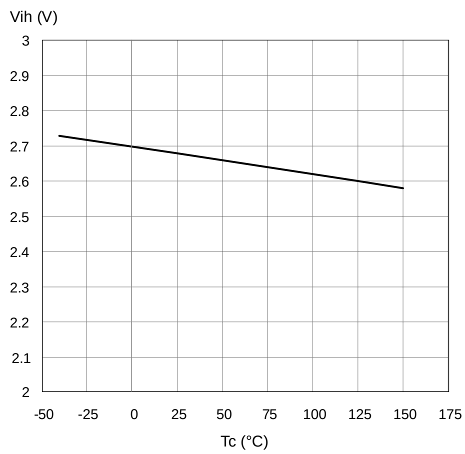


Figure 19. Input Low Level Voltage

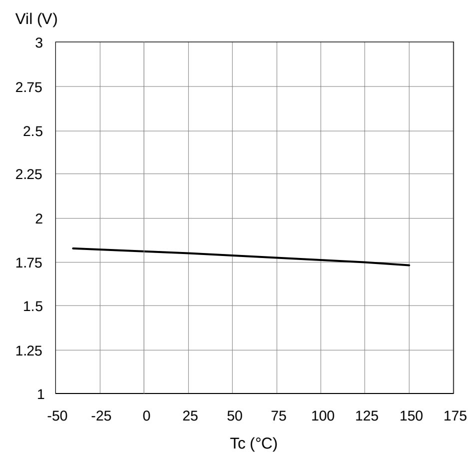


Figure 20. Input Hysteresis Voltage

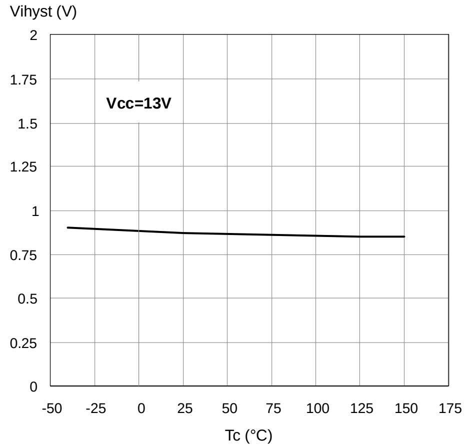


Figure 21. Delay Time during change of operation mode

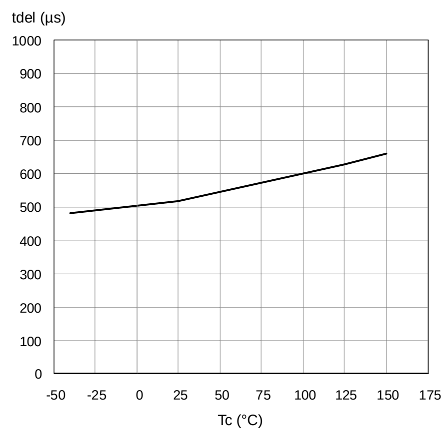


Figure 22. High Level Enable Voltage

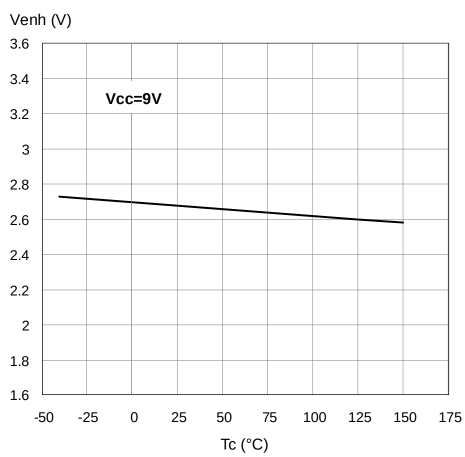


Figure 23. High Level Enable Pin Current

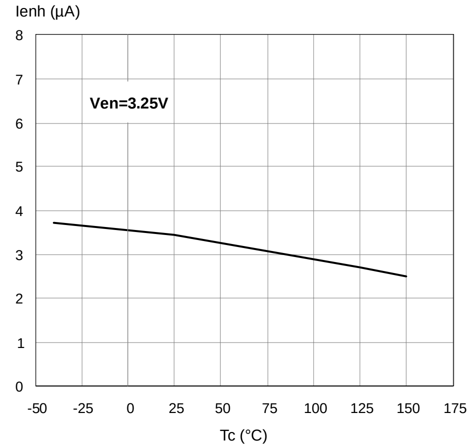


Figure 24. Enable Clamp Voltage

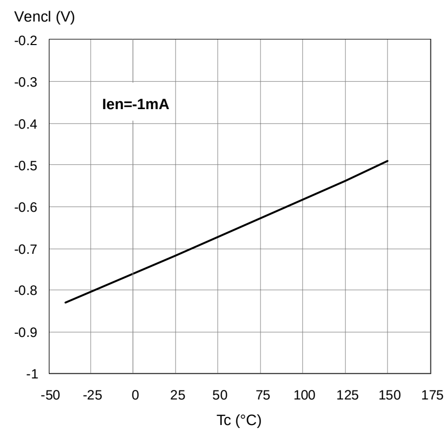


Figure 25. Low Level Enable Voltage

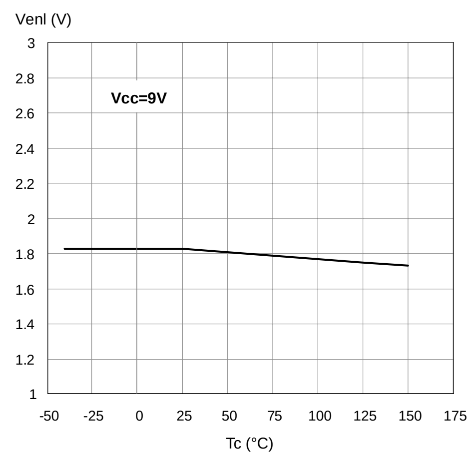


Figure 26. PWM High Level Voltage

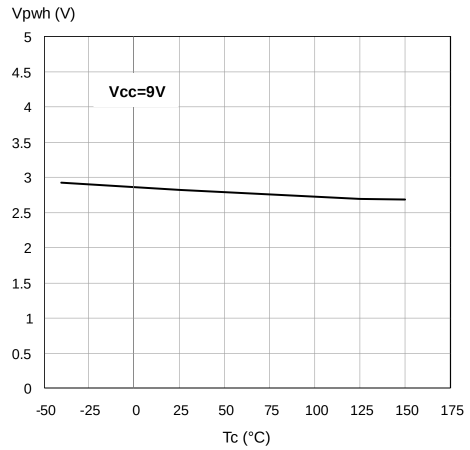


Figure 27. PWM High Level Current

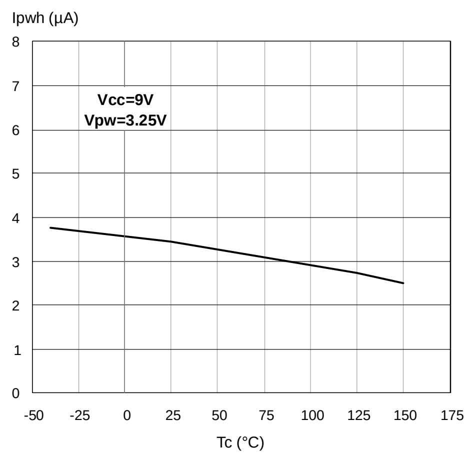


Figure 28. Undervoltage Shutdown

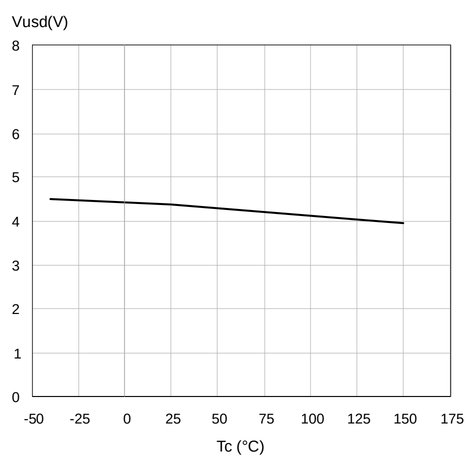


Figure 29. PWM Low Level Voltage

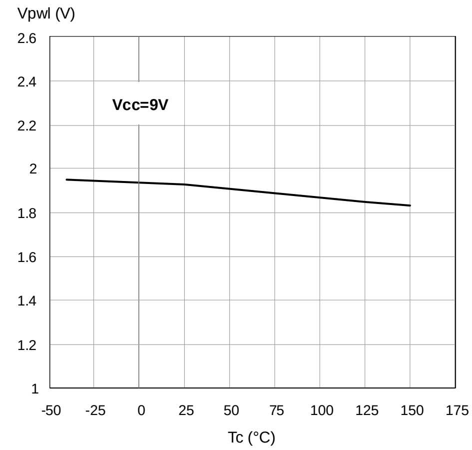


Figure 30. Overvoltage Shutdown

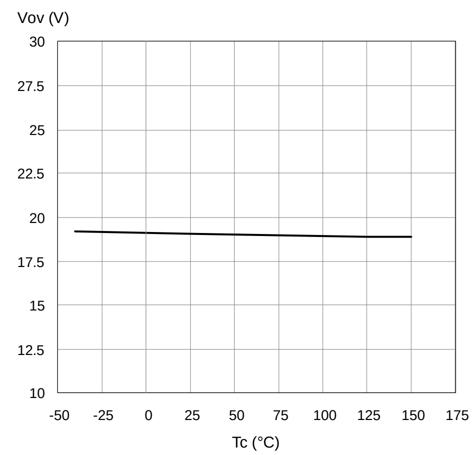


Figure 31. Current Limitation

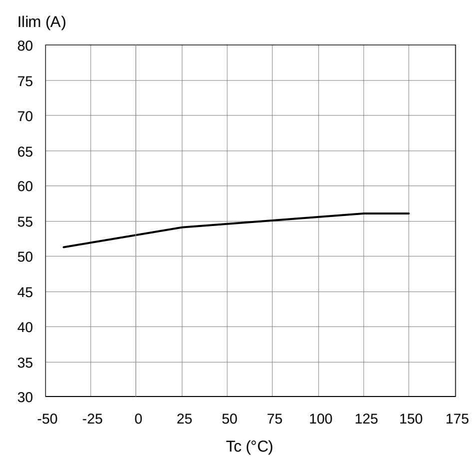


Figure 32. On State High Side Resistance Vs. T_{case}

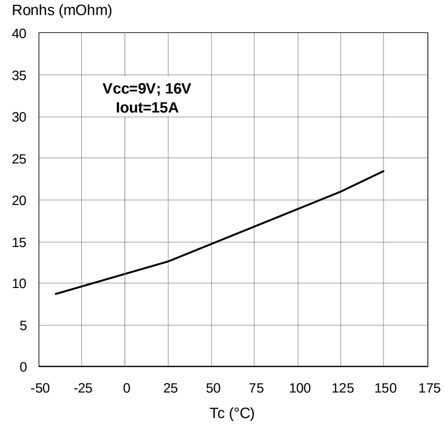


Figure 35. On State Low Side Resistance Vs. T_{case}

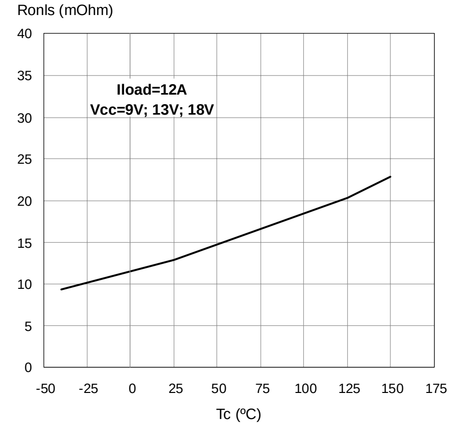


Figure 33. Turn-on Delay Time

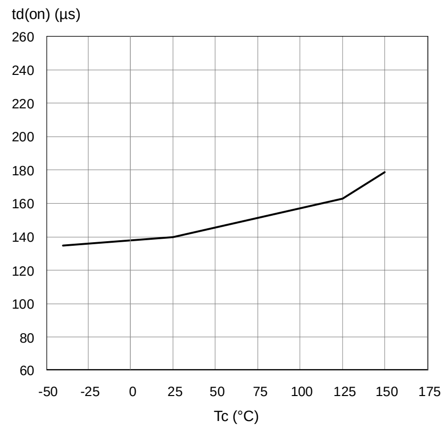


Figure 36. Turn-off Delay Time

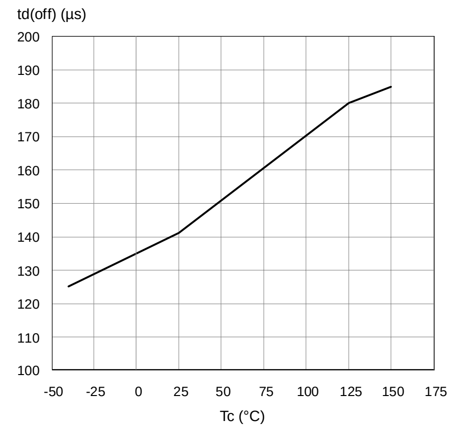


Figure 34. Output Voltage Rise Time

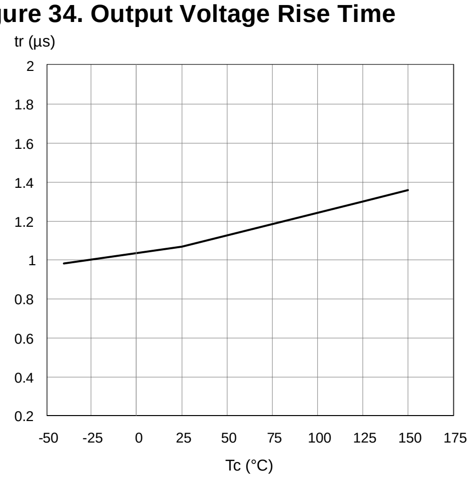
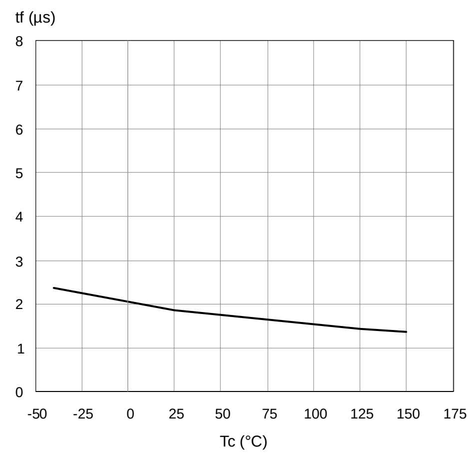
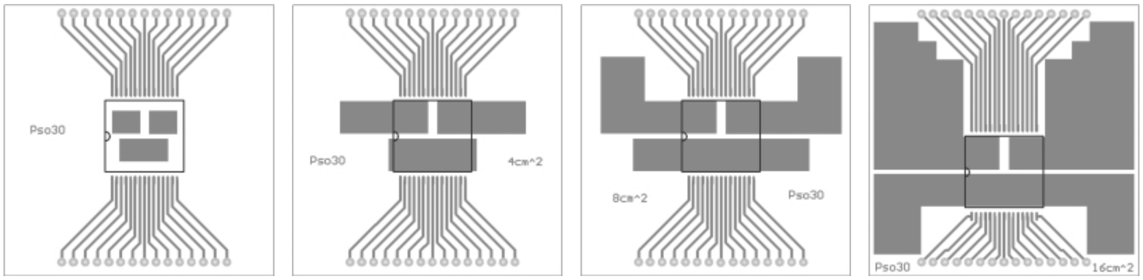


Figure 37. Output Voltage Fall Time



MultiPowerSO-30™ Thermal Data

Figure 38. MultiPowerSO-30™ PC Board



Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area= 58mm x 58mm, PCB thickness=2mm, Cu thickness=35µm, Copper areas: from minimum pad lay-out to 16cm^2).

Figure 39. Chipset Configuration

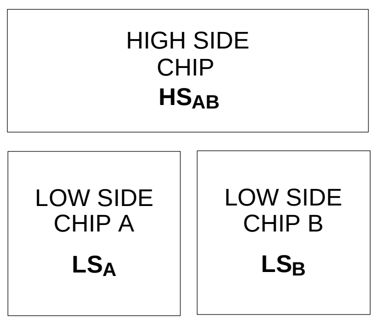


Figure 40. Auto and mutual $R_{thj\text{-}amb}$ Vs PCB copper area in open box free air condition (according to page 20 definitions)

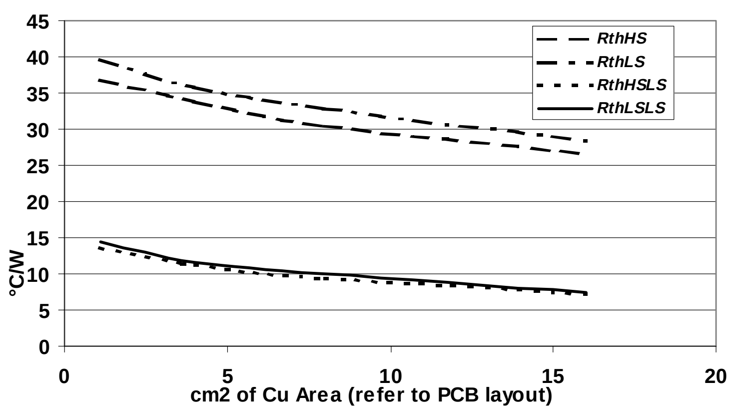


Table 17. Thermal Calculation In Clockwise And Anti-clockwise Operation In Steady-state Mode

HS_A	HS_B	LS_A	LS_B	T_{jHSAB}	T_{jLSA}	T_{jLSB}
ON	OFF	OFF	ON	P_{dHSA} x R_{thHS} + P_{dLSB} x R_{thHSLS} + T_{amb}	P_{dHSA} x R_{thHSLS} + P_{dLSB} x R_{thLSLS} + T_{amb}	P_{dHSA} x R_{thHSLS} + P_{dLSB} x R_{thLS} + T_{amb}
OFF	ON	ON	OFF	P_{dHSB} x R_{thHS} + P_{dLSA} x R_{thHSLS} + T_{amb}	P_{dHSB} x R_{thHSLS} + P_{dLSA} x R_{thLS} + T_{amb}	P_{dHSB} x R_{thHSLS} + P_{dLSA} x R_{thLSLS} + T_{amb}

Thermal Resistances Definition (values according to the PCB heatsink area)

$\mathbf{R_{thHS}}$ = R_{thHSA} = R_{thHSB} = High Side Chip Thermal Resistance Junction to Ambient (HS_A or HS_B in ON state)

$\mathbf{R_{thLS}}$ = R_{thLSA} = R_{thLSB} = Low Side Chip Thermal Resistance Junction to Ambient

$\mathbf{R_{thHSLS}}$ = $R_{thHSALSB}$ = $R_{thHSBLSA}$ = Mutual Thermal Resistance Junction to Ambient between High Side and Low Side Chips

$\mathbf{R_{thLSLS}}$ = $R_{thLSALSB}$ = Mutual Thermal Resistance Junction to Ambient between Low Side Chips

Single Pulse Thermal Impedance Definition (values according to the PCB heatsink area)

$\mathbf{Z_{thHS}}$ = High Side Chip Thermal Impedance Junction to Ambient

$\mathbf{Z_{thLS}}$ = Z_{thLSA} = Z_{thLSB} = Low Side Chip Thermal Impedance Junction to Ambient

$\mathbf{Z_{thHSLS}}$ = $Z_{thHSABLSA}$ = $Z_{thHSABLSB}$ = Mutual Thermal Impedance Junction to Ambient between High Side and Low Side Chips

$\mathbf{Z_{thLSLS}}$ = $Z_{thLSALSB}$ = Mutual Thermal Impedance Junction to Ambient between Low Side Chips

Thermal Calculation In Transient Mode (*)

T_{jHSAB} = Z_{thHS} x P_{dHSAB} + Z_{thHSLS} x (P_{dLSA} + P_{dLSB}) + T_{amb}

T_{jLSA} = Z_{thHSLS} x P_{dHSAB} + Z_{thLS} x P_{dLSA} + Z_{thLSLS} x P_{dLSB} + T_{amb}

T_{jLSB} = Z_{thHSLS} x P_{dHSAB} + Z_{thLSLS} x P_{dLSA} + Z_{thLS} x P_{dLSB} + T_{amb}

Pulse Calculation Formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p / T$

(*) Calculation is valid in any dynamic operating condition. P_d values set by user.

Figure 41. MultiPowerSO-30 HSD Thermal Impedance Junction Ambient Single Pulse

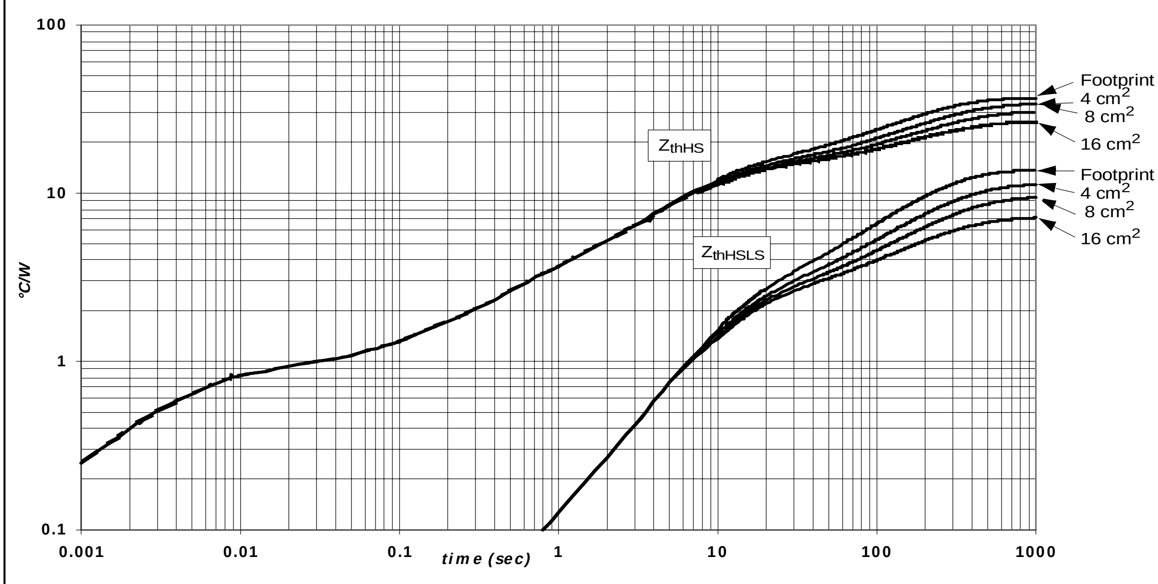


Figure 42. MultiPowerSo-30 LSD Thermal Impedance Junction Ambient Single Pulse

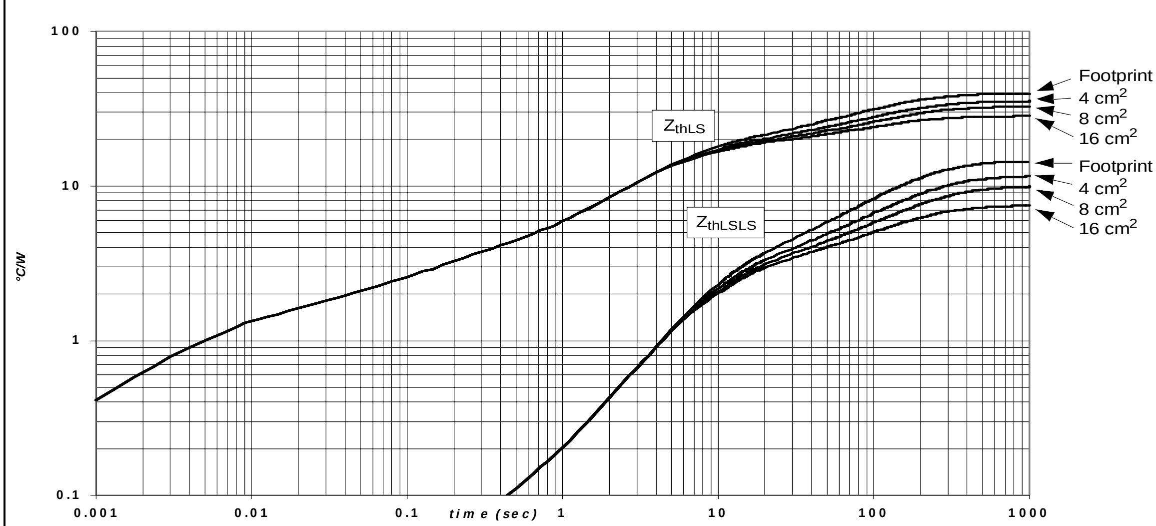


Figure 43. Thermal fitting model of an H-Bridge in MultiPowerSO-30

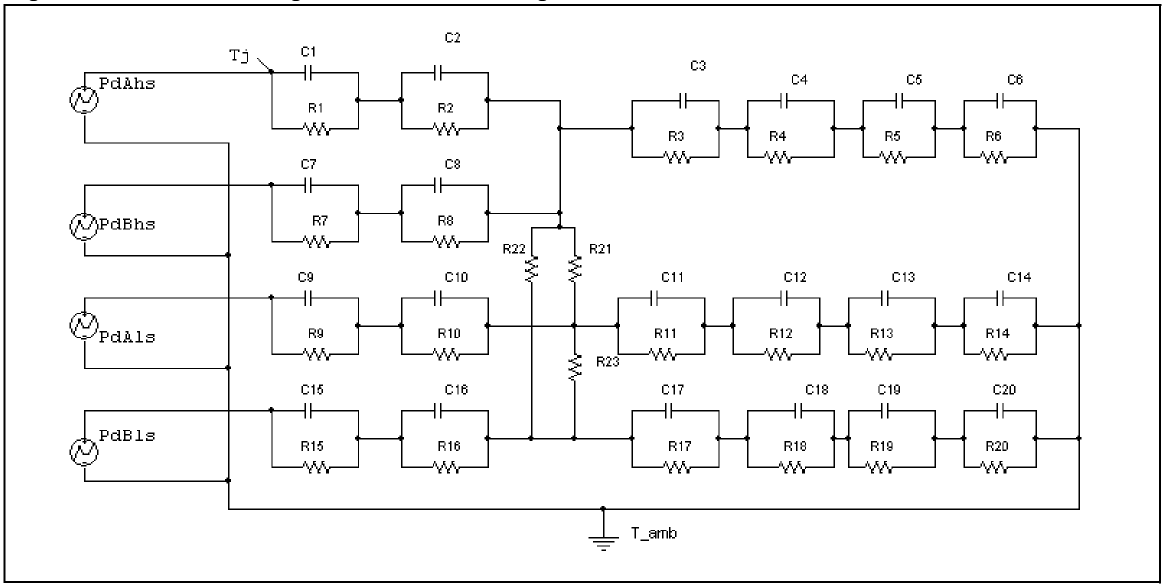


Table 18. Thermal Parameter (*)

Area/island (cm^2)	Footprint	4	8	16
R1=R7 (°C/W)	0.05			
R2=R8 (°C/W)	0.3			
R3 (°C/W)	0.5			
R4 (°C/W)	1.3			
R5 (°C/W)	1.4			
R6 (°C/W)	44.7	39.1	31.6	23.7
R9=R15 (°C/W)	0.2			
R10=R16 (°C/W)	0.4			
R11=R17 (°C/W)	0.8			
R12=R18 (°C/W)	1.5			
R13=R19 (°C/W)	20			
R14=R20 (°C/W)	46.9	36.1	30.4	20.8
R21=R22=R23 (°C/W)	115			
C1=C7 (W.s/°C)	0.005			
C2=C8 (W.s/°C)	0.008			
C3=C11=C17 (W.s/°C)	0.01			
C4=C13=C19 (W.s/°C)	0.3			
C5 (W.s/°C)	0.6			
C6 (W.s/°C)	5	7	9	11
C9=C15 (W.s/°C)	0.003			
C10=C16 (W.s/°C)	0.006			
C12=C18 (W.s/°C)	0.075			
C14=C20 (W.s/°C)	2.5	3.5	4.5	5.5

Note: (*) The blank space means that the value is the same as the previous one.

PACKAGE MECHANICAL

Table 19. MultiPowerSO-30 Mechanical Data

Symbol	millimeters		
	Min.	**Typ**	**Max.**
A			2.35
A2	1.85		2.25
A3	0		0.1
B	0.42		0.58
C	0.23		0.32
D	17.1	17.2	17.3
E	18.85		19.15
E1	15.9	16	16.1
e		1	
F1	5.55		6.05
F2	4.6		5.1
F3	9.6		10.1
L	0.8		1.15
N			10deg
S	0deg		7deg

Figure 44. MultiPowerSO-30 Package Dimensions

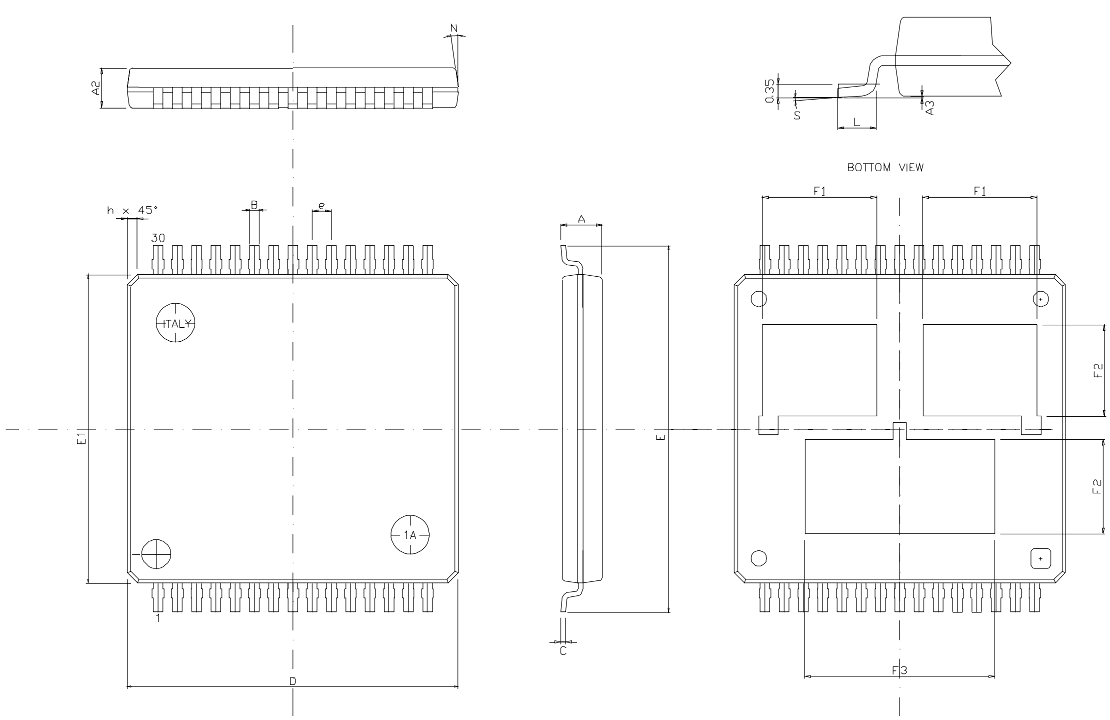
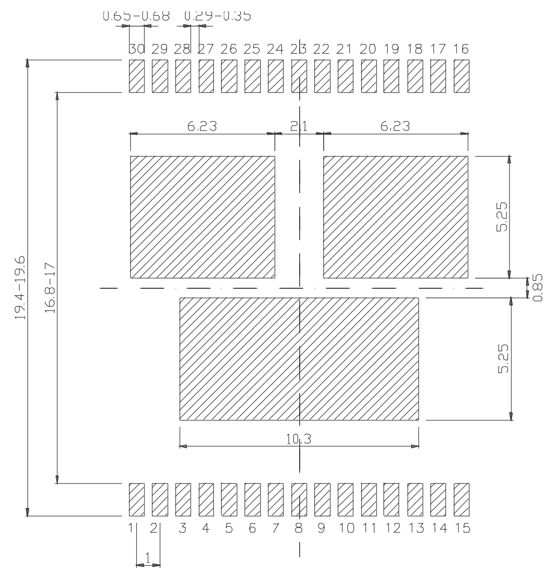


Figure 45. MultiPowerSO-30 Suggested Pad Layout



REVISION HISTORY

Date	Revision	Description of Changes
Sep. 2004	1	- First issue.