IS61LV12816

128K x 16 HIGH-SPEED CMOS STATIC RAM WITH 3.3V SUPPLY

FEBRUARY 2003

FEATURES

- High-speed access time: 10, 12, and 15 ns
- CMOS low power operation
- TTL and CMOS compatible interface levels
- Single 3.3V ± 10% power supply
- Fully static operation: no clock or refresh required
- Three state outputs
- Data control for upper and lower bytes
- Industrial temperature available

DESCRIPTION

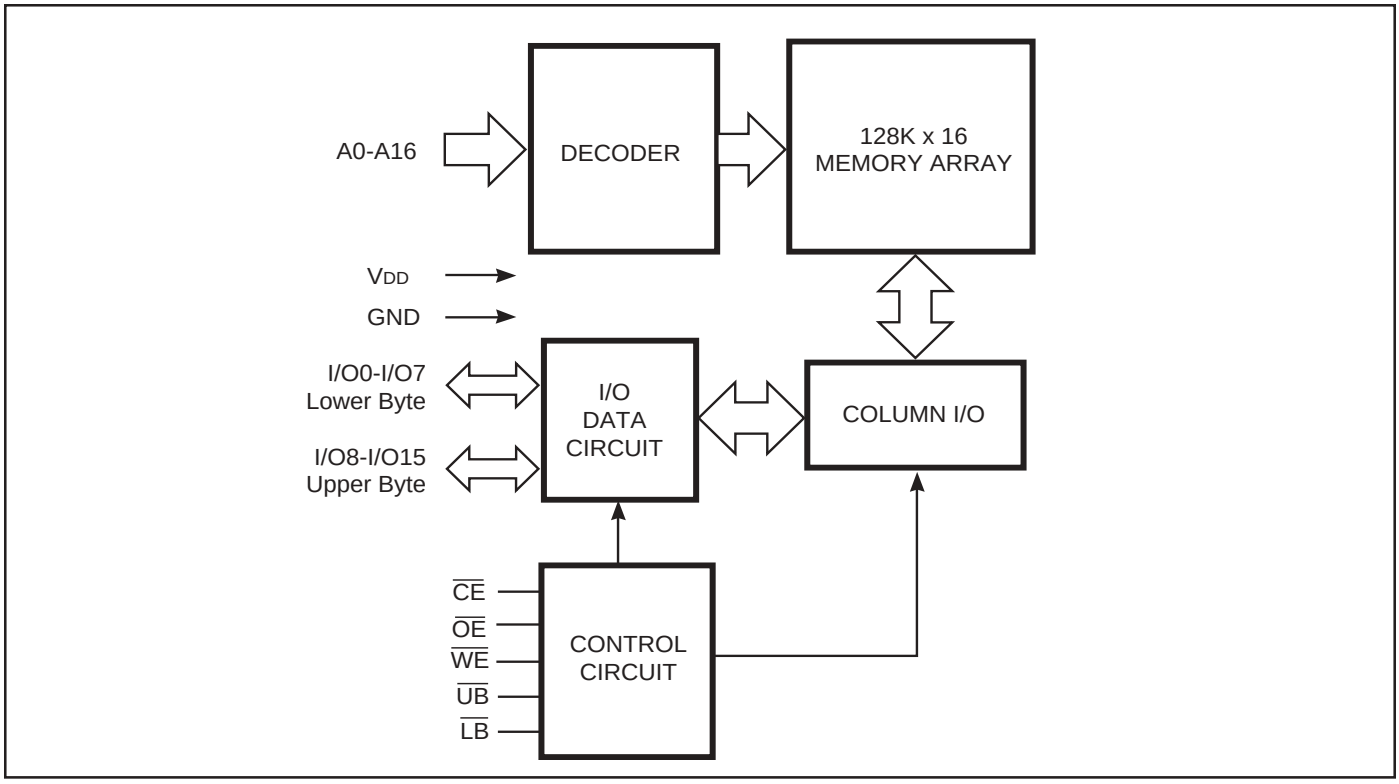
The *ISSI* IS61LV12816 is a high-speed, 2,097,152-bit static RAM organized as 131,072 words by 16 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 10 ns with low power consumption.

When $\overline{CE}$ is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs, $\overline{CE}$ and $\overline{OE}$. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory. A data byte allows Upper Byte ($\overline{UB}$) and Lower Byte ($\overline{LB}$) access.

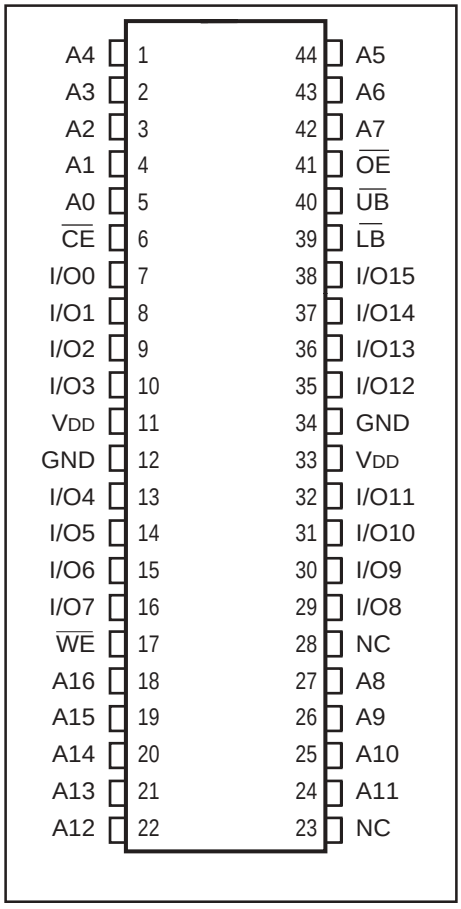
The IS61LV12816 is packaged in the JEDEC standard 44-pin 400-mil SOJ, 44-pin TSOP (Type II), 44-pin LQFP, and 48-pin mini BGA (6mm x 8mm).

FUNCTIONAL BLOCK DIAGRAM

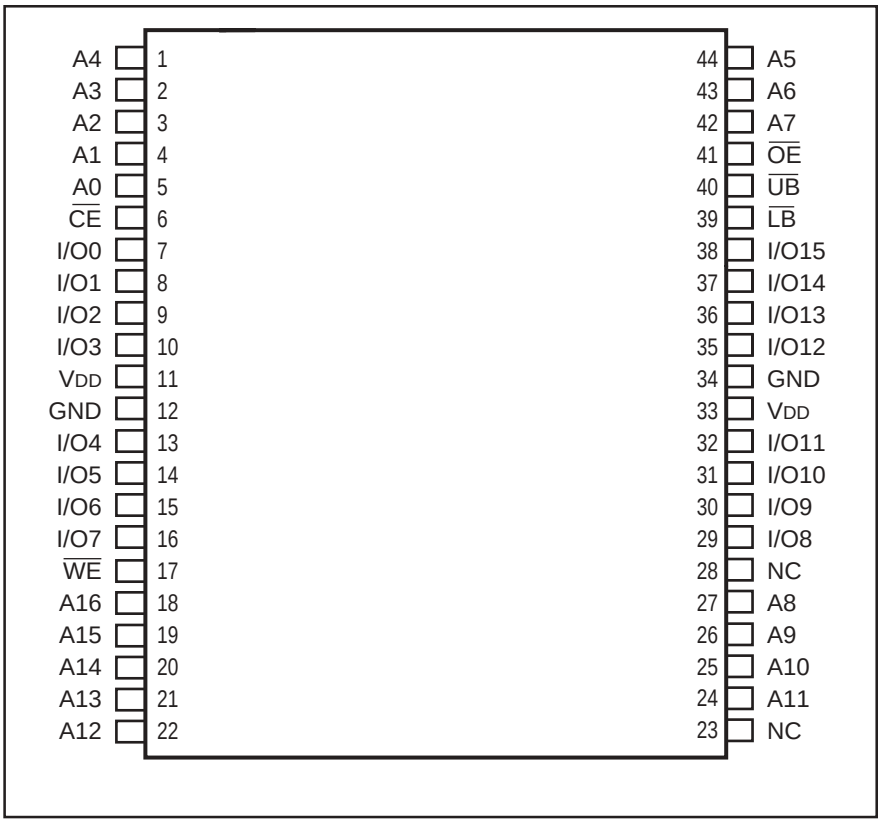


PIN CONFIGURATIONS

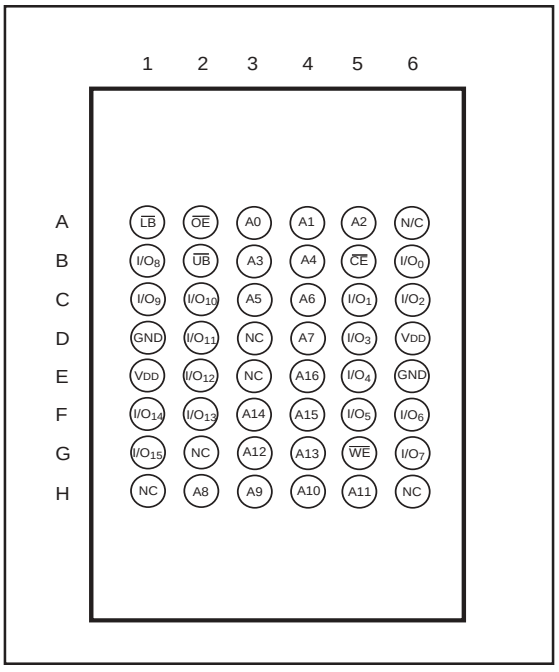
44-Pin SOJ (K)



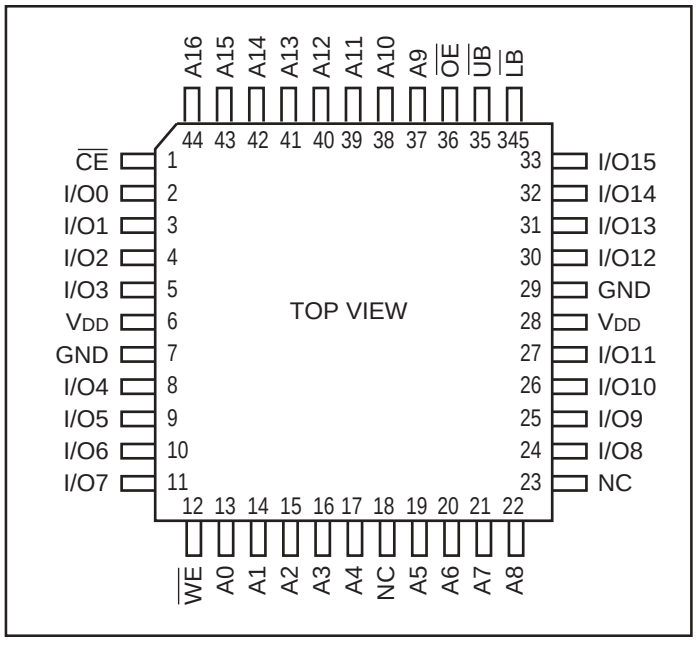
44-Pin TSOP-II (T)



48-Pin mini BGA (B)



44-Pin LQFP (LQ)



PIN DESCRIPTIONS

A0-A16	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
$\overline{LB}$	Lower-byte Control (I/O0-I/O7)
$\overline{UB}$	Upper-byte Control (I/O8-I/O15)
NC	No Connection
V_{DD}	Power
GND	Ground

OPERATING RANGE

Range	Ambient Temperature	V_{DD}
Commercial	0°C to + 70°C	3.3V ± 10%
Industrial	–40°C to + 85°C	3.3V ± 10%

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
V_{DD}	Power Supply Voltage Relative to GND	–0.3 to 4.0	V
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to V_{DD} + 0.5	V
T_{STG}	Storage Temperature	–65 to + 150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	±20	mA

Note:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = –4.0 mA	2.4	—	V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 8.0 mA	—	0.4	V
V_{IH}	Input HIGH Voltage(1)		2	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage(1)		–0.3	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{DD}	–1	1	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD}, Outputs Disabled	–1	1	µA

Note:
1. V_{IL} (min.) = –0.3V DC; V_{IL} (min.) = –2.0V AC (pulse width - 2.0 ns).
   V_{IH} (max.) = V_{DD} + 0.3V DC; V_{IH} (max.) = V_{DD} + 2.0V AC (pulse width - 2.0 ns).

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O PIN I/O0-I/O7	I/O PIN I/O8-I/O15	V_{DD} Current
Not Selected	X	H	X	X	X	High-Z	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	X	X	High-Z	High-Z	I_{CC}
	X	L	X	H	H	High-Z	High-Z	
Read	H	L	L	L	H	D_{OUT}	High-Z	I_{CC}
	H	L	L	H	L	High-Z	D_{OUT}	
	H	L	L	L	L	D_{OUT}	D_{OUT}	
Write	L	L	X	L	H	D_{IN}	High-Z	I_{CC}
	L	L	X	H	L	High-Z	D_{IN}	
	L	L	X	L	L	D_{IN}	D_{IN}	

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		-10 ns Min.	-10 ns Max.	-12 ns Min.	-12 ns Max.	-15 ns Min.	-15 ns Max.	Unit
I_{CC}	V_{DD} Operating Supply Current	V_{DD} = Max., $\overline{CE}$ = V_{IL}	Com.	—	125	—	110	—	90	mA
		I_{OUT} = 0 mA, f = Max.	Ind.	—	135	—	120	—	100	
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{DD} = Max.,	Com.	—	40	—	35	—	30	mA
		V_{IN} = V_{IH} or V_{IL}	Ind.	—	50	—	45	—	40	
		$\overline{CE}$ ≥ V_{IH}, f = max								
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{DD} = Max.,	Com.	—	10	—	10	—	10	mA
		$\overline{CE}$ ≥ V_{DD} – 0.2V,	Ind.	—	20	—	20	—	20	
		V_{IN} ≥ V_{DD} – 0.2V, or								
		V_{IN} ≤ 0.2V, f = 0								

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

CAPACITANCE[1]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0V	8	pF

Note:
1. Tested initially and after any design or process changes that may affect these parameters.

READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

		-10 ns		-12 ns		-15 ns		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{RC}	Read Cycle Time	10	—	12	—	15	—	ns
t_{AA}	Address Access Time	—	10	—	12	—	15	ns
t_{OHA}	Output Hold Time	3	—	3	—	3	—	ns
t_{ACE}	$\overline{CE}$ Access Time	—	10	—	12	—	15	ns
t_{DOE}	$\overline{OE}$ Access Time	—	4	—	5	—	6	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	—	4	—	5	0	6	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	0	—	0	—	0	—	ns
t_{HZCE}[2]	$\overline{CE}$ to High-Z Output	0	4	0	5	0	8	ns
t_{LZCE}[2]	$\overline{CE}$ to Low-Z Output	3	—	3	—	3	—	ns
t_{BA}	$\overline{LB}$, $\overline{UB}$ Access Time	—	4	—	5	—	6	ns
t_{HZB}[2]	$\overline{LB}$, $\overline{UB}$ to High-Z Output	0	4	0	5	0	6	ns
t_{LZB}[2]	$\overline{LB}$, $\overline{UB}$ to Low-Z Output	0	—	0	—	0	—	ns

Notes:
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS

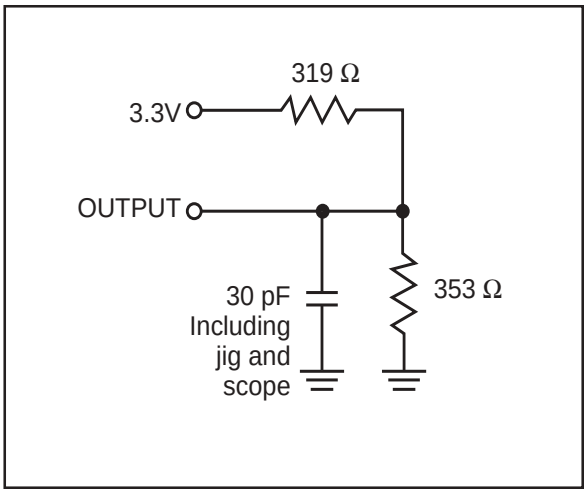


Figure 1.

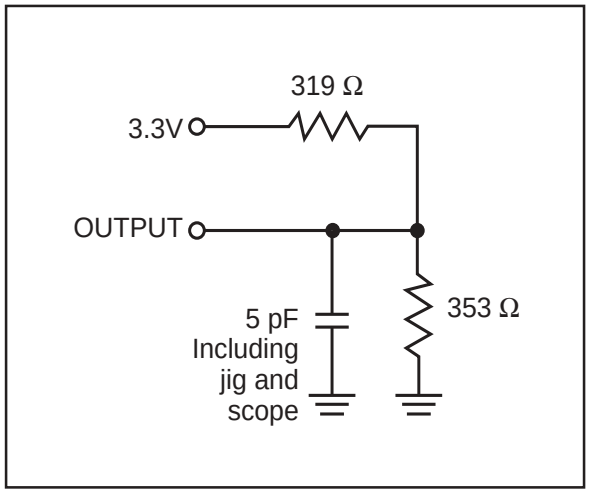
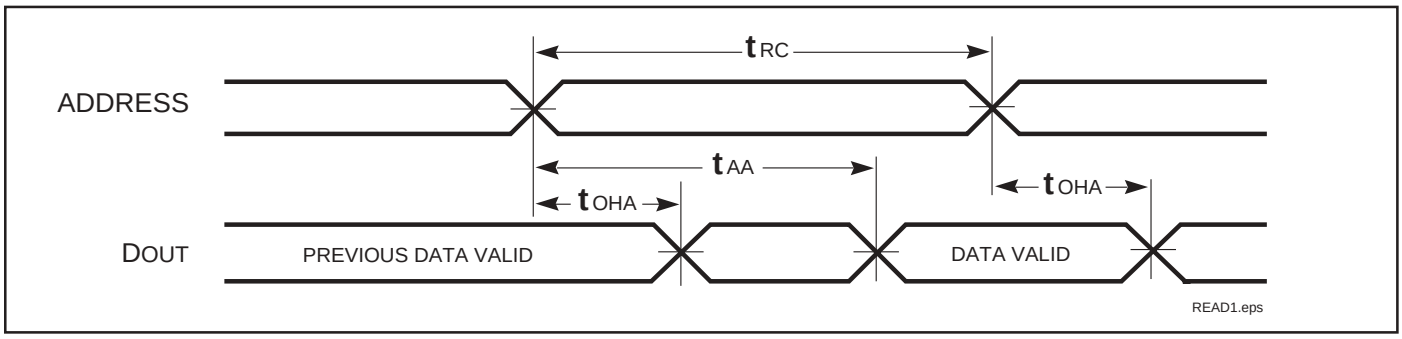


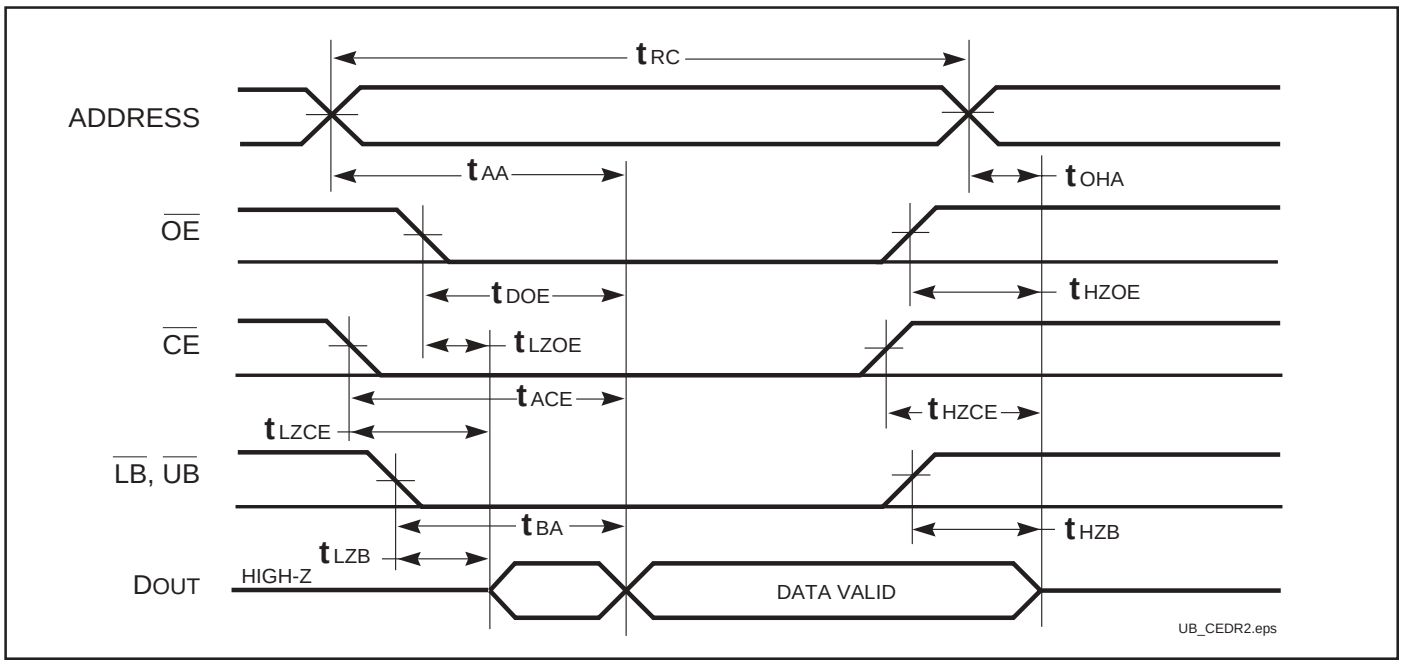
Figure 2.

AC WAVEFORMS

READ CYCLE NO. 1[1,2] (Address Controlled) ($\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{UB}$ or $\overline{LB}$ = V_{IL})



READ CYCLE NO. 2[1,3]



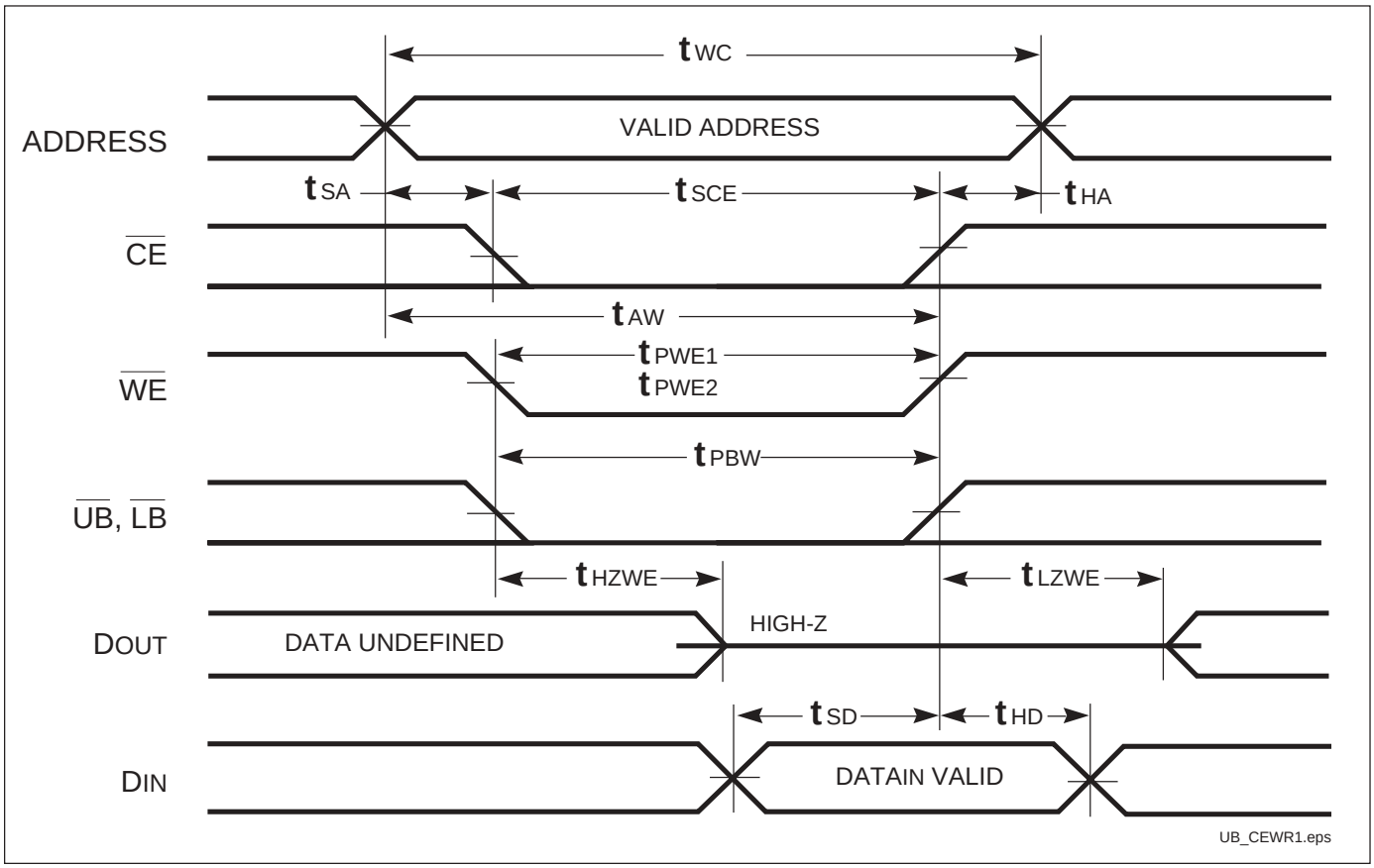
Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{UB}$, or $\overline{LB}$ = V_{IL}.
3. Address is valid prior to or coincident with $\overline{CE}$ LOW transition.

WRITE CYCLE SWITCHING CHARACTERISTICS[1,3] (Over Operating Range)

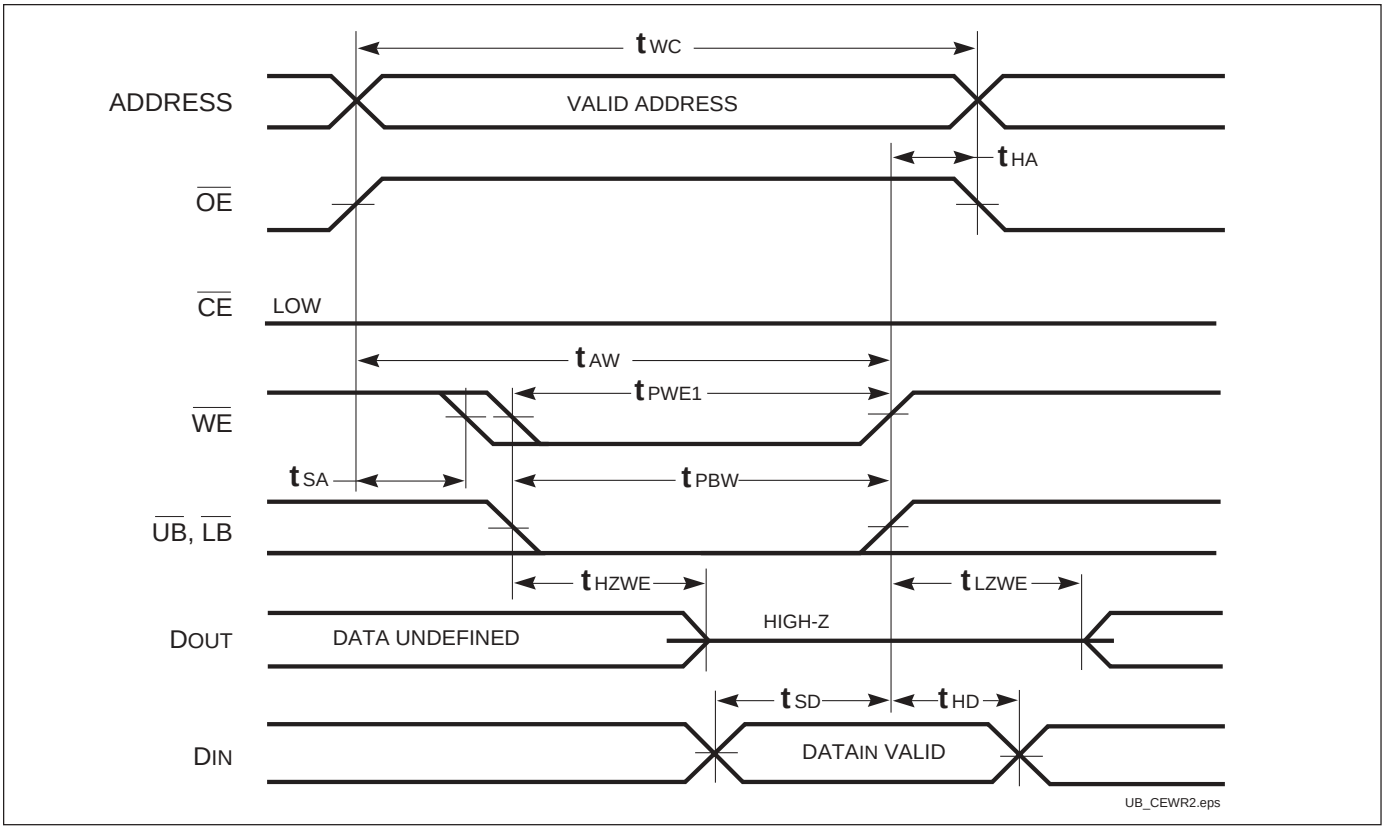
Symbol	Parameter	-10 ns Min.	-10 ns Max.	-12 ns Min.	-12 ns Max.	-15 ns Min.	-15 ns Max.	Unit
t_{WC}	Write Cycle Time	10	—	12	—	15	—	ns
t_{SCE}	$\overline{CE}$ to Write End	8	—	8	—	10	—	ns
t_{AW}	Address Setup Time to Write End	8	—	8	—	10	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	0	—	ns
t_{PWB}	$\overline{LB}$, $\overline{UB}$ Valid to End of Write	8	—	9	—	10	—	ns
t_{PWE1}	$\overline{WE}$ Pulse Width ($\overline{OE}$ = HIGH)	7	—	8	—	10	—	ns
t_{PWE2}	$\overline{WE}$ Pulse Width ($\overline{OE}$ = LOW)	8	—	10	—	11	—	ns
t_{SD}	Data Setup to Write End	5	—	6	—	7	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	0	—	ns
t_{HZWE}[3]	$\overline{WE}$ LOW to High-Z Output	—	4	—	5	—	6	ns
t_{LZWE}[3]	$\overline{WE}$ HIGH to Low-Z Output	0	—	0	—	0	—	ns

Notes:
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{UB}$ or $\overline{LB}$, and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
3. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

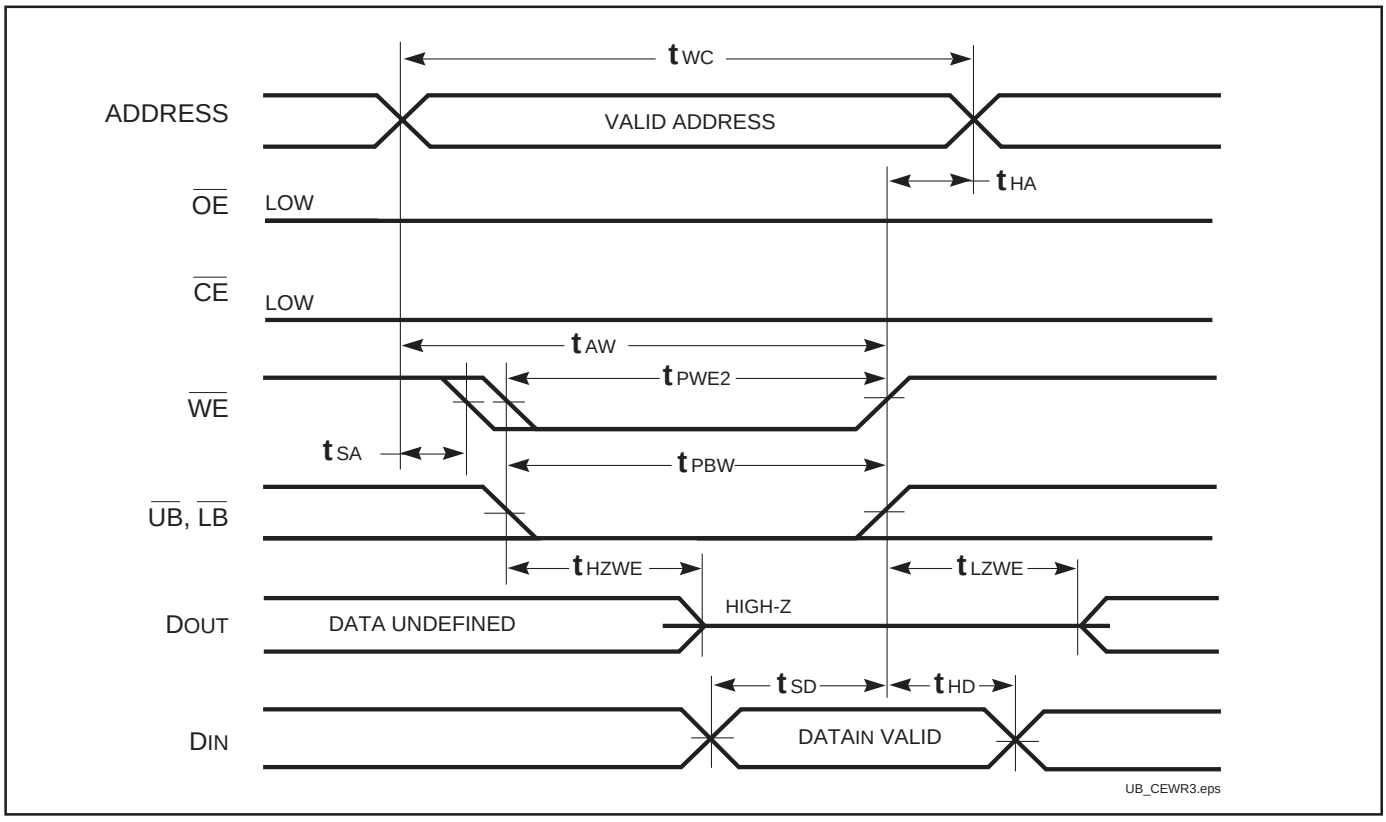
WRITE CYCLE NO. 1[1,2] ($\overline{CE}$ Controlled, $\overline{OE}$ = HIGH or LOW)



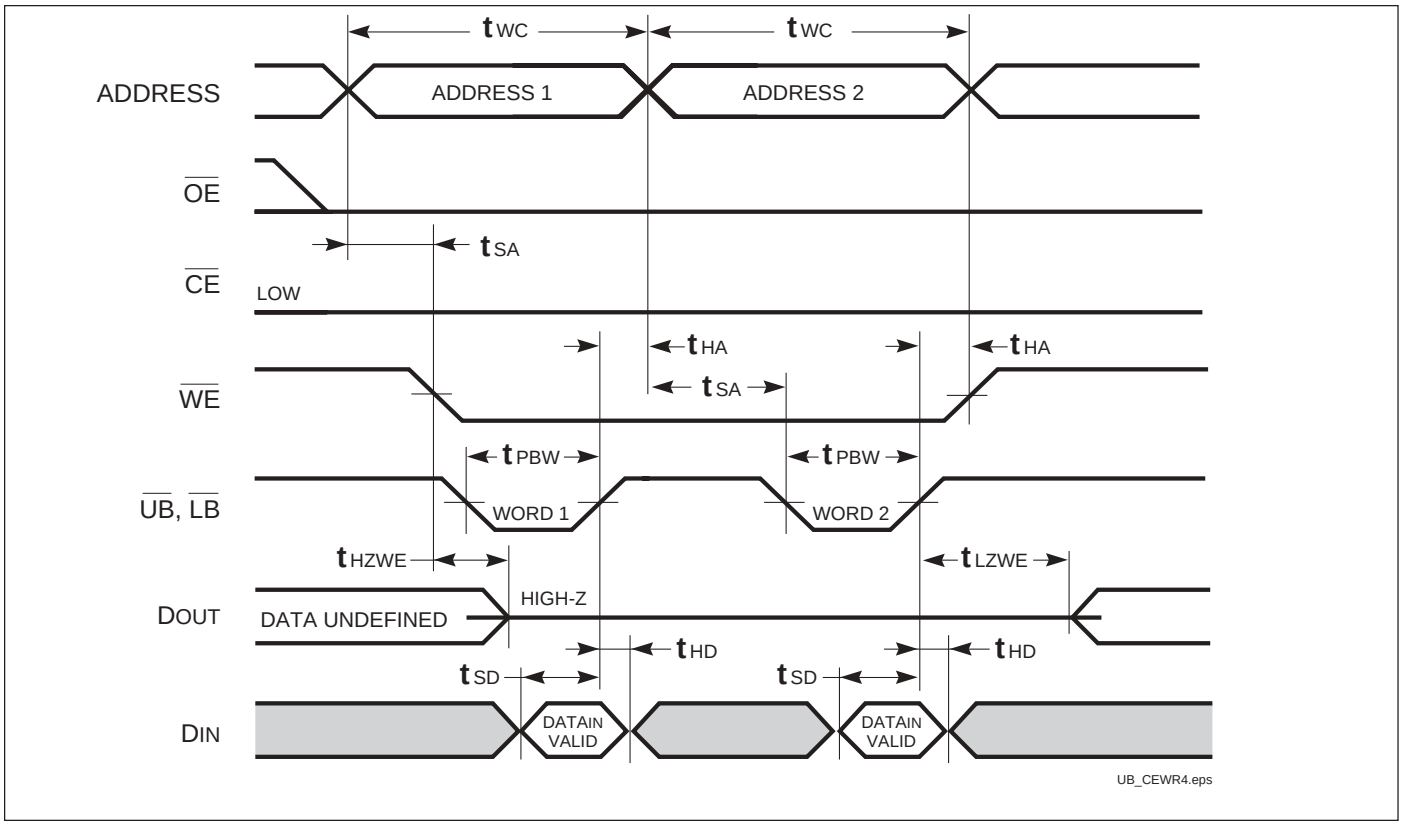
WRITE CYCLE NO. 2[1] ($\overline{WE}$ Controlled, $\overline{OE}$ = HIGH during Write Cycle)



WRITE CYCLE NO. 3 ($\overline{WE}$ Controlled: $\overline{OE}$ is LOW During Write Cycle)



WRITE CYCLE NO. 4 ($\overline{LB}$, $\overline{UB}$ Controlled, Back-to-Back Write) (1,3)



Notes:

1. The internal Write time is defined by the overlap of $\overline{CE}$ = LOW, $\overline{UB}$ and/or $\overline{LB}$ = LOW, and $\overline{WE}$ = LOW. All signals must be in valid states to initiate a Write, but any can be deasserted to terminate the Write. The t_{SA}, t_{HA}, t_{SD}, and t_{HD} timing is referenced to the rising or falling edge of the signal that terminates the Write.
2. Tested with $\overline{OE}$ HIGH for a minimum of 4 ns before $\overline{WE}$ = LOW to place the I/O in a HIGH-Z state.
3. $\overline{WE}$ may be held LOW across many address cycles and the $\overline{LB}$, $\overline{UB}$ pins can be used to control the Write function.

IS61LV12816 STANDARD VERSION ORDERING INFORMATION
Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
10	IS61LV12816-10B	mini BGA (6mm x 8mm)
	IS61LV12816-10K	400-mil Plastic SOJ
	IS61LV12816-10LQ	LQFP
	IS61LV12816-10T	Plastic TSOP-II
12	IS61LV12816-12B	mini BGA (6mm x 8mm)
	IS61LV12816-12K	400-mil Plastic SOJ
	IS61LV12816-12LQ	LQFP
	IS61LV12816-12T	Plastic TSOP-II
15	IS61LV12816-15B	mini BGA (6mm x 8mm)
	IS61LV12816-15LQ	LQFP
	IS61LV12816-15T	Plastic TSOP-II

IS61LV12816 STANDARD VERSION ORDERING INFORMATION
Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
10	IS61LV12816-10BI	mini BGA (6mm x 8mm)
	IS61LV12816-10KI	400-mil Plastic SOJ
	IS61LV12816-10LQI	LQFP
	IS61LV12816-10TI	Plastic TSOP-II
12	IS61LV12816-12LQI	LQFP
	IS61LV12816-12TI	Plastic TSOP-II
15	IS61LV12816-15BI	mini BGA (6mm x 8mm)
	IS61LV12816-15LQI	LQFP
	IS61LV12816-15TI	Plastic TSOP-II