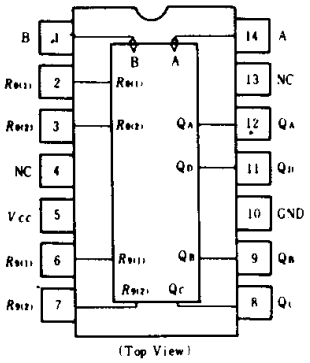
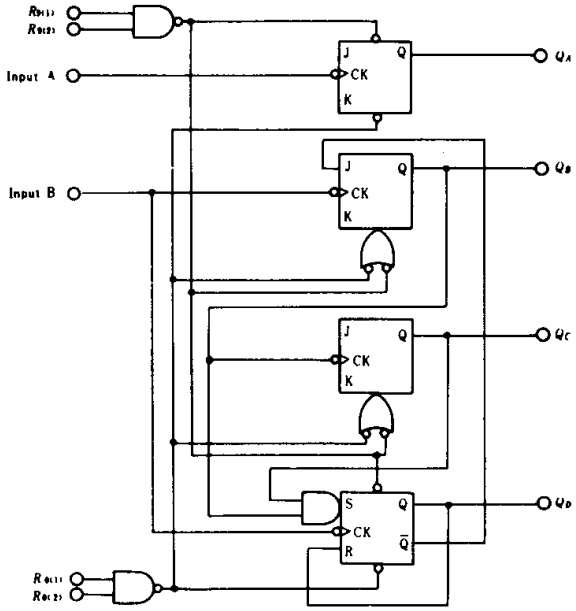
HD74LS90 ●Decade Counters

The HD74LS90 contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and three-stage binary counter for divide-by-five. This device has a gated zero reset and also has gated set-to-nine inputs for use in BCD nine's complement applications. To use this maximum count length of this counter the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are descrived in the appropriate function table. A symmetrical divide-by-ten count can be obtained from HD-74LS90 counter by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

■PIN ARRANGEMENT



■BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS

Item		Symbol	Ratings	Unit
Supply voltage		V_{CC}	7.0	V
Input voltage	R Inputs	V_{IN}	7.0	V
	A, B Inputs		5.5	V
Operating temperature range		T_{opr}	−20 ~ +75	℃
Storage temperature range		T_{stg}	−65 ~ +150	℃

■FUNCTION TABLE

Reset/Count Function Table

Reset Inputs				Outputs			
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	×	L	L	L	L
H	H	×	L	L	L	L	L
×	×	H	H	H	L	L	H
×	L	×	L	Count			
L	×	L	×	Count			
L	×	×	L	Count			
×	L	L	×	Count			

BCD Count Sequence(Notes1)

Count	Outputs			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

Bi-Quinary Count Sequence(Notes2)

Count	Qutputs			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

Notes) 1. Output Q_A is connected to input B for BCD count.
2. Output Q_D is connected to input A for Bi-quinary count.
3. H; high level, L; low level, X; irrelevant.

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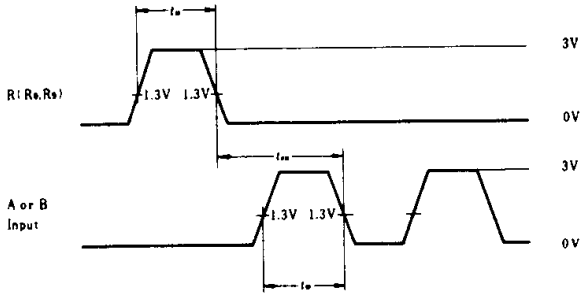
■RECOMMENDED OPERATING CONDITIONS

Item		Symbol	min	typ	max	Unit
Count frequency	A input	f_{count}	0	—	32	MHz
	B input		0	—	16	
Pulse width	A input	t_w	15	—	—	ns
	B input		30	—	—	
	Reset inputs		15	—	—	
Setup time		t_{su}	25	—	—	ns

■TIMING DEFINITION



■ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75°C$)

Item		Symbol	Test Conditions		min	typ*	max	Unit
Input voltage		V_{IH}			2.0	—	—	V
		V_{IL}			—	—	0.8	V
Output voltage		V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	—	—	V
		V_{OL}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$	$I_{OL}=4mA$**	—	—	0.4	V
				$I_{OL}=8mA$**	—	—	0.5	
Input current	Any Reset	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$		—	—	−0.4	mA
	A input				—	—	−2.4	
	B input				—	—	−3.2	
	Any Reset	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$		—	—	20	μA
	A input				—	—	40	
	B input				—	—	80	
	Any Reset	I_I	$V_{CC}=5.25V$	$V_I=7V$	—	—	0.1	mA
	A input			$V_I=5.5V$	—	—	0.2	
	B input				—	—	0.4	
Short-circuit output current		I_{OS}	$V_{CC}=5.25V$		−20	—	−100	mA
Supply current ***		I_{CC}	$V_{CC}=5.25V$		—	9	15	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$, $I_{IN}=-18mA$		—	—	−1.5	V

* V_{CC}=5V, Ta=25°C

** Q_A output is tested at specified I_{OL} plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan out capability.

*** I_{CC} is measured with all outputs open, both R_0 inputs grounded following momentary connection to 4.5V, and all other inputs grounded.

■SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25°C$)

Item	Symbol	Inputs	Outputs	Test Conditions	min	typ	max	Unit
Maximum count frequency	f_{max}	A	Q_A	$C_L=15pF$, $R_L=2k\Omega$	32	42	—	MHz
		B	Q_B		16	—	—	
Propagation delay time	t_{PLH}	A	Q_A		—	10	16	ns
	t_{PHL}				—	12	18	
	t_{PLH}	B	Q_D		—	32	48	ns
	t_{PHL}				—	34	50	
	t_{PLH}	B	Q_B		—	10	16	ns
	t_{PHL}				—	14	21	
	t_{PLH}	B	Q_C		—	21	32	ns
	t_{PHL}				—	23	35	
	t_{PLH}	B	Q_D		—	21	32	ns
	t_{PHL}				—	23	35	
	t_{PHL}	Set-to-0	$Q_A \sim Q_D$		—	26	40	ns
	t_{PLH}	Set-to-9	Q_A, Q_D		—	20	30	ns
	t_{PHL}		Q_B, Q_C		—	26	40	

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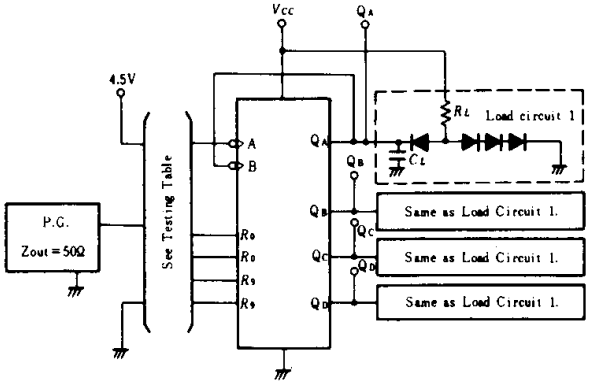
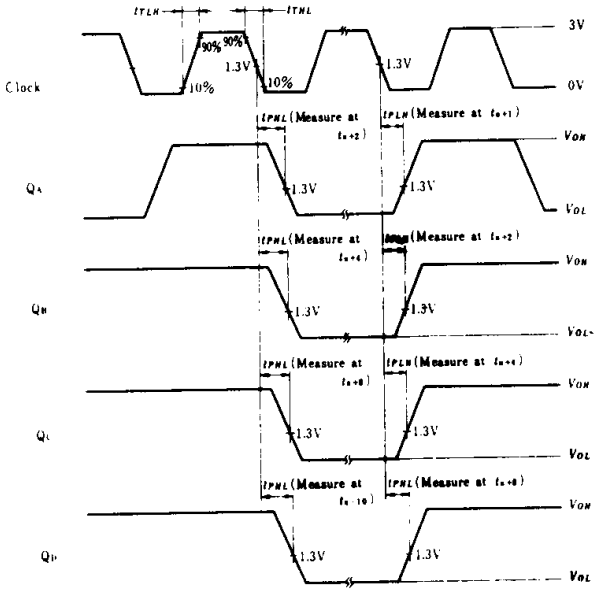
■TESTING METHOD

1) Test Circuit



Notes) 1. Input pulse; $t_{TLH} \leqq 15$ns. $t_{THL} \leqq 6$ns, $PRR = 1$MHz, duty cycle=50%
2. C_L includes probe and jig capacitance.
3. All diodes are 1S2074 Ⓗ.

Waveform-1 f_{max}, t_{PLH}, t_{PHL}(Clock→Q)



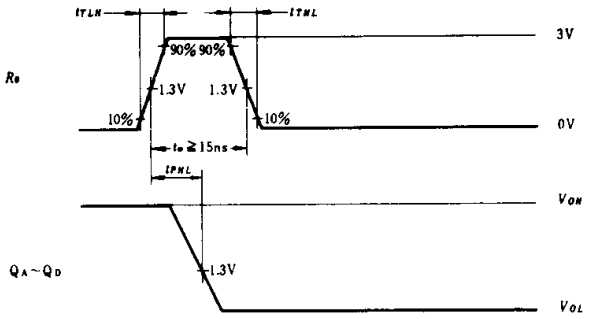
Notes) 1. Input pulse; $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 5$ns, $PRR = 1$MHz, duty cycle=50% and: for f_{max}, $t_{TLH} = t_{THL} \leqq 2.5$ns.
2. t_n is reference bit time when all outputs are low.

2) Testing Table

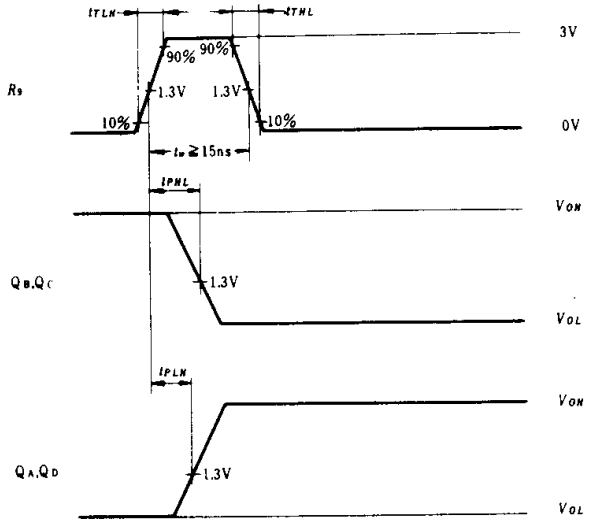
Item	From input to output	Inputs A	B	R_0	R_9	Outputs Q_A	Q_B	Q_C	Q_D
f_{max}	A→Q	IN	to Q_A	GND	GND	Out	Out	Out	Out
	B→Q	4.5V	IN	GND	GND	–	Out	Out	Out
t_{PLH} t_{PHL}	A→Q_A	IN	to Q_A	GND	GND	Out	–	–	–
	A→Q_D	IN	to Q_A	GND	GND	–	–	–	Out
	B→Q_B	4.5V	IN	GND	GND	–	Out	–	–
	B→Q_C	4.5V	IN	GND	GND	–	–	Out	–
	B→Q_D	4.5V	IN	GND	GND	–	–	–	Out
	R_0^{**}→Q	IN*	to Q_A	IN	GND	Out	Out	Out	Out
	R_9^{**}→Q	IN*	to Q_A	GND	IN	Out	Out	Out	Out

*; For initialized
**; Measured with each input and unused inputs at 4.5V.

Waveform-2 t_{PHL}(R_0→Q)



Waveform-3 t_{PLH}, t_{PHL}(R_9→Q)



Notes) 1. $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 5$ns.

PACKAGING INFORMATIONS

T-90-20

Factory orders for circuits described in this databook should include a three-part type number as explained in the following example.

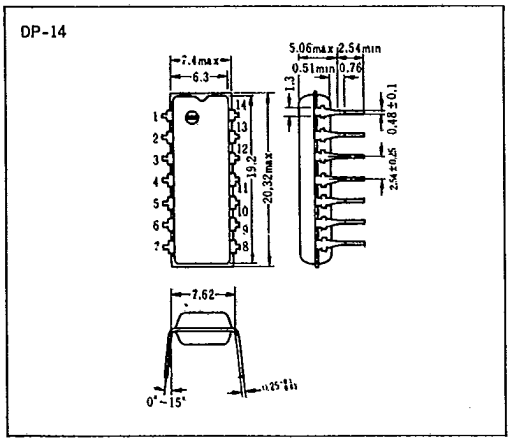
HD 74LS00 P

- Package ; Plastic DIP ; letters P
  Cerdip ; non-letters
- Circuit description
- Prefix : HD ; Hitachi Digital IC

■Plastic DIP

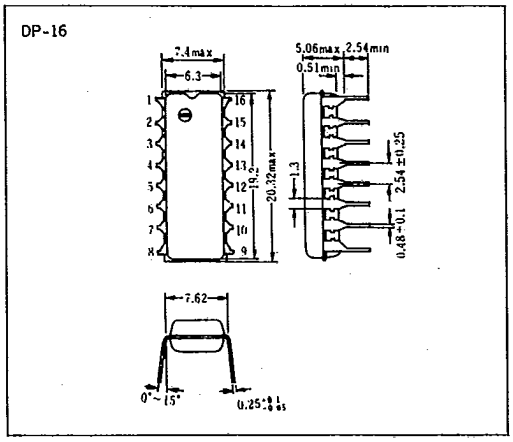
●14 Pin

DP-14



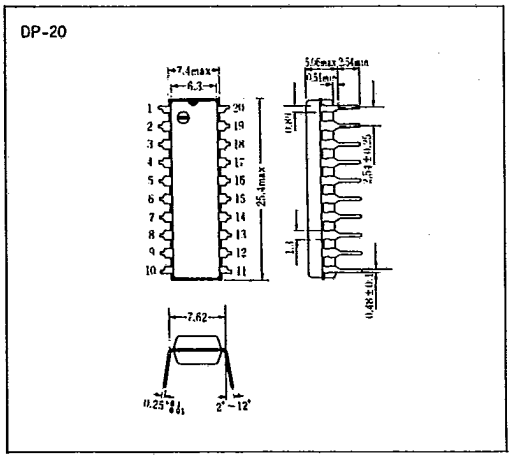
●16 Pin

DP-16



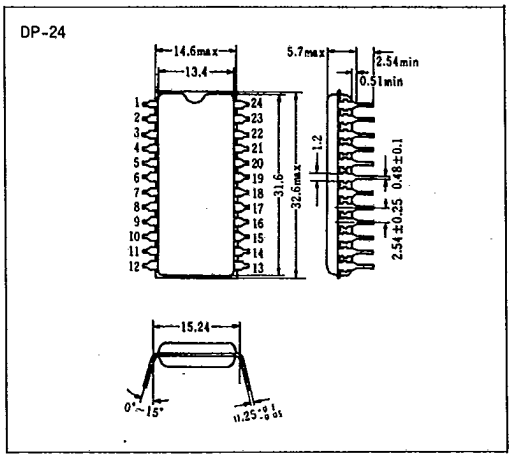
●20 Pin

DP-20



●24 Pin

DP-24

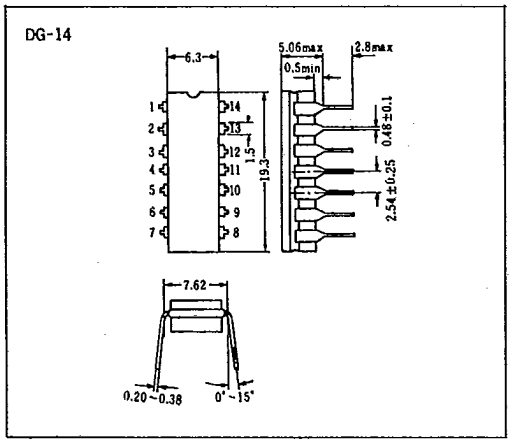


PACKAGING INFORMATIONS

■Cerdip

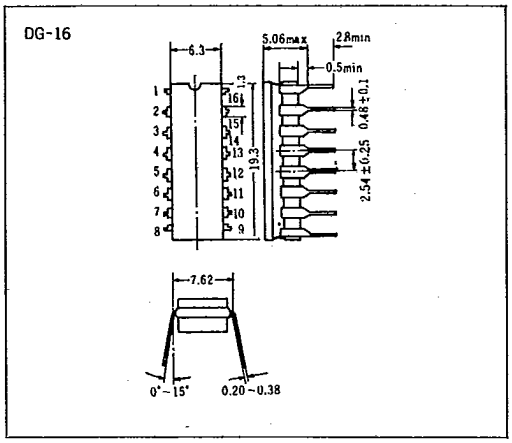
●14 Pin

DG-14



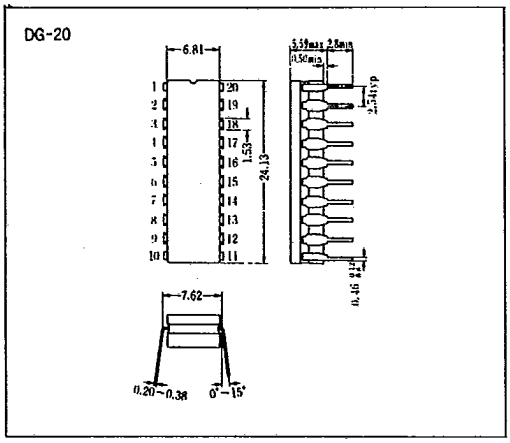
●16 Pin

DG-16



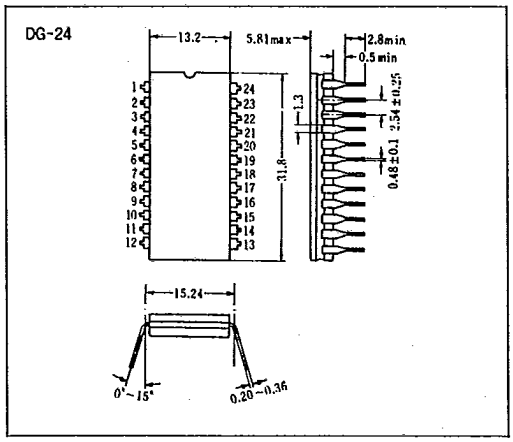
●20 Pin

DG-20



●24 Pin

DG-24



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