

FEATURES

- 3 CMOS outputs with OE tri-state control
- Low current consumption:

PLL600-27T: <4.5mA @ 27MHz with standard

CMOS buffer (3.3V)

PLL600-37T: <3.0mA @ 27MHz with CMOS compatible Clipped buffer, offering the lowest current consumption

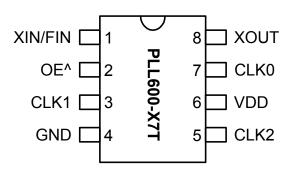
(3.3V)

- 10 to 52MHz fundamental crystal input.
- Low phase noise (-130 dBc @ 10kHz offset).
- Low jitter (RMS): 2.5ps period jitter.
- 12mA drive capability at TTL output.
- 1.62V to 3.63V DC operation.
- Available in 8 pin SOIC.

DESCRIPTION

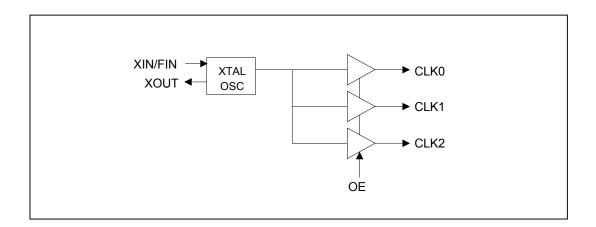
The PLL600-27T/-37T form a low cost family of XO IC's, designed to replace multiple XO solutions saving the cost and board space of clock distribution buffers. In addition, they provide among the lowest current on the market for the 10MHz to 52MHz range. They accept input crystals from 10 to 52MHz (fundamental resonant mode) and provide low phase noise (<-130dBc at 10kHz offset at 30MHz), and very low jitter (2.5 ps RMS period jitter) outputs.

PIN ASSIGNMENT



^: Denotes internal Pull-up

BLOCK DIAGRAM





PIN DESCRIPTION

| Name | Pin # | Туре | Description |
|---------|-------|------|---|
| XIN/FIN | 1 | I | Crystal input (10MHz to 52MHz) or Ref Clock input. |
| OE | 2 | I | Output Enable input. This pin has internal pull-up resistor. All outputs will be tri-stated when low. |
| CLK1 | 3 | 0 | Output clock. |
| GND | 4 | Р | Ground. |
| CLK2 | 5 | 0 | Output clock. |
| VDD | 6 | Р | Power supply. |
| CLK0 | 7 | 0 | Output clock. |
| XOUT | 8 | | Crystal output. |

ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

| PARAMETERS | SYMBOL | MIN. | MAX. | UNITS |
|-----------------------------------|----------|------|----------------------|-------|
| Supply Voltage | V_{DD} | | 4.6 | V |
| Input Voltage, dc | Vı | -0.5 | V _{DD} +0.5 | V |
| Output Voltage, dc | Vo | -0.5 | V _{DD} +0.5 | V |
| Storage Temperature | Ts | -65 | 150 | °C |
| Ambient Operating Temperature* | TA | -40 | 85 | °C |
| Junction Temperature | TJ | | 125 | °C |
| Lead Temperature (soldering, 10s) | | | 260 | °C |
| ESD Protection, Human Body Model | | | 2 | kV |

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

2. AC Electrical Specifications

| PARAMETERS | CONDITIONS | MIN. | TYP. | MAX. | UNITS | |
|-------------------------------|------------------------------------|------|------|------|-------|--|
| Input Crystal Frequency | | 10 | | 52 | MHz | |
| Settling time | At power-up (Vdd reaches 1.62V) | | | 10 | ms | |
| Output Clock Rise/Fall Time | 0.8V ~ 2.0V with 10 pF load | | 1.15 | | ns | |
| Output Clock Rise/Fall Tillle | 0.3V ~ 3.0V with 15 pF load | | 2.4 | | | |
| VDD sensitivity | Frequency vs. VDD +/- 10% | 0.8 | | 0.8 | ppm | |
| Output Clock Duty Cycle | Measured @ 50% V _{DD} | 45 | 50 | 55 | % | |
| Short Circuit Current | | | ±50 | | mA | |

^{*} Note: Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for COMMERCIAL grade only.



3. Jitter and Phase Noise Specifications

| PARAMETERS | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|---|---|------|------|------|--------|
| RMS Period Jitter (1 sigma – 1000 samples) | With capacitive decoupling between VDD and GND. | | 2.1 | 2.5 | ps |
| Phase Noise relative to carrier | 30MHz @100Hz offset | | -80 | | dBc/Hz |
| Phase Noise relative to carrier | 30MHz @1kHz offset | | -110 | | dBc/Hz |
| Phase Noise relative to carrier | 30MHz @10kHz offset | | -130 | | dBc/Hz |
| Phase Noise relative to carrier | 30MHz @100kHz offset | | -138 | | dBc/Hz |
| Phase Noise relative to carrier | 30MHz @1MHz offset | | -145 | | dBc/Hz |

4. DC Specifications

| PARAMETERS | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|--|-----------------|---|-----------------------|-----------|-----------|-------|
| Supply Current, Dynamic, | | At 10MHz, Cload=15pF | | 2.0 / 1.5 | 2.5 / 2.0 | |
| with Loaded Outputs | I _{DD} | At 13.5MHz, Cload=15pF | | 2.4 / 1.6 | 3.0 / 2.0 | |
| (at VDD = 3.3V) | | At 17.7MHz, Cload=15pF | | 3.0 / 2.0 | 3.5 / 2.5 | mA |
| Respectively for PLL600 -27T/-37T | | At 27MHz, Cload=15pF | | 4.0 / 2.5 | 4.5 / 3.0 | |
| -2/1/-3/1 | | At 48MHz, Cload=15pF | | 7.0 / 4.0 | 7.5 / 4.5 | |
| Supply Current in tri-state | I _{DD} | Output disabled | | | 520 | μΑ |
| Operating Voltage | V_{DD} | | 1.62 | | 3.63 | V |
| Output High Voltage | V _{он} | $-27T I_{OH} = -12mA^{(1)} (3.3V)$ | 2.4 | | | V |
| Output High voltage | | $-37T^{(1)}$, I _{OH} = $-12mA^{(1)}$ (3.3V) | 2.4 | 2.9 | | V |
| Output Law Valtage | Vol | $-27T I_{OL} = 12mA^{(1)} (3.3V)$ | | | 0.4 | V |
| Output Low Voltage | | $-37T^{(1)}$, $I_{OL} = 12mA^{(1)}(3.3V)$ | | 0.32 | 0.4 | V |
| Output High Voltage at CMOS level (PLL600-27T) | Vонс | I _{OH} = -4mA | V _{DD} - 0.4 | | | V |
| Output drive current (PLL600-27T) | | At TTL level (3.3V) | 12 | 17 | | mA |

^{(1):} P600-37T has non-standard CMOS VOH and VOL levels for lower current consumption, but meets CMOS input stage needs. P600-37T should be used to drive pure capacitive loads only.

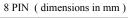
5. Crystal Specifications

| PARAMETERS | SYMBOL | MIN. | TYP. | MAX. | UNITS |
|----------------------------------|-----------------------|------|------|------|-------|
| Crystal Resonator Frequency | FXIN | 10 | | 52 | MHz |
| Crystal Loading Rating | C _{L (xtal)} | | 8.5 | | pF |
| Maximum Sustainable Drive Level | | | | 200 | μW |
| Operating Drive Level | | | 50 | | μW |
| C0 (for frequencies below 30MHz) | | | | 5 | pF |
| C0 (for frequencies above 30MHz) | | | | 4 | pF |
| ESR | Rs | | | 30 | Ω |

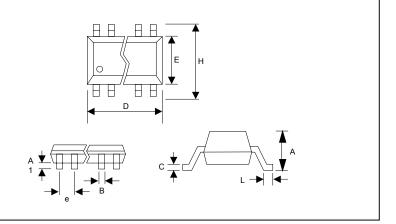
Note: A detailed crystal specification document is also available for this part



PACKAGE INFORMATION



| | Narrow SOIC | | | |
|--------|-------------|------|--|--|
| Symbol | Min. | Max. | | |
| A | 1.47 | 1.73 | | |
| A1 | 0.10 | 0.25 | | |
| В | 0.33 | 0.51 | | |
| C | 0.19 | 0.25 | | |
| D | 4.80 | 4.95 | | |
| Е | 3.80 | 4.00 | | |
| Н | 5.80 | 6.20 | | |
| L | 0.38 1.27 | | | |
| e | 1.27 BSC | | | |



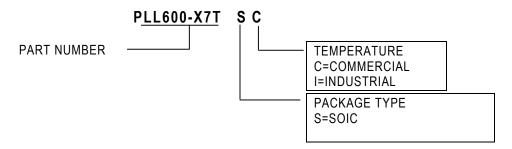
ORDERING INFORMATION

For part ordering, please contact our Sales Department:

47745 Fremont Blvd., Fremont, CA 94538, USA Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of the following: Device number, Package type and Operating temperature range



| Order Number | Marking | Package Option |
|-----------------|-------------|----------------------------|
| PLL600-27T SC | P600-27T SC | 8 pin SOIC - Tubes |
| PLL600-27T SC-R | P600-27T SC | 8 pin SOIC - Tape and Reel |
| PLL600-37T SC | P600-37T SC | 8 pin SOIC - Tubes |
| PLL600-37T SC-R | P600-37T SC | 8 pin SOIC - Tape and Reel |

PhaseLink Corporation, reserves the right to make changes in its products or specifications, or both at any time without notice. The information furnished by PhaseLink is believed to be accurate and reliable. However, PhaseLink makes no guarantee or warranty concerning the accuracy of said information and shall not be responsible for any loss or damage of whatever nature resulting from the use of, or reliance upon this product.

LIFE SUPPORT POLICY: PhaseLink's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of PhaseLink Corporation.