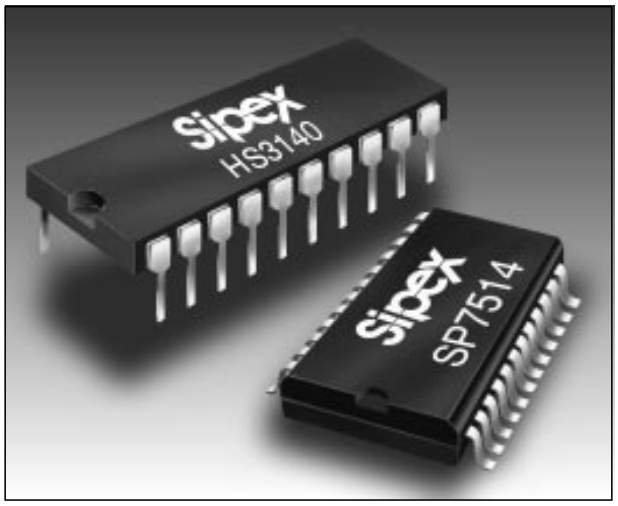
SP7514 and HS3140

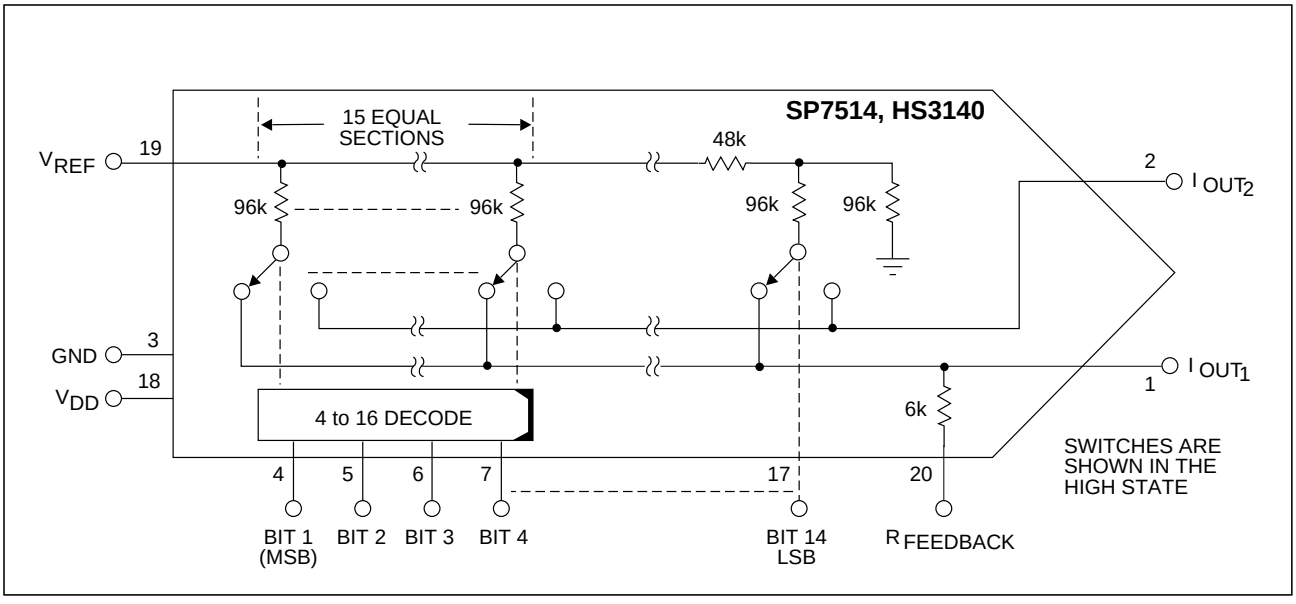
14-Bit Multiplying DACs

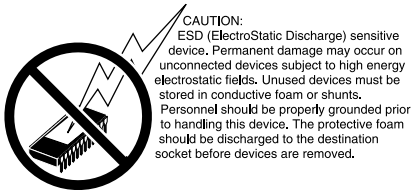
- Monolithic Construction
- 14–Bit Resolution
- 0.003% Non-Linearity
- Four-Quadrant Multiplication
- Latch-up Protected
- Low Power - 30mW
- Single +15V Power Supply



DESCRIPTION…

The **SP7514** and **HS3140** are precision 14-bit multiplying DACs, that provide four-quadrant multiplication. Both parts accept both AC and DC reference voltages. The **SP7514** is available for use in commercial and industrial temperature ranges, packaged in a 20-pin SOIC. The **HS3140** is available in commercial and military temperature ranges, packaged in a 20-pin side-brazed DIP.





SPECIFICATIONS

(Typical @ 25°C, nominal power supply, V_{REF} = +10V, unipolar unless otherwise noted)

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DIGITAL INPUT					
Resolution	14			Bits	
2–Quad, Unipolar Coding		Binary			
4–Quad, Bipolar Coding		Offset Binary			
Logic Compatibility		CMOS, TTL			Note 1
Input Current			±1	µA	
REFERENCE INPUT					
Voltage Range			±25	V	Note 2
Input Impedance	3.25		9.75	KOhms	
ANALOG OUTPUT					
Scale Factor	75		225	$\mu A/V_{REF}$	
Scale Factor Accuracy			±1	%	Note 3
Output Leakage			10	nA	Note 4
Output Capacitance					
C_{OUT} 1, all inputs high		100		pF	
C_{OUT} 1, all inputs low		50		pF	
C_{OUT} 2, all inputs high		50		pF	
C_{OUT} 2, all inputs low		100		pF	
STATIC PERFORMANCE					
Integral Linearity					Note 5
SP7514KN/BN, HS3140–4		±0.003	±0.006	% FSR	
SP7514JN/AN, HS3140–3		±0.006	±0.012	% FSR	
Differential Linearity					Note 6
SP7514KN/BN, HS3140–4		±0.003	±0.006	%FSR	
SP7514JN/AN, HS3140–3		±0.006	±0.012	% FSR	
Monotonicity					
SP7514KN/BN, HS3140–4		Guaranteed to 14 bits			
SP7514JN/AN, HS3140–3		Guaranteed to 13 bits			
STABILITY					(T_{MIN} to T_{MAX})
Scale Factor		4		ppm FSR/°C	Note 7 and 8
Integral Linearity		0.5	1.0	ppm FSR/°C	
Differential Linearity		0.5	1.0	ppm FSR/°C	
Monotonicity Temp. Range					
SP7514JN/KN, **HS3140C**	0		+70	°C	
SP7514AN/BN	–40		+85	°C	
HS3140B	–55		+125	°C	
DYNAMIC PERFORMANCE					
Digital Small Signal Settling		1.0		µS	
Digital Full Scale Settling		2.0		µS	
Reference Feedthrough Error					(V_{REF} = 20Vpp)
@ 1kHz		200		µV	
@ 10kHz		2		mV	
Reference Input Bandwidth		1		MHz	
POWER SUPPLY (V_{DD})					
Operating Voltage		+15 ±5%		V	
Voltage Range	+8		+18	V	
Current			2.0	mA	Note 9
Rejection Ratio		0.005		%/%	

SPECIFICATIONS (continued)

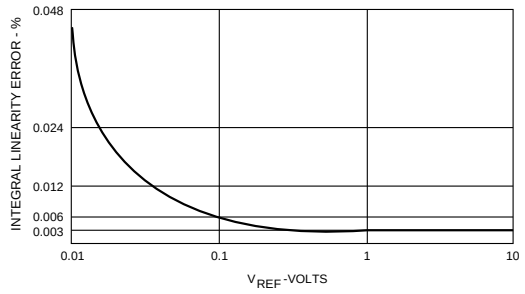
(Typical @ 25°C, nominal power supply, V_{REF} = +10V, unipolar unless otherwise noted)

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
ENVIRONMENTAL AND MECHANICAL					
Operating Temperature					
SP7514JN/KN	0		+70	°C	
SP7514AN/BN	–40		+85	°C	
HS3140–C	0		+70	°C	
HS3140–B	–55		+125	°C	
HS3140–B/883	–55		+125	°C	
Storage Temperature	–65		+150	°C	
Package					
SP7514_N		20-pin SOIC			
HS3140		20–pin Side–Brazed DIP			

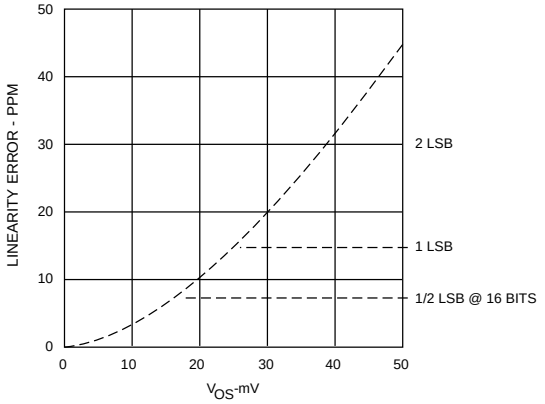
Notes:
1. Digital input voltage must not exceed supply voltage or go below –0.5V ; "0" <0.8V; 2.4V < "1" ≤$V_{DD.}$
2. AC or DC; use R6758–1 for fixed reference applications
3. Using the internal feedback resistor and an external op amp. The Scale Factor can be adjusted externally by variable resistors in series with the reference input and/or in series to the internal feedback resistor. Please refer to the Applications Information section.
4. At 25°C; the output leakage current will create an offset voltage at the external op amps output. It doubles every 10°C temperature increase.
5. Integral Linearity is measured as the arithmetic mean value of the magnitudes of the greatest positive deviation and the greatest negative deviation from the theoretical value for any given input combination.
6. Differential Linearity is the deviation of an output step form the theoretical value of 1LSB for any two adjacent digital input codes.
7. At 25°C, the output leakage current will create an offset voltage output. It doubles every 10°C temperature increase.
8. Using the internal feedback resistor and an external op amp.
9. Use series 470ohm resistor to limit start-up current.

CHARACTERISTIC CURVES

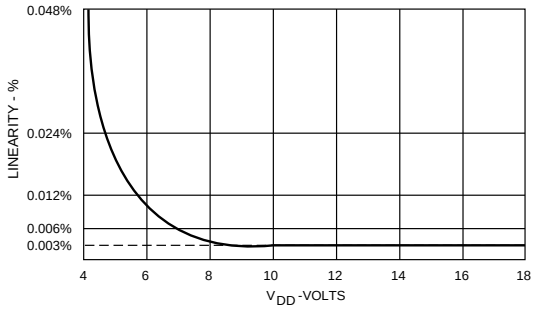
(Typical @ + 25°C, V_{DD} = + 15VDC, V_{REF} = + 10VDC, unless otherwise noted)



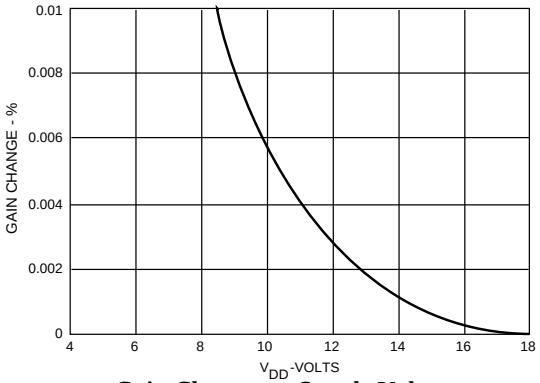
Integral Linearity Error vs. Reference Voltage



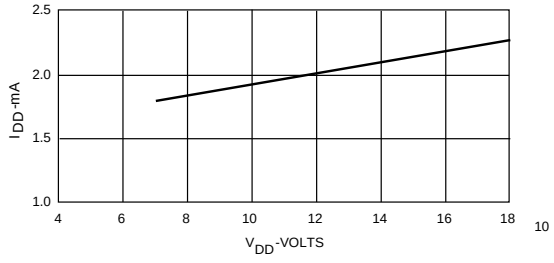
Additional Linearity Error vs. Output-Amplifier Offset-Voltage (V_{REF} = + 10V)



Linearity vs. Supply Voltage



Gain Change vs. Supply Voltage



Power Supply Current vs. Voltage

PIN ASSIGNMENTS...

Pin 1 – IO_1 – Current Output 1.

Pin 2 – IO_2 – Current Output 2.

Pin 3 – GND – Ground.

Pin 4 – DB_{13} – MSB, Data Bit 1.

Pin 5 – DB_{12} – Data Bit 2.

Pin 6 – DB_{11} – Data Bit 3.

Pin 7 – DB_{10} – Data Bit 4.

Pin 8 – DB_9 – Data Bit 5.

Pin 9 – DB_8 – Data Bit 6.

Pin 10 – DB_7 – Data Bit 7.

Pin 11 – DB_6 – Data Bit 8.

Pin 12 – DB_5 – Data Bit 9.

Pin 13 – DB_4 – Data Bit 10.

Pin 14 – DB_3 – Data Bit 11.

Pin 15 – DB_2 – Data Bit 12.

Pin 16 – DB_1 – Data Bit 13.

Pin 17 – DB_0 – LSB, Data Bit 14.

Pin 18 – V_{DD} – Positive Supply Voltage.

Pin 19 – V_{REF} – Reference Voltage Input.

Pin 20 – R_{FB} – Feedback Resistor.

FEATURES...

The **SP7514** and **HS3140** are precision 14-bit multiplying DACs. The DACs are implemented as a one-chip CMOS circuit with a resistor ladder network.

Three output lines are provided on the DACs to allow unipolar and bipolar output connection with a minimum of external components. The feedback resistor is internal. The resistor ladder network termination is externally available, thus eliminating an external resistor for the 1 LSB offset in bipolar mode.

The **SP7514** is available for use in commercial and industrial temperature ranges, packaged in a 20-pin SOIC. The **HS3140** is available in commercial and military temperature ranges, packaged in a 20–pin side–brazed DIP. For product processed and screened to the requirements of MIL–M–38510 and MIL–STD–883C, please consult the factory (**HS3140B** only).

PRINCIPLES OF OPERATION

The **SP7514/HS3140** achieve high accuracy by using a decoded or segmented DAC scheme to implement this function. The following is a brief description of this approach.

The most common technique for building a D/A converter of n bits is to use n switches to turn n current or voltage sources on or off. The n switches and n sources are designed so that each switch or bit contributes twice as much to the D/A converter's output as the preceding bit. This technique is commonly known as binary weighting and allows an n-bit converter to generate 2^n output levels by turning on the proper combination of bits.

In such binary-weighted converter, the switch with the smallest contribution (the LSB) accounts for only 2^{-n} of the converter's full-scale value. Similarly, the switch with the largest contribution (the MSB) accounts for 2^{-1} or half of the converter's full-scale output. Thus it is easy to see that a given percent change in the MSB will have a greater effect on the converter's output than would a similar percent change in the LSB. For example, a 1% change in the LSB of a 10 bit converter would only affect the output by 0.001% of full-scale. A 1% change in the MSB of the same converter would affect the output by 0.5% of FSR.

In order to overcome the problem which results from the large weighting of the MSB, the two MSB's can be decoded to three equally weighted sources. *Table 1* shows that all combinations of the two MSB's of a converter result in four output levels. So by replacing the two MSB's with three bits equally weighted at 1/4 full-scale and decoding the two MSB digital inputs into three lines which drive the equally weighted bits, the same functional performance can be obtained. Thus by replacing the two MSB switches of a conventional converter with three switches properly decoded, the contribution of any switch is reduced from 1/2 to 1/4. This reduction in sensitivity also reduces the

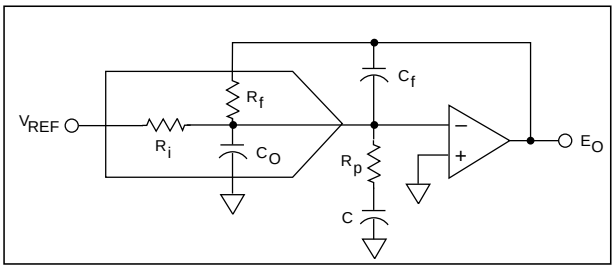


Figure 1. SP7514/HS3140 Equivalent Output Circuit

2^{-1}(MSB)	2^{-2}	Output
0	0	0
0	1	1/4 Full-Scale
1	0	1/2 Full-Scale
1	1	3/4 Full-Scale

Table 1. Contribution of the two MSB's

accuracy required of any switch for a given overall converter accuracy.

With the decoded converter described above, a 1% change in any of the converter's switches will affect the output by no more than 0.25% of full-scale as compared to 0.5% for a conventional converter. In other words the conventional D/A converter can be made less sensitive to the quality of its individual bits by decoding.

In the **SP7514/HS3140** the first four MSB's are decoded into 16 levels which drive 15 equally weighted current sources. The sensitivity of each switch on the output is reduced by a factor of 8. Each of the 15 sources contributes 6.25% output change rather than an MSB change of 50% for the common approach.

Following the decoded section of the DAC a standard binary weighted R-2R approach is used. This divides each of the 16 levels (or 6.25% of F.S.) into 4096 discrete levels (the 12 LSB's).

Output Capacitance

The **SP7514/HS3140** have very low output capacitance (C_O). This is specified both with all switches ON and all switches OFF. Output capacitance varies from 50pF to 100pF over all input codes. This low capacitance is due in part to the decoding technique used. Smaller switches are used with resulting less capacitance. Three important system characteristics are affected by C_O and ΔC_O; namely digital feedthrough,

TRANSFER FUNCTION (N=14)		
BINARY INPUT	UNIPOLAR OUTPUT	BIPOLAR OUTPUT
111...111	$-V_{REF}\ (1 - 2^{-N})$	$-V_{REF}\ (1 - 2^{-(N-1)})$
100...001	$-V_{REF}\ (1/2 + 2^{-N})$	$-V_{REF}\ (2^{-(N-1)})$
100...000	$-V_{REF}/2$	0
011...111	$-V_{REF}\ (1/2 - 2^{-N})$	$V_{REF}\ (2^{-(N-1)})$
000…001	$-V_{REF}\ (2^{(N-1)})$	$V_{REF}\ (1 - 2^{-(N-1)})$
000...000	0	V_{REF}

Table 2. Transfer Function

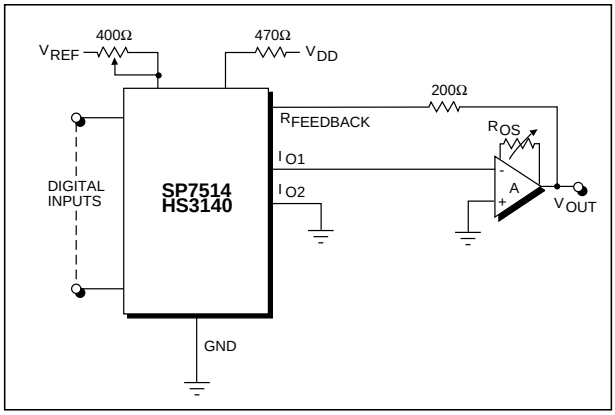


Figure 2. Unipolar Operation

settling time, and bandwidth. The DAC output equivalent circuit can be represented as shown in *Figure 1*.

Digital feedthrough is the change in analog output due to the toggling conditions on the converter input data lines when the analog input V_{REF} is at 0V. The **SP7514/HS3140** very low C_O and therefore will yield low digital feedthrough. Inputs to the DAC can be buffered. This input latch with microprocessor control is shown in *Figure 4*.

Settling time is directly affected by C_O. In *Figure 1*, C_O combines with R_f to add a pole to the open loop response, reducing bandwidth and causing excessive phase shift - which could result in ringing and/or oscillation. A feedback capacitor, C_f must be added to restore stability. Even with C_f, there is still a zero-pole mismatch due to R_iC_O which is code dependent. This code dependent mismatch is minimized when $C_OR_i = R_fC_f$. However C_f must now be made larger to compensate for worst case ΔR_iC_O - resulting in reduced bandwidth and increased settling time. With the **SP7514/HS3140,** small values for C_f must be used.

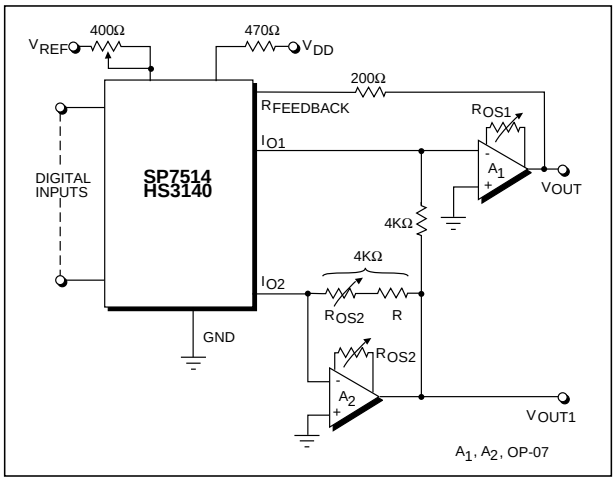


Figure 3. Bipolar Operation

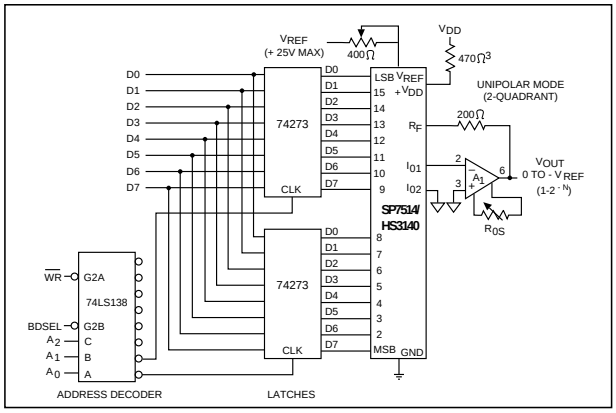


Figure 4. Microprocessor Interface to SP7514/HS3140

Resistor R_p can be added, this will parallel R_f decreasing the effective resistance. If C_f is reduced the bandwidth will be increased and settling time decreased. However a system penalty for lowering C_f is to increase noise gain. The trade-off is noise vs. settling time. If R_p is added then a large value (1µF or greater) non-polarized capacitor C_p should be added in series with R_p to eliminate any DC drifts. If settling time is not important, eliminate R_p and C_p, and adjust C_f to prevent overshoot.

Output Offset

In most applications, the output of the DAC is fed into an amplifier to convert the DAC's current output to voltage. A little known and not commonly discussed parameter is the linearity error versus offset voltage of the output amplifier. All CMOS DAC's must operate into a virtual ground, i.e., the summing junction of an op amp. Any amplifier's offset from the amplifier will appear as an error at the output (which can be related to LSB's of error).

Most all CMOS DAC's currently available are implemented using an R-2R ladder network. The formula for nonlinearity is typically 0.67mV/mV$_{OS}$ (not derived here). However the **SP7516** has a coefficient of only 0.065mV/mVOS. This is due to the decoding technique described earlier. CMOS DAC applications notes (including this one) always show a potentiometer used to null out the amplifier's offset. If an amplifier is chosen having 'pretrimmed' offset it may be possible to eliminate this component. Consider the following calculations:

1. Using LF441A amplifier (low power - 741 pinout)
2. Specified offset: 0.5mV max
3. Temperature coefficient of input offset: 10µV/°C max

V_{OS} max (0°C to 70°C) = 0.5mV + (70µV)10
= 1.2mV
Add'l nonlinearity (max.) = 1.2mV x 0.065mV/mV
= 78µV (1/2 LSB @ 16 Bits)

Where: 78µV = 1/2 LSB @ 16 Bits (10V range)

Via the above configuration, the **SP7514/HS3140** can be used to divide an analog signal by digital code (i.e. for digitally controlled gain). The transfer function is given in *Table 2*, where the value of each bit is 0 or 1. Division by all "0"s is undefined and causes the op amp to saturate.

Applications Information
Unipolar Operation

Figure 2 shows the interconnections for unipolar operation. Connect I_{O1} and FB_1 as shown in diagram. Tie I_{O2} (Pin 7), FB_3 (Pin 3), and FB_4 (Pin 1) to Ground (Pin 8). As shown, a series resistor is recommended in the V_{DD} supply line to limit current during 'turn-on'. To maintain specified linearity, external amplifiers must be zeroed. Apply an ALL "ZEROES" digital input and adjust R_{OS} for V_{OUT} = 0 ± 1mV. The **SP7514** and **HS3140** have been used successfully with OP-07, OP-27 and LF441A. For high speed applications the SP2525 is recommended.

Bipolar Operation

Figure 3 shows the interconnections for bipolar operation. Connect I_{O1}, I_{O2}, FB_1, FB_3, FB_4 as shown in diagram. Tie LDTR to I_{O2}. As shown, a series resistor is recommended in the V_{DD} supply line to limit current during 'turn-on. To maintain specified linearity, external amplifiers must be zeroed. This is best done with V_{REF} set to zero and, the DAC register loaded with 10...0 (MSB = 1). Set R_{0S1} for V_{01} = 0. Set R_{0S2} for V_{OUT} = 0. Set V_{REF} to +10V and adjust R_B for V_{OUT} to be 0V.

Grounding

Connect all GND pins to system analog ground and tie this to digital ground. All unused input pins must be grounded.

ORDERING INFORMATION

Model	Monotonicity	Temperature Range	Package
Double-Buffered 12-Bit Multiplying DAC			
HS3140C-3Q	13-Bit	0°C to +70°C	20-pin, 0.3" Side-Brazed DIP
HS3140B-3Q	13-Bit	-55°C to +125°C	20-pin, 0.3" Side-Brazed DIP
HS3140B-3/883	13-Bit	-55°C to +125°C	20-pin, 0.3" Side-Brazed DIP
HS3140C-4Q	14-Bit	0°C to +70°C	20-pin, 0.3" Side-Brazed DIP
HS3140B-4Q	14-Bit	-55°C to +125°C	20-pin, 0.3" Side-Brazed DIP
HS3140B-4/883	14-Bit	-55°C to +125°C	20-pin, 0.3" Side-Brazed DIP
SP7514JN	13-Bit	0°C to +70°C	20-pin, 0.3" SOIC
SP7514KN	14-Bit	0°C to +70°C	20-pin, 0.3" SOIC
SP7514AN	13-Bit	–40°C to +85°C	20-pin, 0.3" SOIC
SP7514BN	14-Bit	–40°C to +85°C	20-pin, 0.3" SOIC

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