LANSDALE Semiconductor, Inc.

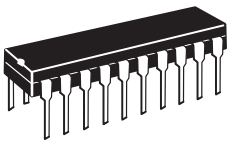
ML145050
ML145051
10-Bit A/D Converter with Serial Interface - CMOS

Legacy Device: *Motorola MC145050, MC145051*

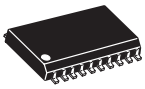
These ratio metric 10-bit ADCs have serial interface ports to provide communication with MCUs and MPUs. Either a 10- or 16-bit format can be used. The 16-bit format can be one continuous 16-bit stream or two intermittent 8-bit streams. The converters operate from a single power supply with no external trimming required. Reference voltages down to 4.0 V are accommodated.

The ML145050 has the same pin out as the 8-bit ML145040 which allows an external clock (ADCLK) to operate the dynamic A/D conversion sequence. The ML145051 has the same pin out as the 8-bit ML145041 which has an internal clock oscillator and an end-of-conversion (EOC) output.

- 11 Analog Input Channels with Internal Sample-and-Hold
- Operating Temperature Range: – 40 to 125°C
- Successive Approximation Conversion Time:
  - ML145050 – 21 µs (with 2.1 MHz ADCLK)
  - ML145051 – 44 µs Maximum
- Maximum Sample Rate:
  - ML145050 – 38 ks/s
  - ML145051 – 20.4 ks/s
- Analog Input Range with 5-Volt Supply: 0 to 5 V
- Monotonic with No Missing Codes
- Direct Interface to Motorola SPI and National MICROWIRE Serial Data Ports
- Digital Inputs/Outputs are TTL, NMOS, and CMOS Compatible
- Low Power Consumption: 14 mW
- Chip Complexity: 1630 Elements (FETs, Capacitors, etc.)
- See Application Note AN1062 for Operation with QSPI



P DIP 20 = RP
PLASTIC
CASE 738



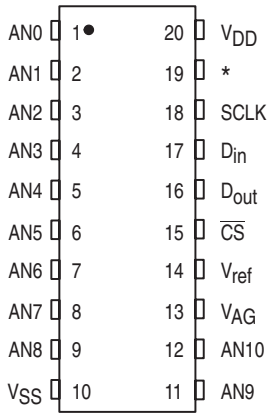
SO 20W = -6P
SOG
CASE 751D

CROSS REFERENCE/ORDERING INFORMATION

PACKAGE	MOTOROLA	LANSDALE
P DIP 20	MC145050P	ML145050RP
SOG 20W	MC145050DW	ML145050-6P
P DIP 20	MC145051P	ML145051RP
SOG 20W	MC145051DW	ML145051-6P

Note: Lansdale lead free (**Pb**) product, as it becomes available, will be identified by a part number prefix change from **ML** to **MLE**.

PIN ASSIGNMENT
*ADCLK (ML145050); EOC (ML145051)



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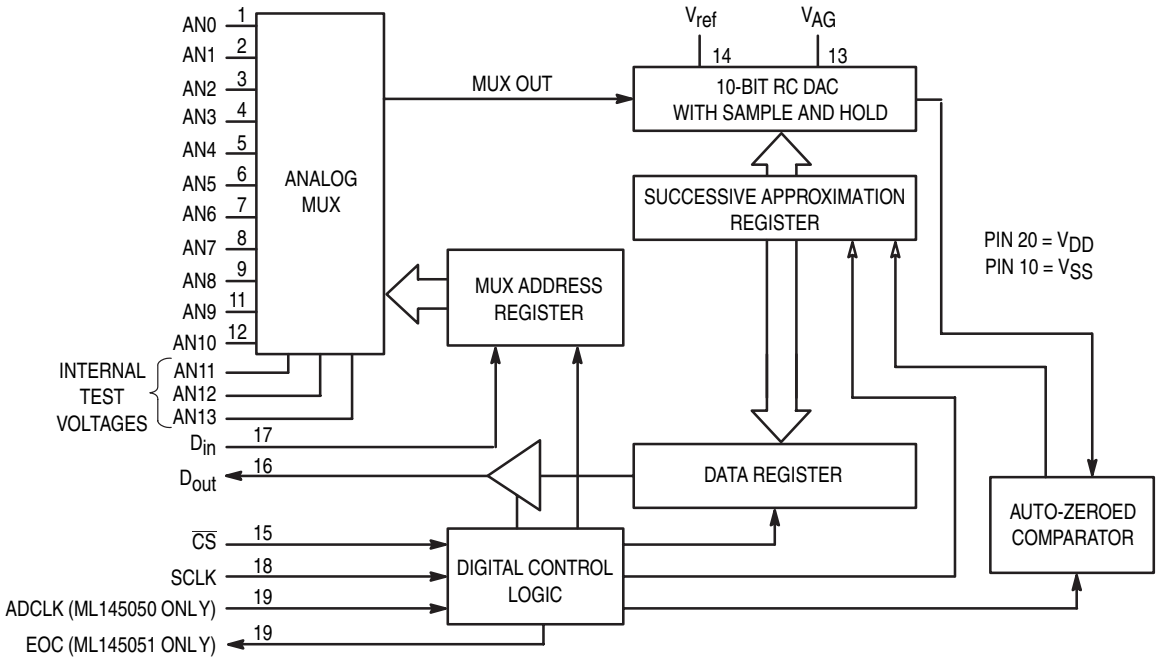
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage (Referenced to V_{SS})	– 0.5 to + 6.0	V
V_{ref}	DC Reference Voltage	V_{AG} to V_{DD} + 0.1	V
V_{AG}	Analog Ground	V_{SS} – 0.1 to V_{ref}	V
V_{in}	DC Input Voltage, Any Analog or Digital Input	V_{SS} – 0.5 to V_{DD} + 0.5	V
V_{out}	DC Output Voltage	V_{SS} – 0.5 to V_{DD} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{DD}, I_{SS}	DC Supply Current, V_{DD} and V_{SS} Pins	± 50	mA
T_{stg}	Storage Temperature	– 65 to 150	C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Operation Ranges below..

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

OPERATION RANGES (Applicable to Guaranteed Limits)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage, Referenced to V_{SS}	4.5 to 5.5	V
V_{ref}	DC Reference Voltage	V_{AG} + 4.0 to V_{DD} + 0.1	V
V_{AG}	Analog Ground	V_{SS} – 0.1 to V_{ref} – 4.0	V
V_{AI}	Analog Input Voltage (See Note)	V_{AG} to V_{ref}	V
V_{in}, V_{out}	Digital Input Voltage, Output Voltage	V_{SS} to V_{DD}	V
T_A	Ambient Operating Temperature	– 40 to 125	C

NOTE: Analog input voltages greater than V_{ref} convert to full scale. Input voltages less than V_{AG} convert to zero. See V_{ref} and V_{AG} pin descriptions.

DC ELECTRICAL CHARACTERISTICS

(Voltages Referenced to V_{SS}, Full Temperature and Voltage Ranges per Operation Ranges Table, unless otherwise indicated)

Symbol	Parameter	Test Condition	Guaranteed Limit	Unit
V_{IH}	Minimum High-Level Input Voltage (D_{in}, SCLK, $\overline{CS}$, ADCLK)		2.0	V
V_{IL}	Maximum Low-Level Input Voltage (D_{in}, SCLK, $\overline{CS}$, ADCLK)		0.8	V
V_{OH}	Minimum High-Level Output Voltage (D_{out}, EOC)	I_{out} = – 1.6 mA I_{out} = – 20 μA	2.4 V_{DD} – 0.1	V
V_{OL}	Minimum Low-Level Output Voltage (D_{out}, EOC)	I_{out} = + 1.6 mA I_{out} = 20 μA	0.4 0.1	V
I_{in}	Maximum Input Leakage Current (D_{in}, SCLK, $\overline{CS}$, ADCLK)	V_{in} = V_{SS} or V_{DD}	± 2.5	μA
I_{OZ}	Maximum Three-State Leakage Current (D_{out})	V_{out} = V_{SS} or V_{DD}	± 10	μA
I_{DD}	Maximum Power Supply Current	V_{in} = V_{SS} or V_{DD}, All Outputs Open	2.5	mA
I_{ref}	Maximum Static Analog Reference Current (V_{ref})	V_{ref} = V_{DD}, V_{AG} = V_{SS}	100	μA
I_{AI}	Maximum Analog Mux Input Leakage Current between all deselected inputs and any selected input (AN0 ± AN10)	V_{AI} = V_{SS} to V_{DD}	± 1	μA

A/D CONVERTER ELECTRICAL CHARACTERISTICS

(Full Temperature and Voltage Ranges per Operation Ranges Table; ML145050: 500 kHz ≤ ADCLK ≤ 2.1 MHz, unless otherwise noted)

Characteristic	Definition and Test Conditions	Guaranteed Limit	Unit
Resolution	Number of bits resolved by the A/D converter	10	Bits
Maximum Nonlinearity	Maximum difference between an ideal and an actual ADC transfer function	± 1	LSB
Maximum Zero Error	Difference between the maximum input voltage of an ideal and an actual ADC for zero output code	± 1	LSB
Maximum Full-Scale Error	Difference between the minimum input voltage of an ideal and an actual ADC for full-scale output code	± 1	LSB
Maximum Total Unadjusted Error	Maximum sum of nonlinearity, zero error, and full-scale error	± 1	LSB
Maximum Quantization Error	Uncertainty due to converter resolution	± 1/2	LSB
Absolute Accuracy	Difference between the actual input voltage and the full-scale weighted equivalent of the binary output code, all error sources included	± 1-1/2	LSB
Maximum Conversion Time	Total time to perform a single analog-to-digital conversion ML145050 ML145051	44 44	ADCLK cycles μs
Data Transfer Time	Total time to transfer digital serial data into and out of the device	10 to 16	SCLK cycles
Sample Acquisition Time	Analog input acquisition time window	6	SCLK cycles
Minimum Total Cycle Time	Total time to transfer serial data, sample the analog input, and perform the conversion ML145050: ADCLK = 2.1 MHz, SCLK = 2.1 MHz ML145051: SCLK = 2.1 MHz	 26 49	μs
Maximum Sample Rate	Rate at which analog inputs may be sampled ML145050: ADCLK = 2.1 MHz, SCLK = 2.1 MHz ML145051: SCLK = 2.1 MHz	 38 20.4	ks/s

AC ELECTRICAL CHARACTERISTICS

(Full Temperature and Voltage Ranges per Operation Ranges Table)

Figure	Symbol	Parameter		Guaranteed Limit	Unit
1	f	Clock Frequency, SCLK Note: Refer to t_{wH}, t_{wL} below	(10-bit xfer) Min (11- to 16-bit xfer) Min (10- to 16-bit xfer) Max)	0 Note 1 2.1	MHz
1	f	Clock Frequency, ADCLK Note: Refer to t_{wH}, t_{wL} below	Minimum Maximum	500 2.1	kHz MHz
1	t_{wH}	Minimum Clock High Time	ADCLK SCLK	190 190	ns
1	t_{wL}	Minimum Clock Low Time	ADCLK SCLK	190 190	ns
1, 7	t_{PLH}, t_{PHL}	Maximum Propagation Delay, SCLK to D_{out}		125	ns
1, 7	t_h	Minimum Hold Time, SCLK to D_{out}		10	ns
2, 7	t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, $\overline{CS}$ to D_{out} High-Z		150	ns
2, 7	t_{PZL}, t_{PZH}	Maximum Propagation Delay, $\overline{CS}$ to D_{out} Driven	ML145050 ML145051	2 ADCLK cycles + 300 2.3	ns μs
3	t_{su}	Minimum Setup Time, D_{in} to SCLK		100	ns
3	t_h	Minimum Hold Time, SCLK to D_{in}		0	ns
4, 7, 8	t_d	Maximum Delay Time, EOC to D_{out} (MSB)	ML145051	100	ns
5	t_{su}	Minimum Setup Time, $\overline{CS}$ to SCLK	ML145050 ML145051	2 ADCLK cycles + 425 2.425	ns μs
–	t_{CSd}	Minimum Time Required Between 10th SCLK Falling Edge (0.8 V) and $\overline{CS}$ to Allow a Conversion	ML145050 ML145051	44 Note 2	ADCLK cycles
–	t_{CAs}	Maximum Delay Between 10th SCLK Falling Edge (2 V) and $\overline{CS}$ to Abort a Conversion	ML145050 ML145051	36 9	ADCLK cycles μs
5	t_h	Minimum Hold Time, Last SCLK to $\overline{CS}$		0	ns
6, 8	t_{PHL}	Maximum Propagation Delay, 10th SCLK to EOC	ML145051	2.35	μs
1	t_r, t_f	Maximum Input Rise and Fall Times	SCLK ADCLK D_{in}, $\overline{CS}$	1 250 10	ms ns μs
1, 4, 6 – 8	t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output		300	ns
–	C_{in}	Maximum Input Capacitance	AN0 – AN10 ADCLK, SCLK, $\overline{CS}$, D_{in}	55 15	pF
–	C_{out}	Maximum Three-State Output Capacitance	D_{out}	15	pF

NOTES:

1. After the 10th SCLK falling edge (≤ 2 V), at least 1 SCLK rising edge (≥ 2 V) must occur within 38 ADCLKs (ML145050) or 18.5 μs (ML145051).
2. On the ML145051, a $\overline{CS}$ edge may be received immediately after an active transition on the EOC pin.

SWITCHING WAVEFORMS

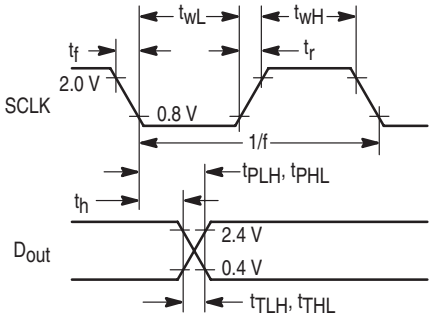


Figure 1.

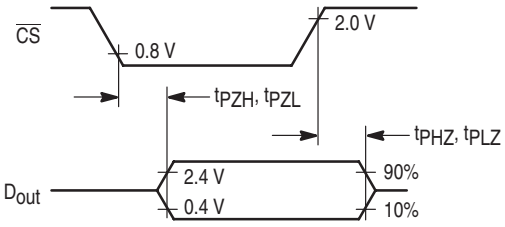


Figure 2.

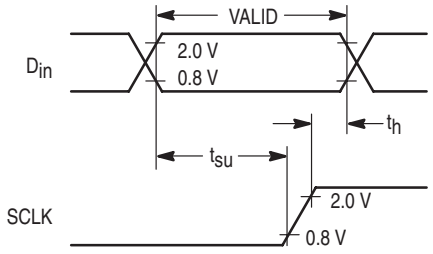
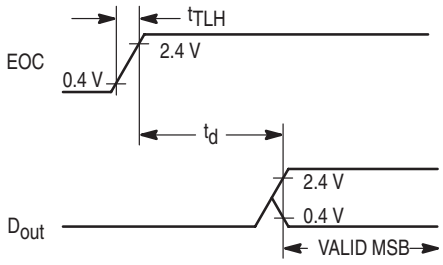


Figure 3.



NOTE: D_{out} is driven only when $\overline{CS}$ is active (low).

Figure 4.

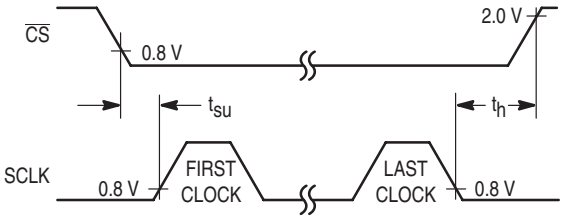


Figure 5.

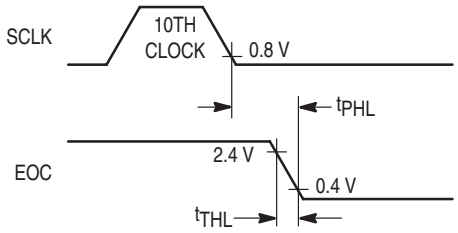


Figure 6.

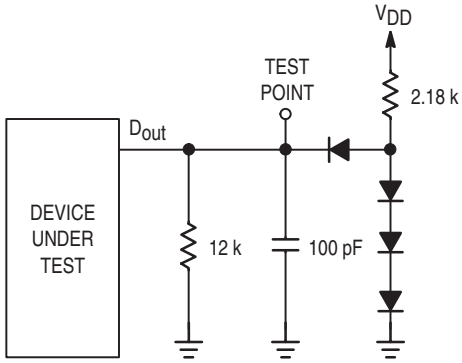


Figure 7. Test Circuit

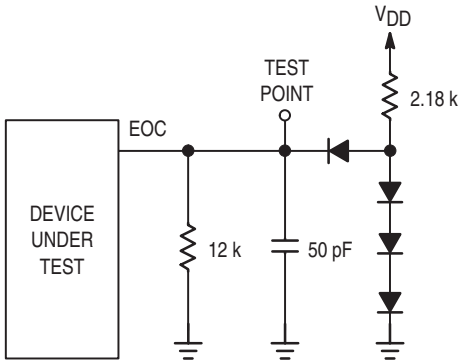


Figure 8. Test Circuit

PIN DESCRIPTIONS

DIGITAL INPUTS AND OUTPUT

The various serial bit-stream formats for the ML145050/51 are illustrated in the timing diagrams of Figures 9 through 14. Table 1 assists in selection of the appropriate diagram. Note that the ADCs accept 16 clocks which makes them SPI (Serial Peripheral Interface) compatible.

Table 1. Timing Diagram Selection

No. of Clocks in Serial Transfer	Using $\overline{CS}$	Serial Transfer Interval	Figure No.
10	Yes	Don't Care	9
10	No	Don't Care	10
11 to 16	Yes	Shorter than Conversion	11
16	No	Shorter than Conversion	12
11 to 16	Yes	Longer than Conversion	13
16	No	Longer than Conversion	14

$\overline{CS}$
Active-Low Chip Select Input (Pin 15)

Chip select initializes the chip to perform conversions and provides 3-state control of the data output pin (D_{out}). While inactive high, $\overline{CS}$ forces D_{out} to the high-impedance state and disables the data input (D_{in}) and serial clock (SCLK) pins. A high-to-low transition on $\overline{CS}$ resets the serial dataport and synchronizes it to the MPU data stream. $\overline{CS}$ can remain active during the conversion cycle and can stay in the active low state for multiple serial transfers or $\overline{CS}$ can be in active high after each transfer. If $\overline{CS}$ is kept active low between transfers, the length of each transfer is limited to either 10 or 16 SCLK cycles. If $\overline{CS}$ is in the inactive high state between transfers, each transfer can be anywhere from 10 to16 SCLK cycles long. See the SCLK pin description for a more detailed discussion of these requirements.

On the ML145050/51 spurious chip selects caused by system noise are minimized by the internal circuitry.

Any transitions on the ML145050 $\overline{CS}$ pin are recognized as valid only if the level is maintained for a setup time plus two falling edges of ADCLK after the transition.

Transitions on the ML145051 $\overline{CS}$ pin are recognized as valid only if the level is maintained for about 2 ms after the transition.

NOTE

If $\overline{CS}$ is inactive high after the 10th SCLK cycle-and then goes active low before the A/D conversion is complete, the conversion is aborted and the chip enters the initial state, ready for another serial transfer/conversion sequence. At this point, the output data register contains the result from the conversion before the aborted conversion. Note that the last step of the A/D conversion sequence is to update the output data register with the result. Therefore, if $\overline{CS}$ goes active low in an attempt to abort the conversion too close to the end of the conversion sequence, the result register may be corrupted and the chip could be thrown out of sync with the processor until $\overline{CS}$ is toggled again (refer to the AC Electrical Characteristics in the spec tables).

D_{out}
Serial Data Output of the A/D Conversion Result(Pin 16)

This output is in the high-impedance state when $\overline{CS}$ is in active high. When the chip recognizes a valid active low on $\overline{CS}$, D_{out} is taken out of the high-impedance state and is driven with the MSB of the previous conversion result. (For the-first transfer after power-up, data on D_{out} is undefined for the entire transfer.) The value on D_{out} changes to the second most significant result bit upon the first falling edge of SCLK. The remaining result bits are shifted out in order, with the LSB appearing on D_{out} upon the ninth falling edge of SCLK. Note that the order of the transfer is MSB to LSB. Upon the 10th falling edge of SCLK, D_{out} is immediately driven low (if allowed by $\overline{CS}$) so that transfers of more than 10 SCLKs read zeroes as the unused LSBs.

When $\overline{CS}$ is held active low between transfers, D_{out} is driven from a low level to the MSB of the conversion result for three cases: Case 1 – upon the 16th SCLK falling edge if the transfer is longer than the conversion time (Figure 14); Case 2 – upon completion of a conversion for a 16-bit transfer interval shorter than the conversion (Figure 12); Case 3– upon completion of a conversion for a 10-bit transfer (Figure 10).

Din
Serial Data Input (Pin 17)

The four-bit serial input stream begins with the MSB of the analog mux address (or the user test mode) that is to be converted next. The address is shifted in on the first four rising edges of SCLK. After the four mux address bits have been received, the data on D_{in} is ignored for the remainder of the present serial transfer. See Table 2 in Applications Information.

SCLK
Serial Data Clock (Pin 18)

This clock input drives the internal I/O state machine to perform three major functions: (1) drives the data shift registers to simultaneously shift in the next mux address from the D_{in} pin and shift out the previous conversion result on the D_{out} pin, (2) begins sampling the analog voltage onto the RCDAC as soon as the new mux address is available, and (3) transfers control to the A/D conversion state machine (driven by ADCLK) after the last bit of the previous conversion result has been shifted out on the D_{out} pin.

The serial data shift registers are completely static, allowing SCLK rates down to the DC. There are some cases, however, that require a minimum SCLK frequency as discussed later in this section. SCLK need not be synchronous to ADCLK. At least ten SCLK cycles are required for each simultaneous data transfer. If the 16-bit format is used, SCLK can be one continuous 16-bit stream or two intermittent 8-bit streams. After the serial port has been initiated to perform a serial transfer*, the new mux address is shifted in on the first

*The serial port can be initiated in three ways: (1) a recognized $\overline{CS}$ falling edge, (2) the end of an A/D conversion if the port is perform-ing either a 10-bit or a 16-bit “shorter-than-conversion” transfer with $\overline{CS}$ active low between transfers, and (3) the 16th falling edge of SCLK if the port is performing 16-bit “longer-than-conversion” transfers with $\overline{CS}$ active low between transfers.

four rising edges of SCLK, and the previous 10-bit conversion result is shifted out on the first nine falling edges of SCLK. After the fourth rising edge of SCLK, the new mux address is available; therefore, on the next edge of SCLK (the fourth falling edge), the analog input voltage on the selected mux input begins charging the RC DAC and continues to do so until the tenth falling edge of SCLK. After this tenth SCLK edge, the analog input voltage is disabled from the RC DAC and the RC DAC begins the "hold" portion of the A/D conversion sequence. Also upon this tenth SCLK edge, control of the internal circuitry is transferred to ADCLK which drives the successive approximation logic to complete the conversion. If 16 SCLK cycles are used during each transfer, then there is a constraint on the minimum SCLK frequency. Specifically, there must be at least one rising edge on SCLK before the A/D conversion is complete. If the SCLK frequency is too low and a rising edge does not occur during the conversion, the chip is thrown out of sync with the processor and $\overline{CS}$ needs to be toggled in order to restore proper operation. If 10 SCLKs are used per transfer, then there is no lower frequency limit on SCLK. Also note that if the ADC is operated such that $\overline{CS}$ is inactive high between transfers, then the number of SCLK cycles per transfer can be anything between 10 and 16 cycles, but the "rising edge" constraint is still in effect if more than 10 SCLKs are used. (If $\overline{CS}$ stays active low for multiple transfers, the number of SCLK cycles must be either 10 or 16.)

ADCLK
A/D Conversion Clock Input (Pin 19, ML145050 Only)

This pin clocks the dynamic A/D conversion sequence, and may be asynchronous to SCLK. Control of the chip passes to ADCLK after the tenth falling edge of SCLK. Control of the chip is passed back to SCLK after the successive approximation conversion sequence is complete (44 ADCLK cycles), or after a valid chip select is recognized. ADCLK also drives the $\overline{CS}$ recognition logic. The chip ignores transitions on $\overline{CS}$ unless the state remains for a setup time plus two falling edges of ADCLK. The source driving ADCLK must be free running.

EOC
End-of-Conversion Output (Pin 19, ML145051 Only)

EOC goes low on the tenth falling edge of SCLK. A low-to-high transition on EOC occurs when the A/D conversion is complete and the data is ready for transfer.

ANALOG INPUTS AND TEST MODE

AN0 through AN10
Analog Multiplexer Inputs (Pins 1 – 9, 11, 12)

The input AN0 is addressed by loading $0 into the mux address register. AN1 is addressed by $1, AN2 by $2, 0, AN10 by $A. Table 2 shows the input format for a 16-bit stream. The mux features a break-before-make switching structure to minimize noise injection into the analog inputs. The source resistance driving these inputs must be ≤1 kΩ.

During normal operation, leakage currents through the analog mux from unselected channels to a selected channel and leakage currents through the ESD protection diodes on the selected channel occur. These leakage currents cause an offset voltage to appear across any series source resistance on the selected channel. Therefore, any source resistance greater than 1 kΩ (Lansdale test condition) may induce errors in excess of guaranteed specifications.

There are three tests available that verify the functionality of all the control logic as well as the successive approximation comparator. These tests are performed by addressing $B, $C, or $D and they convert a voltage of $(V_{ref} + V_{AG})/2$,V_{AG}, or V_{ref}, respectively. The voltages are obtained internally by sampling V_{ref} or V_{AG} onto the appropriate elements of the RC DAC during the sample phase. Addressing $B, $C, or $D produces an output of $200 (half scale), $000, or $3FF (full scale), respectively, if the converter is functioning properly. However, deviation from these values occurs in the presence of sufficient system noise (external to the chip) on V_{DD}, V_{SS}, V_{ref}, or V_{AG}.

POWER AND REFERENCE PINS

V_{SS} and V_{DD}
Device Supply Pins (Pins 10 and 20)

V_{SS} is normally connected to digital ground; V_{DD} is connected to a positive digital supply voltage. Low frequency ($V_{DD} – V_{SS}$) variations over the range of 4.5 to 5.5 volts do not affect the A/D accuracy. (See the Operations Ranges Table for restrictions on V_{ref} and V_{AG} relative to V_{DD} and V_{SS}.) Excessive inductance in the V_{DD} or V_{SS} lines, as on automatic test equipment, may cause A/D offsets > ± 1 LSB. Use of a 0.1 μF bypass capacitor across these pins is recommended.

V_{AG} and V_{ref}
Analog Reference Voltage Pins (Pins 13 and 14)

Analog reference voltage pins which determine the lower and upper boundary of the A/D conversion. Analog input voltages ≤ V_{ref} produce a full scale output and input voltages ≤ V_{AG} produce an output of zero. CAUTION: The analog input voltage must be ≥ V_{SS} and ≤ V_{DD}. The A/D conversion result is ratio metric to $V_{ref} – V_{AG}$. V_{ref} and V_{AG} must be as noise-free as possible to avoid degradation of the A/D conversion. Ideally, V_{ref} and V_{AG} should be single-point connected to the voltage supply driving the system's transducers. Use of a 0.22 μF bypass capacitor across these pins is strongly urged.

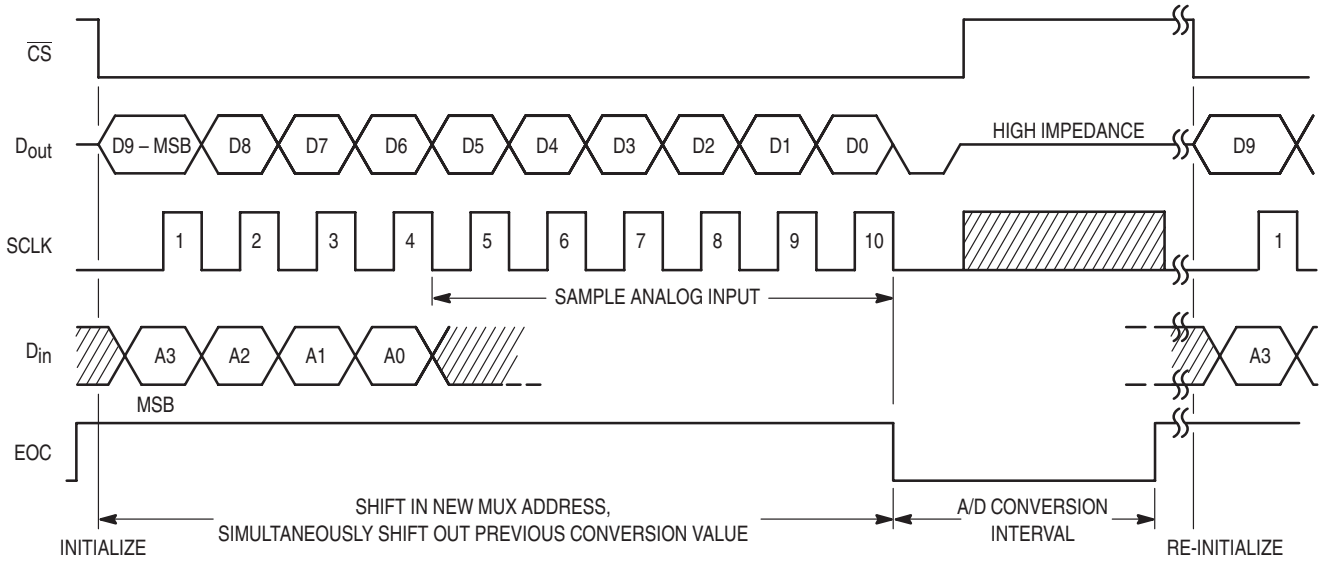


Figure 9. Timing for 10-Clock Transfer Using $\overline{CS}$*

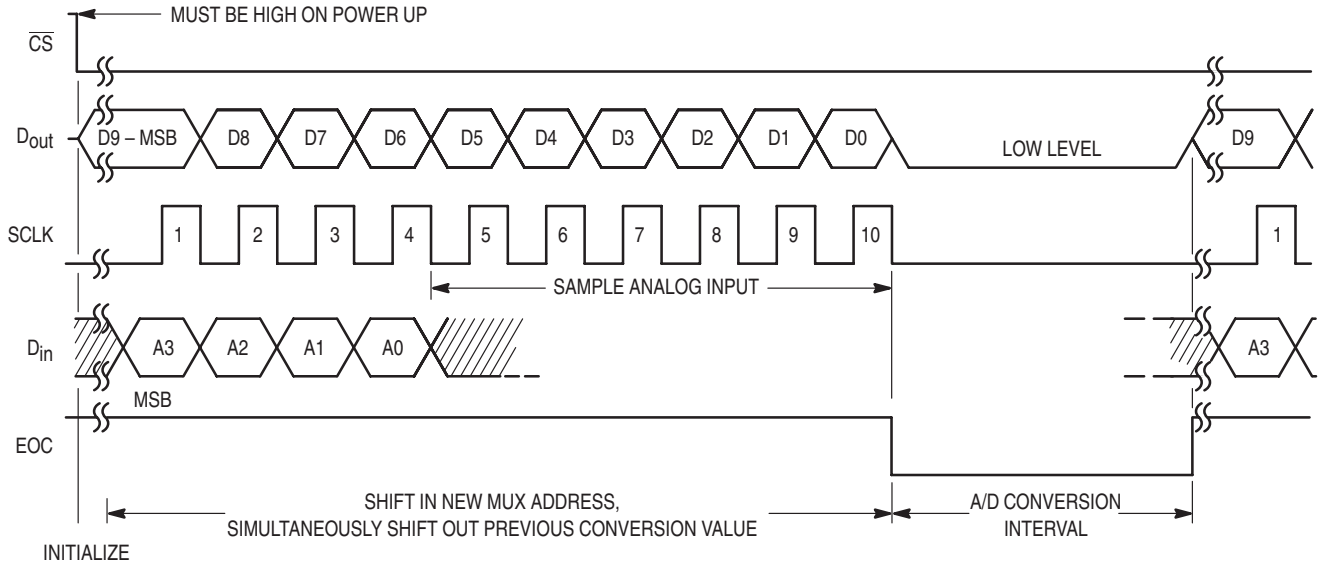


Figure 10. Timing for 10-Clock Transfer Not Using $\overline{CS}$*

NOTES:

1. D9, D8, D7, 0 , D0 = the result of the previous A/D conversion.
2. A3, A2, A1, A0 = the mux address for the next A/D conversion.

* This figure illustrates the behavior of the ML145051. The ML145050 behaves identically except there is no EOC signal and the conversion time is 44 ADCLK cycles (user-controlled time).

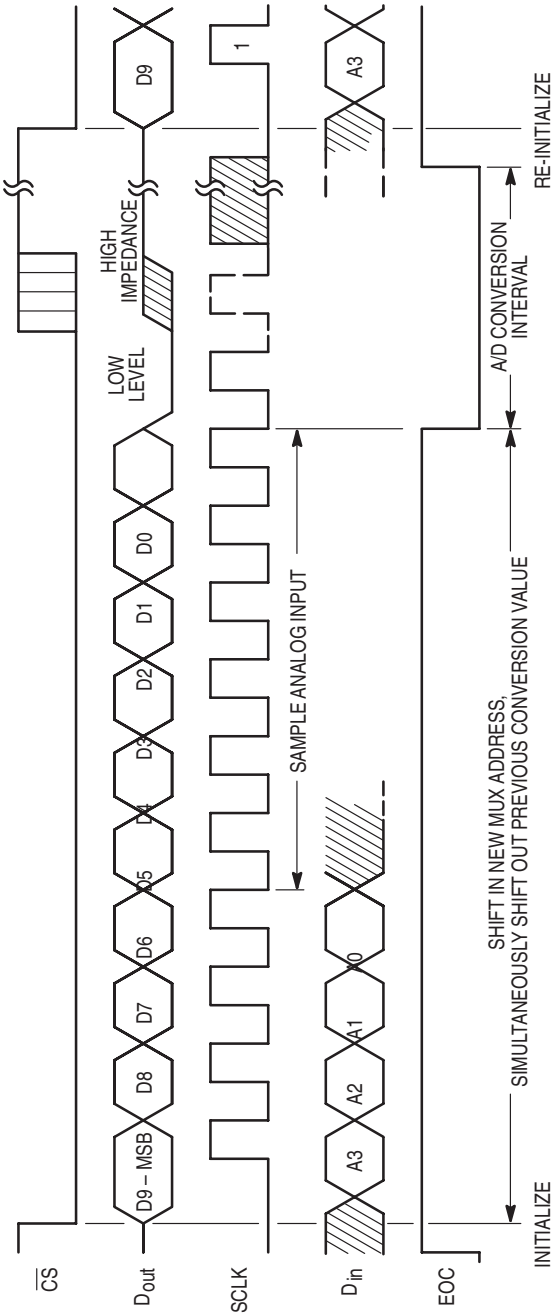


Figure 11. Timing for 11- to 16-Clock Transfer Using $\overline{CS}$* (Serial Transfer Interval Shorter than Conversion)

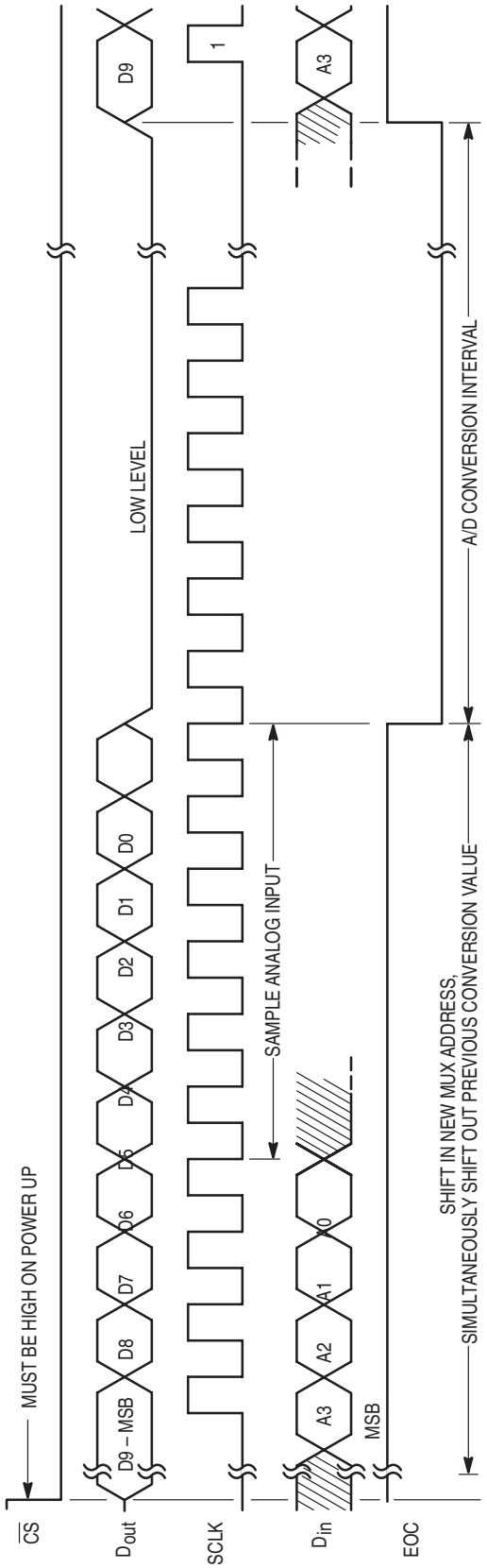


Figure 12. Timing for 16-Clock Transfer Not Using $\overline{CS}$* (Serial Transfer Interval Shorter Than Conversion)

NOTES:
D9, D8, D7, . . . , D0 = the result of the previous A/D conversion.
A3, A2, A1, A0 = the mux address for the next A/D conversion.
*This figure illustrates the behavior of the ML145051. The ML145050 behaves identically except there is no EOC signal and the conversion time is 44 ADCLK cycles (user-controlled time).

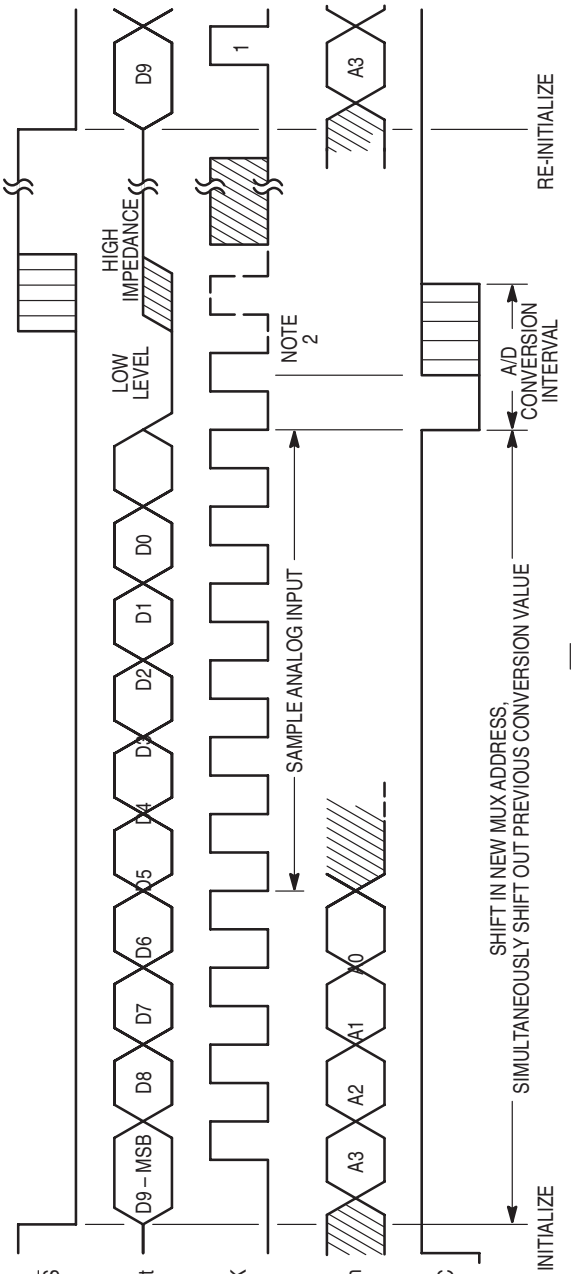


Figure 13. Timing for 11- to 16-Clock Transfer Using $\overline{CS}$* (Serial Transfer Interval Longer Than Conversion)

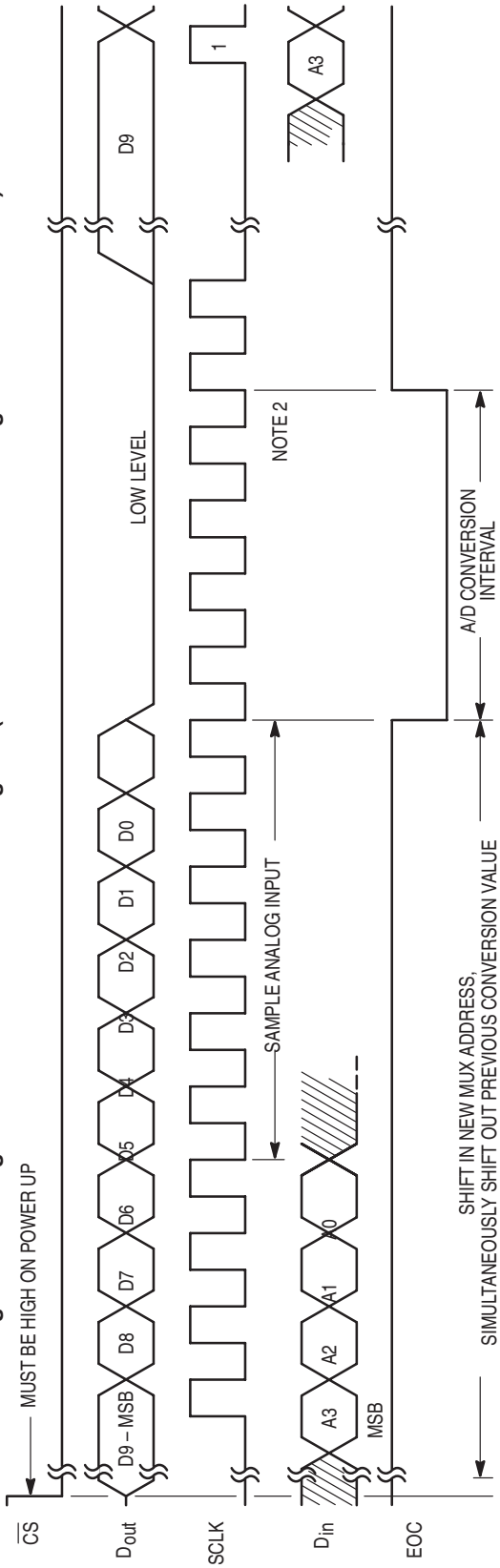


Figure 14. Timing for 16-Clock Transfer Not Using $\overline{CS}$* (Serial Transfer Interval Longer Than Conversion)

NOTES:
D9, D8, D7, . . . , D0 = the result of the previous A/D conversion.
A3, A2, A1, A0 = the mux address for the next A/D conversion.

*NOTES:
1. This figure illustrates the behavior of the ML145051. The ML145050 behaves identically except there is no EOC signal and the conversion time is 44 ADCLK cycles (user-controlled time).
2. The 11th SCLK rising edge must occur before the conversion is complete. Otherwise the serial port is thrown out of sync with the microprocessor for the remainder of the transfer.

Legacy Applications Information

DESCRIPTION

This example application of the ML145050/ML145051 ADCs interfaces three controllers to a microprocessor and processes data in real-time for a video game. The standard joystick X-axis (left/right) and Y-axis (up/down) controls as well as engine thrust controls are accommodated.

Figure 15 illustrates how the ML145050/ML145051 is used as a cost-effective means to simplify this type of circuit design. Utilizing one ADC, three controllers are interfaced to a CMOS or NMOS microprocessor with a serial peripheral interface (SPI) port. Processors with National Semiconductor's MICROWIRE serial port may also be used. Full duplex operation optimizes throughput for this system.

DIGITAL DESIGN CONSIDERATIONS

Motorola's MC68HC05C4 CMOS MCU may be chosen to reduce power supply size and cost. The NMOS MCUs maybe used if power consumption is not critical. A V_{DD} or V_{SS} 0.1 µF bypass capacitor should be closely mounted to the ADC.

Both the ML145050 and ML145051 accommodate all the analog system inputs. The ML145050, when used with a 2 MHz MCU, takes 27 µs to sample the analog input, perform the conversion, and transfer the serial data at 2 MHz. Forty-four ADCLK cycles (2 MHz at input pin 19) must be provided and counted by the MCU before reading the ADC results. The ML145051 has the end-of-conversion (EOC) signal (at output pin 19) to define when data is ready, but has a slower 49 µs cycle time. However, the 49 µs is constant for serial data rates of 2 MHz independent of the MCU clock frequency. Therefore, the ML145051 may be used with the CMOS MCU operating at reduced clock rates to minimize power consumption without severely sacrificing ADC cycle times, with EOC being used to generate an interrupt. (The ML145051 may also be used with MCUs which do not provide a system clock.)

ANALOG DESIGN CONSIDERATIONS

Controllers with output impedances of less than 1 kΩ maybe directly interfaced to these ADCs, eliminating the need for buffer amplifiers. Separate lines connect the V_{ref} and V_{AG} pins on the ADC with the controllers to provide isolation from system noise.

Although not indicated in Figure 15, the V_{ref} and controller output lines may need to be shielded, depending on their length and electrical environment. This should be verified during prototyping with an oscilloscope. If shielding is required, a twisted pair or foil-shielded wire (not coax) is appropriate for this low frequency application. One wire of the pair or the shield must be V_{AG}.

A reference circuit voltage of 5 volts is used for this application. The reference circuitry may be as simple as tying V_{AG} to system ground and V_{ref} to the system's positive supply. (See Figure 16.) However, the system power supply noise may require that a separate supply be used for the voltage reference. This supply must provide source current forV_{ref} as well as current for the controller potentiometers.

A bypass capacitor of approximately 0.22 µF across the V_{ref} and V_{AG} pins is recommended. These pins are adjacent on the ADC package which facilitates mounting the capacitor very close to the ADC.

SOFTWARE CONSIDERATIONS

The software flow for acquisition is straight forward. The nine analog inputs, AN0 through AN8, are scanned by reading the analog value of the previously addressed channel into the MCU and sending the address of the next channel to be read to the ADC, simultaneously.

If the design is realized using the ML145050, 44 ADCLK cycles (at pin 19) must be counted by the MCU to allow time for A/D conversion. The designer utilizing the MC145051 has the end-of-conversion signal (at pin 19) to define the conversion interval. EOC may be used to generate an interrupt, which is serviced by reading the serial data from the ADC. The software flow should then process and format the data, and transfer the information to the video circuitry for updating the display.

When these ADCs are used with a 16-bit (2-byte) transfer, there are two types of offsets involved. In the first type of offset, the channel information sent to the ADCs is offset by 12 bits. That is, in the 16-bit stream, only the first 4 bits (4 MSBs) contain the channel information. The balance of the bits are don't cares. This results in 3 don't-care nibbles, as shown in Table 2. The second type of offset is in the conversion result returned from the ADCs; this is offset by 6 bits. In the 16-bit stream, the first 10 bits (10 MSBs) contain the conversion results. The last 6 bits are zeroes. The hexadecimal result is shown in the first column of Table 3. The second column shows the result after the offset is removed by a microprocessor routine. If the 16-bit format is used, these ADCs can transfer one continuous 16-bit stream or two intermittent 8-bitstreams.

Legacy Applications Information

Table 2. Programmer's Guide for 16-Bit Transfers: Input Code

Input Address in Hex	Channel to be Converted Next	Comment
$0XXX	AN0	Pin 1
$1XXX	AN1	Pin 2
$2XXX	AN2	Pin 3
$3XXX	AN3	Pin 4
$4XXX	AN4	Pin 5
$5XXX	AN5	Pin 6
$6XXX	AN6	Pin 7
$7XXX	AN7	Pin 8
$8XXX	AN8	Pin 9
$9XXX	AN9	Pin 11
$AXXX	AN10	Pin 12
$BXXX	AN11	Half Scale Test: Output = $8000
$CXXX	AN12	Zero Test: Output = $0000
$DXXX	AN13	Full Scale Test: Output = $FFC0
$EXXX	None	Not Allowed
$FXXX	None	Not Allowed

Table 3. Programmer's Guide for 16-Bit Transfers: Output Code

Conversion Result Without Offset Removed	Conversion Result With Offset Removed	Value
$0000	$0000	Zero
$0040	$0001	Zero + 1 LSB
$0080	$0002	Zero + 2 LSBs
$00C0	$0003	Zero + 3 LSBs
$0100	$0004	Zero + 4 LSBs
$0140	$0005	Zero + 5 LSBs
$0180	$0006	Zero + 6 LSBs
$01C0	$0007	Zero + 7 LSBs
$0200	$0008	Zero + 8 LSBs
$0240	$0009	Zero + 9 LSBs
$0280	$000A	Zero + 10 LSBs
$02C0	$000B	Zero + 11 LSBs
$FF40	$03FD	Full Scale – 2 LSBs
$FF80	$03FE	Full Scale – 1 LSB
$FFC0	$03FF	Full Scale

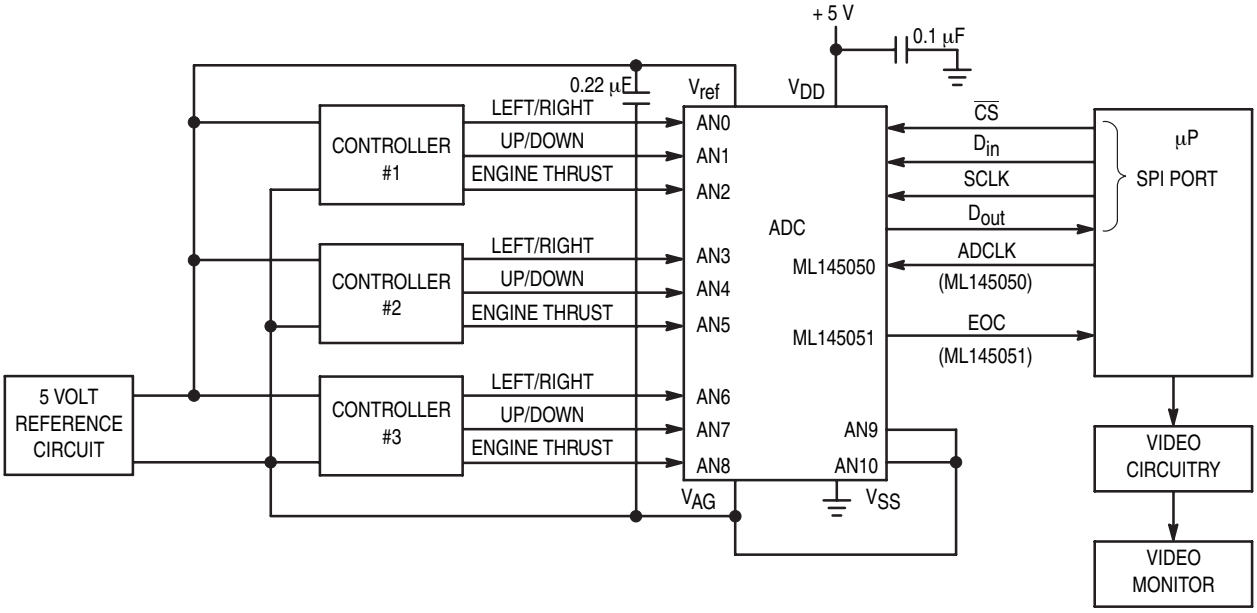


Figure 15. Joystick Interface

Legacy Applications Information

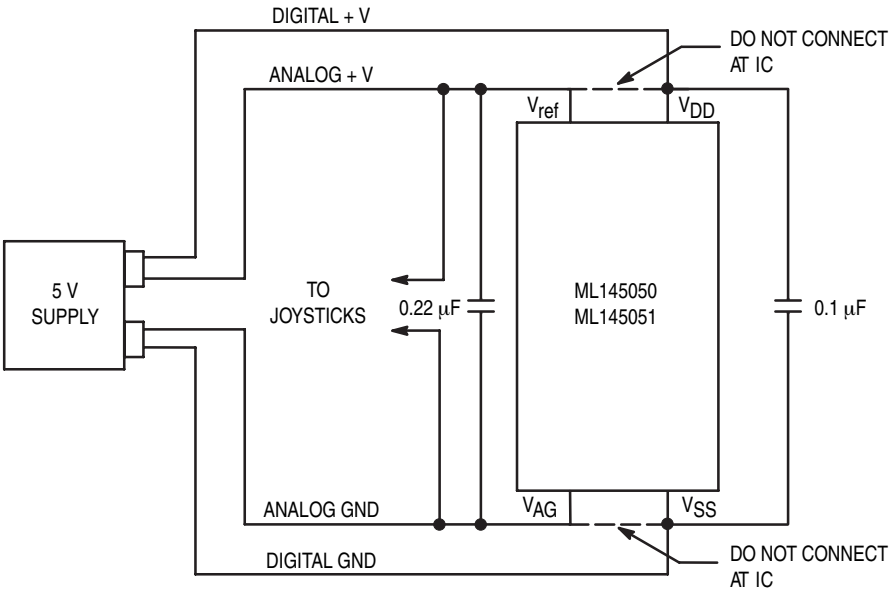


Figure 16. Alternate Configuration Using the Digital Supply for the Reference Voltage

Compatible Motorola MCUs/MPUs

This is not a complete listing of Motorola's MCUs/MPUs.
Contact your Motorola representative if you need
additional information.

Instruction Set	Memory (Bytes)		SPI SCI	Device Number
	ROM	EEPROM		
M6805	2096	–	–	MC68HC05C2
	2096	–	Yes	MC68HC05C3
	4160	–	Yes	MC68HC05C4
	4160	–	Yes	MC68HSC05C5
	8K	–	Yes	MC68HSC05C8
	4160	–	Yes	MC68HCL05C4
	8K	–	Yes	MC68HCL05C8
	7700	–	Yes	MC68HC05C8
	–	4160	–	MC68HC805C5
M68000	–	–	–	MC68HC000

SPI = Serial Peripheral Interface.

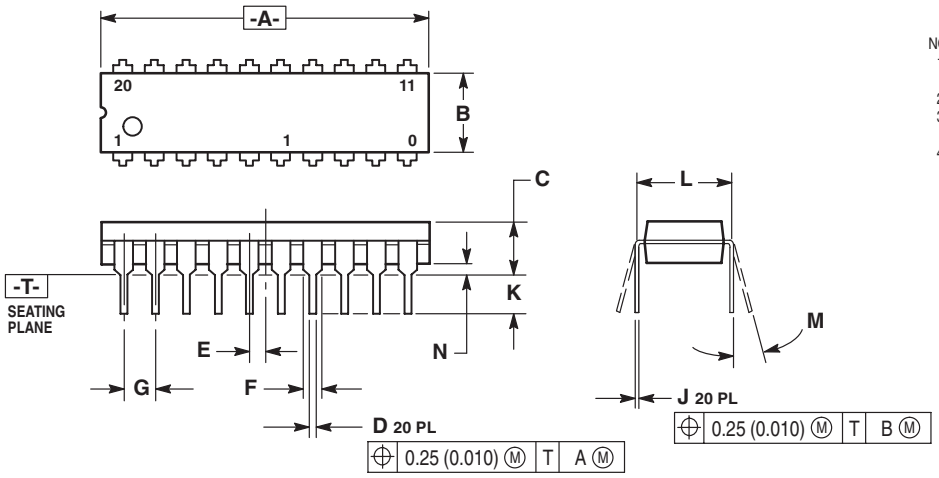
SCI = Serial Communication Interface.

† High Speed.

† Low Power.

OUTLINE DIMENSIONS

P DIP 20 = RP
(ML145050RP, ML145051RP)
CASE 738-03

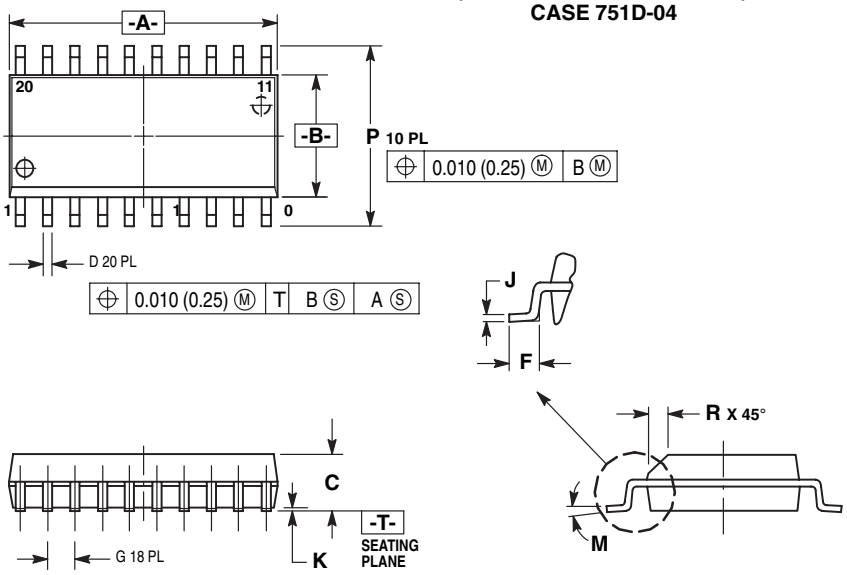


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

OUTLINE DIMENSIONS

SOG 20W = -6P
(ML145050-6P, ML145051-6P)
CASE 751D-04



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOW ABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029