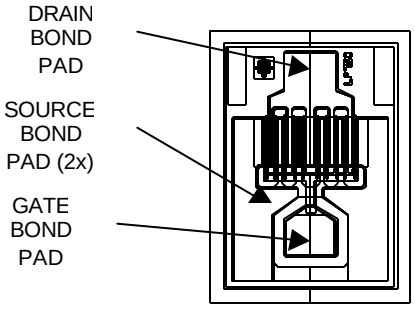
- FEATURES
  - 28 dBm Output Power at 1-dB Compression at 18 GHz
  - 10 dB Power Gain at 18 GHz
  - 24 dBm Output Power at 1-dB Compression at 3.3V
  - 55% Power-Added Efficiency



DIE SIZE: 12.6X16.9 mils (320x430 µm)
DIE THICKNESS: 3 mils (75 µm)
BONDING PADS: 3.3X2.4 mils (85x60 µm)

- DESCRIPTION AND APPLICATIONS

The LP750 is an Aluminum Gallium Arsenide / Indium Gallium Arsenide (AlGaAs/InGaAs) Pseudomorphic High Electron Mobility Transistor (PHEMT), utilizing an Electron-Beam direct-write 0.25 µm by 750 µm Schottky barrier gate. The recessed "mushroom" gate structure minimizes parasitic gate-source and gate resistances. The epitaxial structure and processing have been optimized for reliable high-power applications. The LP750 also features Si_3N_4 passivation and is available in a variety of packages, including SOT89 and P100 packages.

Typical applications include commercial and other types of high-performance power amplifiers, including use within SATCOM uplink transmitters, PCS/Cellular low-voltage high-efficiency output amplifiers, and medium-haul digital radio transmitters.

- ELECTRICAL SPECIFICATIONS @ $T_{Ambient}$ = 25°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Saturated Drain-Source Current	I_{DSS}	V_{DS} = 2 V; V_{GS} = 0 V	180	225	265	mA
Power at 1-dB Compression	P-1dB	V_{DS} = 8 V; I_{DS} = 50% I_{DSS}	26.5	28		dBm
Power Gain at 1-dB Compression	G-1dB	V_{DS} = 8 V; I_{DS} = 50% I_{DSS}	8	10		dB
Power-Added Efficiency	PAE	V_{DS} = 8 V; I_{DS} = 50% I_{DSS}; P_{IN} = 10 dBm		55		%
Maximum Drain-Source Current	I_{MAX}	V_{DS} = 2 V; V_{GS} = 1 V		400		mA
Transconductance	G_M	V_{DS} = 2 V; V_{GS} = 0 V	180	230		mS
Gate-Source Leakage Current	I_{GSO}	V_{GS} = -3 V		5	40	µA
Pinch-Off Voltage	V_P	V_{DS} = 2 V; I_{DS} = 4 mA	-0.25	-1.2	-2.0	V
Gate-Source Breakdown Voltage Magnitude	$\|V_{BDGS}\|$	I_{GS} = 4 mA	-12	-15		V
Gate-Drain Breakdown Voltage Magnitude	$\|V_{BDGD}\|$	I_{GD} = 4 mA	-12	-16		V
Thermal Resistivity	Θ_{JC}			65		°C/W

frequency=18 GHz

• ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Test Conditions	Min	Max	Units
Drain-Source Voltage	V_{DS}	$T_{Ambient}$ = 22 ± 3 °C		12	V
Gate-Source Voltage	V_{GS}	$T_{Ambient}$ = 22 ± 3 °C		-4	V
Drain-Source Current	I_{DS}	$T_{Ambient}$ = 22 ± 3 °C		$2xI_{DSS}$	mA
Gate Current	I_G	$T_{Ambient}$ = 22 ± 3 °C		7.5	mA
RF Input Power	P_{IN}	$T_{Ambient}$ = 22 ± 3 °C		300	mW
Channel Operating Temperature	T_{CH}	$T_{Ambient}$ = 22 ± 3 °C		175	ºC
Storage Temperature	T_{STG}	—	-65	175	ºC
Total Power Dissipation	P_{TOT}	$T_{Ambient}$ = 22 ± 3 °C		2.2	W

Notes:

- Operating conditions that exceed the Absolute Maximum Ratings could result in permanent damage to the device.
- Power Dissipation defined as: $P_{TOT} \equiv (P_{DC} + P_{IN}) - P_{OUT}$, where
  P_{DC}: DC Bias Power
  P_{IN}: RF Input Power
  P_{OUT}: RF Output Power
- Absolute Maximum Power Dissipation to be de-rated as follows above 25°C:
  P_{TOT}= 2.2W – (0.015W/°C) x T_{HS}
  where T_{HS} = heatsink or ambient temperature.

• HANDLING PRECAUTIONS

To avoid damage to the devices care should be exercised during handling. Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing. These devices should be treated as Class 1A (0-500 V). Further information on ESD control measures can be found in MIL-STD-1686 and MIL-HDBK-263.

• ASSEMBLY INSTRUCTIONS

The recommended die attach is gold/tin eutectic solder under a nitrogen atmosphere. Stage temperature should be 280-290°C; maximum time at temperature is one minute. The recommended wire bond method is thermo-compression wedge bonding with 0.7 or 1.0 mil (0.018 or 0.025 mm) gold wire. Stage temperature should be 250-260°C.

• APPLICATIONS NOTES & DESIGN DATA

Applications Notes are available from your local Filtronic Sales Representative or directly from the factory. Complete design data, including S-parameters, noise data, and large-signal models are available on the Filtronic web site.

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