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S3062

Multi-Rate Performance Monitor with Forward Error Correction

Product Status: Production Release

S3062 - Multi-Rate Performance Monitor

Features

- Single 3.3 V supply
- 352-pin SBGA (Super Ball Grid Array) package
- Bellcore, ITU-T and IEEE compliant
- Functions with AMCC MUX/DeMUX chipsets
- Provides a 16 bit input and a 16 bit output single-ended PECL data path
- Provides a FPGA interface for SONET/SDH overhead insertion/extraction as well as PM count retrieval
- Provides a micro processor interface for register access as well as SONET/SDH overhead insertion/extraction
- Provides optional Reed Solomon encoding of data for Forward Error Correction (FEC)
- Provides optional Reed Solomon decoding of data for Forward Error Correction (FEC)
- Optionally differentially decodes and encodes incoming and outgoing data
- Provides on-chip clock dividers to simplify external clock generation for Forward Error Correction (FEC)
- Extracts and optionally inserts SONET/SDH overhead bytes via an MPC860 microprocessor port
- Extracts and optionally inserts SONET/SDH overhead bytes via a 21 bit FPGA port
- Extracts and optionally inserts orderwire bytes (E1 and E2) via serial I/O
- Extracts and optionally inserts the data communication channels (D1-3 and D4-12) via serial I/O
- Performs frame and byte alignment and outputs frame pulses
- Performs optional frame-synchronous scrambling and descrambling
- Monitors FEC data for total corrected bit errors, corrected ones, corrected zeros, corrected bytes, and uncorrectable blocks
- Monitors for Loss of Signal and outputs alarm (LOS)
- Monitors for Out of Frame and outputs alarm (OOF)
- Monitors for Loss of Frame and outputs alarm (LOF)
- Monitors J0 byte for section trace messages
- Monitors B1 byte for Bit Interleave parity errors and outputs error indications (B1ERR) Monitors B2 byte for Bit interleave parity errors, Signal Degrade (SD) and Signal Fail (SF)
- Monitors K1, K2 bytes for Automatic Protection Switching (APS) changes, line AIS and line RDI
- Monitors the S1 byte for mismatches and inconsistent values
- Monitors the M1 byte for Remote Error Indications (REI)
- Monitors for Gigabit Ethernet Loss of Synchronization (LOS), 8B/10B code violations, and disparity errors
- Optionally provides a data link in the FEC framing bytes for transmission of messages, error

Product Documents

Click here for ALL available documents/types listed.

NOTE: Additional documents may be available when logged in.

Related Products

S19208
S19227
S3052
S4815

information, orderwire, etc.
- Optionally calculates and inserts section bit interleaved parity (B1)
- Optionally calculates and inserts line bit interleaved parity (B2)
- Optionally turns OFF (sets low) all transmitted data
- Optionally inserts AIS, either automatically depending on line conditions or under user control
- Optionally inserts valid SONET/SDH section and line overhead on any data format with clock inputs
- Generates valid SONET/SDH section (regenerator) overhead with line AIS data with only a clock input
- Optionally permits transparent pass through of all data regardless of format
- Optionally injects bit errors in any data type

Applications
- SONET/SDH-based transmission systems and test equipment
- Gigabit Ethernet-based transmission systems
- Add Drop Multiplexers (ADM)
- Fiber optic terminators, repeaters and test equipment
- FEC augmented applications for reliable data transmission over impaired channels

General Description

The S3062 Multi-Rate SONET/SDH STS-3/STM-1, STS-12/STM-4, STS-48/STM-16 & Gigabit Ethernet (GBE) Performance Monitor chip with FEC is a fully integrated checking device complying with SONET/SDH transmission standards. The S3062 implements all necessary Performance Monitoring functions on the SONET/SDH section and line overhead bytes at three different rates (STS-3/STM-1, STS-12/STM-4, and STS-48/STM-16). It also has a mode of operation permitting it to monitor a Gigabit Ethernet data stream for loss of synchronization, 8B/10B code violations and disparity errors. Furthermore, any type of data entering and leaving the chip can be FEC and differentially encoded/decoded.

The Typical Monitor and Insertion Application diagram shows a typical network application for the Performance Monitor. Data is received from the fiber and passed through a clock/data recovery device (CDR) and a de-multiplexer device to the S3062. The S3062, optionally, carries out performance monitor error checking, and overhead data extraction, and insertion. Detected errors and accumulated error counts can be accessed by the user either through a processor interface, an FPGA interface, or in a number of cases, from I/O pins. The data stream is then transmitted out onto the fiber via a high-speed multiplexer, and an optics device. All SONET/GBE performance monitor error checking and overhead insertion may be bypassed by selecting the low-power pass-through mode of operation.