AWT6321

HELP2™ Dual-band Cellular/PCS CDMA
3.4 V Linear Power Amplifier Module

Data Sheet - Rev 2.2

FEATURES

- InGaP HBT Technology
- High Efficiency:
  19 % @ +16 dBm
  39 % @ +28 dBm
- Low Quiescent Current: 15 mA
- Internal Voltage Regulation
- Common V_{MODE} Control Line
- Simplified V_{CC} Bus PCB routing
- Reduced External Component Count
- Low Profile Surface Mount Package: 1 mm
- RoHS Compliant Package, 250 °C MSL-3
- Suitable for BC10 (806-824 MHz) band applications

M28 Package
14 Pin 3 mm x 5 mm x 1 mm
Surface Mount Module

APPLICATIONS

- CDMA/EVDO & Cell & PCS Dual-band Wireless Handsets and Data Devices

PRODUCT DESCRIPTION

The AWT6321 addresses the demand for increased integration in dual-band handsets for North American CDMA network deployments. The small footprint 3 mm x 5 mm x 1 mm surface mount RoHS compliant package contains independent RF PA paths to ensure optimal performance in both frequency bands, while achieving a 25% PCB space savings compared with solutions requiring two single-band PAs. The package pinout was chosen to enable handset manufacturers to easily route V_{CC} to both power amplifiers and simplify control with a common V_{MODE} pin. The device is manufactured on an advanced InGaP HBT MMIC technology offering state-of-the-art reliability, temperature stability, and ruggedness. The AWT6321 is part of ANADIGICS' High-Efficiency-at-Low-Power (HELP™) family of CDMA power amplifiers, which deliver low quiescent currents and significantly greater efficiency without a costly external DAC or DC-DC converter. Through selectable bias modes, the AWT6321 achieves optimal efficiency across different output power levels, specifically at low- and mid-range power levels where the PA typically operates, thereby dramatically increasing handset talk-time and standby-time. Its built-in voltage regulator eliminates the need for external switches. The 3 mm x 5 mm x 1 mm surface mount package incorporates matching networks optimized for output power, efficiency and linearity in a 50 Ω system.

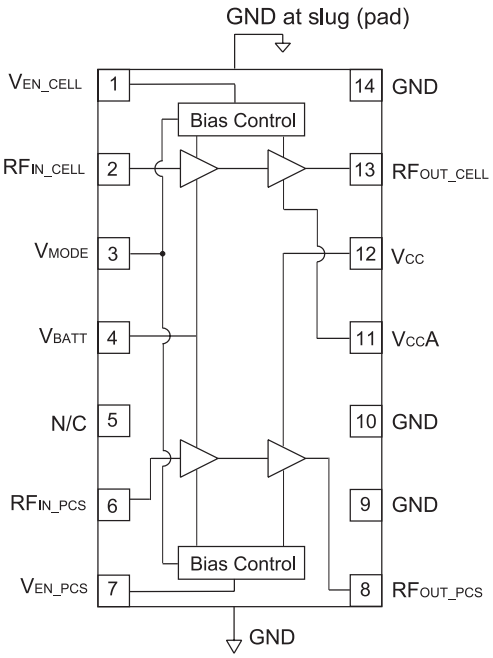


Figure 1: Block Diagram

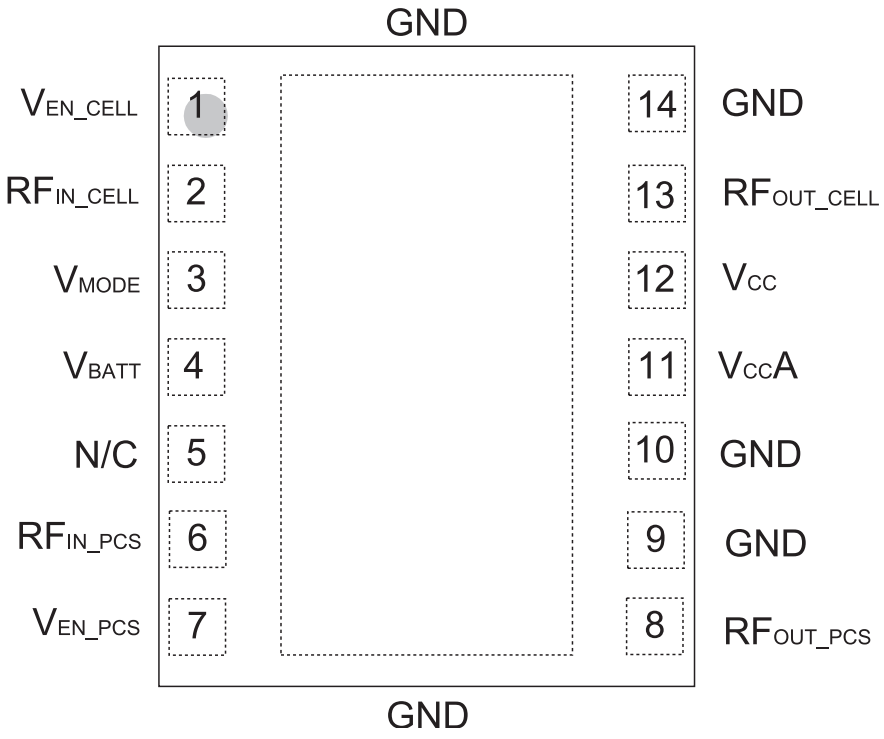


Figure 2: Pinout

Table 1: Pin Description

PIN	NAME	DESCRIPTION
1	V_{EN_CELL}	Enable Voltage for Cell Band
2	RF_{IN_CELL}	RF Input for Cell Band
3	V_{MODE}	Mode Control Voltage for Cell and PCS Bands
4	V_{BATT}	Battery Voltage
5	N/C	No Connection
6	RF_{IN_PCS}	RF Input for PCS Band
7	V_{EN_PCS}	Enable Voltage for PCS Band
8	RF_{OUT_PCS}	RF Output for PCS Band
9	GND	Ground
10	GND	Ground
11	$V_{CC}A$	Battery Voltage A
12	V_{CC}	Supply Voltage
13	RF_{OUT_CELL}	RF Output for Cell Band
14	GND	Ground

ELECTRICAL CHARACTERISTICS

Table 2: Absolute Minimum and Maximum Ratings

PARAMETER	MIN	MAX	UNIT
Supply Voltage (V_{BATT}, V_{CC}, $V_{CC}A$)	0	+5	V
Mode Control Voltage (V_{MODE})	0	+3.5	V
Enable Voltage (V_{EN_CELL}, V_{EN_PCS})	0	+3.5	V
RF Input Power (P_{IN})	-	+10	dBm
Storage Temperature (T_{STG})	-40	+150	°C

Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability.

Table 3: Operating Ranges

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Operating Frequency (f)	824 1850	-	849 1915	MHz	Cellular PCS
Supply Voltage (V_{CC} and V_{BATT})	+3.2	+3.4	+4.2	V	
Enable Voltage (V_{EN})	+2.2 0	+2.4 -	+3.1 +0.5	V	PA "on" PA "shut down"
Mode Control Voltage (V_{MODE})	+2.2 0	+2.4 -	+3.1 +0.5	V	Low Bias Mode High Bias Mode
Cellular RF Output Power (P_{OUT}) CDMA	+27.5 (1)	+28.0	-	dBm	
PCS RF Output Power (P_{OUT}) CDMA	+27.5 (1)	+28.0	-	dBm	
Case Temperature (T_C)	-30	-	+85	°C	

The device may be operated safely over these conditions; however, parametric performance is guaranteed only over the conditions defined in the electrical specifications.

Notes:

(1) For operation at V_{CC} = +3.2 V, P_{OUT} is derated by 0.5 dB.

Table 4: Electrical Specifications - Cellular Band
(T_C = +25 °C, V_{BATT} = V_{CC} = +3.4 V, V_{ENABLE} = +2.4 V, 50 Ω system, IS-95 uplink waveform)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Gain	24.0 15.0 15.5	26.0 16.5 17.0	29.0 19.0 20.0	dB	P_{OUT} = +28 dBm, V_{MODE} = 0 V P_{OUT} = +16 dBm, V_{MODE} = +2.4 V P_{OUT} = +17 dBm, V_{MODE} = +2.4 V, V_{CC} = +3.7 V
Adjacent Channel Power at ±885 kHz offset (1) Primary Channel BW = 1.23 MHZ Adjacent Channel BW = 30 kHz	- - -	-50 -53 -53	-46.5 -47 -47	dBc	P_{OUT} = +28 dBm, V_{MODE} = 0 V P_{OUT} = +16 dBm, V_{MODE} = +2.4 V P_{OUT} = +17 dBm, V_{MODE} = +2.4 V, V_{CC} = +3.7 V
Adjacent Channel Power at ±1.98 MHz offset (1) Primary Channel BW = 1.23 MHZ Adjacent Channel BW = 30 kHz	- -	-65 -60	-57 -57	dBc	P_{OUT} = +28 dBm, V_{MODE} = 0 V P_{OUT} = +16 dBm, V_{MODE} = +2.4 V
Power-Added Efficiency (1)	36 18	39 22	- -	%	P_{OUT} = +28 dBm, V_{MODE} = 0 V P_{OUT} = +16 dBm, V_{MODE} = +2.4 V
Quiescent Current (Icq)	-	15	20	mA	V_{MODE} = +2.4 V, Low Bias
Enable Current	-	0.4	0.8	mA	through V_{EN} pin, V_{MODE} = +2.4 V
Battery Current	-	2.5	5	mA	through V_{BATT} pin, V_{MODE} = +2.4 V
Mode Control Current	-	0.75	1.0	mA	through V_{MODE} pin, V_{MODE} = +2.4 V
Leakage Current	-	<1	5	μA	V_{CC} = +4.2 V, V_{EN} = 0 V, V_{MODE} = 0 V
Noise in Receive Band	-	-133	-131	dBm/Hz	869 MHz to 894 MHz
Harmonics 2fo 3fo, 4fo	- -	-42 -50	-30 -30	dBc	
Input Impedance	-	-	2:1	VSWR	
Spurious Output Level (all spurious outputs)	-	-	-65	dBc	P_{OUT} ≤ +28 dBm In-band Load VSWR < 5:1 Out-of-band Load VSWR < 10:1 Applies over all operating conditions
Load mismatch stress with no permanent degradation or failure	8:1	-	-	VSWR	Applies over all operating conditions

Notes:
(1) PAE and ACP limit applies at 836.5 MHz.

Table 5: Electrical Specifications - PCS Band
(T_C = +25 °C, V_{BATT} = V_{CC} = +3.4 V, V_{ENABLE} = +2.4 V, 50 Ω system, IS-95 uplink waveform)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Gain	25.0 12.5 13.0	27.0 14.5 15.5	30.0 17.0 18.0	dB	P_{OUT} = +28 dBm, V_{MODE} = 0 V P_{OUT} = +16 dBm, V_{MODE} = +2.4 V P_{OUT} = +18 dBm, V_{MODE} = +2.4 V, V_{CC} = +3.7 V
Adjacent Channel Power at ±1.25 MHz offset Primary Channel BW =1.23 MHz Adjacent Channel BW = 30 kHz	- - -	-50 -55 -51	-46.5 -47 -47	dBc	P_{OUT} = +28 dBm, V_{MODE} = 0 V P_{OUT} = +16 dBm, V_{MODE} = +2.4 V P_{OUT} = +18 dBm, V_{MODE} = +2.4 V, V_{CC} = +3.7 V
Adjacent Channel Power at ± 1.98 MHz offset Primary Channel = 1.23 MHz Adjacent Channel = 30 kHz	- -	-56 -56	-53 -53	dBc	P_{OUT} = +28 dBm, V_{MODE} = 0 V P_{OUT} = +16 dBm, V_{MODE} = +2.4 V
Adjacent Channel Power at ±2.25 MHz offset Primary Channel BW =1.23 MHz Adjacent Channel BW = 30 kHz	- -	-63 -61	-57 -57	dBc	P_{OUT} = +28 dBm, V_{MODE} = 0 V P_{OUT} = +16 dBm, V_{MODE} = +2.4 V
Power-Added Efficiency	35.5 15	39 17	- -	%	P_{OUT} = +28 dBm, V_{MODE} = 0 V P_{OUT} = +16 dBm, V_{MODE} = +2.4 V
Quiescent Current (Icq)	-	15	20	mA	through V_{CC} pin, V_{MODE} = +2.4 V
Enable Current	-	0.3	0.8	mA	through V_{EN} pin, PA "on"
Mode Control Current	-	0.75	1.0	mA	through V_{MODE} pin, V_{MODE} = +2.4 V
Battery Current	-	3	5	mA	through V_{BATT} pin, V_{MODE} = +2.4 V
Leakage Current	-	<1	5	µA	V_{CC} = +4.2 V, V_{EN} = 0 V, V_{MODE} = 0 V
Noise in Receive Band	-	-134	-132	dBm/Hz	1930 MHz to 1990 MHz
Harmonics 2fo 3fo, 4fo	- -	-43 -55	-30 -30	dBc	
Input Impedance	-	-	2:1	VSWR	
Spurious Output Level (all spurious outputs)	-	-	-65	dBc	P_{OUT} ≤ +28 dBm In-band load VSWR < 5:1 Out-of-band load VSWR < 10:1 Applies over all operating ranges
Load mismatch stress with no permanent degradation or failure	8:1	-	-	VSWR	Applies over full operating range

Notes:
1. ACPRs and Efficiency limits at mid-band only.

APPLICATION INFORMATION

To ensure proper performance, refer to all related Application Notes on the ANADIGICS web site: http://www.anadigics.com

Shutdown Mode

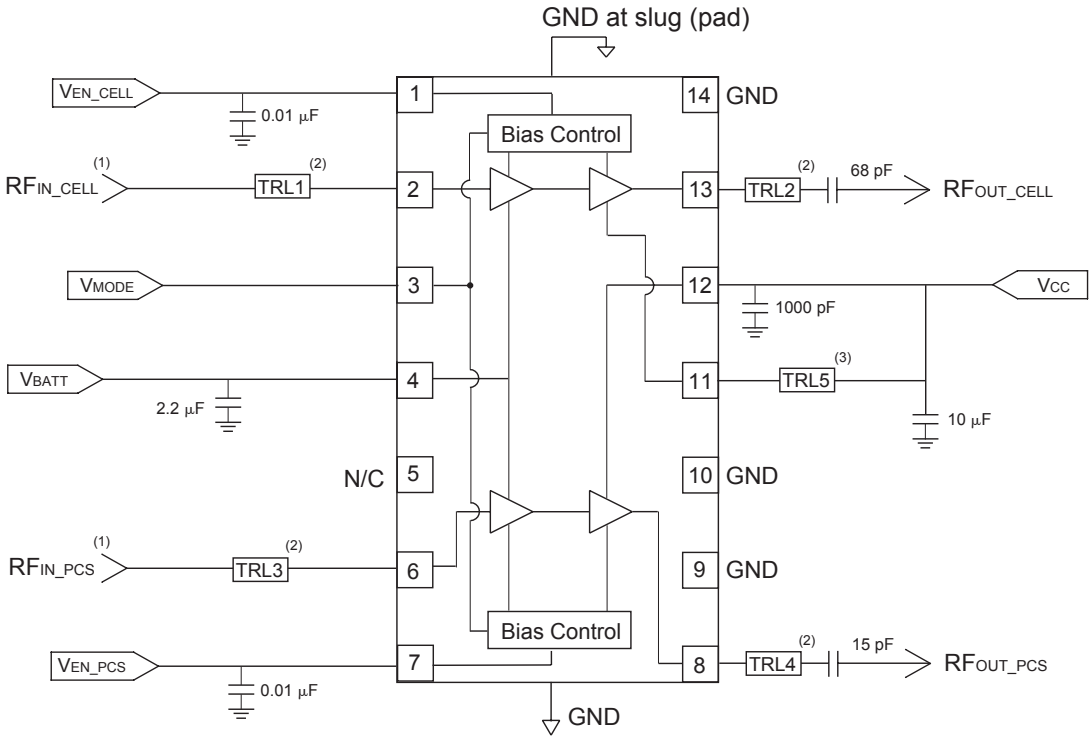
The power amplifier may be placed in a shutdown mode by applying logic low levels (see Operating Ranges table) to the V_{ENABLE} and V_{MODE} voltages.

Bias Modes

The power amplifier may be placed in either a Low Bias mode or a High Bias mode by applying the appropriate logic level (see Operating Ranges table) to the V_{MODE} voltages. The Bias Control table lists the recommended modes of operation for various applications.

Table 6: Bias Control

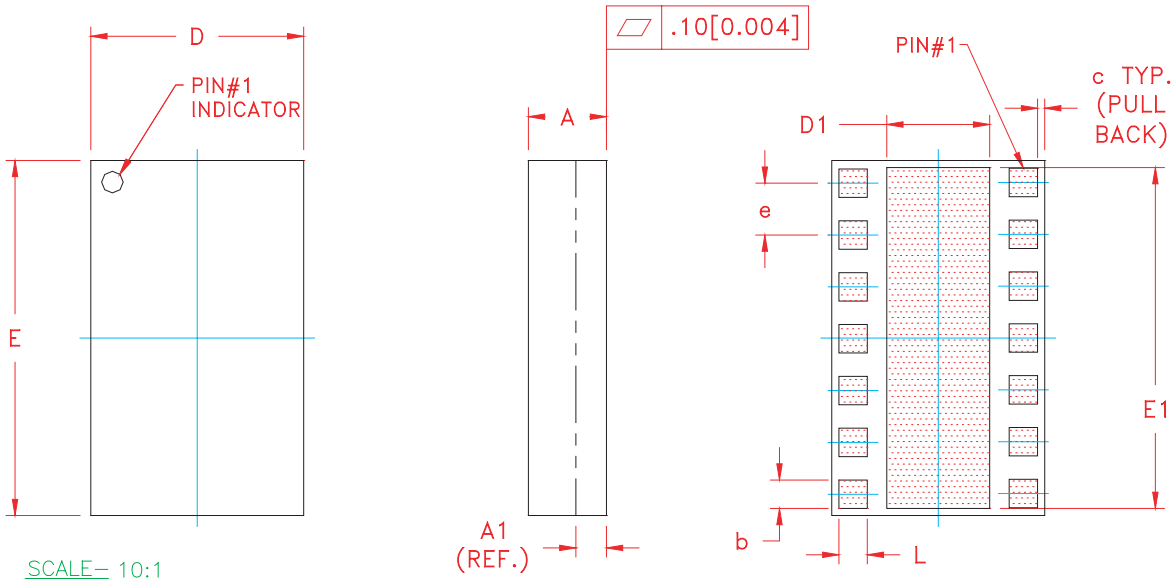
APPLICATION	P_{OUT} LEVELS	BIAS MODE	V_{ENABLE}	V_{MODE}	V_{CC}	V_{BATT}
CDMA - low power	≤ +16 dBm	Low	+2.4 V	+2.4 V	3.2 - 4.2 V	≥ 3.2 V
CDMA - high power	> +16 dBm	High	+2.4 V	0 V	3.2 - 4.2 V	≥ 3.2 V
Optional lower V_{CC} in low power mode	≤ +7 dBm	Low	+2.4 V	+2.4 V	1.5 V	≥ 3.2 V
Shutdown	-	Shutdown	0 V	0 V	3.2 - 4.2 V	≥ 3.2 V



Note:
(1) Add blocking cap if DC voltage is present on input pin.
(2) TRL should be short and of 50 Ω characteristic impedance.
(3) TRL 5 should be as long as possible (minimum of 0.1 λ at 800 MHz) and capable of handling 1200 mA current.

Figure 3: Application Circuit

PACKAGE OUTLINE



SYMBOL	MILLIMETERS			INCHES			NOTE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	0.90	1.00	1.10	0.035	0.039	0.043	–
A1	0.35 (REF.)			0.014 (REF.)			–
b	0.37	–	0.57	0.015	–	0.022	3
c	–	0.10	–	–	0.004	–	–
D	2.88	3.00	3.12	0.113	0.118	0.123	–
D1	1.58	–	1.83	0.062	–	0.072	3
E	4.88	5.00	5.12	0.192	0.197	0.202	–
E1	4.75	–	4.85	0.187	–	0.190	3
e	–	0.73	–	–	0.029	–	4
L	0.33	–	0.52	0.013	–	0.020	3

NOTES:

1. CONTROLLING DIMENSIONS: MILLIMETERS
2. UNLESS SPECIFIED TOLERANCE=±0.076[0.003].
3. PADS (INCLUDING CENTER) SHOWN UNIFORM SIZE FOR REFERENCE ONLY. ACTUAL PAD SIZE AND LOCATION WILL VARY WITHIN MIN. AND MAX. DIMENSIONS ACCORDING TO SPECIFIC LAMINATE DESIGN.
4. PITCH MEASUREMENT (e) TAKEN CENTERLINE TO CENTERLINE OF SOLDER MASK OPENINGS.
5. UNLESS SPECIFIED DIMENSIONS ARE SYMMETRICAL ABOUT CENTER LINES SHOWN.

Figure 4: Package Outline - 14 Pin 3 mm x 5 mm x 1 mm Surface Mount Module

TOP BRAND

NOTES:

1. ANADIGICS LOGO SIZE: NONE
2. PART NUMBER: FOUR DIGIT NUMERICAL
3. WAFER LOT NUMBER: LLLL = LOT NUMBER
   NN = WAFER I.D.
4. PIN 1 INDICATOR: LASER DOT
5. B.O.M. # BBB
6. COUNTRY CODE: CC = TH–for–THAILAND, TW–for–TAIWAN
   CC = PH–for–PHILIPPINES, CH–for–CHINA
7. TYPE : ARIAL
   SIZE : 1.5–POINT
   COLOR : LASER
8. DATE CODE YY - YEAR
   WW - WORK WEEK

Figure 5: Branding Specification

ORDERING INFORMATION

ORDER NUMBER	TEMPERATURE RANGE	PACKAGE DESCRIPTION	COMPONENT PACKAGING
AWT6321RM28Q7	-20 °C to +85 °C	RoHS Compliant 14 Pin 3 mm x 5 mm x 1 mm Surface Mount Module	Tape and Reel, 2500 pieces per Reel
AWT6321RM28P9	-20 °C to +85 °C	RoHS Compliant 14 Pin 3 mm x 5 mm x 1 mm Surface Mount Module	Partial Tape and Reel

ANADIGICS, Inc.
141 Mount Bethel Road
Warren, New Jersey 07059, U.S.A.
Tel: +1 (908) 668-5000
Fax: +1 (908) 668-5132

URL: http://www.anadigics.com
E-mail: Mktg@anadigics.com

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