Nonvolatile DACPOT™ Electronic Potentiometer With Debounced Push Button Interface

FEATURES

Digitally Controlled Electronic Potentiometer

- **8-Bit Digital-to-Analog Converter (DAC)**
  - **Independent Reference Inputs**
  - **Differential Non-Linearity - ±0.5LSB max**
  - **Integral Non-Linearity - ±1LSB max**
- **V_{OUT} Value in EEPROM for Power-On Recall**
  - **Equivalent to 256-Step Potentiometer**
- **Unity Gain Op Amp Drives up to 1mA**
- **Simple Trimming Adjustment**
  - **Debounced Push Button Interface**
- **Low Noise Operation**
- **"Clickless" Transitions between DAC Steps**
- **No Mechanical Wearout Problem**
  - **1,000,000 Stores (typical)**
  - **100 Year Data Retention**
- **Operation from +2.7V to +5.5V Supply**
- **Low Power, 1mW max at +5V**

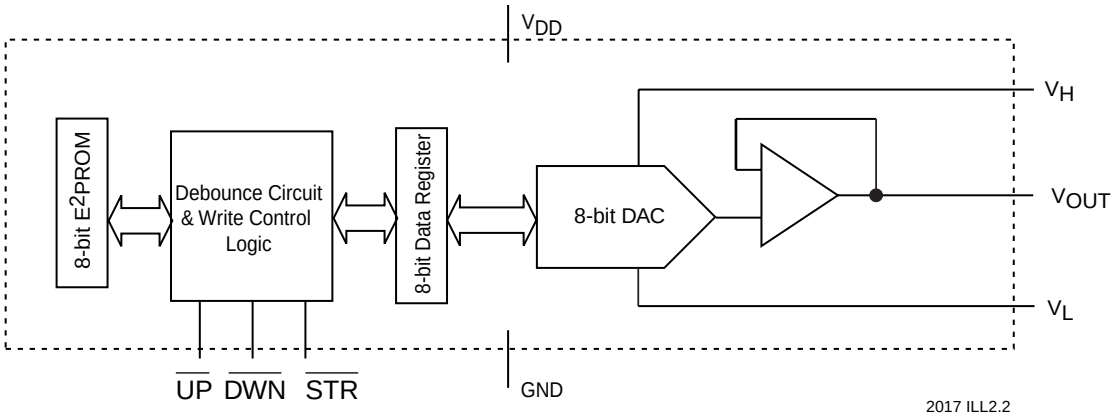
OVERVIEW

The S9518 DACPOT trimmer is an 8-bit nonvolatile DAC designed to replace mechanical potentiometers. The S9518 includes a unity-gain amplifier to buffer the DAC output and enables V_{OUT} to swing from rail to rail. The DACPOT trimmer operates over a supply voltage range of 2.7V to 5.5V.

The S9518's simple push button input provides an ideal interface for operator adjusted equipment. This interface allows for quick and easy adjustment of even the most sophisticated systems.

The S9518 is a pin-compatible performance upgrade for other industry nonvolatile potentiometers. The S9518 offers double the resolution of these devices and provides 'clickless' transitions of V_{OUT}.

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

Symbol	Description
$\overline{UP}$	PB Input, Moves V_{OUT} Toward V_H Input
$\overline{DWN}$	PB Input, Moves V_{OUT} Toward V_L Input
V_H	Vref High
GND	Ground
V_{OUT}	Trimmed Voltage Output
V_L	Vref Low
$\overline{STR}$	Store Input, Providing a Control Input to Initiate a Store Operation
V_{DD}	Supply Voltage (2.7V to 5.5V)

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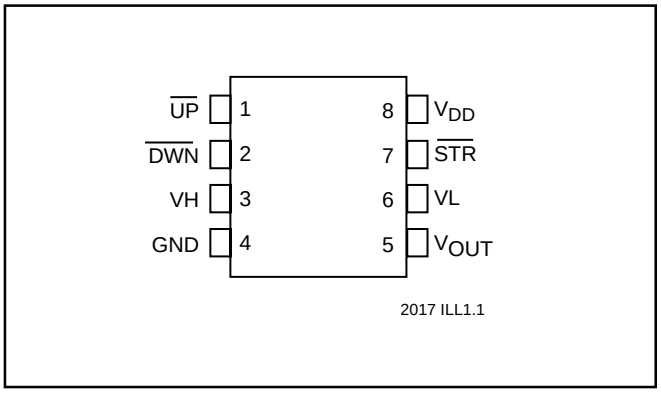
PINOUT



Analog Section

The S9518 is an 8-bit, voltage output digital-to-analog converter (DAC). The DAC consists of a resistor network that converts 8-bit digital values into equivalent analog output voltages in proportion to the applied reference voltage.

Reference Inputs

The voltage differential between the V_L and V_H inputs sets the full-scale output voltage range. V_L must be equal to or greater than ground (a positive voltage). V_H must be greater than V_L and less than or equal to V_{DD}. See specifications on page 5 for guaranteed operating limits.

Output Buffer Amplifier

The voltage output is from a precision unity-gain follower that can slew up to 1V/µs.

Digital Interface

The interface provides simple push button control of an up/down counter that drives the DAC. The DAC output is a ratiometric voltage output.

$\overline{UP}$ is an active low push-button input. An internal pull-up resistor, with nominal value of 50kohm, eliminates an external resistor that would be required with push button control. A 30ms debounce period is included in the input timing to prevent multiple pulsing of the counter. Either a switch closure to ground or a LOW logic level will, after the debounce time, change the potentiometer tap position. $\overline{UP}$ moves the output voltage towards the V_H reference input. If the $\overline{UP}$ push-button is kept depressed, the counter will continue to increment at the rate of one count every 250ms for one second. After one second the counter increments faster, one count every 50ms, until the push-button is released. Changes to the DAC output using the $\overline{UP}$ input do not alter the data stored in EEPROM. The $\overline{STR}$ input updates the nonvolatile EEPROM memory.

$\overline{DWN}$ is an active low push-button input that decrements the counter and moves the potentiometer output voltage towards the V_L reference input. The $\overline{DWN}$ control input also includes an internal 50kohm pull-up resistor and a 30ms debounce period to prevent multiple pulsing. A LOW logic level will also change the potentiometer tap position after the debounce period. If the $\overline{DWN}$ push-button is kept depressed, the counter continues to decrement at the rate of one count every 250ms for one second. After one second the counter decrements at one count every 50ms until the push-button is released. Changes to the DAC output using the $\overline{DWN}$ input do not alter the data stored in EEPROM.

$\overline{STR}$ This input can be used in two ways:

1) If the input is tied LOW, then AUTOSTORE is enabled. When V_{DD} powers-down an automatic store cycle takes place that updates the nonvolatile EEPROM memory.

2) $\overline{STR}$ is an active low push-button input that also updates the nonvolatile memory. The input is debounced but does not have an internal pull-up resistor. For every valid push, the S9518 will store the current potentiometer position to EEPROM.

DEVICE OPERATION

There are five main blocks to the S9518: an 8-bit EEPROM memory; input debounce circuits, control logic, and 8-bit counter; 8-bit data register; decode section and resistor ladder (DAC); and the buffer amplifier. The input control section operates just like an up/down counter. The output of this counter is fed to the data register and then decoded to activate one of 255 electronic switches connected to the resistor ladder. Each switch connects a point on the ladder to the buffer amplifier input. When requested, the contents of the counter can be stored in EEPROM memory and retained for future use. The ladder is comprised of 256 resistors of equal value connected in series. At the bottom of the ladder and at the junctions of the resistors there are electronic switches that transfer the voltage at each point to the buffer amplifier and hence to the output. The S9518 is designed to interface directly to two push button switches that effectively move the potentiometer wiper up or down. The $\overline{UP}$ and $\overline{DWN}$ inputs increment or decrement the 8-bit counter respectively. The data input to the DAC is decoded to select one of the 256 wiper positions along the resistive ladder. The wiper increment input, $\overline{UP}$ and the wiper decrement input, $\overline{DWN}$ are connected to internal pull-ups so that they normally remain HIGH. When pulled LOW by an external push button switch or a logic LOW level input, the wiper will be switched to the next adjacent tap position. Internal debounce circuitry prevents inadvertent switching of the wiper position if $\overline{UP}$ or $\overline{DWN}$ remain LOW for less than 30ms (typical). Each of the buttons can be pushed either once for a single increment/decrement or held low continuously for a multiple increments/decrements. The number of increments/decrements of the wiper position depends on how long the button is pushed. When making a continuous push, after the first second, the increment/decrement speed increases. For the first second the device will be in the slow scan mode. Then if the button is held for longer than one second the device will go into the fast scan mode. As soon as the button is released the S9518 will return to a standby condition. The DAC, whether set to 00 or FF, acts like its mechanical equivalent and does not move beyond the last position. That is, the counter does not wrap around when clocked beyond FF or below 00.

AUTOSTORE

The value of the counter is stored in EEPROM memory whenever the chip senses a power-down of V_{DD} while $\overline{STR}$ is enabled (held LOW). When power is restored, the contents of the memory are recalled and the counter reset to the last value stored. If AUTOSTORE is to be implemented, $\overline{STR}$ is typically hard wired to GND. If $\overline{STR}$ is held HIGH during power-up and then taken LOW, the wiper will not respond to the $\overline{UP}$ or $\overline{DWN}$ inputs until $\overline{STR}$ is brought HIGH and the store is complete. Figure 1.

Manual (Push Button) Store

When $\overline{STR}$ is not enabled (held HIGH) a push button switch may be used to pull $\overline{STR}$ LOW and released to perform a manual store of the wiper position in EEPROM memory. Figure 2.

Effect of V_{DD} Removal

The resistor ladder, connected between V_H and V_L, does not change value when V_{DD} is removed. However, the buffer amplifier no longer functions and consequently a high impedance appears at the V_{OUT} pin.

Figure 1: Typical circuit with $\overline{STR}$ store pin used in AUTOSTORE mode

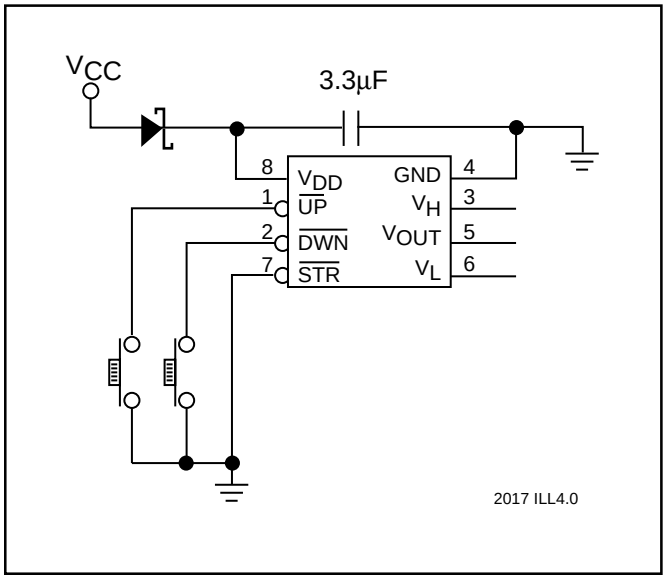
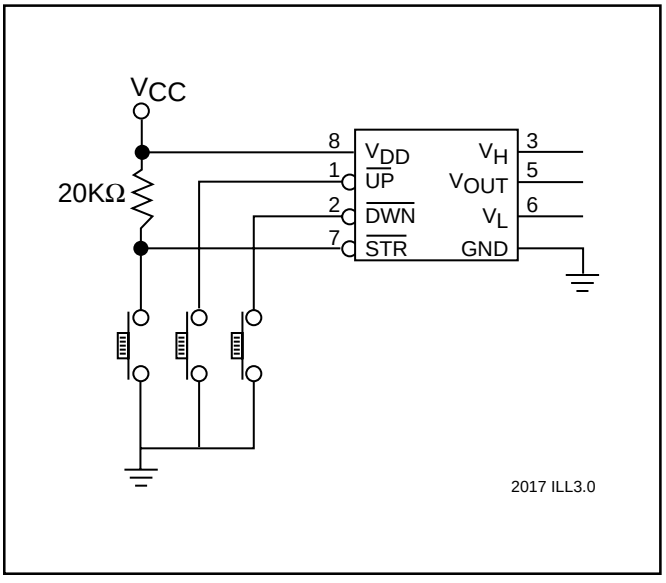


Figure 2: Typical circuit with $\overline{STR}$ store pin controlled by push button switch



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on pins with reference to GND:	
Analog Inputs	-0.5V to V_{DD}+.5V
Digital Inputs	-0.5V to V_{DD}+.5V
Analog Outputs	-0.5V to V_{DD}+.5V
Digital Outputs	-0.5V to V_{DD}+.5V
Lead Solder Temperature (10 secs)	300°C

***COMMENT**

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside those listed in the operation sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RECOMMENDED OPERATING CONDITIONS

Condition	Min	Max
Temperature	-40°C	+85°C
V_{DD}	+2.7V	+5.5V

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DAC DC ELECTRICAL CHARACTERISTICS

V_{DD} = +2.7V to +5.5V, V_{refH} = V_{DD}, V_{refL} = 0V, T_A = -40°C to +85°C, unless specified otherwise

	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Accuracy	INL	Integral Non-Linearity	I_{LOAD} = 100µA,	-	0.5	±1	LSB
	DNL	Differential Non-Linearity	I_{LOAD} = 100µA, Guaranteed but not tested	-	0.1	±0.5	LSB
References	V_H	V_{refH} Input Voltage		V_{refL}	-	V_{DD}	V
	V_L	V_{refL} Input Voltage		Gnd	-	V_{refH}	V
	R_{IN}	V_{refH} to V_{refL} Resistance		-	38k	-	Ω
	TCR_{IN}	Temperature Coefficient of R_{IN}	V_{refH} to V_{refL}	-	600	-	ppm/°C
Analog	G_{EFS}	Full-Scale Gain Error	DATA = FF			±1	LSB
Output	$V_{OUT}ZS$	Zero-Scale Output Voltage	DATA = 00	0		20	mV
	TCV_{OUT}	V_{OUT} Temperature Coefficient	V_{DD} = +5, I_{LOAD} = 50µA, V_{refH} = +5V, V_{refL} = 0V Guaranteed but not tested	-	-	50	µV/°C
	I_L	Amplifier Output Load Current		-200		+1000	µA
	R_{OUT}	Amplifier Output Resistance	I_{LOAD} = 100µA V_{DD} = +5V V_{DD} = +3V	- -	10 20		Ω Ω
	PSRR	Power Supply Rejection	I_{LOAD} = 10µA	-	-	1	LSB/V
	e_N	Amplifier Output Noise	f = 1kHz, V_{DD} = +5V	-	90	-	nV/ $\sqrt{Hz}$
	THD	Total Harmonic Distortion	V_{IN} = 1V rms, f = 1kHz	-	0.08	-	%
	BW	Bandwidth - 3dB	V_{IN} = 100mV rms	-	300	-	kHz

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RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min	Max	Unit	Test Method
V_{ZAP}	ESD Susceptibility	2000		V	MS-883, TM 3015
I_{LTH}	Latch-Up	100		mA	JEDEC Standard 17
T_{DR}	Data Retention	100		Years	MS-883, TM 1008
N_{END}	Endurance	1,000,000		Stores	MS-883, TM 1033

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DC ELECTRICAL CHARACTERISTICS V_{DD} = +2.7V to +5.5V, $V_H = V_{DD}$, V_L = 0V, Unless otherwise specified

Symbol	Parameter	Conditions	Min	Max	Units
I_{DD}	Supply Current during store, note 1	$\overline{STR}$ = ⊓_		1.2	mA
I_{SB}	Supply Standby Current			200	µA
I_{IH}	Input Leakage Current	$V_{IN} = V_{DD}$		10	µA
I_{IL}	Input Leakage Current, note 2	V_{IN} = 0V		-100	µA
V_{IH}	High Level Input Voltage		2	V_{DD}	V
V_{IL}	Low Level Input Voltage		0	0.8	V

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Notes:

1. I_{DD} is the supply current drawn while the EEPROM is being updated. I_{DD} does not include the current that flows through the Reference resistor chain.
2. $\overline{UP}$ and $\overline{DWN}$ have internal pull-up resistors of approximately 50kΩ. When the input is pulled to ground the resulting output current will be V_{DD}/50kΩ.

AC OPERATING CHARACTERISTICS V_{DD} = +4.5V to +5.5V

Symbol	Parameter	Limits			Units
		Min.	Typ.	Max.	
f_{GAP}	Time Between Two Separate Push Button Events	0			µs
t_{DB}	Debounce Time		30	60	ms
$t_{S\ SLOW}$	After Debounce to Wiper Change on a Slow Mode	100	250	375	ms
$t_{S\ FAST}$	Wiper Change on a Fast Mode	25	50	75	ms
t_{PU}	Power-Up to Wiper Stable			500	µs
$t_R\ V_{DD}$	V_{DD} Power-Up Rate	0.2		50	mV/µs
t_{ASTO}	AUTOSTORE Cycle Time	2			ms
t_{ASTH}	AUTOSTORE Threshold Voltage		4		V
t_{ASEND}	AUTOSTORE Cycle End Voltage		3.5		V

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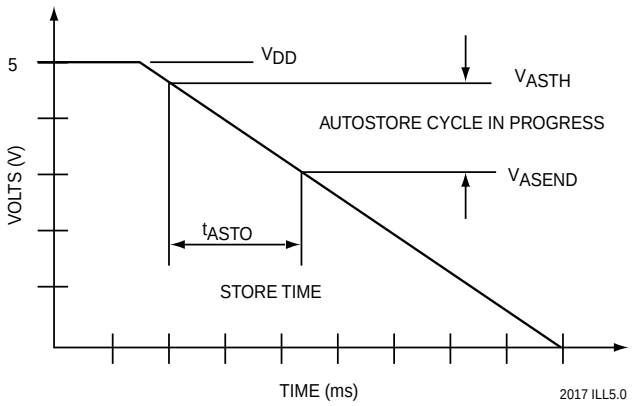


FIGURE 3. AUTOSTORE CYCLE TIMING DIAGRAM

Notes:

V_{ASTH} - AUTOSTORE threshold voltage

V_{ASEND} - AUTOSTORE cycle end voltage

t_{ASTO} - AUTOSTORE cycle time

(6) Typical values are for T_A = 25°C and nominal supply voltage.

(7) This parameter is periodically sampled and not 100% tested.

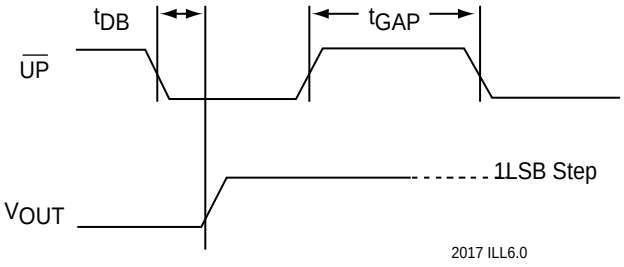


FIGURE 4. SLOW MODE TIMING

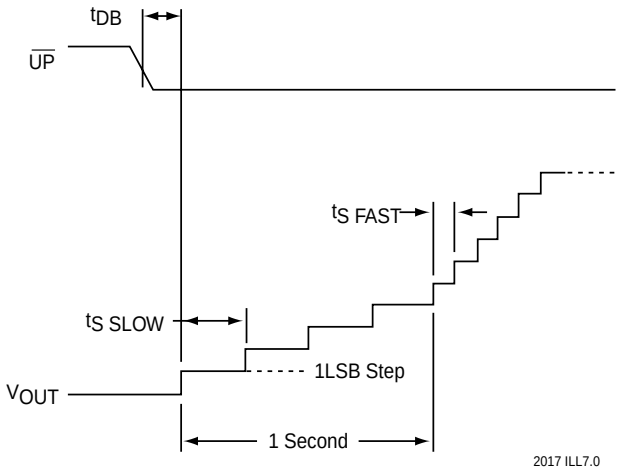
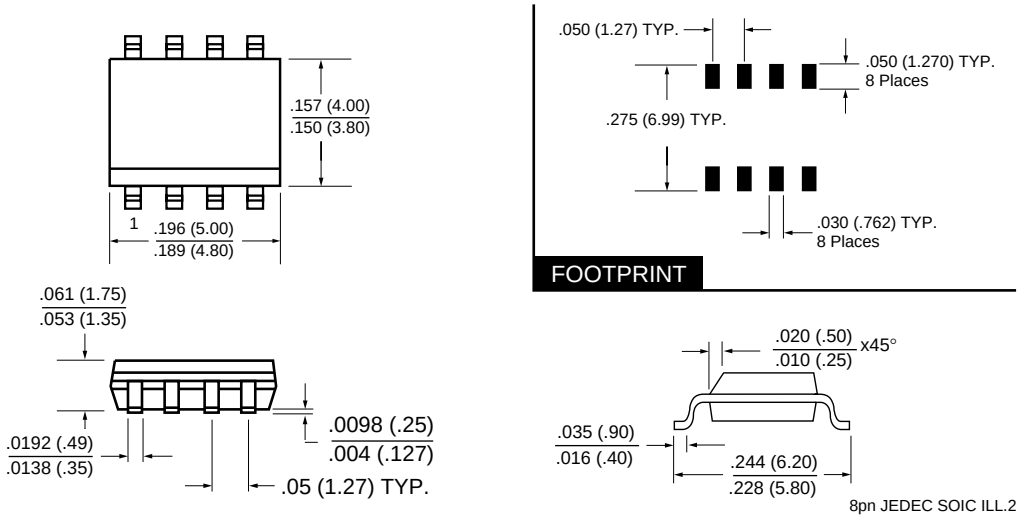


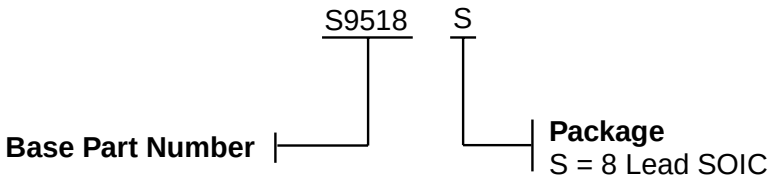
FIGURE 5. FAST MODE TIMING

8 Pin SOIC (Type S) Package JEDEC (150 mil body width)



8pn JEDEC SOIC ILL.2

ORDERING INFORMATION



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