

GENERAL DESCRIPTION

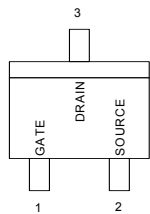
This N-Channel enhancement mode field effect transistor is produced using high cell density, DMOS technology. These products have been designed to minimize on-state resistance while provide rugged, reliable, and fast switching performance. It can be used in most applications requiring up to 115mA DC and can deliver pulsed currents up to 800mA. This product is particularly suited for low voltage, low current applications such as small servo motor control, power MOSFET gate drivers, and other switching applications.

FEATURES

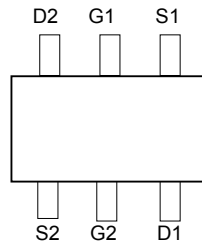
- ◆ High Density Cell Design for Low $R_{DS(ON)}$
- ◆ Voltage Controlled Small Signal Switch
- ◆ Rugged and Reliable
- ◆ High Saturation Current Capability

PIN CONFIGURATION

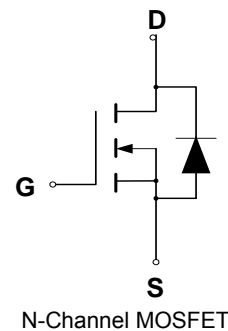
SOT-23, SOT-323
Top View



SOT-363
Top View



SYMBOL



ORDERING INFORMATION

Part Number	Package
CMT2N7002	SOT-23
CMT2N7002G*	SOT-23
CMT2N7002WG*	SOT-323
CMT2N7002DWG*	SOT-363
CMT2N7002X*	SOT-23
CMT2N7002WX*	SOT-323
CMT2N7002DWX*	SOT-363

***Note:** G : Suffix for Pb Free Product W: Suffix for Package SOT-323 X : Suffix for Halogen Free Product

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain Source Voltage	V_{DSS}	60	V
Drain-Gate Voltage ($R_{GS} = 1.0M\Omega$)	V_{DGR}	60	V
Drain to Current – Continuous	I_D	115	mA
– Pulsed	I_{DM}	800	
Gate-to-Source Voltage – Continue	V_{GS}	± 20	V
– Non-repetitive	V_{GSM}	± 40	V
Total Power Dissipation	P_D	225	mW
Derate above 25°C		1.8	mW/°C
Single Pulse Drain-to-Source Avalanche Energy – $T_J = 25^\circ C$ ($V_{DD} = 50V, V_{GS} = 10V, I_{AS} = 0.8A, L = 30mH, R_G = 25\Omega$)	E_{AS}	9.6	mJ
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to 150	°C
Thermal Resistance – Junction to Ambient	θ_{JA}	417	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T_L	300	°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $T_J = 25^\circ\text{C}$.

Characteristic	Symbol	CMT2N7002			Units
		Min	Typ	Max	
Drain-Source Breakdown Voltage ($V_{GS} = 0\text{ V}$, $I_D = 10\ \mu\text{A}$)	$V_{(BR)DSS}$	60			V
Drain-Source Leakage Current ($V_{DS} = 60\text{ V}$, $V_{GS} = 0\text{ V}$) ($V_{DS} = 60\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125^\circ\text{C}$)	I_{DSS}			1.0 0.5	μA mA
Gate-Source Leakage Current-Forward ($V_{gsf} = 20\text{ V}$)	I_{GSSF}			100	nA
Gate-Source Leakage Current-Reverse ($V_{gsf} = -20\text{ V}$)	I_{GSSF}			-100	nA
Gate Threshold Voltage * ($V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$)	$V_{GS(th)}$	1.0		2.5	V
On-State Drain Current ($V_{DS} \geq 2.0 V_{DS(on)}$, $V_{GS} = 10\text{V}$)	$I_{d(on)}$	500			mA
Static Drain-Source On-Resistance * ($V_{GS} = 10\text{ V}$, $I_D = 0.5\text{A}$) ($V_{GS} = 10\text{ V}$, $I_D = 0.5\text{A}$, $T_J = 125^\circ\text{C}$) ($V_{GS} = 5.0\text{ V}$, $I_D = 50\text{mA}$) ($V_{GS} = 5.0\text{ V}$, $I_D = 50\text{mA}$, $T_J = 125^\circ\text{C}$)	$R_{DS(on)}$			7.5 13.5 7.5 13.5	Ω
Drain-Source On-Voltage * ($V_{GS} = 10\text{ V}$, $I_D = 0.5\text{A}$) ($V_{GS} = 5.0\text{ V}$, $I_D = 50\text{mA}$)	$V_{DS(on)}$			3.75 0.375	V
Forward Transconductance ($V_{DS} \geq 2.0 V_{DS(on)}$, $I_D = 200\text{mA}$) *	g_{FS}	80			mmhos
Input Capacitance	$(V_{DS} = 25\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1.0\text{ MHz}$)	C_{iss}		50	pF
Output Capacitance		C_{oss}		25	pF
Reverse Transfer Capacitance		C_{rss}		5.0	pF
Turn-On Delay Time	$(V_{DD} = 25\text{ V}$, $I_D = 500\text{ mA}$, $V_{gen} = 10\text{ V}$, $R_G = 25\Omega$, $R_L = 50\Omega$) *	$t_{d(on)}$		20	ns
Turn-Off Delay Time		$t_{d(off)}$		40	ns
Diode Forward On-Voltage ($I_S = 115\text{ mA}$, $V_{GS} = 0\text{V}$)	V_{SD}			-1.5	V
Source Current Continuous (Body Diode)	I_S			-115	mA
Source Current Pulsed	I_{SM}			-800	mA

* Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$

TYPICAL ELECTRICAL CHARACTERISTICS

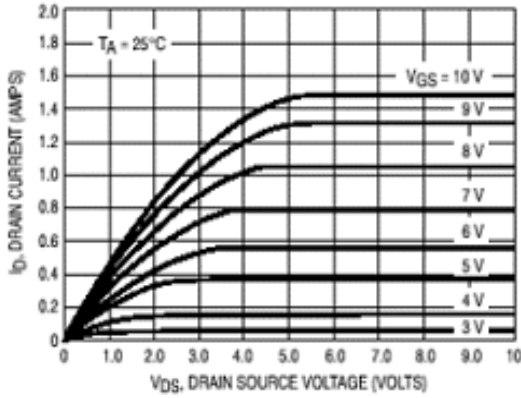


Figure 1. Ohmic Region

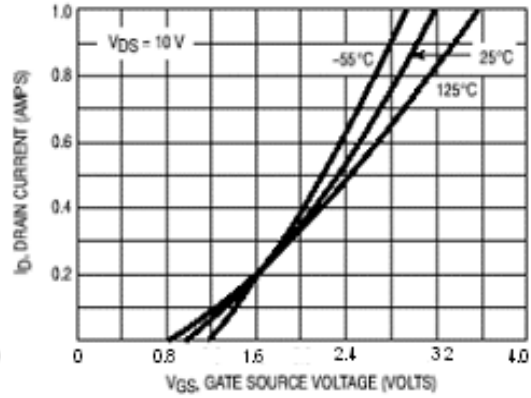


Figure 2. Transfer Characteristics

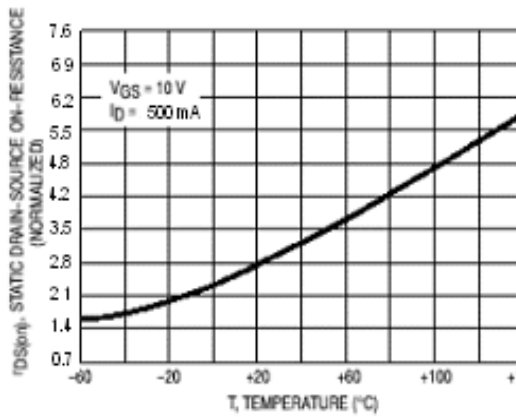


Figure 3. Temperature versus Static Drain-Source On-Resistance

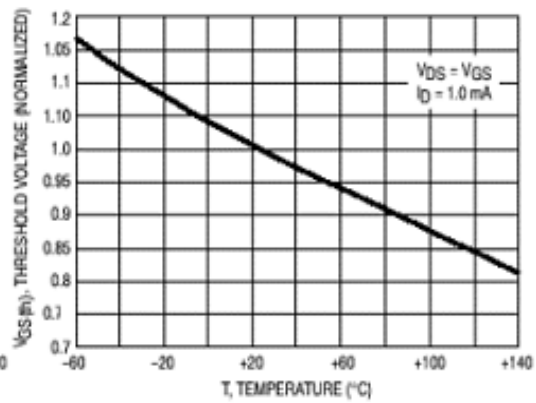


Figure 4. Temperature versus Gate Threshold Voltage

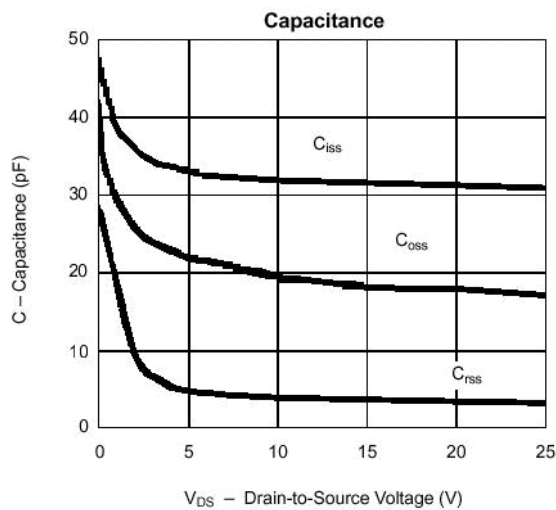
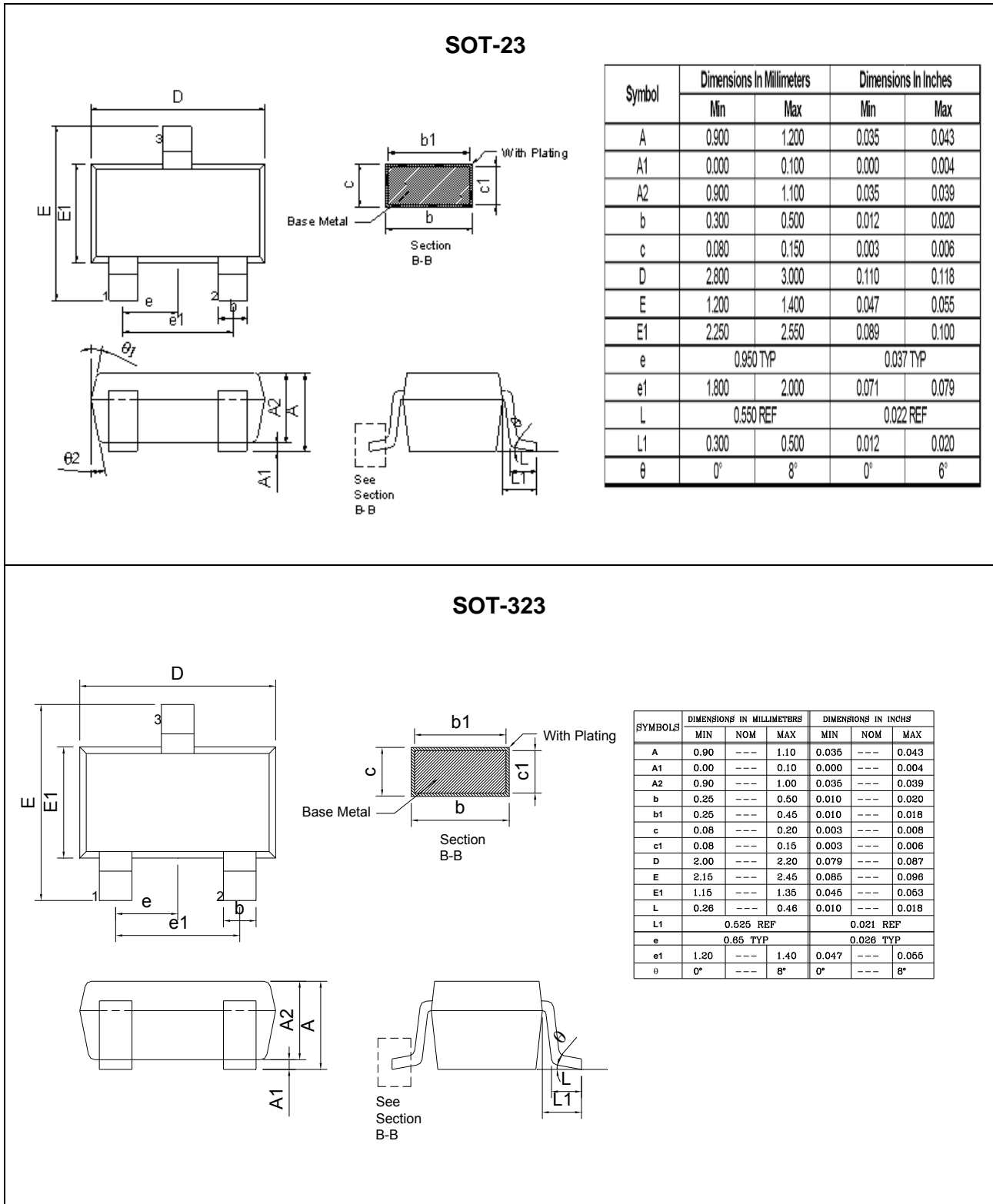
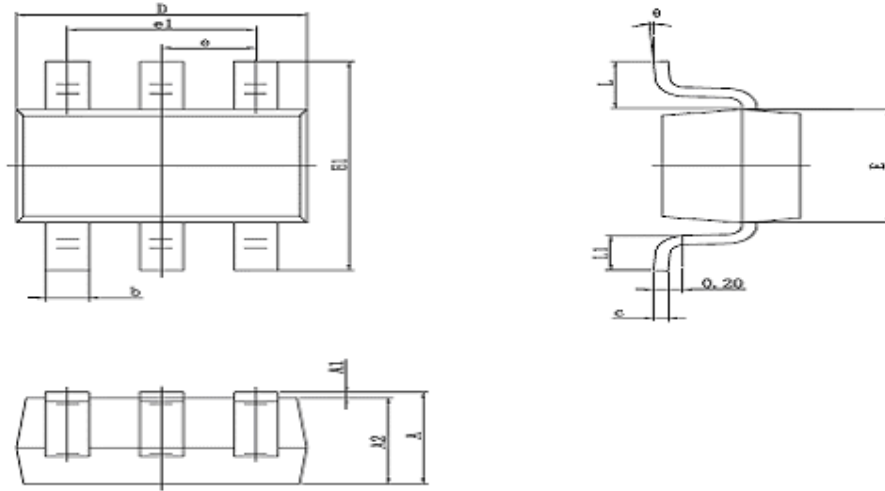


Figure 5. Capacitance

PACKAGE DIMENSION



SOT-363



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.150	0.350	0.006	0.014
c	0.080	0.150	0.003	0.006
D	2.000	2.200	0.079	0.087
E	1.150	1.350	0.045	0.053
E1	2.150	2.450	0.085	0.096
e	0.650TYP		0.026TYP	
e1	1.200	1.400	0.047	0.055
L	0.525REF		0.021REF	
L1	0.260	0.460	0.010	0.018
θ	0°	8°	0°	8°

IMPORTANT NOTICE

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