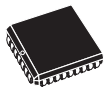
M29F010B

1 Mbit (128Kb x8, uniform block) single supply Flash memory

Feature summary

- Single 5V±10% supply voltage for Program, Erase and Read operations
- Access time: 45 ns
- Programming time
  - 8 µs per byte typical
- 8 uniform 16 Kbytes memory blocks
- Program/Erase controller
  - Embedded byte Program algorithm
  - Embedded multi-block/Chip Erase algorithm
  - Status Register Polling and Toggle bits
- Erase Suspend and Resume modes
  - Read and Program another block during Erase Suspend
- Unlock Bypass Program command
  - Faster Production/Batch programming
- Low power consumption
  - Standby and Automatic Standby
- 100,000 Program/Erase cycles per block
- 20 years data retention
- Defectivity below 1 ppm/year
- Electronic signature
  - Manufacturer code: 20h
  - Device code: 20h
- ECOPACK® packages available



PLCC32 (K)

TSOP32 (N)
8 x 20mm

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1 Summary description

The M29F010B is a 1 Mbit (128Kb x8) non-volatile memory that can be read, erased and reprogrammed. These operations can be performed using a single 5V supply. On power-up the memory defaults to its Read mode where it can be read in the same way as a ROM or EPROM.

The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased. Each block can be protected independently to prevent accidental Program or Erase commands from modifying the memory. Program and Erase commands are written to the Command Interface of the memory. An on-chip Program/Erase Controller simplifies the process of programming or erasing the memory by taking care of all of the special operations that are required to update the memory contents. The end of a program or erase operation can be detected and any error conditions identified. The command set required to control the memory is consistent with JEDEC standards.

Chip Enable, Output Enable and Write Enable signals control the bus operation of the memory. They allow simple connection to most microprocessors, often without additional logic.

The memory is offered in PLCC32, TSOP32 (8 x 20mm) packages and it is supplied with all the bits erased (set to '1').

In order to meet environmental requirements, ST offers the M29F010B in ECOPACK® packages. ECOPACK packages are Lead-free. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97.

The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 1. Logic diagram

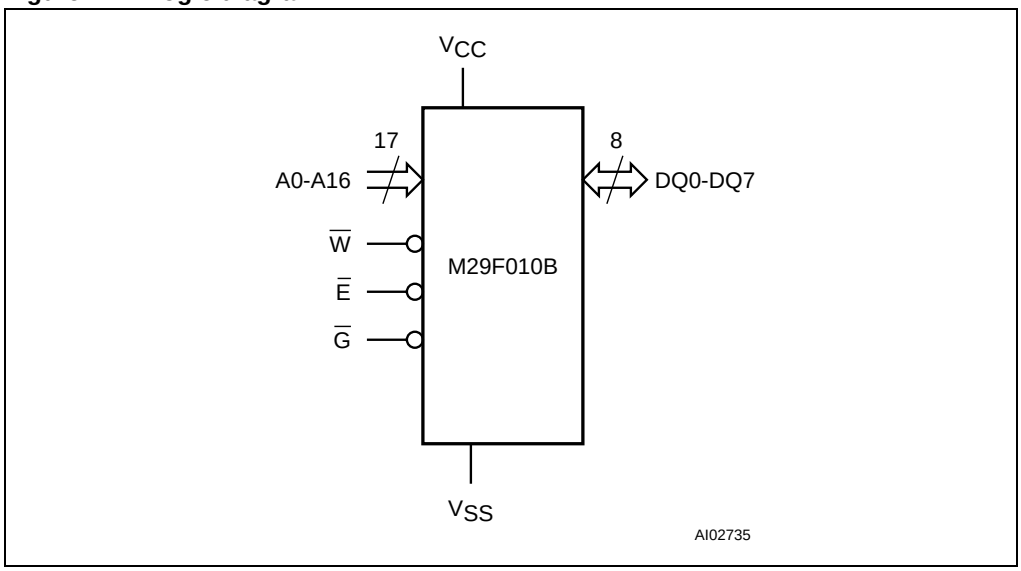


Table 1. Signal names

A0-A16	Address Inputs
DQ0-DQ7	Data Inputs/Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply voltage
V_{SS}	Ground
NCI	Not Connected Internally

Figure 2. PLCC connections

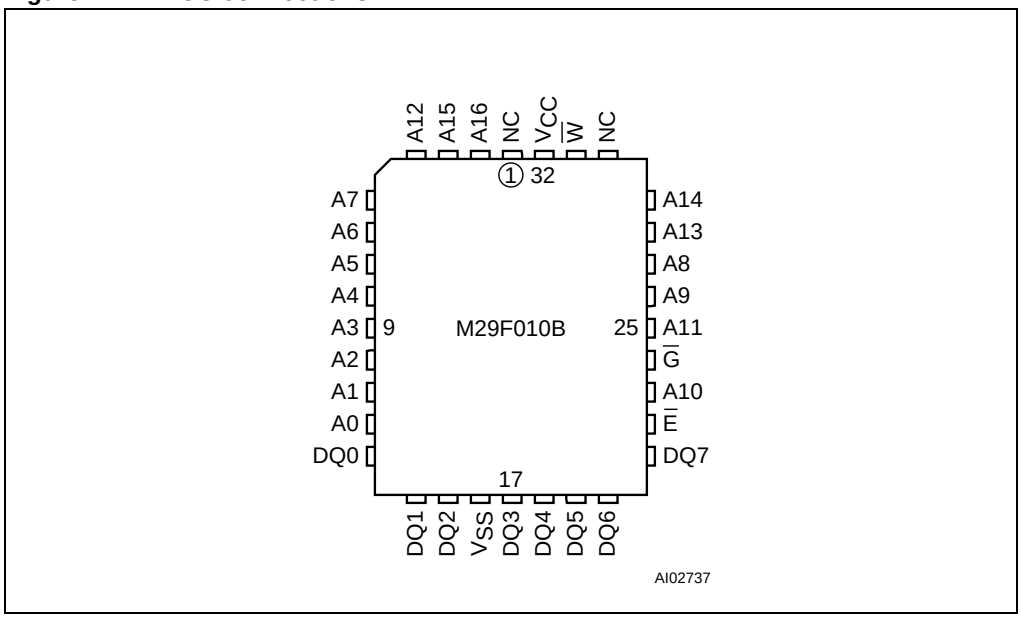


Figure 3. TSOP connections

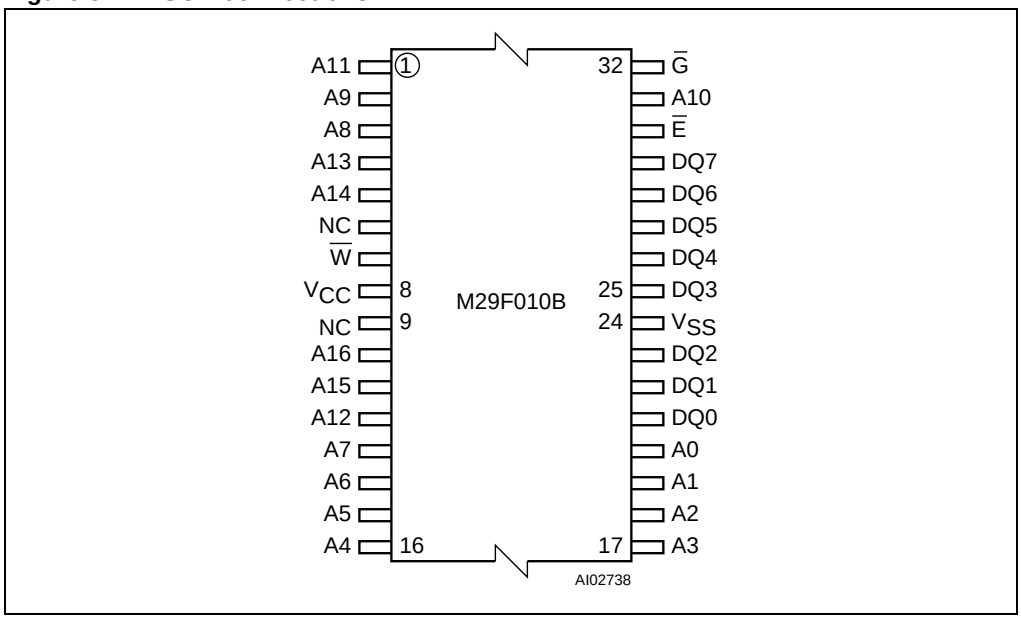


Table 2. Uniform block addresses

#	Size (Kbytes)	Address range
7	16	1C000h-1FFFFh
6	16	18000h-1BFFFh
5	16	14000h-17FFFh
4	16	10000h-13FFFh
3	16	0C000h-0FFFFh
2	16	08000h-0BFFFh
1	16	04000h-07FFFh
0	16	00000h-03FFFh

2 Signal descriptions

See *Figure 1: Logic diagram* and *Table 1: Signal names*, for a brief overview of the signals connected to this device.

2.1 Address Inputs (A0-A16)

The Address Inputs select the cells in the memory array to access during Bus Read operations. During Bus Write operations they control the commands sent to the Command Interface of the internal state machine.

2.2 Data Inputs/Outputs (DQ0-DQ7)

The Data Inputs/Outputs output the data stored at the selected address during a Bus Read operation. During Bus Write operations they represent the commands sent to the Command Interface of the internal state machine.

2.3 Chip Enable ($\overline{E}$)

The Chip Enable, $\overline{E}$, activates the memory, allowing Bus Read and Bus Write operations to be performed. When Chip Enable is High, V_{IH}, all other pins are ignored.

2.4 Output Enable ($\overline{G}$)

The Output Enable, $\overline{G}$, controls the Bus Read operation of the memory.

2.5 Write Enable ($\overline{W}$)

The Write Enable, $\overline{W}$, controls the Bus Write operation of the memory's Command Interface.

2.6 V_{CC} supply voltage

The V_{CC} Supply Voltage supplies the power for all operations (Read, Program, Erase etc.).

The Command Interface is disabled when the V_{CC} Supply Voltage is less than the Lockout Voltage, V_{LKO}. This prevents Bus Write operations from accidentally damaging the data during power up, power down and power surges. If the Program/Erase Controller is programming or erasing during this time then the operation aborts and the memory contents being altered will be invalid.

A 0.1µF capacitor should be connected between the V_{CC} Supply Voltage pin and the V_{SS} Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations, I_{CC4}.

2.7 Vss Ground

The V_{SS} Ground is the reference for all voltage measurements.

3 Bus operations

There are five standard bus operations that control the device. These are Bus Read, Bus Write, Output Disable, Standby and Automatic Standby. See *Table 3: Bus operations*, for a summary. Typically glitches of less than 5ns on Chip Enable or Write Enable are ignored by the memory and do not affect bus operations.

3.1 Bus Read

Bus Read operations read from the memory cells, or specific registers in the Command Interface. A valid Bus Read operation involves setting the desired address on the Address Inputs, applying a Low signal, V_{IL}, to Chip Enable and Output Enable and keeping Write Enable High, V_{IH}. The Data Inputs/Outputs will output the value, see *Figure 8: Read Mode AC waveforms* and *Table 11: Read AC characteristics*, for details of when the output becomes valid.

3.2 Bus Write

Bus Write operations write to the Command Interface. A valid Bus Write operation begins by setting the desired address on the Address Inputs. The Address Inputs are latched by the Command Interface on the falling edge of Chip Enable or Write Enable, whichever occurs last. The Data Inputs/Outputs are latched by the Command Interface on the rising edge of Chip Enable or Write Enable, whichever occurs first. Output Enable must remain High, V_{IH}, during the whole Bus Write operation. See *Figure 9: Write AC waveforms, Write Enable controlled*, *Figure 10: Write AC waveforms, Chip Enable controlled*, *Table 12: Write AC characteristics, Write Enable controlled* and *Table 13: Write AC characteristics, Chip Enable controlled*, for details of the timing requirements.

3.3 Output Disable

The Data Inputs/Outputs are in the high impedance state when Output Enable is High, V_{IH}.

3.4 Standby

When Chip Enable is High, V_{IH}, the Data Inputs/Outputs pins are placed in the high-impedance state and the Supply Current is reduced to the Standby level.

When Chip Enable is at V_{IH} the Supply Current is reduced to the TTL Standby Supply Current I_{CC2}. To further reduce the Supply Current to the CMOS Standby Supply Current, I_{CC3}, Chip Enable should be held within V_{CC} ± 0.2V. For Standby current levels see *Table 10: DC characteristics*.

During program or erase operations the memory will continue to use the Program/Erase Supply Current, I_{CC4}, for Program or Erase operations until the operation completes.

3.5 Automatic Standby

If CMOS levels (V_{CC} ± 0.2V) are used to drive the bus and the bus is inactive for 150ns or more the memory enters Automatic Standby where the internal Supply Current is reduced to the CMOS Standby Supply Current, I_{CC3}. The Data Inputs/Outputs will still output data if a Bus Read operation is in progress.

3.6 Special bus operations

Additional bus operations can be performed to read the Electronic Signature and also to apply and remove Block Protection. These bus operations are intended for use by programming equipment and are not usually used in applications. They require V_{ID} to be applied to some pins.

3.7 Electronic Signature

The memory has two codes, the manufacturer code and the device code, that can be read to identify the memory. These codes can be read by applying the signals listed in *Table 3: Bus operations*.

3.8 Block Protection and Blocks Unprotection

Each block can be separately protected against accidental Program or Erase. Protected blocks can be unprotected to allow data to be changed. Block Protection and Blocks Unprotection operations must only be performed on programming equipment. For further information refer to Application Note AN1122, Applying Protection and Unprotection to M29 Series Flash memory.

Table 3. Bus operations(1)

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	Address Inputs	Data Inputs/Outputs
Bus Read	V_{IL}	V_{IL}	V_{IH}	Cell address	Data Output
Bus Write	V_{IL}	V_{IH}	V_{IL}	Command address	Data Input
Output Disable	X	V_{IH}	V_{IH}	X	Hi-Z
Standby	V_{IH}	X	X	X	Hi-Z
Read Manufacturer code	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IL}, A1 = V_{IL}, A9 = V_{ID}, others V_{IL} or V_{IH}	20h
Read Device code	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IH}, A1 = V_{IL}, A9 = V_{ID}, others V_{IL} or V_{IH}	20h

1. X = V_{IL} or V_{IH}.

4 Command interface

All Bus Write operations to the memory are interpreted by the Command Interface. Commands consist of one or more sequential Bus Write operations. Failure to observe a valid sequence of Bus Write operations will result in the memory returning to Read mode. The long command sequences are imposed to maximize data security.

The commands are summarized in *Table 4: Commands*. Refer to *Table 4* in conjunction with the text descriptions below.

4.1 Read/Reset command

The Read/Reset command returns the memory to its Read mode where it behaves like a ROM or EPROM. It also resets the errors in the Status Register. Either one or three Bus Write operations can be used to issue the Read/Reset command.

If the Read/Reset command is issued during a Block Erase operation or following a Programming or Erase error then the memory will take upto 10µs to abort. During the abort period no valid data can be read from the memory. Issuing a Read/Reset command during a Block Erase operation will leave invalid data in the memory.

4.2 Auto Select command

The Auto Select command is used to read the Manufacturer code, the Device code and the Block Protection status. Three consecutive Bus Write operations are required to issue the Auto Select command. Once the Auto Select command is issued the memory remains in Auto Select mode until another command is issued.

From the Auto Select mode the Manufacturer code can be read using a Bus Read operation with A0 = V_{IL} and A1 = V_{IL}. The other address bits may be set to either V_{IL} or V_{IH}. The Manufacturer code for STMicroelectronics is 20h.

The Device code can be read using a Bus Read operation with A0 = V_{IH} and A1 = V_{IL}. The other address bits may be set to either V_{IL} or V_{IH}. The Device code for the M29F010B is 20h.

The Block Protection status of each block can be read using a Bus Read operation with A0 = V_{IL}, A1 = V_{IH}, and A14-A16 specifying the address of the block. The other address bits may be set to either V_{IL} or V_{IH}. If the addressed block is protected then 01h is output on the Data Inputs/Outputs, otherwise 00h is output.

4.3 Program command

The Program command can be used to program a value to one address in the memory array at a time. The command requires four Bus Write operations, the final write operation latches the address and data in the internal state machine and starts the Program/Erase Controller.

If the address falls in a protected block then the Program command is ignored, the data remains unchanged. The Status Register is never read and no error condition is given.

During the program operation the memory will ignore all commands. It is not possible to issue any command to abort or pause the operation. Typical program times are given in *Table 5: Program Erase times and Program Erase Endurance cycles*. Bus Read operations during the program operation will output the Status Register on the Data Inputs/Outputs. See the section on the Status Register for more details.

After the program operation has completed the memory will return to the Read mode, unless an error has occurred. When an error occurs the memory will continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read mode.

Note that the Program command cannot change a bit set at ’0’ back to ’1’. One of the Erase Commands must be used to set all the bits in a block or in the whole memory from ’0’ to ’1’.

4.4 Unlock Bypass command

The Unlock Bypass command is used in conjunction with the Unlock Bypass Program command to program the memory. When the access time to the device is long (as with some EPROM programmers) considerable time saving can be made by using these commands. Three Bus Write operations are required to issue the Unlock Bypass command.

Once the Unlock Bypass command has been issued the memory will only accept the Unlock Bypass Program command and the Unlock Bypass Reset command. The memory can be read as if in Read mode.

4.5 Unlock Bypass Program command

The Unlock Bypass Program command can be used to program one address in memory at a time. The command requires two Bus Write operations, the final write operation latches the address and data in the internal state machine and starts the Program/Erase Controller.

The Program operation using the Unlock Bypass Program command behaves identically to the Program operation using the Program command. A protected block cannot be programmed; the operation cannot be aborted and the Status Register is read. Errors must be reset using the Read/Reset command, which leaves the device in Unlock Bypass Mode. See the Program command for details on the behavior.

4.6 Unlock Bypass Reset command

The Unlock Bypass Reset command can be used to return to Read/Reset mode from Unlock Bypass Mode. Two Bus Write operations are required to issue the Unlock Bypass Reset command.

4.7 Chip Erase command

The Chip Erase command can be used to erase the entire chip. Six Bus Write operations are required to issue the Chip Erase Command and start the Program/Erase Controller.

If any blocks are protected then these are ignored and all the other blocks are erased. If all of the blocks are protected the Chip Erase operation appears to start but will terminate within about 100µs, leaving the data unchanged. No error condition is given when protected blocks are ignored.

During the erase operation the memory will ignore all commands. It is not possible to issue any command to abort the operation. Typical chip erase times are given in *Table 5: Program Erase times and Program Erase Endurance cycles*. All Bus Read operations during the Chip Erase operation will output the Status Register on the Data Inputs/Outputs. See the section on the Status Register for more details.

After the Chip Erase operation has completed the memory will return to the Read Mode, unless an error has occurred. When an error occurs the memory will continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read Mode.

The Chip Erase Command sets all of the bits in unprotected blocks of the memory to ’1’. All previous data is lost.

4.8 Block Erase command

The Block Erase command can be used to erase a list of one or more blocks. Six Bus Write operations are required to select the first block in the list. Each additional block in the list can be selected by repeating the sixth Bus Write operation using the address of the additional block. The Block Erase operation starts the Program/Erase Controller about 50µs after the last Bus Write operation. Once the Program/Erase Controller starts it is not possible to select any more blocks. Each additional block must therefore be selected within 50µs of the last block. The 50µs timer restarts when an additional block is selected. The Status Register can be read after the sixth Bus Write operation. See the Status Register for details on how to identify if the Program/Erase Controller has started the Block Erase operation.

If any selected blocks are protected then these are ignored and all the other selected blocks are erased. If all of the selected blocks are protected the Block Erase operation appears to start but will terminate within about 100µs, leaving the data unchanged. No error condition is given when protected blocks are ignored.

During the Block Erase operation the memory will ignore all commands except the Erase Suspend and Read/Reset commands. Typical block erase times are given in *Table 5: Program Erase times and Program Erase Endurance cycles*. All Bus Read operations during the Block Erase operation will output the Status Register on the Data Inputs/Outputs. See the section on the Status Register for more details.

After the Block Erase operation has completed the memory will return to the Read Mode, unless an error has occurred. When an error occurs the memory will continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read mode.

The Block Erase Command sets all of the bits in the unprotected selected blocks to ’1’. All previous data in the selected blocks is lost.

4.9 Erase Suspend command

The Erase Suspend Command may be used to temporarily suspend a Block Erase operation and return the memory to Read mode. The command requires one Bus Write operation.

The Program/Erase Controller will suspend within 15µs of the Erase Suspend Command being issued. Once the Program/Erase Controller has stopped the memory will be set to Read mode and the Erase will be suspended. If the Erase Suspend command is issued during the period when the memory is waiting for an additional block (before the Program/Erase Controller starts) then the Erase is suspended immediately and will start immediately when the Erase Resume Command is issued. It will not be possible to select any further blocks for erasure after the Erase Resume.

During Erase Suspend it is possible to Read and Program cells in blocks that are not being erased; both Read and Program operations behave as normal on these blocks. Reading from blocks that are being erased will output the Status Register. It is also possible to enter the Auto Select mode: the memory will behave as in the Auto Select mode on all blocks until a Read/Reset command returns the memory to Erase Suspend mode.

4.10 Erase Resume command

The Erase Resume command must be used to restart the Program/Erase Controller from Erase Suspend. An erase can be suspended and resumed more than once.

Table 4. Commands(1)

Command	Length	Bus Write operations											
		1st		2nd		3rd		4th		5th		6th	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read/Reset(2)	1	X	F0										
	3	555	AA	2AA	55	X	F0						
Auto Select(3)	3	555	AA	2AA	55	555	90						
Program(4)	4	555	AA	2AA	55	555	A0	PA	PD				
Unlock Bypass(5)	3	555	AA	2AA	55	555	20						
Unlock Bypass Program(4)	2	X	A0	PA	PD								
Unlock Bypass Reset(6)	2	X	90	X	00								
Chip Erase(4)	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Block Erase(4)	6 +	555	AA	2AA	55	555	80	555	AA	2AA	55	BA	30
Erase Suspend(7)	1	X	B0										
Erase Resume(8)	1	X	30										

1. All values in the table are in hexadecimal. X Don't Care, PA Program Address, PD Program Data, BA Any address in the Block. The Command Interface only uses address bits A0-A10 to verify the commands, the upper address bits are Don't Care.
2. After a Read/Reset command, read the memory as normal until another command is issued.
3. After an Auto Select command, read Manufacturer ID, Device ID or Block Protection Status.
4. After Program, Unlock Bypass Program, Chip Erase, and Block Erase commands read the Status Register until the Program/Erase Controller completes and the memory returns to Read Mode. Add additional Blocks during Block Erase Command with additional Bus Write Operations until the Timeout bit is set.
5. After the Unlock Bypass command issue Unlock Bypass Program or Unlock Bypass Reset commands.
6. After the Unlock Bypass Reset command read the memory as normal until another command is issued.
7. After the Erase Suspend command read non-erasing memory blocks as normal, issue Auto Select and Program commands on non-erasing blocks as normal.
8. After the Erase Resume command the suspended Erase operation resumes, read the Status Register until the Erase Controller completes and the memory returns to Read Mode.

Table 5. Program Erase times and Program Erase Endurance cycles(1)

Parameter	Min	Typ(2)	Typical after 100k W/E cycles(2)	Max	Unit
Chip Erase (all bits in the memory set to '0')		0.6	0.6		sec
Chip Erase		1.3	1.3	6	sec
Block Erase (16 Kbytes)		0.3	0.3	2	sec
Program		8	8	150	µs
Chip Program		1.2	1.2	4.5	sec
Program/Erase cycles (per block)	100,000				cycles

1. T_A = 0 to 70°C, –40 to 85°C.
2. T_A = 25°C, V_{CC} = 5V.

5 Status Register

Bus Read operations from any address always read the Status Register during Program and Erase operations. It is also read during Erase Suspend when an address within a block being erased is accessed.

The bits in the Status Register are summarized in *Table 6: Status Register bits*.

5.1 Data Polling bit (DQ7)

The Data Polling bit can be used to identify whether the Program/Erase Controller has successfully completed its operation or if it has responded to an Erase Suspend. The Data Polling bit is output on DQ7 when the Status Register is read.

During Program operations the Data Polling bit outputs the complement of the bit being programmed to DQ7. After successful completion of the Program operation the memory returns to Read mode and Bus Read operations from the address just programmed output DQ7, not its complement.

During Erase operations the Data Polling bit outputs ’0’, the complement of the erased state of DQ7. After successful completion of the Erase operation the memory returns to Read Mode.

In Erase Suspend mode the Data Polling bit will output a ’1’ during a Bus Read operation within a block being erased. The Data Polling bit will change from a ’0’ to a ’1’ when the Program/Erase Controller has suspended the Erase operation.

Figure 4: Data Polling flowchart, gives an example of how to use the Data Polling bit. A Valid Address is the address being programmed or an address within the block being erased.

5.2 Toggle bit (DQ6)

The Toggle bit can be used to identify whether the Program/Erase Controller has successfully completed its operation or if it has responded to an Erase Suspend. The Toggle bit is output on DQ6 when the Status Register is read.

During Program and Erase operations the Toggle bit changes from ’0’ to ’1’ to ’0’, etc., with successive Bus Read operations at any address. After successful completion of the operation the memory returns to Read mode.

During Erase Suspend mode the Toggle bit will output when addressing a cell within a block being erased. The Toggle bit will stop toggling when the Program/Erase Controller has suspended the Erase operation.

Figure 5: Data Toggle flowchart, gives an example of how to use the Data Toggle bit.

5.3 Error bit (DQ5)

The Error bit can be used to identify errors detected by the Program/Erase Controller. The Error bit is set to ’1’ when a Program, Block Erase or Chip Erase operation fails to write the correct data to the memory. If the Error bit is set a Read/Reset command must be issued before other commands are issued. The Error bit is output on DQ5 when the Status Register is read.

Note that the Program command cannot change a bit set at ’0’ back to ’1’ and attempting to do so may or may not set DQ5 at ‘1’. In both cases, a successive Bus Read operation will show the bit is still ’0’. One of the Erase commands must be used to set all the bits in a block or in the whole memory from ’0’ to ’1’.

5.4 Erase Timer bit (DQ3)

The Erase Timer bit can be used to identify the start of Program/Erase Controller operation during a Block Erase command. Once the Program/Erase Controller starts erasing the Erase Timer bit is set to ’1’. Before the Program/Erase Controller starts the Erase Timer bit is set to ’0’ and additional blocks to be erased may be written to the Command Interface. The Erase Timer bit is output on DQ3 when the Status Register is read.

5.5 Alternative Toggle bit (DQ2)

The Alternative Toggle bit can be used to monitor the Program/Erase controller during Erase operations. The Alternative Toggle bit is output on DQ2 when the Status Register is read.

During Chip Erase and Block Erase operations the Toggle bit changes from ’0’ to ’1’ to ’0’, etc., with successive Bus Read operations from addresses within the blocks being erased. Once the operation completes the memory returns to Read mode.

During Erase Suspend the Alternative Toggle bit changes from ’0’ to ’1’ to ’0’, etc. with successive Bus Read operations from addresses within the blocks being erased. Bus Read operations to addresses within blocks not being erased will output the memory cell data as if in Read mode.

After an Erase operation that causes the Error bit to be set the Alternative Toggle bit can be used to identify which block or blocks have caused the error. The Alternative Toggle bit changes from ’0’ to ’1’ to ’0’, etc. with successive Bus Read Operations from addresses within blocks that have not erased correctly. The Alternative Toggle bit does not change if the addressed block has erased correctly.

Table 6. Status Register bits(1)

Operation	Address	DQ7	DQ6	DQ5	DQ3	DQ2
Program	Any address	$\overline{DQ7}$	Toggle	0	–	–
Program during Erase Suspend	Any address	$\overline{DQ7}$	Toggle	0	–	–
Program Error	Any address	$\overline{DQ7}$	Toggle	1	–	–
Chip Erase	Any address	0	Toggle	0	1	Toggle
Block Erase before timeout	Erasing block	0	Toggle	0	0	Toggle
	Non-Erasing block	0	Toggle	0	0	No toggle
Block Erase	Erasing block	0	Toggle	0	1	Toggle
	Non-Erasing block	0	Toggle	0	1	No toggle
Erase Suspend	Erasing block	1	No toggle	0	–	Toggle
	Non-Erasing block	Data read as normal				
Erase Error	Good block address	0	Toggle	1	1	No toggle
	Faulty block address	0	Toggle	1	1	Toggle

1. Unspecified data bits should be ignored.

Figure 4. Data Polling flowchart

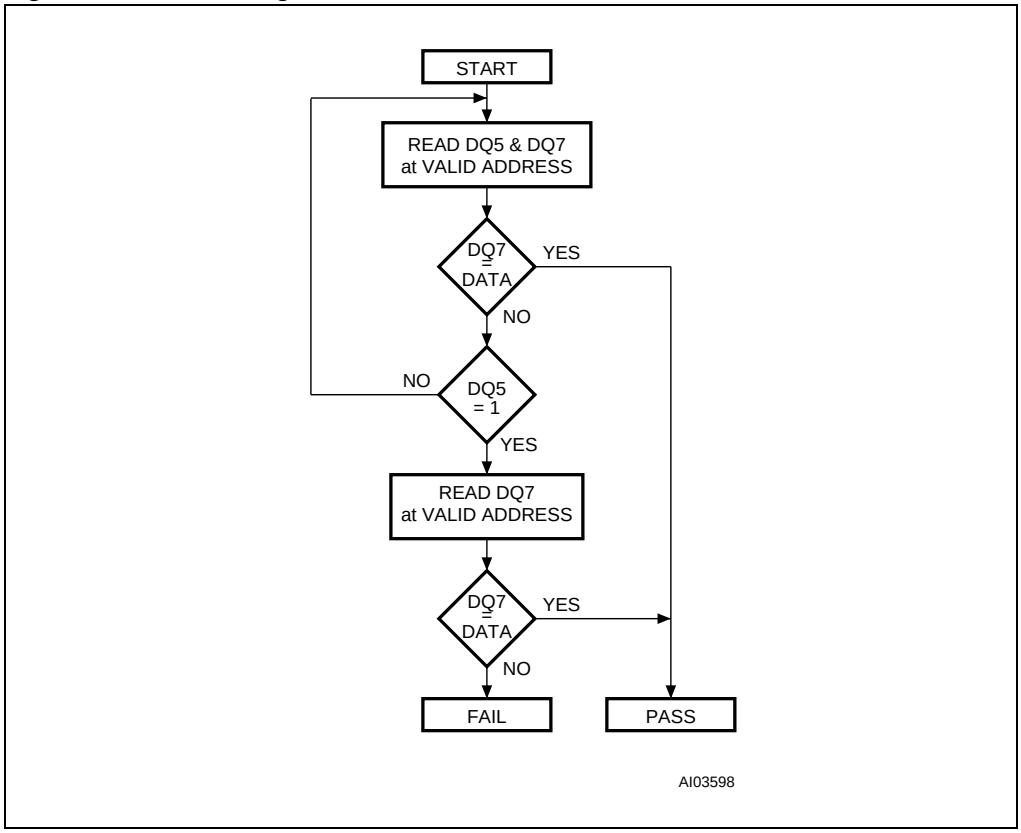
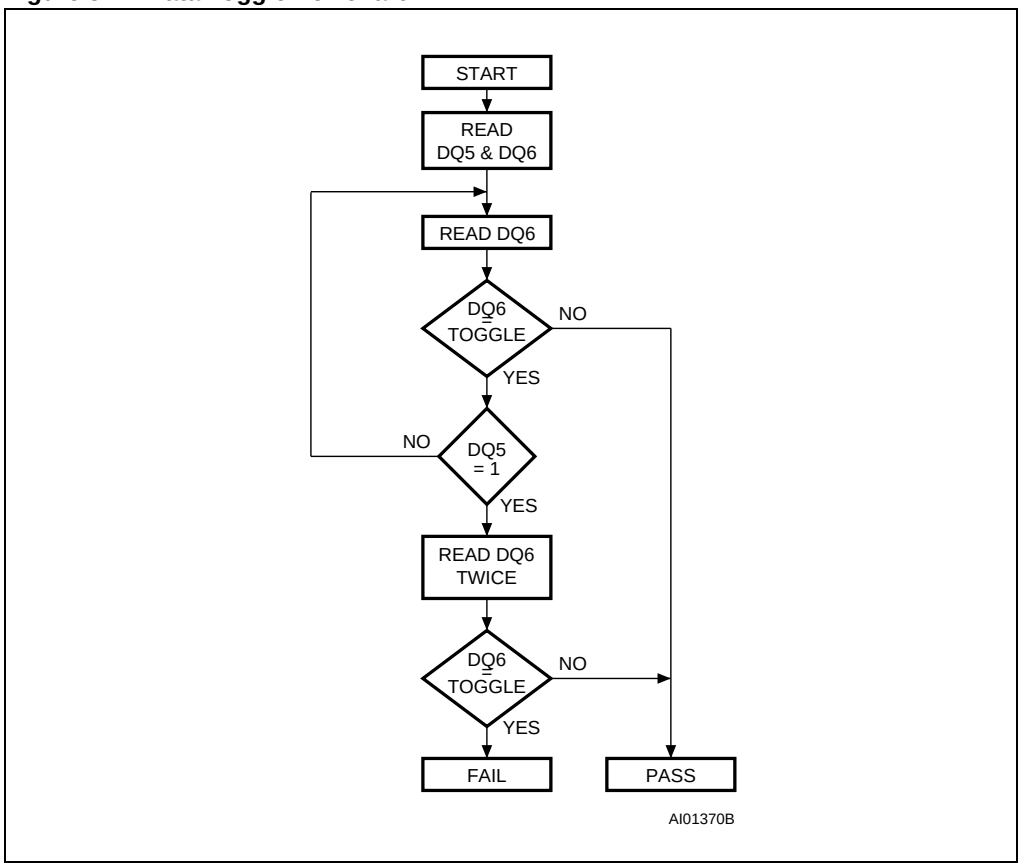


Figure 5. Data Toggle flowchart



6 Maximum rating

Except for the rating "Operating Temperature Range", stresses above those listed in *Table 7: Absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 7. Absolute maximum ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating temperature (Temperature Range 1)	0 to 70	°C
	Ambient Operating temperature (Temperature Range 6)	–40 to 85	°C
T_{BIAS}	Temperature under Bias	–50 to 125	°C
T_{STG}	Storage temperature	–65 to 150	°C
V_{IO}(1)	Input or Output voltage	–0.6 to 6	V
V_{CC}	Supply voltage	–0.6 to 6	V
V_{ID}	Identification voltage	–0.6 to 13.5	V

1. Minimum voltage may undershoot to –2V during transition and for less than 20ns during transitions.

7 DC and AC parameters

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the measurement conditions summarized in *Table 8: AC measurement conditions*. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 8. AC measurement conditions

Parameter	45	70/90/120
AC test conditions	High speed	Standard
Load capacitance (C_L)	30pF	100pF
Input Rise and Fall times	≤10ns	≤10ns
Input pulse voltages	0 to 3V	0.45 to 2.4V
Input and Output Timing Ref. voltages	1.5V	0.8V and 2V

Figure 6. AC testing Input/Output waveform

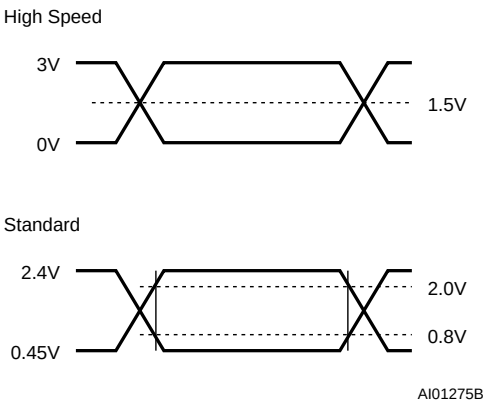


Figure 7. AC testing load circuit

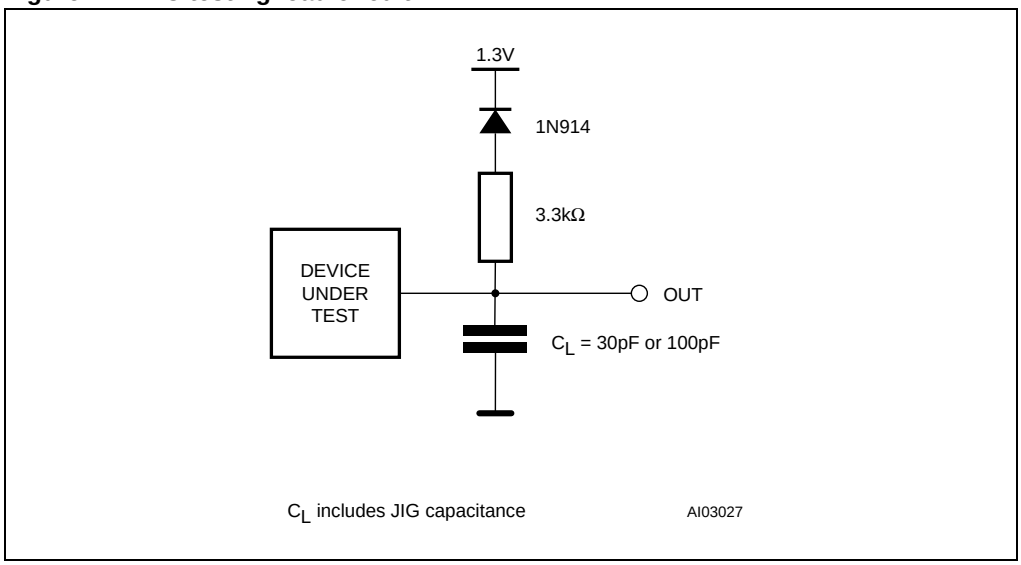


Table 9. Capacitance(1)(2)

Symbol	Parameter	Test condition	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output capacitance	V_{OUT} = 0V		12	pF

1. T_A = 25 °C, f = 1 MHz.
2. Sampled only, not 100% tested.

Table 10. DC characteristics(1)

Symbol	Parameter	Test condition	Min	Typ (2)	Max	Unit
I_{LI}	Input Leakage current	$0V \le V_{IN} \le V_{CC}$			±1	µA
I_{LO}	Output Leakage current	$0V \le V_{OUT} \le V_{CC}$			±1	µA
I_{CC1}	Supply current (Read)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$, f = 6MHz		5	15	mA
I_{CC2}	Supply current (Standby) TTL	$\overline{E} = V_{IH}$			1	mA
I_{CC3}	Supply current (Standby) CMOS	$\overline{E} = V_{CC}$ ±0.2V		30	100	µA
I_{CC4}(3)	Supply current (Program/Erase)	Program/Erase controller active			20	mA
V_{IL}	Input Low voltage		–0.5		0.8	V
V_{IH}	Input High voltage		2		V_{CC} +0.5	V
V_{OL}	Output Low voltage	I_{OL} = 5.8mA			0.45	V
V_{OH}	Output High voltage TTL	I_{OH} = –2.5mA	2.4			V
	Output High voltage CMOS	I_{OH} = –100µA	V_{CC} –0.4			V
V_{ID}	Identification voltage		11.5		12.5	V
I_{ID}	Identification current	$A9 = V_{ID}$			100	µA
V_{LKO}(3)	Program/Erase Lockout supply voltage		3.2		4.2	V

1. T_A = 0 to 70°C, –40 to 85°C.
2. T_A = 25°, V_{CC} = 5V.
3. Sampled only, not 100% tested.

Table 11. Read AC characteristics(1)

Symbol	Alt	Parameter	Test condition		45	70/90/120	Unit
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	$\overline{E} = V_{IL}, \overline{G} = V_{IL}$	Min	45	70	ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}, \overline{G} = V_{IL}$	Max	45	70	ns
t_{ELQX}(2)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G} = V_{IL}$	Min	0	0	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$	Max	45	70	ns
t_{GLQX}(2)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E} = V_{IL}$	Min	0	0	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$	Max	25	30	ns
t_{EHQZ}(2)	t_{HZ}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	Max	15	20	ns
t_{GHQZ}(2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	Max	15	20	ns
t_{EHQX}, t_{GHQX}, t_{AXQX}	t_{OH}	Chip Enable, Output Enable or Address Transition to Output Transition		Min	0	0	ns

1. TA = 0 to 70°C, –40 to 85°C.
2. Sampled only, not 100% tested.

Figure 8. Read Mode AC waveforms

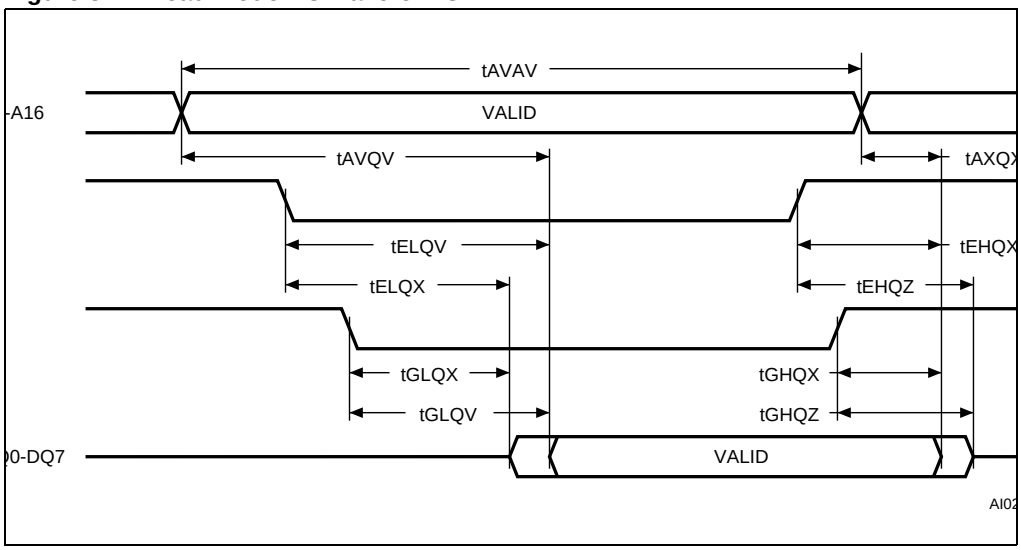


Table 12. Write AC characteristics, Write Enable controlled(1)

Symbol	Alt	Parameter		45	70/90/120	Unit
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	Min	45	70	ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	Min	0	0	ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	Min	40	45	ns
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	Min	25	30	ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	Min	0	0	ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	Min	0	0	ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	Min	20	20	ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	Min	0	0	ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	Min	40	45	ns
t_{GHWL}		Output Enable High to Write Enable Low	Min	0	0	ns
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low	Min	0	0	ns
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low	Min	50	50	µs

1. T_A = 0 to 70 °C, –40 to 85 °C.

Figure 9. Write AC waveforms, Write Enable controlled

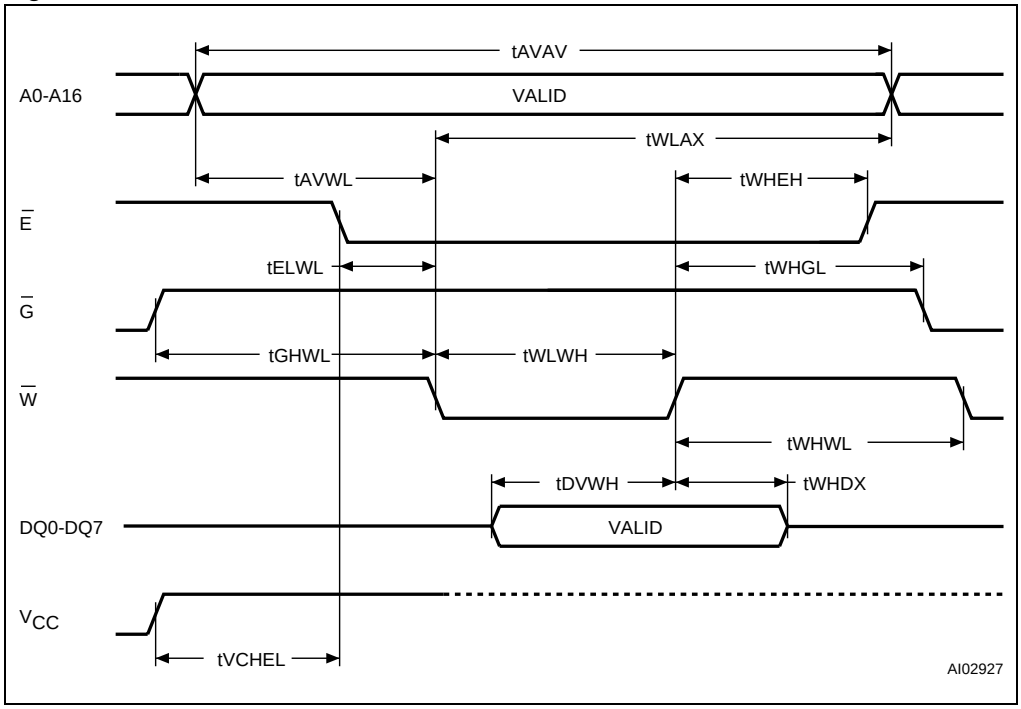
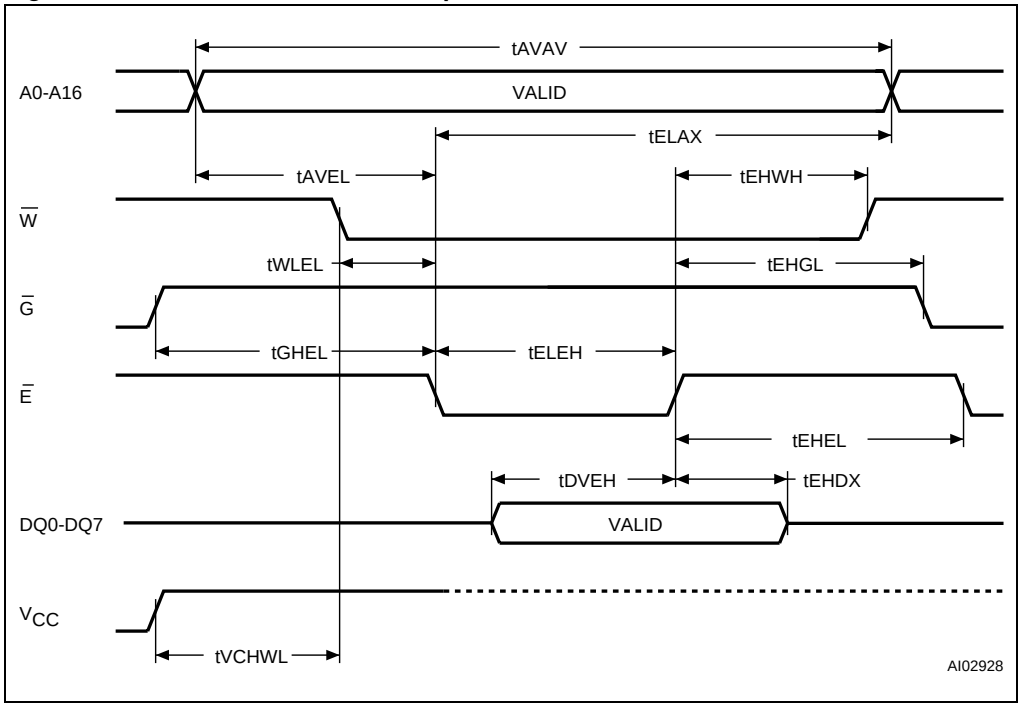


Table 13. Write AC characteristics, Chip Enable controlled(1)

Symbol	Alt	Parameter		45	70/90/120	Unit
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	Min	45	70	ns
t_{WLEL}	t_{WS}	Write Enable Low to Chip Enable Low	Min	0	0	ns
t_{ELEH}	t_{CP}	Chip Enable Low to Chip Enable High	Min	40	45	ns
t_{DVEH}	t_{DS}	Input Valid to Chip Enable High	Min	25	30	ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition	Min	0	0	ns
t_{EHWH}	t_{WH}	Chip Enable High to Write Enable High	Min	0	0	ns
t_{EHEL}	t_{CPH}	Chip Enable High to Chip Enable Low	Min	20	20	ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	Min	0	0	ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition	Min	40	45	ns
t_{GHEL}		Output Enable High Chip Enable Low	Min	0	0	ns
t_{EHGL}	t_{OEH}	Chip Enable High to Output Enable Low	Min	0	0	ns
t_{VCHWL}	t_{VCS}	V_{CC} High to Write Enable Low	Min	50	50	µs

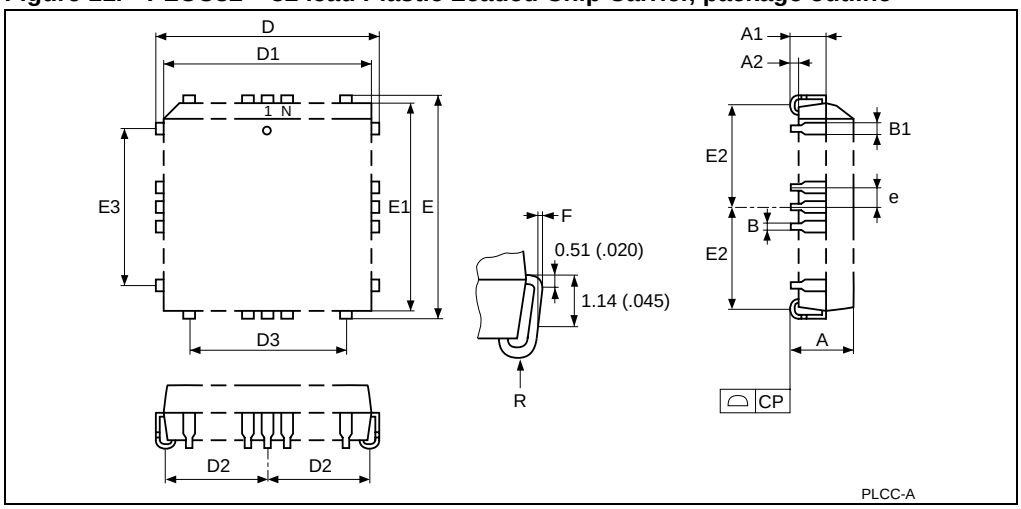
1. T_A = 0 to 70 °C, –40 to 85 °C.

Figure 10. Write AC waveforms, Chip Enable controlled



8 Package mechanical

Figure 11. PLCC32 – 32 lead Plastic Leaded Chip Carrier, package outline

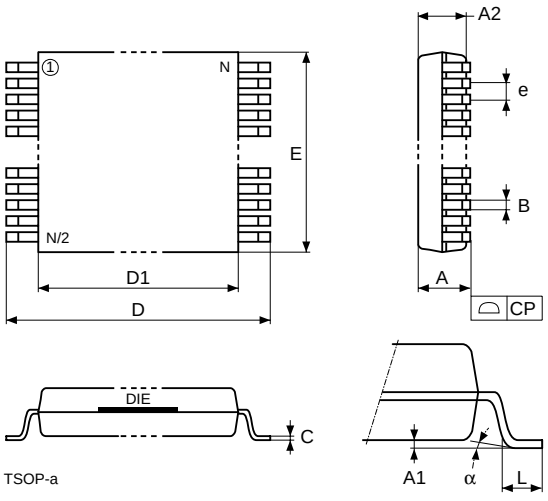


1. Drawing is not to scale.

Table 14. PLCC32 – 32 lead Plastic Leaded Chip Carrier, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.17	3.56		0.125	0.140
A1		1.53	2.41		0.060	0.095
A2		0.38	–		0.015	–
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
CP			0.10			0.004
D		12.32	12.57		0.485	0.495
D1		11.35	11.51		0.447	0.453
D2		4.78	5.66		0.188	0.223
D3	7.62	–	–	0.300	–	–
E		14.86	15.11		0.585	0.595
E1		13.89	14.05		0.547	0.553
E2		6.05	6.93		0.238	0.273
E3	10.16	–	–	0.400	–	–
e	1.27	–	–	0.050	–	–
F		0.00	0.13		0.000	0.005
N	32			32		
R	0.89	–	–	0.035	–	–

Figure 12. TSOP32 – 32 lead Plastic Thin Small Outline, 8 x 20mm, package outline



Note: Drawing is not to scale.

Table 15. TSOP32 – 32 lead Plastic Thin Small Outline, 8 x 20mm, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.0472
A1		0.05	0.15		0.0020	0.0059
A2		0.95	1.05		0.0374	0.0413
B		0.17	0.25		0.0067	0.0098
C		0.10	0.21		0.0039	0.0083
D		19.80	20.20		0.7795	0.7953
D1		18.30	18.50		0.7205	0.7283
E		7.90	8.10		0.3110	0.3189
e	0.50	–	–	0.0197	–	–
L		0.50	0.70		0.0197	0.0276
α		0°	5°		0°	5°
N	32			32		
CP			0.10			0.0039

9 Part numbering

Table 16. Ordering information scheme(1)

Example: M29 F010B 70 N 1 T

Device type

M29

Operating voltage

F = V_{CC} = 5V ± 10%

Device function

010B = 1 Mbit (128Kb x8), uniform block

Speed

45 = 45 ns

70 = 70 ns

90 = 90 ns

120 = 120ns

Package

K = PLCC32

N = TSOP32: 8 x 20 mm

Temperature range

1 = 0 to 70°C

6 = –40 to 85°C

Option

Blank = Standard packing

T = Tape & Reel packing

E = ECOPACK Package, standard packing

F = ECOPACK Package, Tape & Reel packing

1. The last two characters of the ordering code may be replaced by a letter code for preprogrammed parts, otherwise devices are shipped from the factory with the memory content bits erased to '1'.

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

10 Revision history

Table 17. Revision history

Date	Revision	Revision details
July 1999	-01	First Issue
28-Jul-2000	-02	New document template Document type: from Preliminary Data to Data Sheet Status Register bit DQ5 clarification Data Polling Flowchart diagram change (*Figure 4*) Data Toggle Flowchart diagram change (*Figure 5*) Program/Erase Times specification change (Table 5) I_{CC1} and I_{CC3} Typ. specification added (Table 10)
22-Apr-2002	-03	PLCC32 package mechanical data modified
19-Sep-2005	4.0	PDIP32 package removed. *Table 16: Ordering information scheme*: standard package added and ECOPACK version added for both standard package, and Tape & Reel packing.
06-Nov-2006	5	Converted document to new template; updated package mechanical data in *Section 8: Package mechanical*; removed temperature range 3 (–40 to 125°C) from entire document.

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