



# MX29F200T/B

## 2M-BIT [256Kx8/128Kx16] CMOS FLASH MEMORY

### FEATURES

- 5.0V±10% for read, erase and write operation
- 131072x16/262144x8 switchable
- Fast access time: 55/70/90/120ns
- Low power consumption
  - 40mA maximum active current@5MHz
  - 1uA typical standby current
- Command register architecture
  - Byte/Word Programming (7us/12us typical)
  - Erase (16K-Bytex1, 8K-Bytex2, 32K-Bytex1, and 64K-Byte x3)
- Auto Erase (chip) and Auto Program
  - Automatically erase any combination of sectors or the whole chip with Erase Suspend capability.
  - Automatically program and verify data at specified address
- Status Reply
  - Data polling & Toggle bit for detection of program and erase cycle completion.
- Ready/Busy pin(RY/BY)
  - Provides a hardware method of detecting program or erase cycle completion
- Compatibility with JEDEC standard
  - Pinout and software compatible with single-power supply Flash
- Superior inadvertent write protection
- Sector protection
  - Hardware method to disable any combination of sectors from program or erase operations
  - Sector protect/unprotect for 5V only system or 5V/12V system
- 100,000 minimum erase/program cycles
- Latch-up protected to 100mA from -1V to VCC+1V
- Boot Code Sector Architecture
  - T = Top Boot Sector
  - B = Bottom Boot Sector
- Low VCC write inhibit is equal to or less than 3.2V
- Package type:
  - 44-pin SOP
  - 48-pin TSOP
- Erase suspend/ Erase Resume
  - Suspends an erase operation to read data from, or program data to a sector that is not being erased, then resume the erase operation.
- Hardware RESET pin
  - Resets internal state machine to the read mode
- 20 years data retention

### GENERAL DESCRIPTION

The MX29F200T/B is a 2-mega bit, single 5 Volt Flash memory organized as 1M word x16 or 2M bytex8 MXIC's Flash memories offer the most cost-effective and reliable read/write non-volatile random access memory. The MX29F200T/B is packaged in 44-pin SOP and 48-pin TSOP. It is designed to be reprogrammed and erased in-system or in-standard EPROM programmers.

The standard MX29F200T/B offers access time as fast as 55ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the MX29F200T/B has separate chip enable (CE) and output enable (OE) controls.

MXIC's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The MX29F200T/B uses a command register to manage this functionality. The command register allows for 100%

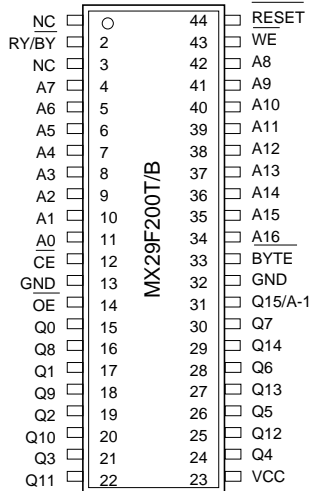
TTL level control inputs and fixed power supply levels during erase and programming, while maintaining maximum EPROM compatibility.

MXIC Flash technology reliably stores memory contents even after 100,000 erase and program cycles. The MXIC cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The MX29F200T/B uses a 5.0V ± 10% VCC supply to perform the High Reliability Erase and auto Program/Erase algorithms.

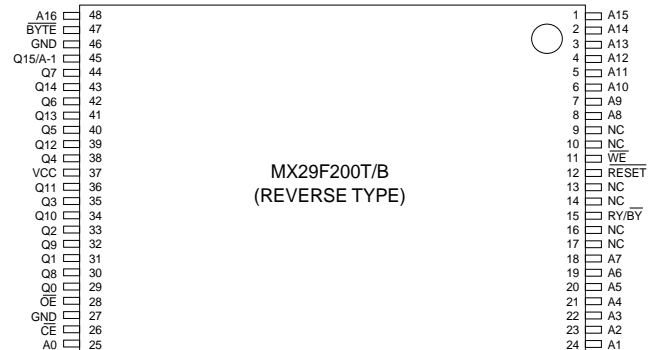
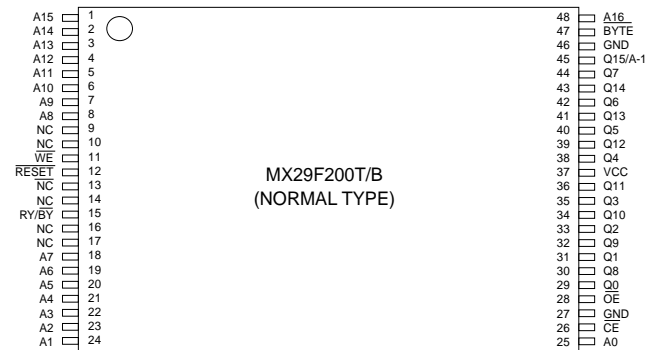
The highest degree of latch-up protection is achieved with MXIC's proprietary non-epi process. Latch-up protection is proved for stresses up to 100 milliamps on address and data pin from -1V to VCC + 1V.

## PIN CONFIGURATIONS

### 44 SOP(500mil)



### 48 TSOP(TYPE I) (12mm x 20mm)



## PIN DESCRIPTION

SYMBOL	PIN NAME
A0-A16	Address Input
Q0-Q14	Data Input/Output
Q15/A-1	Q15(Word mode)/LSB addr.(Byte mode)
CE	Chip Enable Input
OE	Output Enable Input
RESET	Hardware Reset Pin, Active low
WE	Write Enable Input
RY/BY	Read/Busy Output
BYTE	Word/Byte Selection Input
VCC	Power Supply Pin (+5V)
GND	Ground Pin
NC	Pin Not Connected Internally

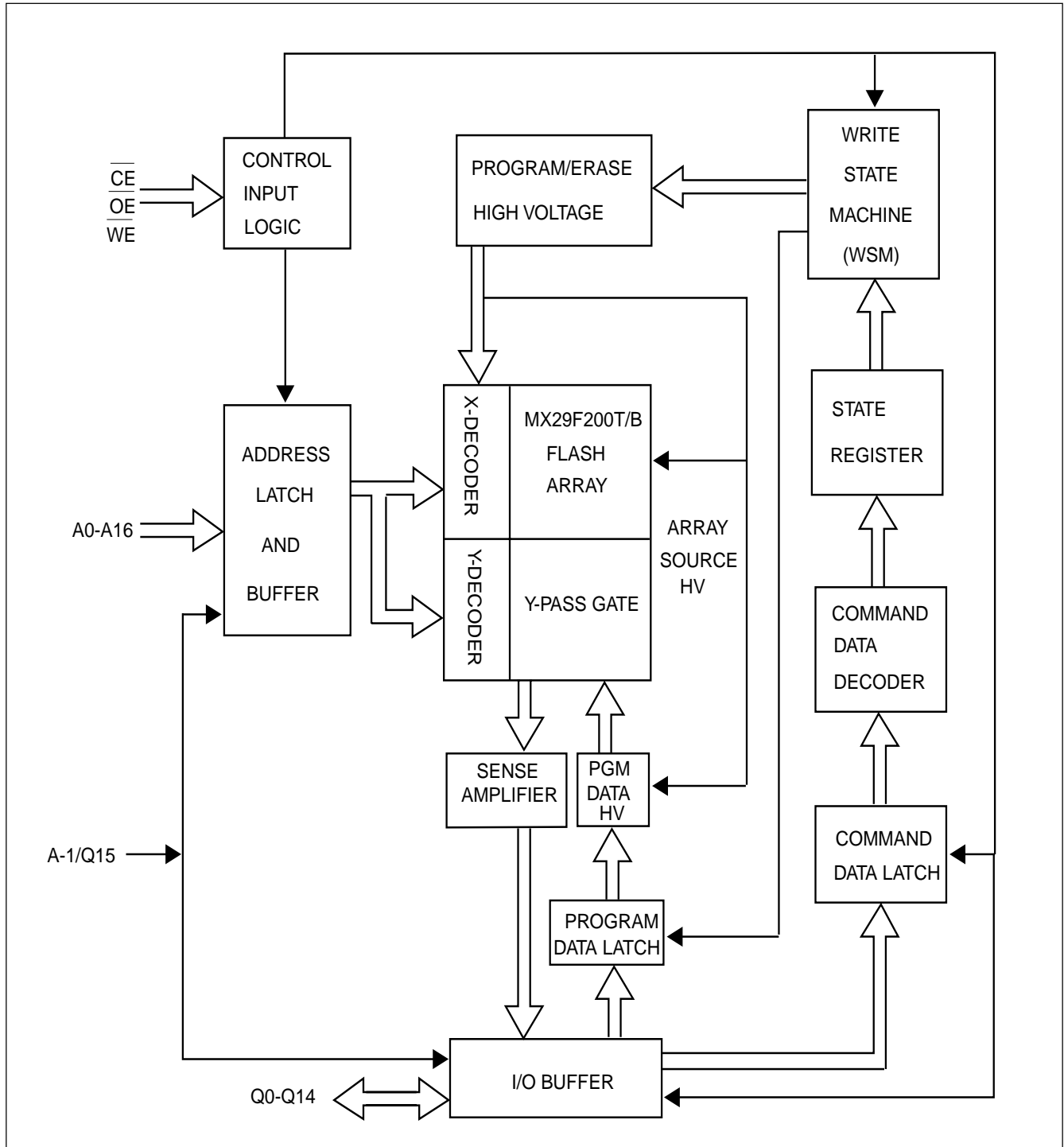
**SECTOR STRUCTURE**
**MX29F200T Top Boot Sector Addresses Tables**

						Sector Size	Address Range (in hexadecimal)	
	A16	A15	A14	A13	A12	(Kbytes/ Kwords)	(x8)Address Range	(x16) Address Range
SA0	0	0	X	X	X	64/32	00000h-0FFFFh	00000h-07FFFh
SA1	0	1	X	X	X	64/32	10000h-1FFFFh	08000h-0FFFFh
SA2	1	0	X	X	X	64/32	20000h-2FFFFh	10000h-17FFFh
SA3	1	1	0	X	X	32/16	30000h-37FFFh	18000h-1BFFFh
SA4	1	1	1	0	0	8/4	38000h-39FFFh	1C000h-1CFFFh
SA5	1	1	1	0	1	8/4	3A000h-3BFFFh	1D000h-1DFFFh
SA6	1	1	1	1	X	16/8	3C000h-3FFFFh	1E000h-1FFFFh

**MX29F200B Bottom Boot Sector Addresses Tables**

						Sector Size	Address Range (in hexadecimal)	
	A16	A15	A14	A13	A12	(Kbytes/ Kwords)	(x8)Address Range	(x16) Address Range
SA0	0	0	0	0	X	16/8	00000h-03FFFh	00000h-01FFFh
SA1	0	0	0	1	0	8/4	04000h-05FFFh	02000h-02FFFh
SA2	0	0	0	1	1	8/4	06000h-07FFFh	03000h-03FFFh
SA3	0	0	1	X	X	32/16	08000h-0FFFFh	04000h-07FFFh
SA4	0	1	X	X	X	64/32	10000h-1FFFFh	08000h-0FFFFh
SA5	1	0	X	X	X	64/32	20000h-2FFFFh	10000h-17FFFh
SA6	1	1	X	X	X	64/32	30000h-3FFFFh	18000h-1FFFFh

## BLOCK DIAGRAM



## **AUTOMATIC PROGRAMMING**

The MX29F200T/B is byte programmable using the Automatic Programming algorithm. The Automatic Programming algorithm does not require the system to time out sequence or verify the data programmed. The typical chip programming time of the MX29F200T/B at room temperature is less than 2 seconds.

## **AUTOMATIC CHIP ERASE**

The entire chip is bulk erased using 10 ms erase pulses according to MXIC's Automatic Chip Erase algorithm. Typical erasure at room temperature is accomplished in less than two second. The Automatic Erase algorithm automatically programs the entire array prior to electrical erase. The timing and verification of electrical erase are internally controlled by the device.

## **AUTOMATIC SECTOR ERASE**

The MX29F200T/B is sector(s) erasable using MXIC's Auto Sector Erase algorithm. Sector erase modes allow sectors of the array to be erased in one erase cycle. The Automatic Sector Erase algorithm automatically programs the specified sector(s) prior to electrical erase. The timing and verification of electrical erase are internally controlled by the device.

## **AUTOMATIC PROGRAMMING ALGORITHM**

MXIC's Automatic Programming algorithm requires the user to only write program set-up commands (include 2 unlock write cycle and A0H) and a program command (program data and address). The device automatically times the programming pulse width, verifies the program, and counts the number of sequences. A status bit similar to  $\overline{DATA}$  polling and a status bit toggling between consecutive read cycles, provides feedback to the user as to the status of the programming operation.

## **AUTOMATIC ERASE ALGORITHM**

MXIC's Automatic Erase algorithm requires the user to write commands to the command register using standard microprocessor write timings. The device will automatically pre-program and verify the entire array. Then the device automatically times the erase pulse width, verifies the erase and counts the number of sequences. A status bit toggling between consecutive read cycles provides feedback to the user as to the status of the programming operation.

Register contents serve as inputs to an internal state-machine which controls the erase and programming circuitry. During write cycles, the command register internally latches addresses and data needed for the programming and erase operations. During a system write cycle, addresses are latched on the falling edge, and data are latched on the rising edge of WE .

MXIC's Flash technology combines years of EPROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The MX29F200T/B electrically erases all bits simultaneously using Fowler-Nordheim tunneling. The bytes are programmed by using the EPROM programming mechanism of hot electron injection.

During a program cycle, the state-machine will control the program sequences and command register will not respond to any command set. During a Sector Erase cycle, the command register will only respond to Erase Suspend command. After Erase Suspend is complete, the device stays in read mode. After the state machine has completed its task, it will allow the command register to respond to its full command set.

**TABLE1. SOFTWARE COMMAND DEFINITIONS**

Command	Bus	First Bus Cycle		Second Bus Cycle		Third Bus Cycle		Fourth Bus Cycle		Fifth Bus Cycle		Sixth Bus Cycle	
		Cycle	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr
Reset	1	XXXH	F0H										
Read	1	RA	RD										
Read Silicon ID	Word	4	555H	AAH	2AAH	55H	555H	90H	ADI	DDI			
	Byte	4	AAAH	AAH	555H	55H	AAAH	90H	ADI	DDI			
Sector Protect Verify	Word	4	555H	AAH	2AAH	55H	555H	90H	(SA) X02H	XX00H			
	Byte	4	AAAH	AAH	555H	55H	AAAH	90H	(SA) X04H	00 01			
Program	Word	4	555H	AAH	2AAH	55H	555H	A0H	PA	PD			
	Byte	4	AAAH	AAH	555H	55H	AAAH	A0H	PA	PD			
Chip Erase	Word	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	555H 10H
	Byte	6	AAAH	AAH	555H	55H	AAAH	80H	AAAH	AAH	555H	55H	AAAH 10H
Sector Erase	Word	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	SA 30H
	Byte	6	AAAH	AAH	555H	55H	AAAH	80H	AAAH	AAH	555H	55H	SA 30H
Sector Erase Suspend	1	XXXH	B0H										
Sector Erase Resume	1	XXXH	30H										
Unlock for sector protect/unprotect	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	555H	20H

**NOTE:**

1. ADI = Address of Device identifier; A1=0, A0 =0 for manufacture code, A1=0, A0 =1 for device code.(Refer to Table 3)  
DDI = Data of Device identifier : C2H for manufacture code,51H/57H(x8) and 2251H/2257H(x16) for device code.  
X = X can be VIL or VIH  
RA=Address of memory location to be read.  
RD=Data to be read at location RA.
2. PA = Address of memory location to be programmed.  
PD = Data to be programmed at location PA.  
SA = Address to the sector to be erased.
3. The system should generate the following address patterns: 555H or 2AAH to Address A0~A10.  
Address bit A11~A16=X=Don't care for all address commands except for Program Address (PA) and Sector Address (SA).  
Write Sequence may be initiated with A11~A16 in either state.
4. For Sector Protection Verify Operation : If read out data is 01H, it means the sector has been protected. If read out data is 00H, it means the sector is still not being protected.

**COMMAND DEFINITIONS**

Device operations are selected by writing specific address and data sequences into the command register. Writing incorrect address and data values or writing them in the improper sequence will reset the device to the read mode. Table 1 defines the valid register

command sequences. Note that the Erase Suspend (B0H) and Erase Resume (30H) commands are valid only while the Sector Erase operation is in progress. Either of the two reset command sequences will reset the device(when applicable).

**TABLE 2. MX29F200T/B BUS OPERATION**

Mode \ Pins	CE	OE	WE	A0	A1	A6	A9	Q0 ~ Q15
Read Silicon ID Manufacturer Code(1)	L	L	H	L	L	X	V <sub>ID</sub> (2)	C2H(Byte mode) 00C2H(Word mode)
Read Silicon ID Device Code(1)	L	L	H	H	L	X	V <sub>ID</sub> (2)	51H/57H(Byte mode) 2251H/2257H(Word mode)
Read	L	L	H	A0	A1	A6	A9	D <sub>OUT</sub>
Standby	H	X	X	X	X	X	X	HIGH Z
Output Disable	L	H	H	X	X	X	X	HIGH Z
Write	L	H	L	A0	A1	A6	A9	D <sub>IN</sub> (3)
Sector Protect with 12V system(6)	L	V <sub>ID</sub> (2)	L	X	X	L	V <sub>ID</sub> (2)	X
Chip Unprotect with 12V system(6)	L	V <sub>ID</sub> (2)	L	X	X	H	V <sub>ID</sub> (2)	X
Verify Sector Protect with 12V system	L	L	H	X	H	X	V <sub>ID</sub> (2)	Code(5)
Sector Protect without 12V system (6)	L	H	L	X	X	L	H	X
Chip Unprotect without 12V system (6)	L	H	L	X	X	H	H	X
Verify Sector Protect/ Unprotect without 12V system (7)	L	L	H	X	H	X	H	Code(5)
Reset	X	X	X	X	X	X	X	HIGH Z

**NOTES:**

1. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 1.
2. VID is the Silicon-ID-Read high voltage, 11.5V to 12.5V.
3. Refer to Table 1 for valid Data-In during a write operation.
4. X can be VIL or VIH.
5. Code=00H/0000H means unprotected.  
Code=01H/0001H means protected.  
A16~A12=Sector address for sector protect.
6. Refer to sector protect/unprotect algorithm and waveform.  
Must issue "unlock for sector protect/unprotect" command before "sector protect/unprotect without 12V system" command.
7. The "verify sector protect/unprotect without 12V sysytem" is only following "Sector protect/unprotect without 12V system" command.

### READ/RESET COMMAND

The read or reset operation is initiated by writing the read/reset command sequence into the command register. Microprocessor read cycles retrieve array data. The device remains enabled for reads until the command register contents are altered.

If program-fail or erase-fail happen, the write of F0H will reset the device to abort the operation. A valid command must then be written to place the device in the desired state.

### SILICON-ID-READ COMMAND

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacturer and device codes must be accessible while the device resides in the target system. PROM programmers typically access signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto address lines is not generally desired system design practice.

The MX29F200T/B contains a Silicon-ID-Read operation to supplement traditional PROM programming methodology. The operation is initiated by writing the read silicon ID command sequence into the command register. Following the command write, a read cycle with A1=VIL, A0=VIL retrieves the manufacturer code of C2H/00C2H. A read cycle with A1=VIL, A0=VIH returns the device code of 51H/2251H for MX29F200T, 57H/2257H for MX29F200B.

### SET-UP AUTOMATIC CHIP/SECTOR ERASE COMMANDS

Chip erase is a six-bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command 80H. Two more "unlock" write cycles are then followed by the chip erase command 10H.

The Automatic Chip Erase does not require the device to be entirely pre-programmed prior to executing the Automatic Chip Erase. Upon executing the Automatic Chip Erase, the device will automatically program and verify the entire memory for an all-zero data pattern. When the device is automatically verified to contain an all-zero pattern, a self-timed chip erase and verify begin. The erase and verify operations are completed when the data on Q7 is "1" at which time the device returns to the Read mode. The system does not require to provide any control or timing during these operations.

When using the Automatic Chip Erase algorithm, note that the erase automatically terminates when adequate erase margin has been achieved for the memory array (no erase-verified command is required).

If the Erase operation was unsuccessful, the data on Q5 is "1" (see Table 4), indicating an erase operation exceed internal timing limit.

The automatic erase begins on the rising edge of the last WE pulse in the command sequence and terminates when the data on Q7 is "1" and the data on Q6 stops toggling for two consecutive read cycles, at which time the device returns to the Read mode.

**TABLE 3. EXPANDED SILICON ID CODE**

Pins		A0	A1	Q15~Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Code(Hex) Code
Manufacture code	Word	VIL	VIL	00H	1	1	0	0	0	0	1	0	00C2H
	Byte	VIL	VIL	X	1	1	0	0	0	0	1	0	C2H
Device code for MX29F200T	Word	VIH	VIL	22H	0	1	0	1	0	0	0	1	2251H
	Byte	VIH	VIL	X	0	1	0	1	0	0	0	1	51H
Device code for MX29F200B	Word	VIH	VIL	22H	0	1	0	1	0	1	1	1	2257H
	Byte	VIH	VIL	X	0	1	0	1	0	1	1	1	57H
Sector Portection Verification		X	VIH	X	0	0	0	0	0	0	0	1	01H(Protected)
		X	VIH	X	0	0	0	0	0	0	0	0	00H(Unprotected)



## SECTOR ERASE COMMANDS

The Automatic Sector Erase does not require the device to be entirely pre-programmed prior to executing the Automatic Set-up Sector Erase command and Automatic Sector Erase command. Upon executing the Automatic Sector Erase command, the device will automatically program and verify the sector(s) memory for an all-zero data pattern. The system does not require to provide any control or timing during these operations.

When the sector(s) is automatically verified to contain an all-zero pattern, a self-timed sector erase and verification begin. The erase and verification operations are complete when the data on Q7 is "1" and the data on Q6 stops toggling for two consecutive read cycles, at which time the device returns to the Read mode. The system does not require to provide any control or timing during these operations.

When using the Automatic Sector Erase algorithm, note that the erase automatically terminates when adequate erase margin has been achieved for the memory array (no erase-verified command is required). Sector erase is a six-bus cycle operation. There are two "unlock" write cycles. These are followed by writing the set-up command 80H. Two more "unlock" write cycles are then followed by the sector erase command 30H. The sector address is latched on the falling edge of  $\overline{WE}$ , while the command(data) is latched on the rising edge of  $\overline{WE}$ . Sector addresses selected are loaded into internal register on the sixth falling edge of  $\overline{WE}$ . Each successive sector load cycle started by the falling edge of  $\overline{WE}$  must begin within 30us from the rising edge of the preceding  $\overline{WE}$ . Otherwise, the loading period ends and internal auto sector erase cycle starts. (Monitor Q3 to determine if the sector erase timer window is still open, see section Q3, Sector Erase Timer.) Any command other than Sector Erase (30H) or Erase Suspend (B0H) during the time-out period resets the device to read mode.

## ERASE SUSPEND

This command is only valid while the state machine is executing Automatic Sector Erase operation, and therefore will only be responded to period during Automatic Sector Erase operation. Writing the Erase Suspend command during the Sector Erase time-out immediately terminates the time-out period and suspends the erase operation. After this command has been executed, the command register will initiate erase suspend mode. The state machine will return to read mode automatically after suspend is ready. At this time, state machine only allows the command register to respond to the Read Memory Array, Erase Resume and Program commands.

The system can determine the status of the program operation using the Q7 or Q6 status bits, just as in the standard program operation. After an erase-suspend program operation is complete, the system can once again read array data within non-suspended sectors.

**Table 4. Write Operation Status**

	Status	Q7	Q6	Q5	Q3	Q2	RY/BY	
		Note1		Note2				
In Progress	Byte Program in Auto Program Algorithm		$\overline{Q7}$	Toggle	0	N/A	No Toggle	0
	Auto Erase Algorithm		0	Toggle	0	1	Toggle	0
	Erase Suspended Mode	Erase Suspend Read (Erase Suspended Sector)	1	No Toggle	0	N/A	Toggle	1
		Erase Suspend Read (Non-Erase Suspended Sector)	Data	Data	Data	Data	Data	1
	Erase Suspend Program		$\overline{Q7}$	Toggle	0	N/A	N/A	0
Exceeded Time Limits	Byte Program in Auto Program Algorithm		$\overline{Q7}$	Toggle	1	N/A	No Toggle	0
	Auto Erase Algorithm		0	Toggle	1	1	Toggle	0
	Erase Suspend Program		$\overline{Q7}$	Toggle	1	N/A	N/A	0

**Note:**

1. Q7 and Q2 require a valid address when reading status information. Refer to the appropriate subsection for further details.
2. Q5 switches to '1' when an Auto Program or Auto Erase operation has exceeded the maximum timing limits. See "Q5:Exceeded Timing Limits " for more information.

## ERASE RESUME

This command will cause the command register to clear the suspend state and return back to Sector Erase mode but only if an Erase Suspend command was previously issued. Erase Resume will not have any effect in all other conditions. Another Erase Suspend command can be written after the chip has resumed erasing.

## SET-UP AUTOMATIC PROGRAM COMMANDS

To initiate Automatic Program mode, A three-cycle command sequence is required. There are two "unlock" write cycles. These are followed by writing the Automatic Program command A0H.

Once the Automatic Program command is initiated, the next  $\overline{WE}$  pulse causes a transition to an active programming operation. Addresses are latched on the falling edge, and data are internally latched on the rising edge of the  $\overline{WE}$  pulse. The rising edge of  $\overline{WE}$  also begins the programming operation. The system does not require to provide further controls or timings. The device will automatically provide an adequate internally generated program pulse and verify margin.

If the program operation was unsuccessful, the data on Q5 is "1" (see Table 4), indicating the program operation exceed internal timing limit. The automatic programming operation is completed when the data read on Q6 stops toggling for two consecutive read cycles and the data on Q7 and Q6 are equivalent to data written to these two bits, at which time the device returns to the Read mode (no program verify command is required).

## WRITE OPERATION STATUS DATA POLLING-Q7

The MX29F200T/B also features  $\overline{Data}$  Polling as a method to indicate to the host system that the Automatic Program or Erase algorithms are either in progress or completed.

While the Automatic Programming algorithm is in operation, an attempt to read the device will produce the complement data of the data last written to Q7. Upon completion of the Automatic Program Algorithm an attempt to read the device will produce the true data last written to Q7. The  $\overline{Data}$  Polling feature is valid after the rising edge of the fourth  $\overline{WE}$  pulse of the four write pulse sequences for automatic program.

While the Automatic Erase algorithm is in operation, Q7 will read "0" until the erase operation is completed. Upon completion of the erase operation, the data on Q7 will read "1". The  $\overline{Data}$  Polling feature is valid after the rising edge of the sixth  $\overline{WE}$  pulse of six write pulse sequences for automatic chip/sector erase.

The  $\overline{Data}$  Polling feature is active during Automatic Program/Erase algorithm or sector erase time-out. (see section Q3 Sector Erase Timer)

## $\overline{RY}/\overline{BY}$ : Ready/Busy

The  $\overline{RY}/\overline{BY}$  is a dedicated, open-drain output pin that indicates whether an Automatic Erase/Program algorithm is in progress or complete. The  $\overline{RY}/\overline{BY}$  status is valid after the rising edge of the final  $\overline{WE}$  pulse in the command sequence. Since  $\overline{RY}/\overline{BY}$  is an open-drain output, several  $\overline{RY}/\overline{BY}$  pins can be tied together in parallel with a pull-up resistor to  $V_{cc}$ .

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is ready to read array data (including during the Erase Suspend mode), or is in the standby mode.

## Q6: Toggle BIT I

Toggle Bit I on Q6 indicates whether an Automatic Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final  $\overline{WE}$  pulse in the command sequence (prior to the program or erase operation), and during the sector time-out.

During an Automatic Program or Erase algorithm operation, successive read cycles to any address cause Q6 to toggle. The system may use either  $\overline{OE}$  or  $\overline{CE}$  to control the read cycles. When the operation is complete, Q6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, Q6 toggles and returns to reading array data. If not all selected sectors are protected, the Automatic Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use Q6 and Q2 together to determine whether a sector is actively erasing or is erase suspended. When the device is actively erasing (that is, the Automatic Erase algorithm is in progress), Q6 toggling. When the device enters the Erase Suspend mode, Q6 stops toggling. However, the system must also use Q2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use Q7.

If a program address falls within a protected sector, Q6 toggles for approximately 2 $\mu$ s after the program command sequence is written, then returns to reading array data.

Q6 also toggles during the erase-suspend-program mode, and stops toggling once the Automatic Program algorithm is complete.

Table 4 shows the outputs for Toggle Bit I on Q6.

## Q2: Toggle Bit II

The "Toggle Bit II" on Q2, when used with Q6, indicates whether a particular sector is actively erasing (that is, the Automatic Erase algorithm is in process), or whether that sector is erase-suspended. Toggle Bit I is valid after the rising edge of the final  $\overline{WE}$  pulse in the command sequence.

Q2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either  $\overline{OE}$  or  $\overline{CE}$  to control the read cycles.) But Q2 cannot distinguish whether the sector is actively erasing or is erase-suspended. Q6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sectors and mode information. Refer to Table 4 to compare outputs for Q2 and Q6.

## Reading Toggle Bits Q6/ Q2

Whenever the system initially begins reading toggle bit status, it must read Q7-Q0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on Q7-Q0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of Q5 is high (see the section on Q5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as Q5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that system initially determines that the toggle bit is toggling and Q5 has not gone high. The system may continue to monitor the toggle bit and Q5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation.

## **Q5**

### **Exceeded Timing Limits**

Q5 will indicate if the program or erase time has exceeded the specified limits (internal pulse count). Under these conditions Q5 will produce a "1". This time-out condition which indicates that the program or erase cycle was not successfully completed. Data Polling and Toggle Bit are the only operating functions of the device under this condition.

If this time-out condition occurs during sector erase operation, it specifies that a particular sector is bad and it may not be reused. However, other sectors are still functional and may be used for the program or erase operation. The device must be reset to use other sectors. Write the Reset command sequence to the device, and then execute program or erase command sequence. This allows the system to continue to use the other active sectors in the device.

If this time-out condition occurs during the chip erase operation, it specifies that the entire chip is bad or combination of sectors are bad.

If this time-out condition occurs during the byte programming operation, it specifies that the entire sector containing that byte is bad and this sector may not be reused, (other sectors are still functional and can be reused).

The time-out condition may also appear if a user tries to program a non blank location without erasing. In this case the device locks out and never completes the Automatic Algorithm operation. Hence, the system never reads a valid data on Q7 bit and Q6 never stops toggling. Once the Device has exceeded timing limits, the Q5 bit will indicate a "1". Please note that this is not a device failure condition since the device was incorrectly used.

## **Q3**

### **Sector Erase Timer**

After the completion of the initial sector erase command sequence, the sector erase time-out will begin. Q3 will remain low until the time-out is complete. Data Polling and Toggle Bit are valid after the initial sector erase command sequence.

If  $\overline{\text{Data}}$  Polling or the Toggle Bit indicates the device has been written with a valid erase command, Q3 may be used to determine if the sector erase timer window is still open. If Q3 is high ("1") the internally controlled erase cycle has begun; attempts to write subsequent commands to the device will be ignored until the erase operation is completed as indicated by  $\overline{\text{Data}}$  Polling or Toggle Bit. If Q3 is low ("0"), the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of Q3 prior to and following each subsequent sector erase command. If Q3 were high on the second status check, the command may not have been accepted.

## **DATA PROTECTION**

The MX29F200T/B is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transition. During power up the device automatically resets the state machine in the Read mode. In addition, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences. The device also incorporates several features to prevent inadvertent write cycles resulting from VCC power-up and power-down transition or system noise.

## **TEMPORARY SECTOR UNPROTECT**

This feature allows temporary unprotection of previously protected sector to change data in-system. The Temporary Sector Unprotect mode is activated by setting the  $\overline{\text{RESET}}$  pin to VID (11.5V-12.5V). During this mode, formerly protected sectors can be programmed or erased as un-protected sector. Once VID is removed from the  $\overline{\text{RESET}}$  pin, all the previously protected sectors are protected again.

## **WRITE PULSE "GLITCH" PROTECTION**

Noise pulses of less than 5ns (typical) on  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$  will not initiate a write cycle.

## **LOGICAL INHIBIT**

Writing is inhibited by holding any one of  $\overline{\text{OE}} = \text{VIL}$ ,  $\overline{\text{CE}} = \text{VIH}$  or  $\overline{\text{WE}} = \text{VIH}$ . To initiate a write cycle  $\overline{\text{CE}}$  and  $\overline{\text{WE}}$  must be a logical zero while  $\overline{\text{OE}}$  is a logical one.

## POWER SUPPLY DECOUPLING

In order to reduce power switching effect, each device should have a 0.1uF ceramic capacitor connected between its VCC and GND.

## SECTOR PROTECTION WITH 12V SYSTEM

The MX29F200T/B features hardware sector protection. This feature will disable both program and erase operations for these sectors protected. To activate this mode, the programming equipment must force VID on address pin A9 and control pin OE, (suggest VID = 12V) A6 = VIL and CE = VIL.(see Table 2) Programming of the protection circuitry begins on the falling edge of the WE pulse and is terminated on the rising edge. Please refer to sector protect algorithm and waveform.

To verify programming of the protection circuitry, the programming equipment must force VID on address pin A9 (with CE and OE at VIL and WE at VIH. When A1=1, it will produce a logical "1" code at device output Q0 for a protected sector. Otherwise the device will produce 00H for the unprotected sector. In this mode, the addresses,except for A1, are in "don't care" state. Address locations with A1 = VIL are reserved to read manufacturer and device codes.(Read Silicon ID)

It is also possible to determine if the sector is protected in the system by writing a Read Silicon ID command. Performing a read operation with A1=VIH, it will produce a logical "1" at Q0 for the protected sector.

## CHIP UNPROTECT WITH 12V SYSTEM

The MX29F200T/B also features the chip unprotect mode, so that all sectors are unprotected after chip unprotect is completed to incorporate any changes in the code. It is recommended to protect all sectors before activating chip unprotect mode.

To activate this mode, the programming equipment must force VID on control pin OE and address pin A9. The CE pins must be set at VIL. Pins A6 must be set to VIH.(see Table 2) Refer to chip unprotect algorithm and waveform for the chip unprotect algorithm. The unprotection mechanism begins on the falling edge of the WE pulse and is terminated on the rising edge .

It is also possible to determine if the chip is unprotected

in the system by writing the Read Silicon ID command. Performing a read operation with A1=VIH, it will produce 00H at data outputs(Q0-Q7) for an unprotected sector. It is noted that all sectors are unprotected after the chip unprotect algorithm is completed.

## SECTOR PROTECTION WITHOUT 12V SYSTEM

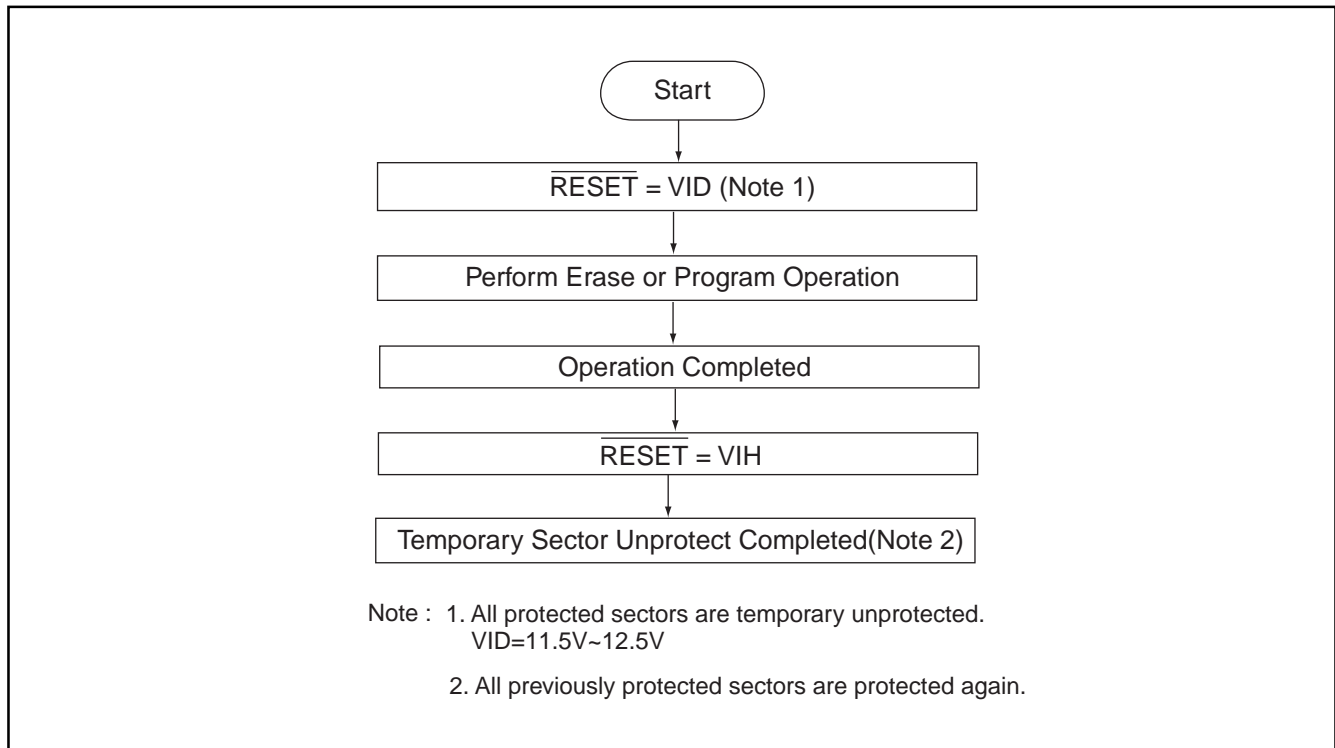
The MX29F200T/B also feature a hardware sector protection method in a system without 12V power supply. The programming equipment do not need to supply 12 volts to protect sectors. The details are shown in sector protect algorithm and waveform.

## CHIP UNPROTECT WITHOUT 12V SYSTEM

The MX29F200T/B also feature a hardware chip unprotection method in a system without 12V power supply. The programming equipment do not need to supply 12 volts to unprotect all sectors. The details are shown in chip unprotect algorithm and waveform.

## POWER-UP SEQUENCE

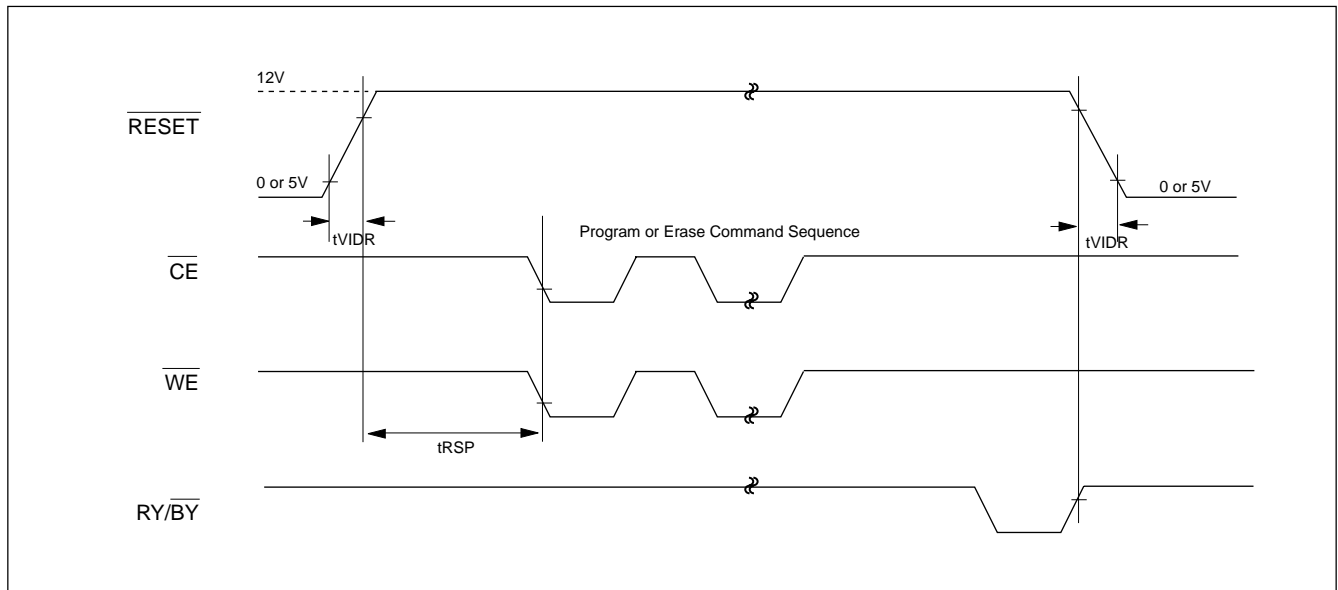
The MX29F200T/B powers up in the Read only mode. In addition, the memory contents may only be altered after successful completion of the predefined command sequences.

**Temporary Sector Unprotect Operation**

**TEMPORARY SECTOR UNPROTECT**

Parameter Std.	Description	Test Setup	AllSpeed Options	Unit
tVIDR	VID Rise and Fall Time (See Note)	Min	500	ns
tRSP	RESET Setup Time for Temporary Sector Unprotect	Min	4	us

Note:  
Not 100% tested

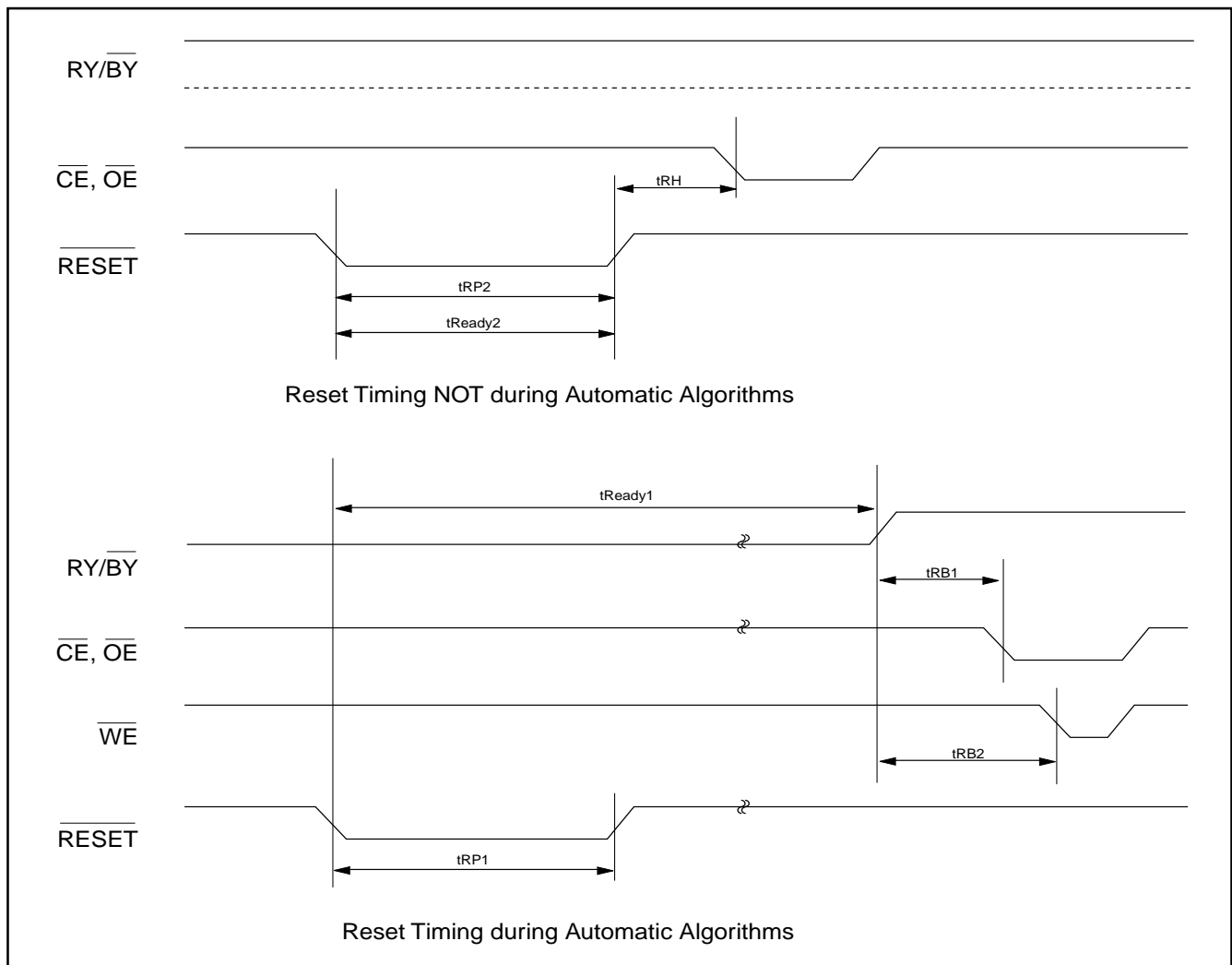
**Temporary Sector Unprotect Timing Diagram**




Parameter Std	Description	Test Setup	All Speed Options	Unit
tREADY1	RESET PIN Low (During Automatic Algorithms) to Read or Write (See Note)	MAX	20	us
tREADY2	RESET PIN Low (NOT During Automatic Algorithms) to Read or Write (See Note)	MAX	500	ns
tRP1	RESET Pulse Width (During Automatic Algorithms)	MIN	10	us
tRP2	RESET Pulse Width (NOT During Automatic Algorithms)	MIN	500	ns
tRH	RESET High Time Before Read(See Note)	MIN	0	ns
tRB1	RY/BY Recovery Time(to CE, OE go low)	MIN	0	ns
tRB2	RY/BY Recovery Time(to WE go low)	MIN	50	ns

Note:Not 100% tested

### RESET TIMING WAVFORM



**ABSOLUTE MAXIMUM RATINGS**

RATING	VALUE
Ambient Operating Temperature	-40°C to 85°C
Ambient Temperature with Power Applied	-55°C to 125°C
Storage Temperature	-65°C to 125°C
Applied Input Voltage	-0.5V to 7.0V
Applied Output Voltage	-0.5V to 7.0V
VCC to Ground Potential	-0.5V to 7.0V
A9&OE	-0.5V to 13.5V

**NOTICE:**

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

**NOTICE:**

Specifications contained within the following tables are subject to change.

**DC/AC Operating Conditions for Read Operation**

		<b>MX29F200T/B</b>			
		<b>-55</b>	<b>-70</b>	<b>-90</b>	<b>-12</b>
Operating Temperature	Commercial	0°C to 70°C	0°C to 70°C	0°C to 70°C	0°C to 70°C
	Industrial		-40°C to 85°C	-40°C to 85°C	-40°C to 85°C
	Automotive			-40°C to 125°C	-40°C to 125°C
Vcc Power Supply		5V±5%	5V±10%	5V±10%	5V±10%

**CAPACITANCE TA = 25°C, f = 1.0 MHz**

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS
CIN1	Input Capacitance			8	pF	VIN = 0V
CIN2	Control Pin Capacitance			12	pF	VIN = 0V
COUT	Output Capacitance			12	pF	VOU = 0V

**READ OPERATION**
**DC CHARACTERISTICS**

Symbol	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS
ILI	Input Leakage Current			1(Note3)	uA	VIN = GND to VCC
ILO	Output Leakage Current			10	uA	VOUT = GND to VCC
ISB1	Standby VCC current			1	mA	$\overline{CE} = V_{IH}$
ISB2			1(Note5)	5(Note5)	uA	$\overline{CE} = V_{CC} + 0.3V$
ICC1	Operating VCC current			40(Note4)	mA	IOUT = 0mA, f=5MHz
ICC2				50	mA	IOUT = 0mA, f=10MHz
VIL	Input Low Voltage	-0.3(Note1)			0.8	V
VIH	Input High Voltage	2.0		VCC+0.3	V	
VOL	Output Low Voltage			0.45	V	IOL = 2.1mA
VOH1	Output High Voltage(TTL)	2.4			V	IOH = -2mA
VOH2	Output High Voltage(CMOS)	VCC-0.4			V	IOH = -100uA, VCC=VCC MIN

**NOTES:**

- VIL min. = -1.0V for pulse width is equal to or less than 50 ns.  
VIL min. = -2.0V for pulse width is equal to or less than 20 ns.
- VIH max. = VCC + 1.5V for pulse width is equal to or less than 20 ns  
If VIH is over the specified maximum value, read operation cannot be guaranteed.
- ILI=10uA for Industrial Grade.
- ICC1=45mA for Industrial Grade.
- ISB2 maximum 20uA for automotive grade.

## AC CHARACTERISTICS

SYMBOL	PARAMETER	29F200T/B-55		29F200T/B-70		UNIT	CONDITIONS
		MIN.	MAX.	MIN.	MAX.		
tACC	Address to Output Delay		55		70	ns	$\overline{CE}=\overline{OE}=\text{VIL}$
tCE	$\overline{CE}$ to Output Delay		55		70	ns	$\overline{OE}=\text{VIL}$
tOE	$\overline{OE}$ to Output Delay		20		40	ns	$\overline{CE}=\text{VIL}$
tDF	$\overline{OE}$ High to Output Float (Note1)	0	20	0	20	ns	$\overline{CE}=\text{VIL}$
tOH	Address to Output hold	0		0		ns	$\overline{CE}=\overline{OE}=\text{VIL}$

SYMBOL	PARAMETER	29F200T/B-90		29F200T/B-12		UNIT	CONDITIONS
		MIN.	MAX.	MIN.	MAX.		
tACC	Address to Output Delay		90		120	ns	$\overline{CE}=\overline{OE}=\text{VIL}$
tCE	$\overline{CE}$ to Output Delay		90		120	ns	$\overline{OE}=\text{VIL}$
tOE	$\overline{OE}$ to Output Delay		40		50	ns	$\overline{CE}=\text{VIL}$
tDF	$\overline{OE}$ High to Output Float (Note1)	0	30	0	30	ns	$\overline{CE}=\text{VIL}$
tOH	Address to Output hold	0		0		ns	$\overline{CE}=\overline{OE}=\text{VIL}$

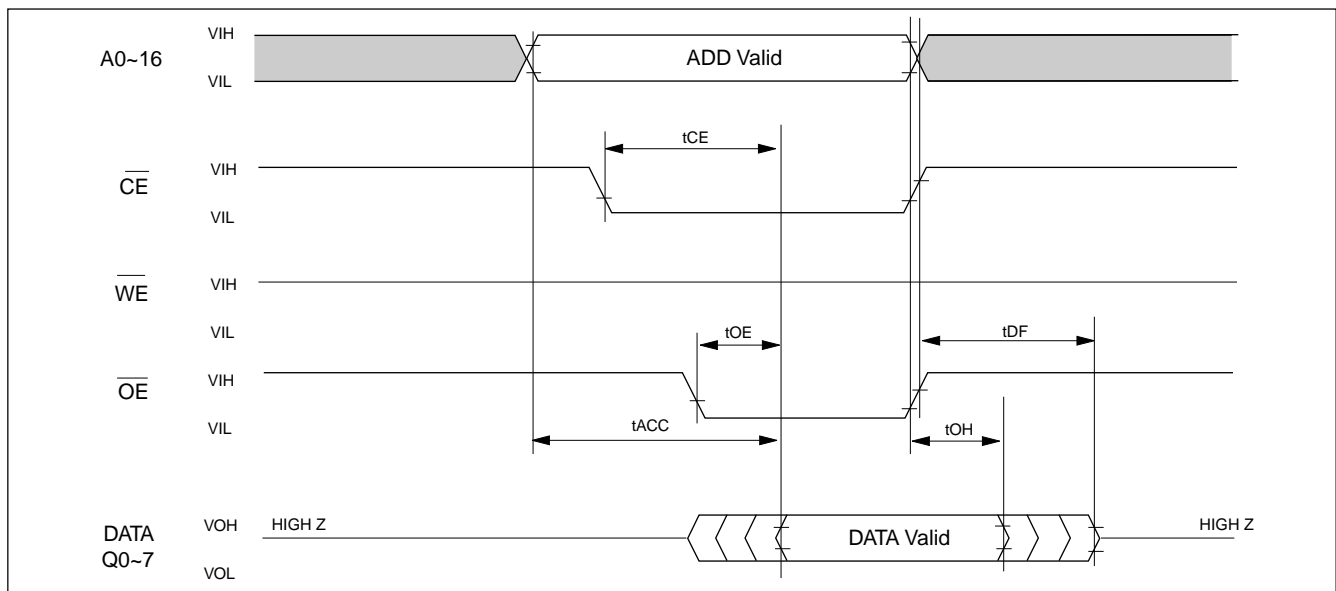
### TEST CONDITIONS:

- Input pulse levels: 0.45V/2.4V for 70ns max, 0V/3V for 55ns
- Input rise and fall times: is equal to or less than 10ns for 70ns max, 5ns for 55ns
- Output load: 1 TTL gate + 100pF (Including scope and jig) for 70ns max.  
:1TTLgate+30pF for 55ns max.
- Reference levels for measuring timing: 0.8V, 2.0V for 70ns max.; 1.5V for 55ns

### NOTE:

1. tDF is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

## READ TIMING WAVEFORMS



**COMMAND PROGRAMMING/DATA PROGRAMMING/ERASE OPERATION**
**DC/AC Operating Conditions for Programming/Erase Operation**

		<b>MX29F200T/B</b>			
		<b>-55</b>	<b>-70</b>	<b>-90</b>	<b>-12</b>
Operating Temperature	Commercial	0°C to 70°C	0°C to 70°C	0°C to 70°C	0°C to 70°C
	Industrial		-40°C to 85°C	-40°C to 85°C	-40°C to 85°C
	Automotive			-40°C to 125°C	-40°C to 125°C
Vcc Power Supply		5V±5%	5V±10%	5V±10%	5V±10%

**DC CHARACTERISTICS**

<b>SYMBOL</b>	<b>PARAMETER</b>	<b>MIN.</b>	<b>TYP</b>	<b>MAX.</b>	<b>UNIT</b>	<b>CONDITIONS</b>
ICC1 (Read)	Operating VCC Current			40(Note5)	mA	IOUT=0mA, f=5MHz
ICC2				50	mA	IOUT=0mA, F=10MHz
ICC3 (Program)				50	mA	In Programming
ICC4 (Erase)				50	mA	In Erase
ICCES	VCC Erase Suspend Current		2		mA	$\overline{CE}=VIH$ , Erase Suspended

**NOTES:**

1. VIL min. = -0.6V for pulse width is equal to or less than 20ns.
2. If VIH is over the specified maximum value, programming operation cannot be guaranteed.
3. ICCES is specified with the device de-selected. If the device is read during erase suspend mode, current draw is the sum of ICCES and ICC1 or ICC2.
4. All current are in RMS unless otherwise noted.
5. ICC1 (Read)=45mA for Industrial Grade.

**AC CHARACTERISTICS**

SYMBOL	PARAMETER	29F200T/B-55(Note2)		29F200T/B-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
tOES	OE setup time	0		0		ns
tCWC	Command programming cycle	70		70		ns
tCEP	$\overline{WE}$ programming pulse width	45		45		ns
tCEPH1	$\overline{WE}$ programming pluse width High	20		20		ns
tCEPH2	$\overline{WE}$ programming pluse width High	20		20		ns
tAS	Address setup time	0		0		ns
tAH	Address hold time	45		45		ns
tDS	Data setup time	20		30		ns
tDH	Data hold time	0		0		ns
tCESC	$\overline{CE}$ setup time before command write	0		0		ns
tDF	Output disable time (Note 1)		20		30	ns
tAETC	Total erase time in auto chip erase	3(TYP.)	24	3(TYP.)	24	s
tAETB	Total erase time in auto sector erase	1(TYP.)	8	1(TYP.)	8	s
tAVT	Total programming time in auto verify	7/12(TYP.)	210/360	7/12(TYP.)	210/360	us
tBAL	Sector address load time	100		100		us
tCH	$\overline{CE}$ Hold Time	0		0		ns
tCS	$\overline{CE}$ setup to $\overline{WE}$ going low	0		0		ns
tVLHT	Voltge Transition Time	4		4		us
tOESP	$\overline{OE}$ Setup Time to $\overline{WE}$ Active	4		4		us
tWPP	Write pulse width for sector protect	10		10		us
tWPP2	Write pulse width for sector unprotect	12		12		ms

**NOTES:**

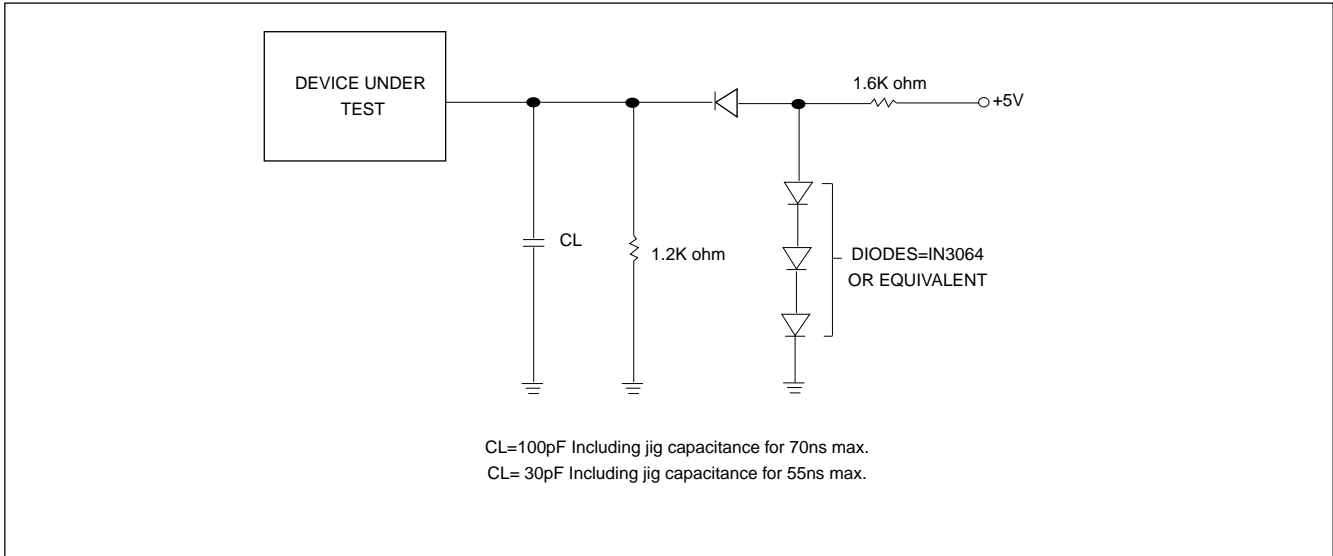
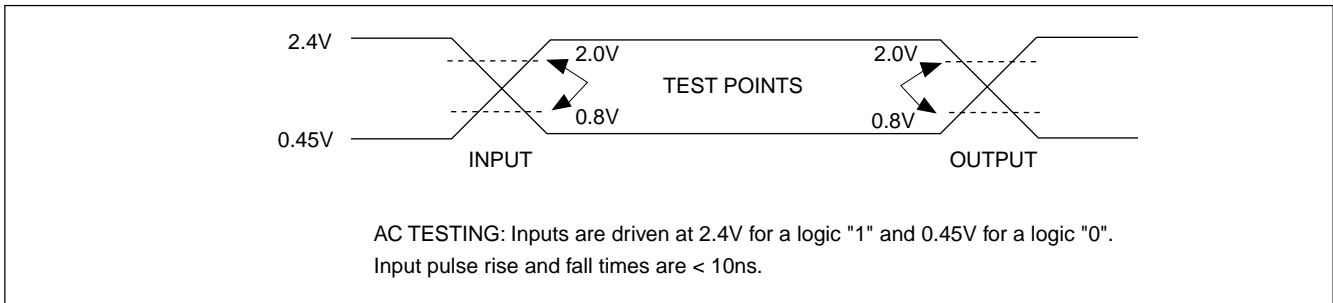
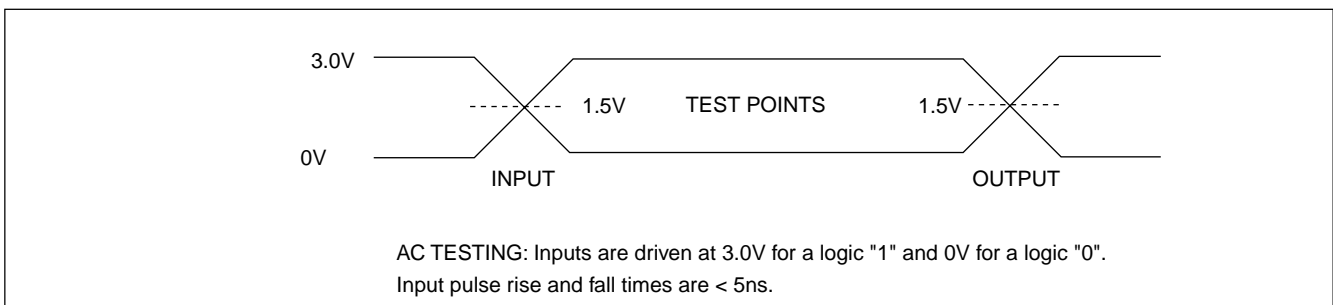
1. tDF defined as the time at which the output achieves the open circuit condition and data is no longer driven.
2. Under condition of VCC=5V±5%, CL=30pF, VIH/VIL=3.0V/0V, VOH/VOL=1.5V/1.5V, IOL=2mA, IOH=2mA.

**AC CHARACTERISTICS**

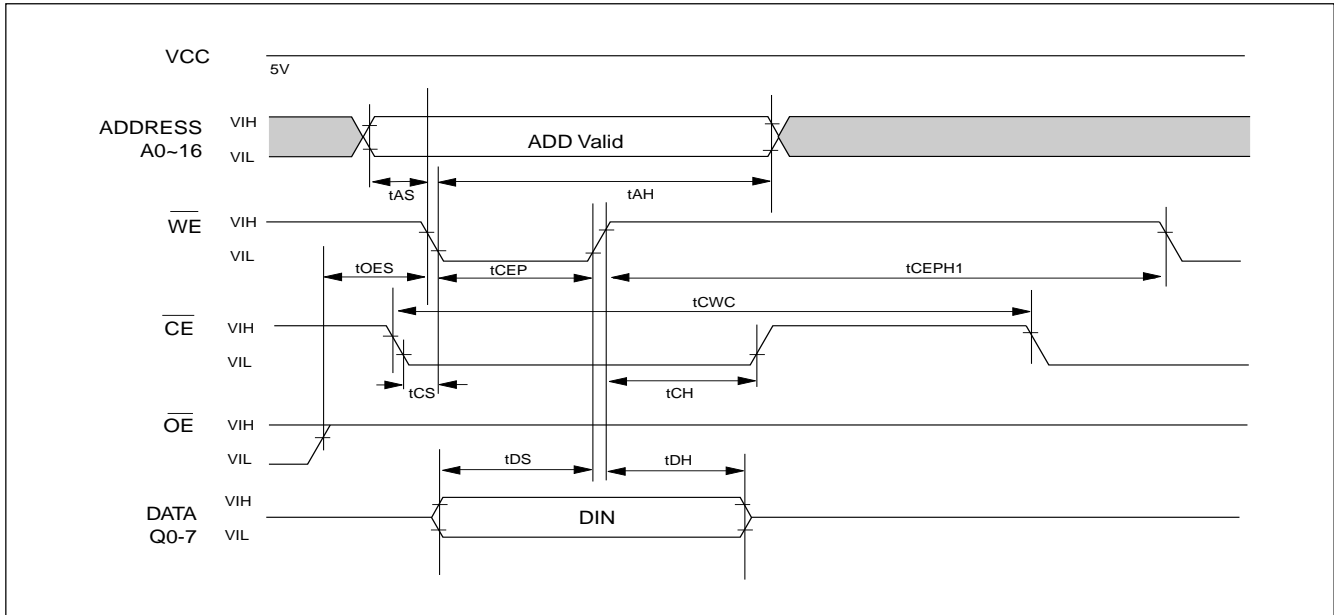
SYMBOL	PARAMETER	29F200T/B-90		29F200T/B-120		UNIT
		MIN.	MAX.	MIN.	MAX.	
tOES	OE setup time	0		0		ns
tCWC	Command programming cycle	90		120		ns
tCEP	$\overline{WE}$ programming pulse width	45		50		ns
tCEPH1	$\overline{WE}$ programming pluse width High	20		20		ns
tCEPH2	$\overline{WE}$ programming pluse width High	20		20		ns
tAS	Address setup time	0		0		ns
tAH	Address hold time	45		50		ns
tDS	Data setup time	45		50		ns
tDH	Data hold time	0		0		ns
tCESC	$\overline{CE}$ setup time before command write	0		0		ns
tDF	Output disable time (Note 1)		40		40	ns
tAETC	Total erase time in auto chip erase	3(TYP.)	24	3(TYP.)	24	s
tAETB	Total erase time in auto sector erase	1(TYP.)	8	1(TYP.)	8	s
tAVT	Total programming time in auto verify	7/12(TYP.)	210/360	7/12(TYP.)	210/360	us
tBAL	Sector address load time	100		100		us
tCH	$\overline{CE}$ Hold Time	0		0		ns
tCS	$\overline{CE}$ setup to WE going low	0		0		ns
tVLHT	Voltge Transition Time	4		4		us
tOESP	$\overline{OE}$ Setup Time to $\overline{WE}$ Active	4		4		us
tWPP	Write pulse width for sector protect	10		10		us
tWPP2	Write pulse width for sector unprotect	12		12		ms

**NOTES:**

1. tDF defined as the time at which the output achieves the open circuit condition and data is no longer driven.
2. Under condition of VCC=5V±5%, CL=30pF, VIH/VIL=3.0V/0V, VOH/VOL=1.5V/1.5V, IOL=2mA, IOH=2mA.

**SWITCHING TEST CIRCUITS**

**SWITCHING TEST WAVEFORMS(I) for 29F200T/B-70, 29F200T/B-90, 29F200T/B-12**

**SWITCHING TEST WAVEFORMS(II) for 29F200T/B-55**




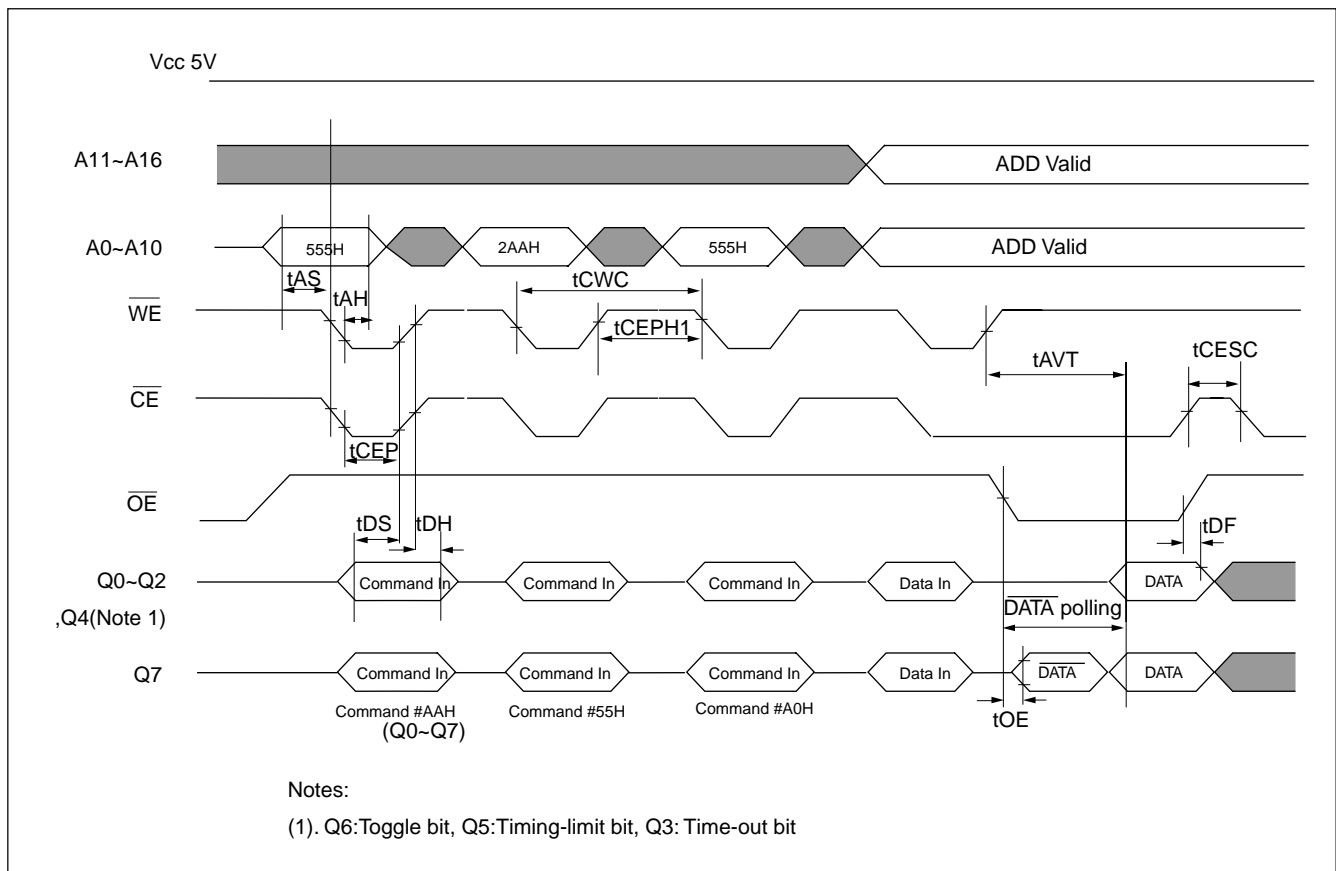
**COMMAND WRITE TIMING WAVEFORM**


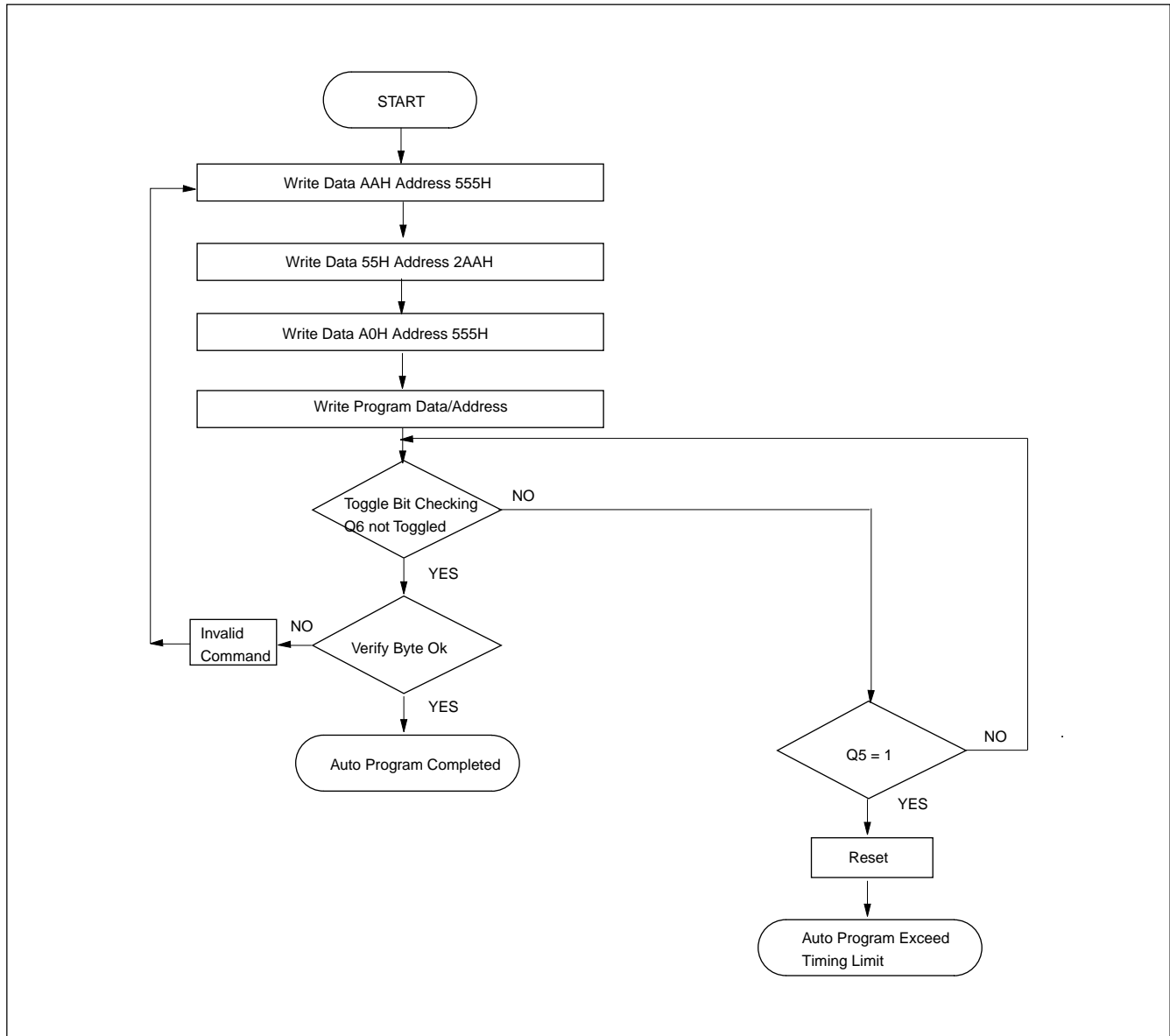
### AUTOMATIC PROGRAMMING TIMING WAVEFORM

One byte data is programmed. Verify in fast algorithm and additional programming by external control are not required because these operations are executed automatically by internal control circuit. Programming completion can be verified by DATA polling and toggle

bit checking after automatic verification starts. Device outputs DATA during programming and DATA after programming on Q7.(Q6 is for toggle bit; see toggle bit, DATA polling, timing waveform).

### AUTOMATIC PROGRAMMING TIMING WAVEFORM (WORD MODE)

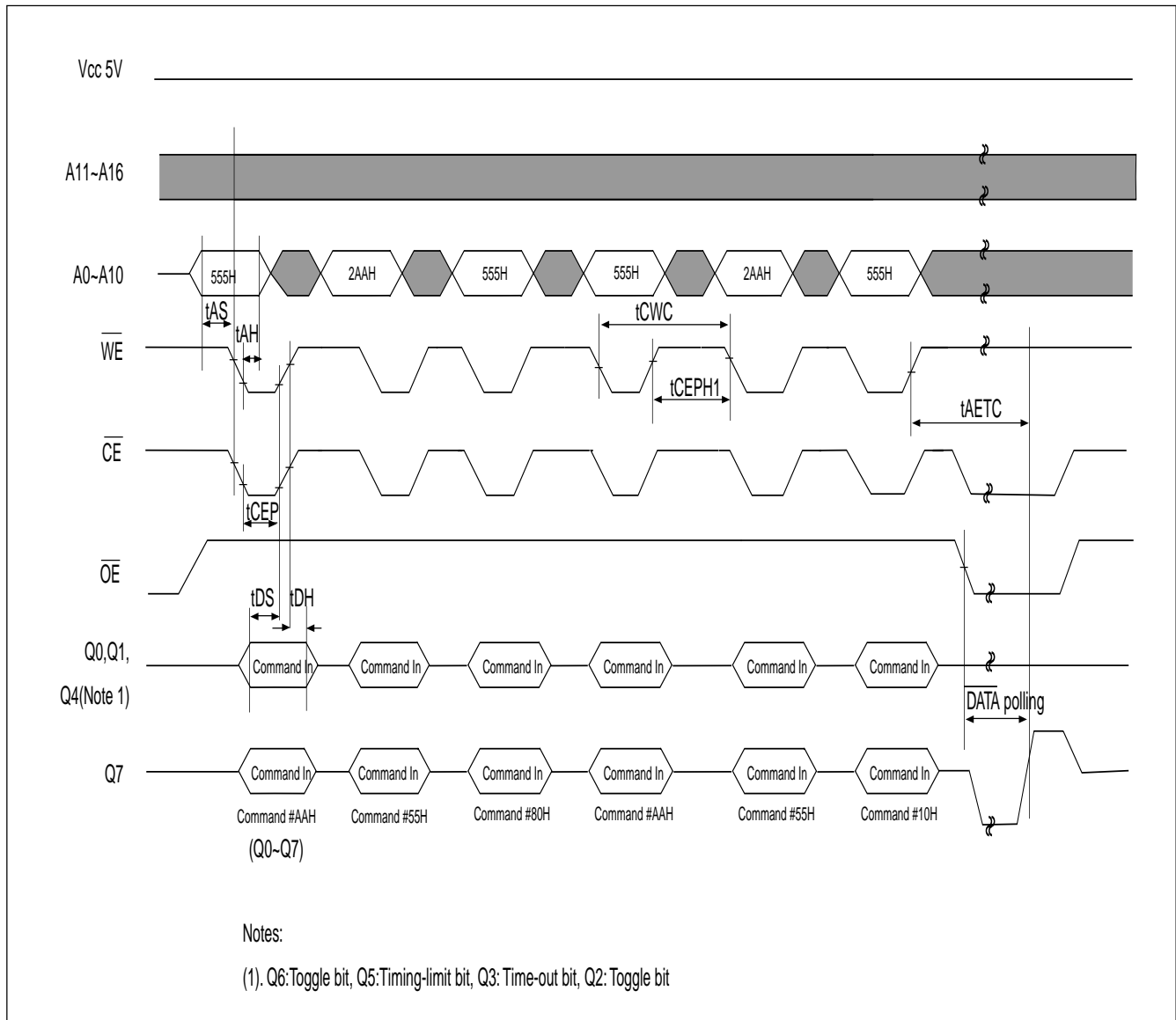


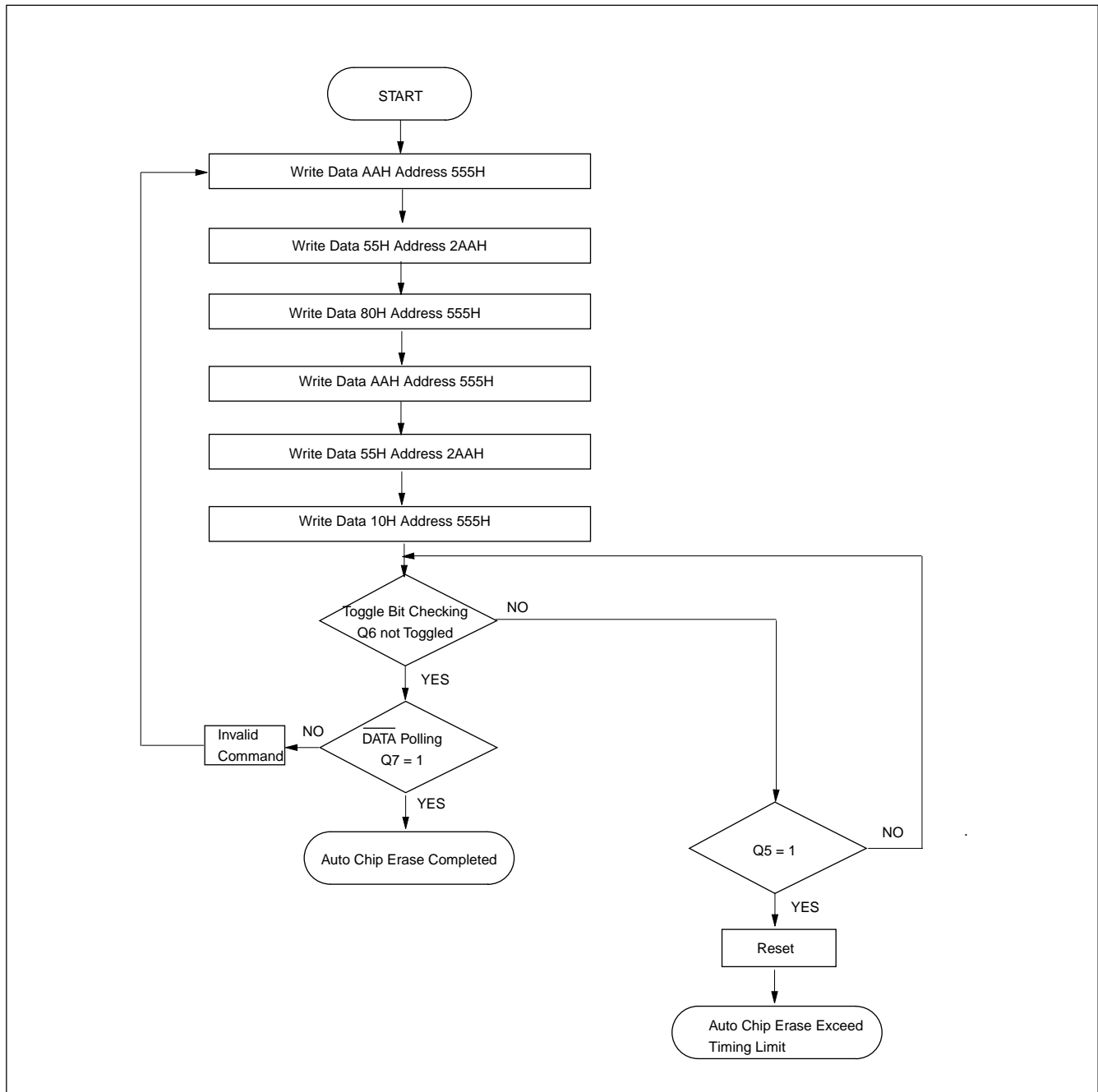
**AUTOMATIC PROGRAMMING ALGORITHM FLOWCHART (WORD MODE)**

**AUTOMATIC CHIP ERASE TIMING WAVEFORM**

All data in chip are erased. External erase verification is not required because data is erased automatically by internal control circuit. Erasure completion can be verified by DATA polling and toggle bit checking after

automatic erase starts. Device outputs 0 during erasure and 1 after erasure 0n Q7. (Q6 is for toggle bit; see toggle bit, DATA polling, timing waveform)

**AUTOMATIC CHIP ERASE TIMING WAVEFORM (WORD MODE)**


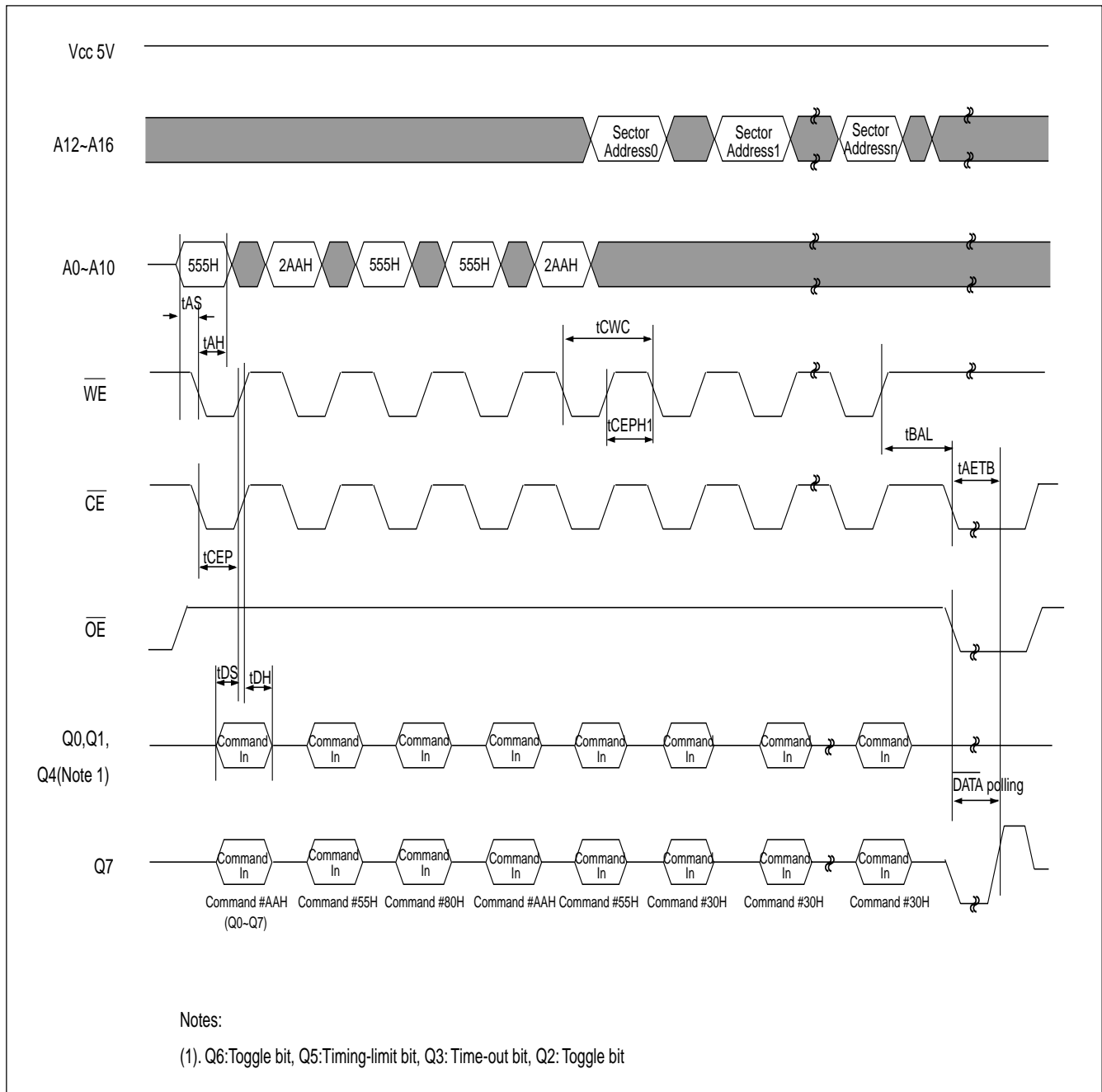
**AUTOMATIC CHIP ERASE ALGORITHM FLOWCHART (WORD MODE)**


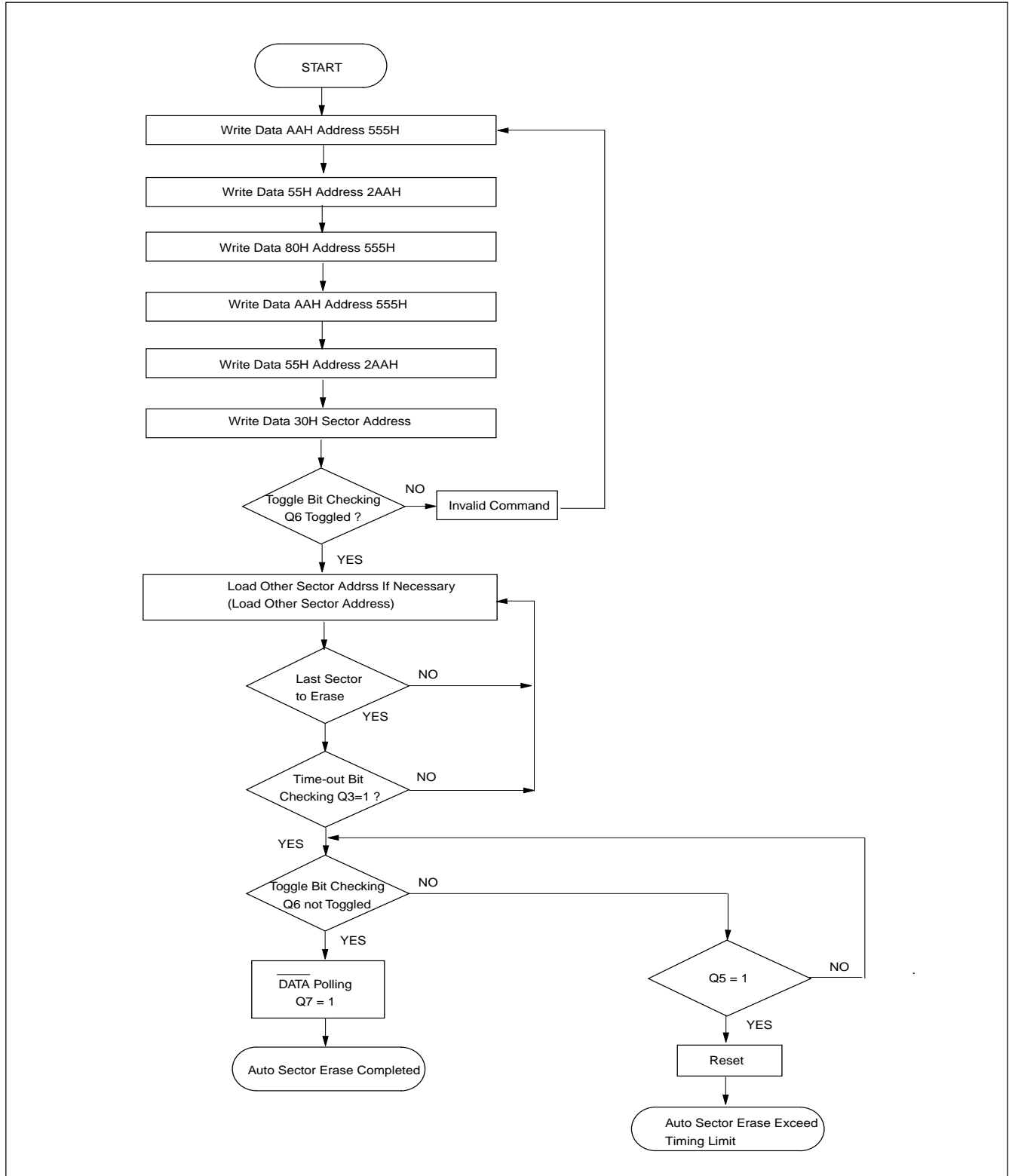
## AUTOMATIC SECTOR ERASE TIMING WAVEFORM

Sector data indicated by A12 to A16 are erased. External erase verification is not required because data are erased automatically by internal control circuit. Erasure completion can be verified by DATA polling and toggle

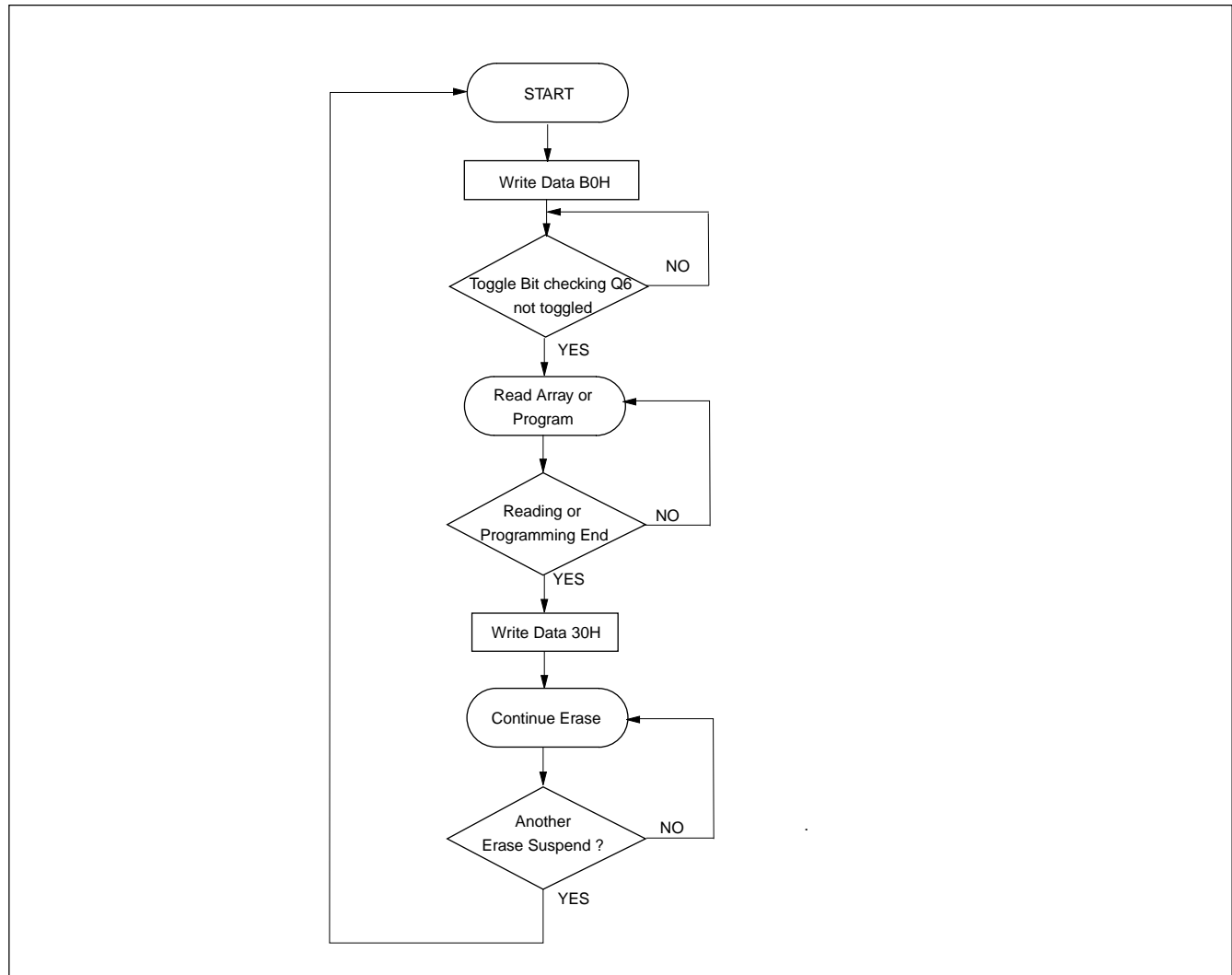
bit checking after automatic erase starts. Device outputs 0 during erasure and 1 after erasure on Q7. (Q6 is for toggle bit; see toggle bit, DATA polling, timing waveform)

## AUTOMATIC SECTOR ERASE TIMING WAVEFORM (WORD MODE)

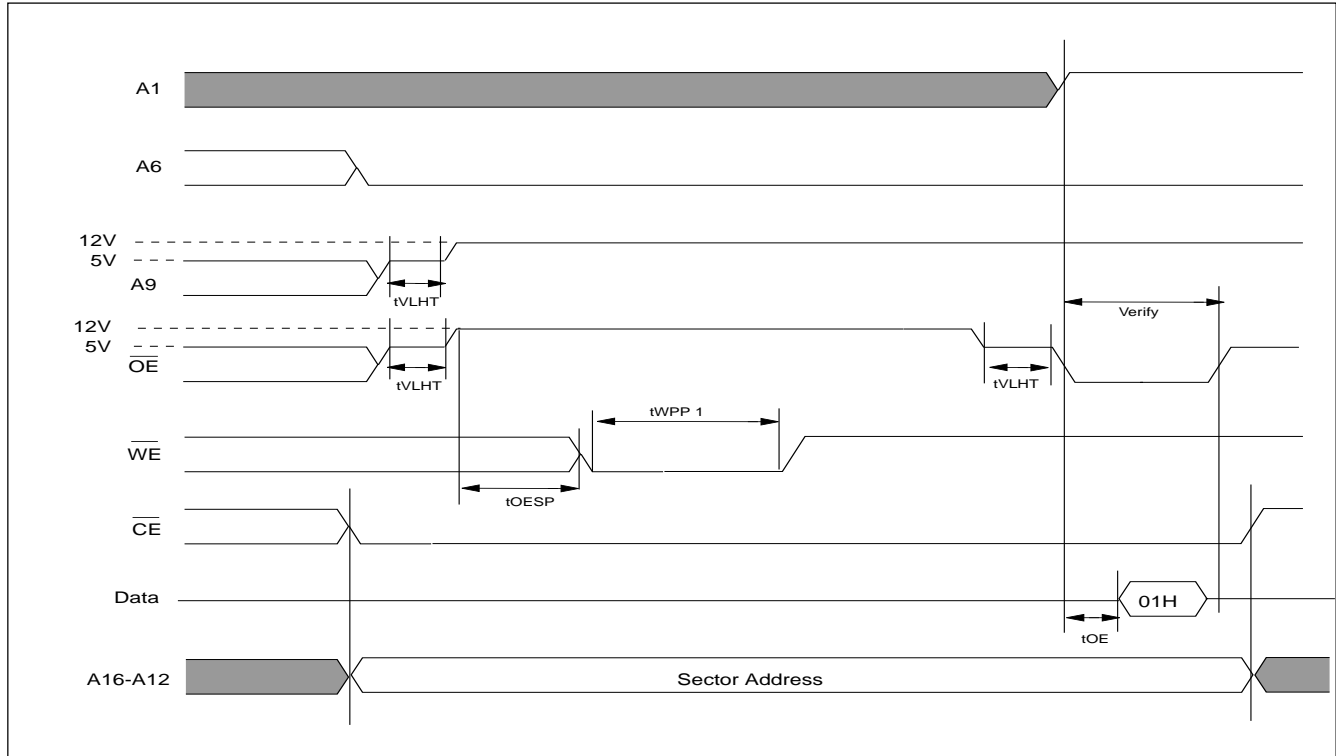
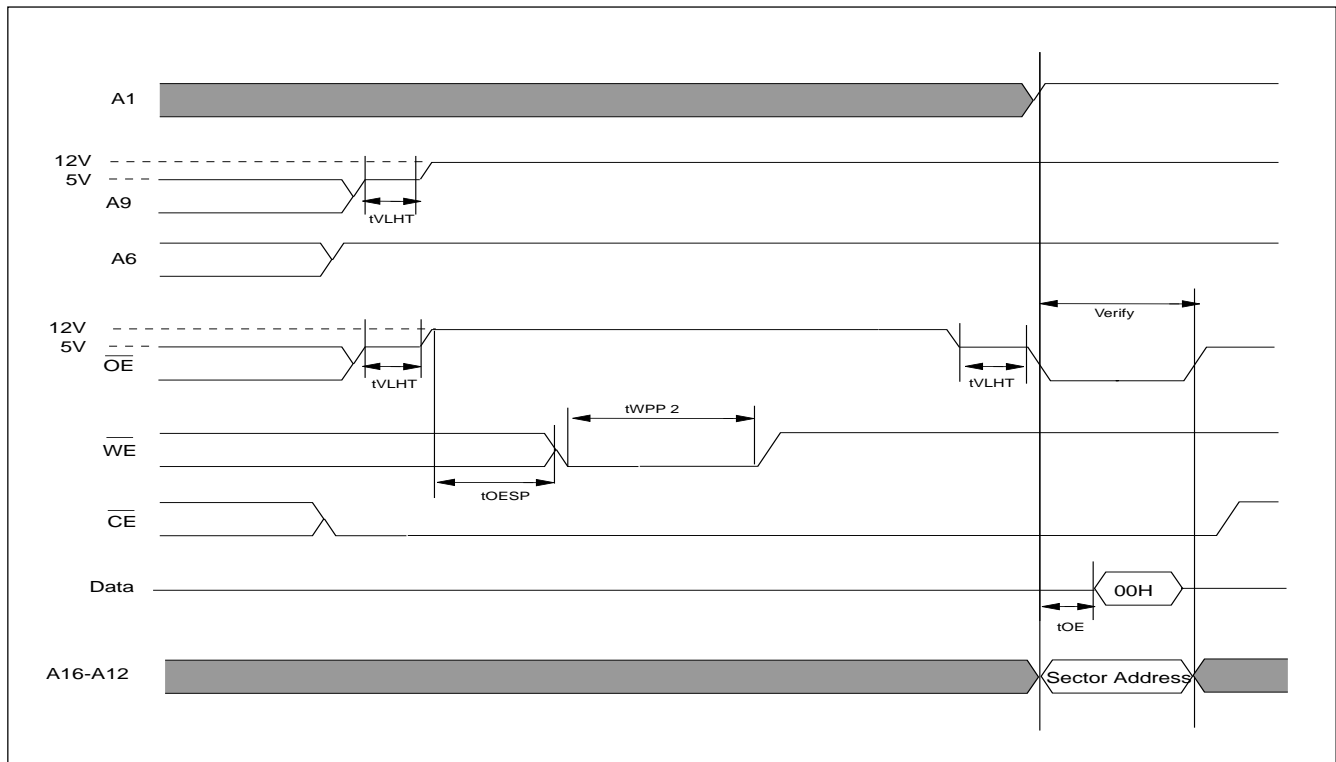


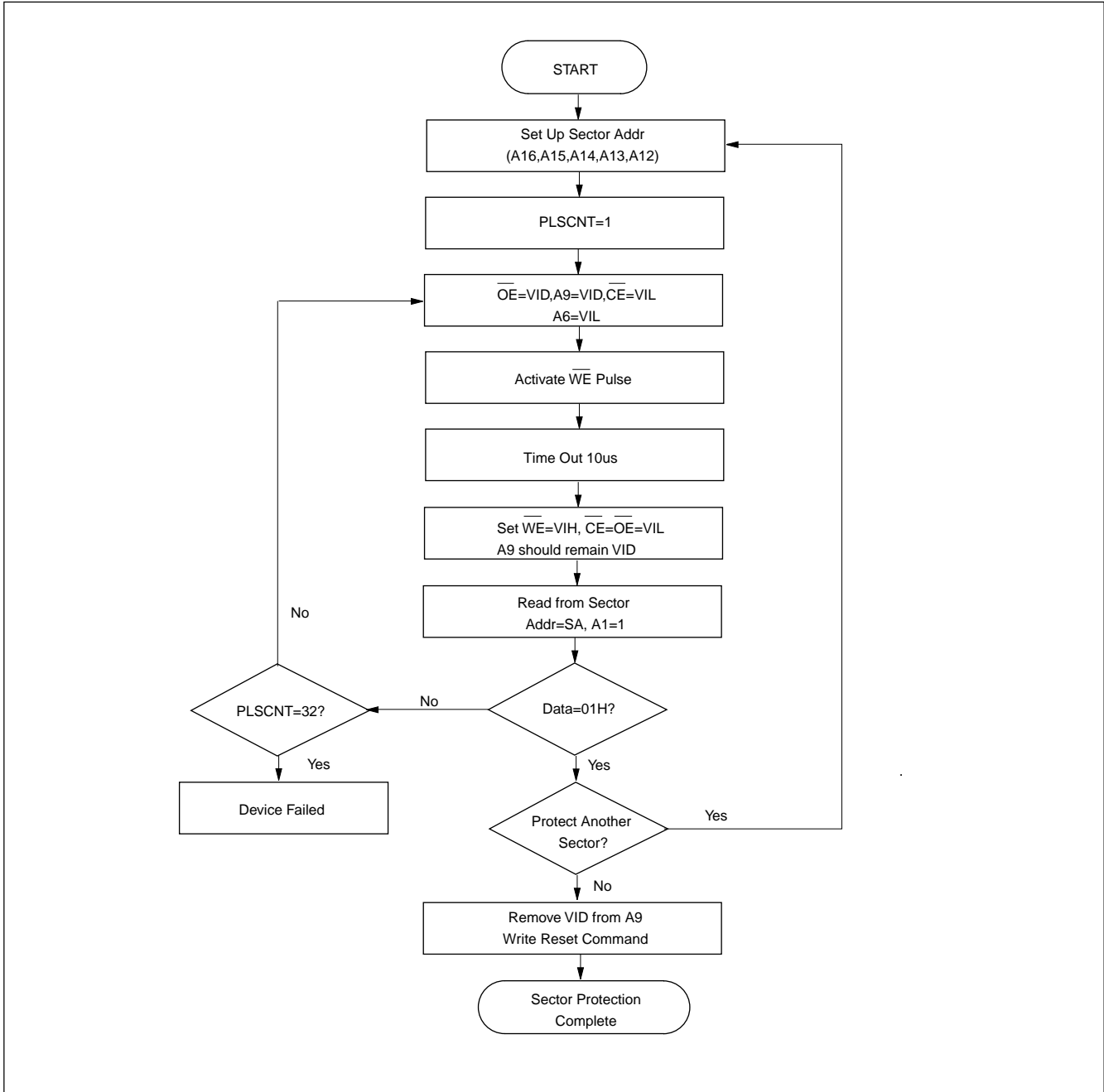
**AUTOMATIC SECTOR ERASE ALGORITHM FLOWCHART**


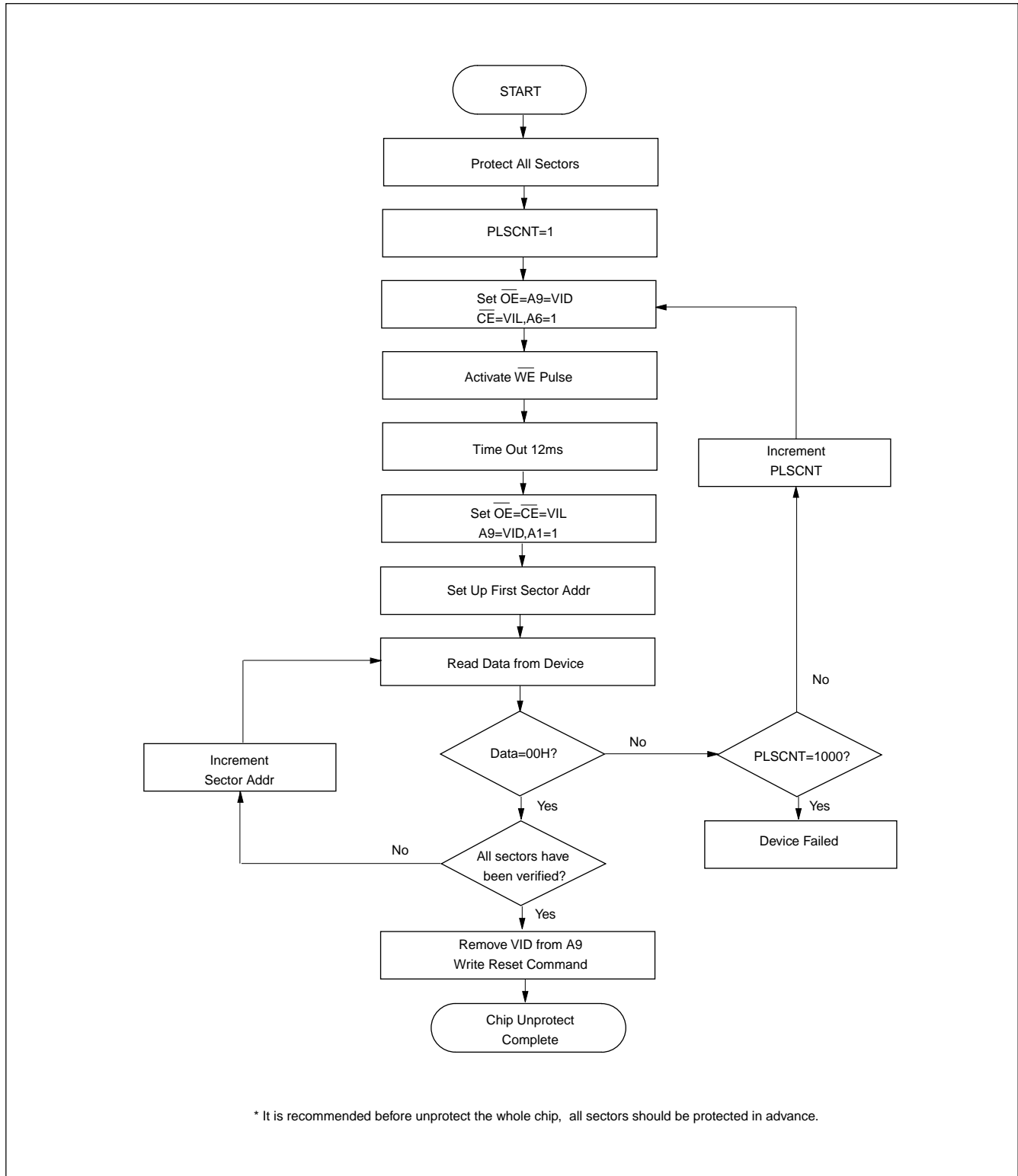
ERASE SUSPEND/ERASE RESUME FLOWCHART



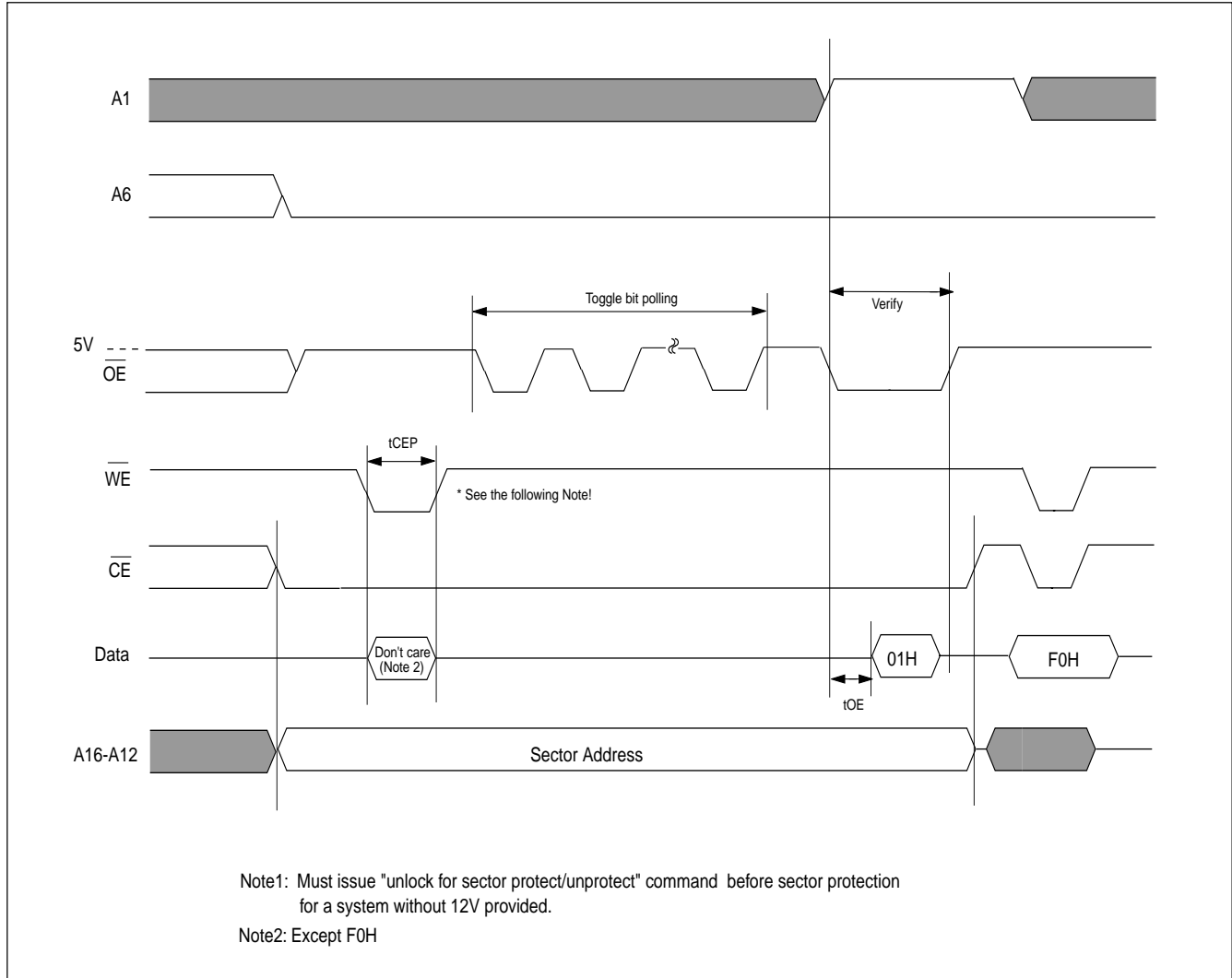


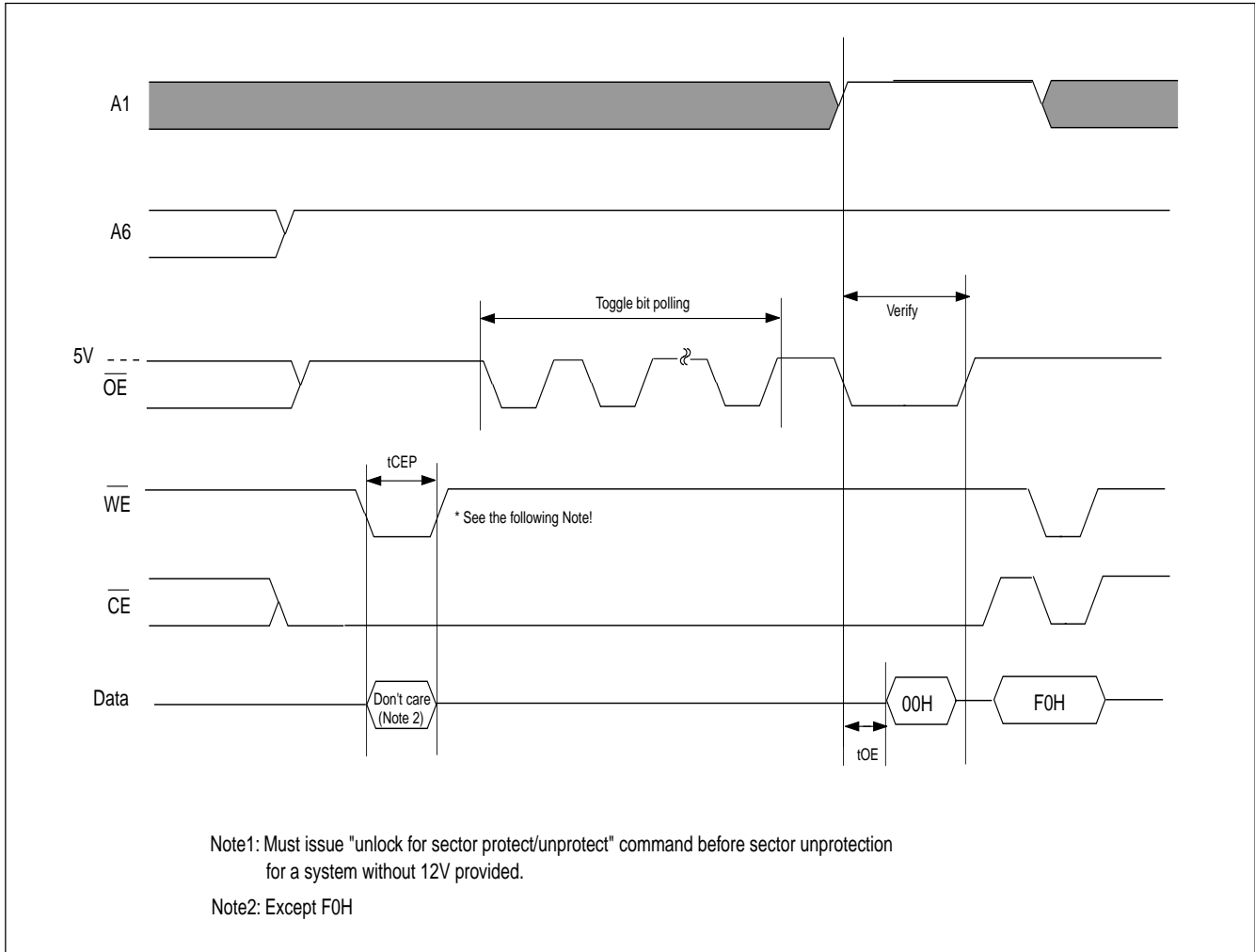
**TIMING WAVEFORM FOR SECTOR PROTECTION FOR SYSTEM WITH 12V**

**TIMING WAVEFORM FOR CHIP UNPROTECTION FOR SYSTEM WITH 12V**


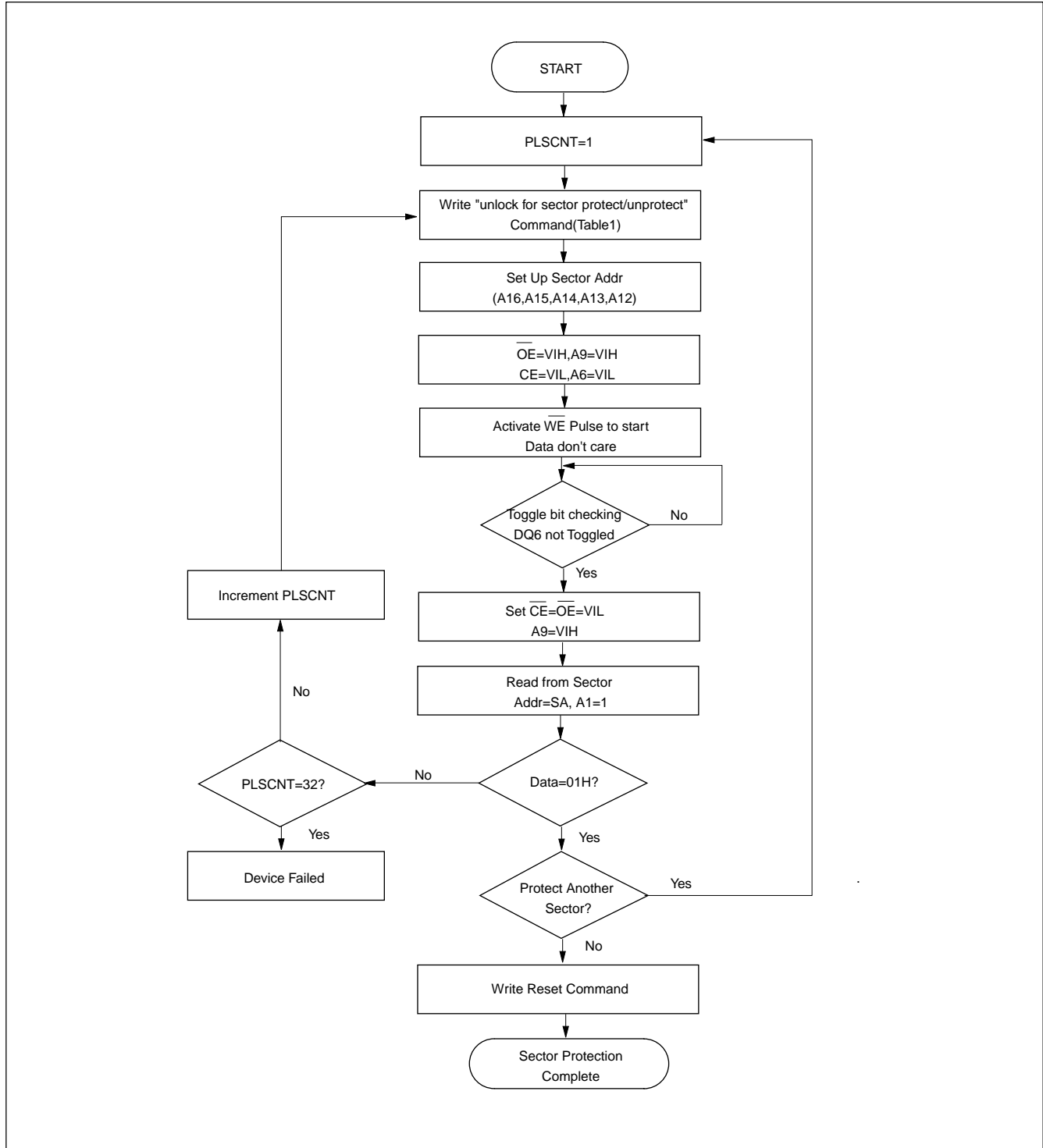
**SECTOR PROTECTION ALGORITHM FOR SYSTEM WITH 12V**


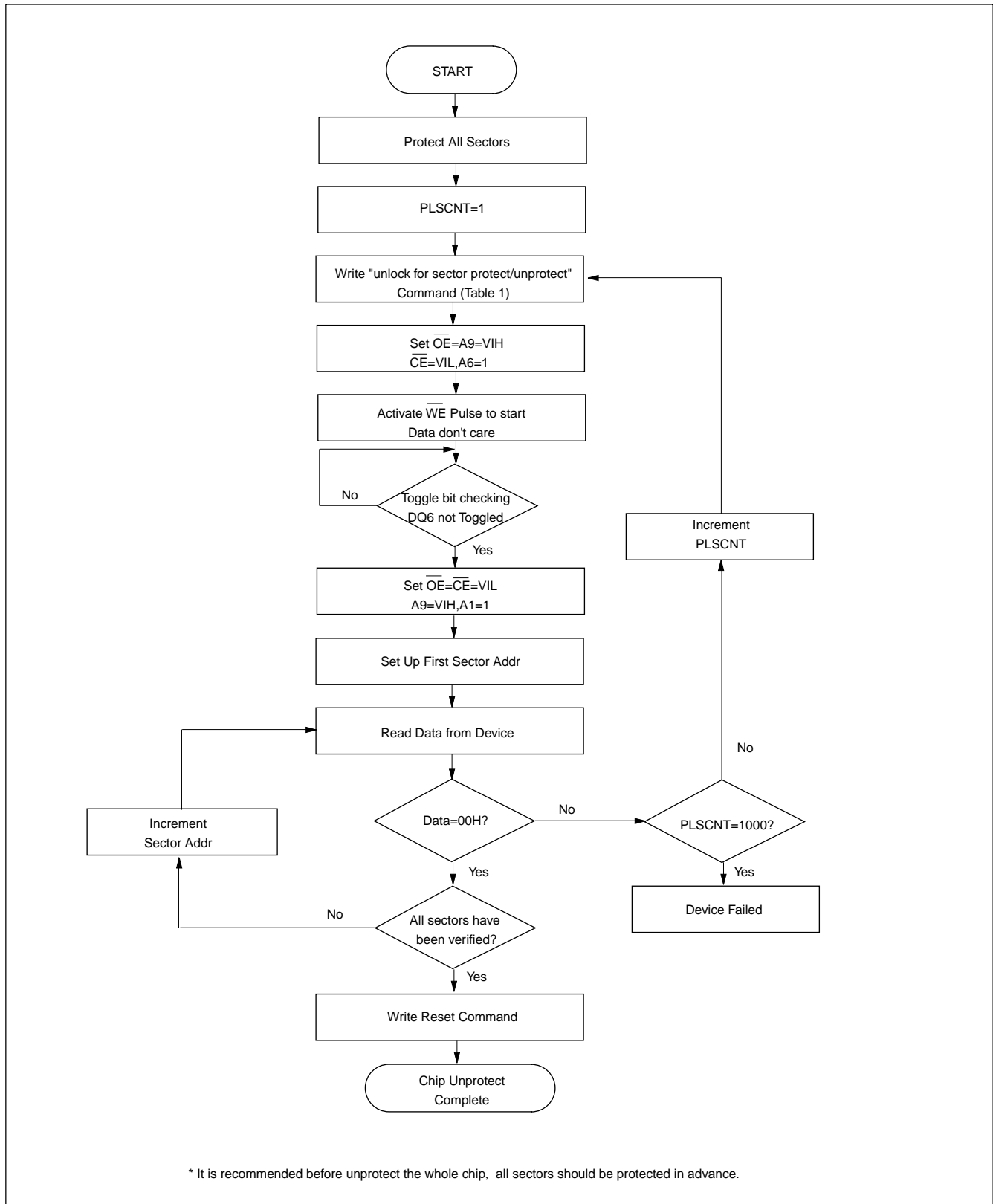
**CHIP UNPROTECTION ALGORITHM FOR SYSTEM WITH 12V**


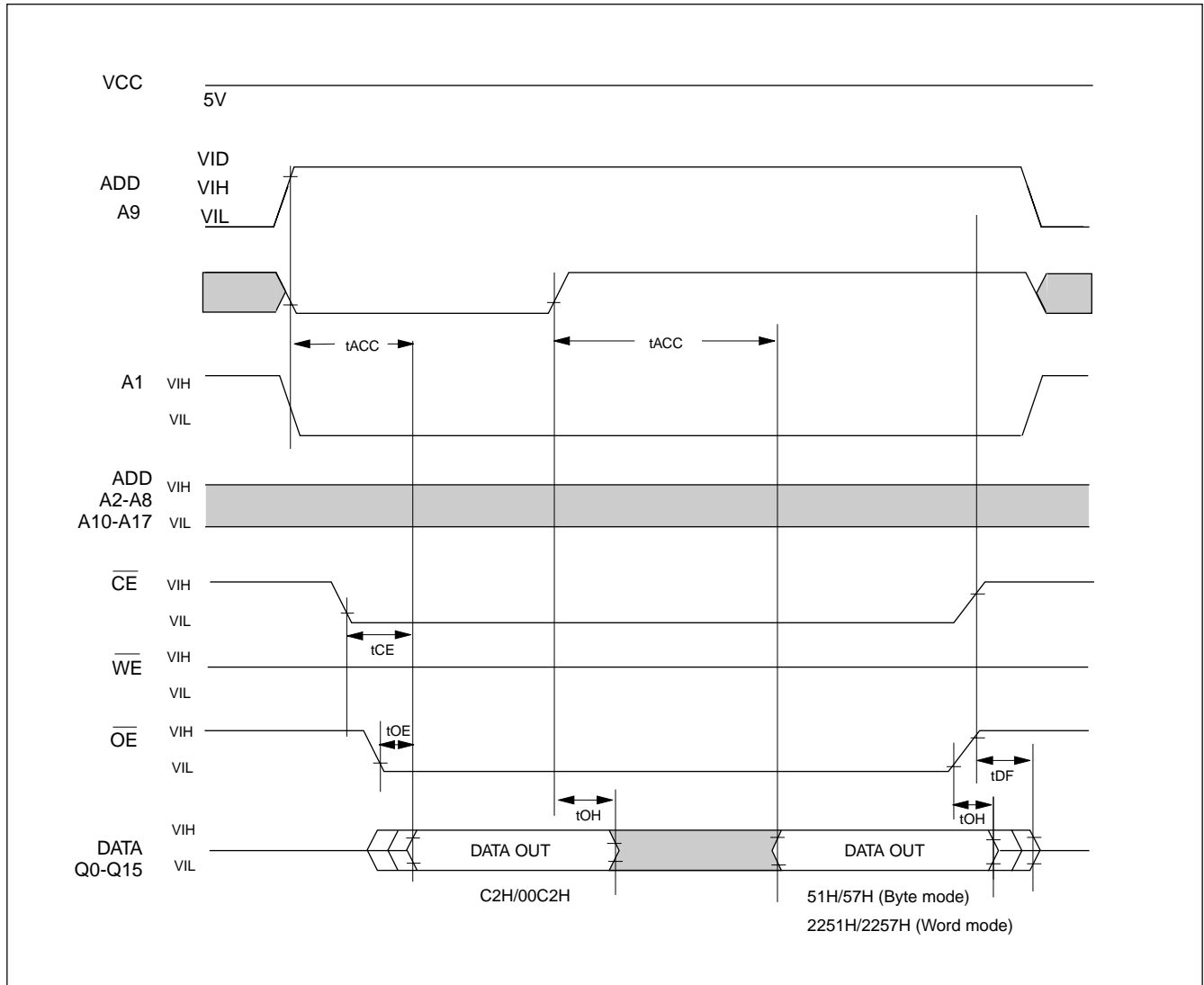
\* It is recommended before unprotect the whole chip, all sectors should be protected in advance.

**TIMING WAVEFORM FOR SECTOR PROTECTION FOR SYSTEM WITHOUT 12V**


**TIMING WAVEFORM FOR CHIP UNPROTECTION FOR SYSTEM WITHOUT 12V**


**SECTOR PROTECTION ALGORITHM FOR SYSTEM WITHOUT 12V**


**SECTOR UNPROTECTION ALGORITHM FOR SYSTEM WITHOUT 12V**


**ID CODE READ TIMING WAVEFORM**




**ERASE AND PROGRAMMING PERFORMANCE(1)**

PARAMETER	LIMITS			UNITS
	MIN.	TYP.(2)	MAX.(3)	
Sector Erase Time		1	8	s
Chip Erase Time		3	24	s
Byte Programming Time		7	210	us
Word Programming Time		12	360	us
Chip Programming Time		3.5	10.5	sec
Erase/Program Cycles	100,000			Cycles

Note: 1.Not 100% Tested, Excludes external system level over head.  
2.Typical values measured at 25°C,5V.  
3.Maximum values measured at 25°C,4.5V.

**LATCHUP CHARACTERISTICS**

	MIN.	MAX.
Input Voltage with respect to GND on all pins except I/O pins	-1.0V	13.5V
Input Voltage with respect to GND on all I/O pins	-1.0V	Vcc + 1.0V
Current	-100mA	+100mA
Includes all pins except Vcc. Test conditions: Vcc = 5.0V, one pin at a time.		

**DATA RETENTION**

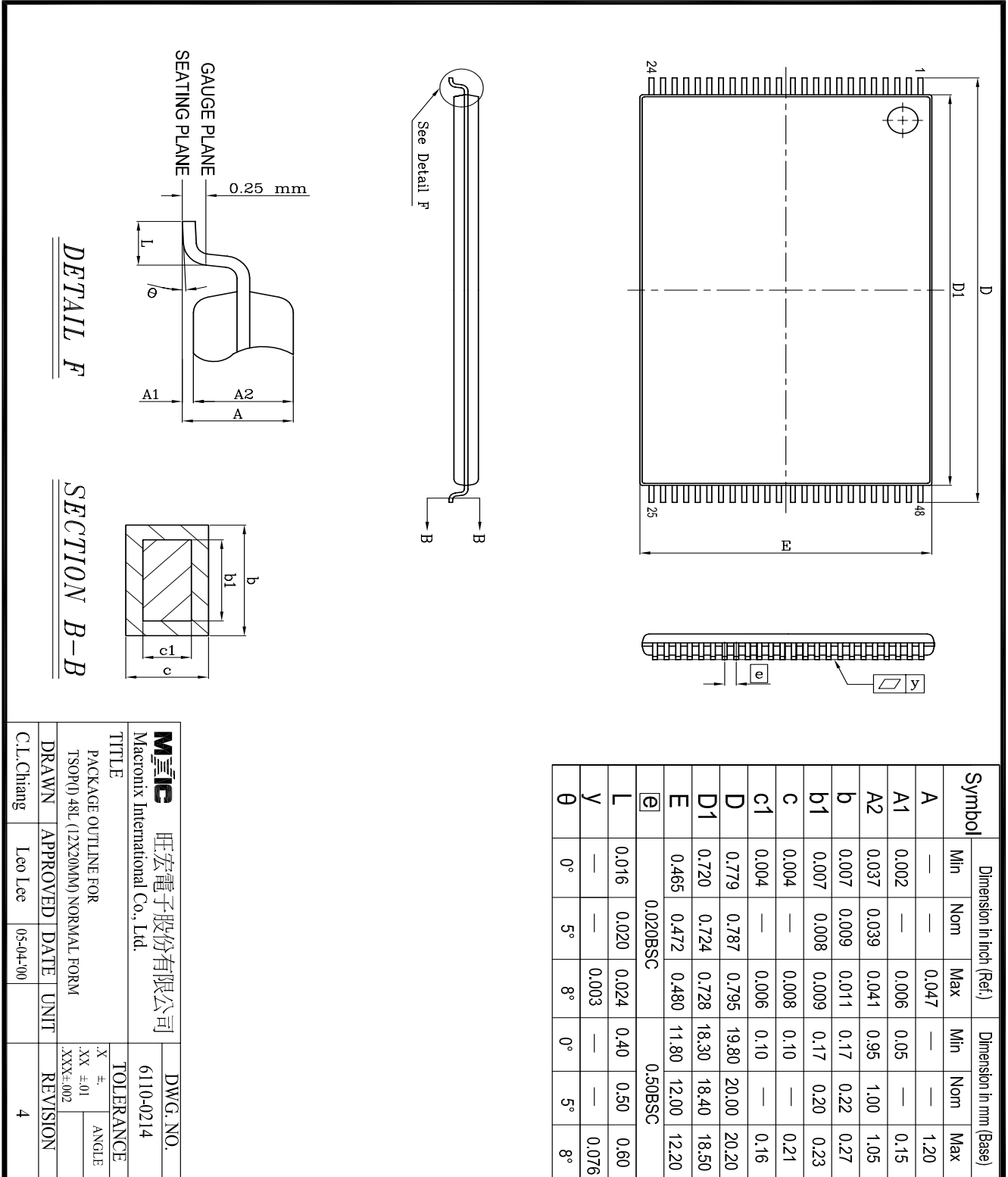
PARAMETER	MIN.	UNIT
Data Retention Time	20	Years

**ORDERING INFORMATION**
**PLASTIC PACKAGE**

PART NO.	Access Time (ns)	Operating Current (mA)	Standby Current MAX.( $\mu$ A)	Temperature Range	PACKAGE
MX29F200TMC-55	55	40	5	0°C~70°C	44 Pin SOP
MX29F200TMC-70	70	40	5	0°C~70°C	44 Pin SOP
MX29F200TMC-90	90	40	5	0°C~70°C	44 Pin SOP
MX29F200TMC-12	120	40	5	0°C~70°C	44 Pin SOP
MX29F200TTC-55	55	40	5	0°C~70°C	48 Pin TSOP (Normal Type)
MX29F200TTC-70	70	40	5	0°C~70°C	48 Pin TSOP (Normal Type)
MX29F200TTC-90	90	40	5	0°C~70°C	48 Pin TSOP (Normal Type)
MX29F200TTC-12	120	40	5	0°C~70°C	48 Pin TSOP (Normal Type)
MX29F200BMC-55	55	40	5	0°C~70°C	44 Pin SOP
MX29F200BMC-70	70	40	5	0°C~70°C	44 Pin SOP
MX29F200BMC-90	90	40	5	0°C~70°C	44 Pin SOP
MX29F200BMC-12	120	40	5	0°C~70°C	44 Pin SOP
MX29F200BTC-55	55	40	5	0°C~70°C	48 Pin TSOP (Normal Type)
MX29F200BTC-70	70	40	5	0°C~70°C	48 Pin TSOP (Normal Type)
MX29F200BTC-90	90	40	5	0°C~70°C	48 Pin TSOP (Normal Type)
MX29F200BTC-12	120	40	5	0°C~70°C	48 Pin TSOP (Normal Type)
MX29F200TMI-70	70	45	5	-40°C~85°C	44 Pin SOP
MX29F200TMI-90	90	45	5	-40°C~85°C	44 Pin SOP
MX29F200TMI-12	120	45	5	-40°C~85°C	44 Pin SOP
MX29F200TTI-70	70	45	5	-40°C~85°C	48 Pin TSOP (Normal Type)
MX29F200TTI-90	90	45	5	-40°C~85°C	48 Pin TSOP (Normal Type)
MX29F200TTI-12	120	45	5	-40°C~85°C	48 Pin TSOP (Normal Type)
MX29F200BMI-70	70	45	5	-40°C~85°C	44 Pin SOP
MX29F200BMI-90	90	45	5	-40°C~85°C	44 Pin SOP
MX29F200BMI-12	120	45	5	-40°C~85°C	44 Pin SOP
MX29F200BTI-70	70	45	5	-40°C~85°C	48 Pin TSOP (Normal Type)
MX29F200BTI-90	90	45	5	-40°C~85°C	48 Pin TSOP (Normal Type)
MX29F200BTI-12	120	45	5	-40°C~85°C	48 Pin TSOP (Normal Type)
MX29F200TTA-90	90	45	20	-40°C~125°C	48 Pin TSOP (Normal Type)
MX29F200TTA-12	120	45	20	-40°C~125°C	48 Pin TSOP (Normal Type)

## PACKAGE INFORMATION

### 48-PIN PLASTIC TSOP



**DETAIL F**

**SECTION B-B**

<b>Mxic</b> 旺宏電子股份有限公司 Macronix International Co., Ltd.		DWG. NO. 6110-0214	
TITLE PACKAGE OUTLINE FOR TSOP(0) 48L (12X20MM) NORMAL FORM			
DRAWN	APPROVED	DATE	UNIT
C.L.Chang	Leo Lee	05-04-00	
TOLERANCE		REVISION	
.X ±0.1		4	
.XX ±0.01			
.XXX ±0.002			

## 44-PIN PLASTIC SOP

Symbol	Dimension in mm (Base)			Dimension in Inch (Ref.)		
	Min	Nom	Max	Min	Nom	Max
A	—	—	3.00	—	—	0.118
A1	0.10	—	—	0.004	—	—
A2	2.57	2.69	2.82	0.101	0.106	0.111
b	—	0.41 REF	—	—	0.016 REF	—
C	—	0.20 REF	—	—	0.008 REF	—
D	28.37	28.50	28.63	1.117	1.122	1.127
E	15.77	16.03	16.28	0.621	0.631	0.641
E1	12.47	12.60	12.73	0.491	0.496	0.501
e	—	1.27 REF	—	—	0.050 REF	—
L	0.58	0.79	0.99	0.023	0.031	0.039
$\theta$	—	5°	—	—	5°	—

REFERENCE DOCUMENT: JEDEC SPEC MO-175

<b>Mxic</b> 旺宏電子股份有限公司 Macronix International Co., Ltd.		DWG. NO. 61110-0207	
TITLE PACKAGE OUTLINE FOR SOP 44L (500 MIL)		TOLERANCE XX ±.01 .XXX±.002	
DRAWN C.L.Chang	APPROVED Rick Chiu	DATE 11-08-01	UNIT INCH
REVISION 3			

**REVISION HISTORY**

<b>Revision</b>	<b>Description</b>	<b>Page</b>	<b>Date</b>
1.0	1.To remove "Advanced Information" datasheet marking and contain information on products in full production 2.The modification summary of Revision 0.9.9 to Revision 1.0: 2-1.Program/erase cycle times:10K cycles-->100K cycles 2-2.To add data retention 20 years 2-3.Industrial grade range from "Read Mode" to "Full Range" 2-4.To remove A9 from "timing waveform for sector protection for system without 12V" To remove A9 from "timing waveform for chip unprotection for system without 12V"	P1  P1,42 P1,42 P20,21,22,40 P35 P36	DEC/20/1999
1.1	To modify "Package Information"	P42,43	JUN/15/2001
1.2	Add automotive Grade	P18,19,21,41	NOV/12/2001
1.3	Correct sector address SA2 from 11XXX to 10XXX	P3	DEC/24/2001



**MX29F200T/B**

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