M95040
M95020 M95010

4 Kbit, 2 Kbit and 1 Kbit Serial SPI bus EEPROM with high speed Clock

Feature summary

- Compatible with SPI bus serial interface (Positive Clock SPI Modes)
- Single supply voltage:
  - 4.5 V to 5.5 V for M950x0
  - 2.5 V to 5.5 V for M950x0-W
  - 1.8 V to 5.5 V for M950x0-R
- High Speed
  - 10 MHz Clock rate, 5 ms Write time
- Status Register
- Byte and Page Write (up to 16 bytes)
- Self-timed programming cycle
- Adjustable size read-only EEPROM area
- Enhanced ESD Protection
- More than 1 Million Write cycles
- More than 40-year data retention
- Packages
  - ECOPACK® (RoHS compliant)

SO8 (MN)
150 mil width

TSSOP8 (DW)
169 mil width

UFDFPN8 (MB)
2 × 3mm

Table 1. Product list

Reference	Part Number
M95040	M95040
	M95040-W
	M95040-R
M95020	M95020
	M95020-W
	M95020-R
M95010	M95010
	M95010-W
	M95010-R

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1 Summary description

The M95040 is a 4 Kbit (512 x 8) electrically erasable programmable memory (EEPROM), accessed by a high speed SPI-compatible bus. The other members of the family (M95020 and M95010) are identical, though proportionally smaller (2 and 1 Kbit, respectively).

Each device is accessed by a simple serial interface that is SPI-compatible. The bus signals are C, D and Q, as shown in *Table 2* and *Figure 1*.

The device is selected when Chip Select ($\overline{S}$) is taken Low. Communications with the device can be interrupted using Hold ($\overline{HOLD}$). WRITE instructions are disabled by Write Protect ($\overline{W}$).

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages.
ECOPACK® packages are Lead-free and RoHS compliant.

ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*.

Figure 1. Logic diagram

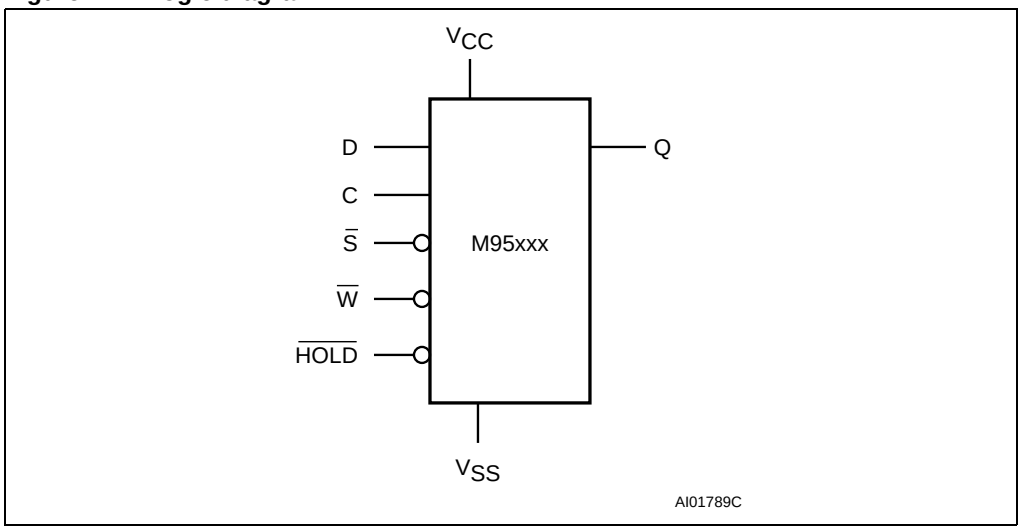
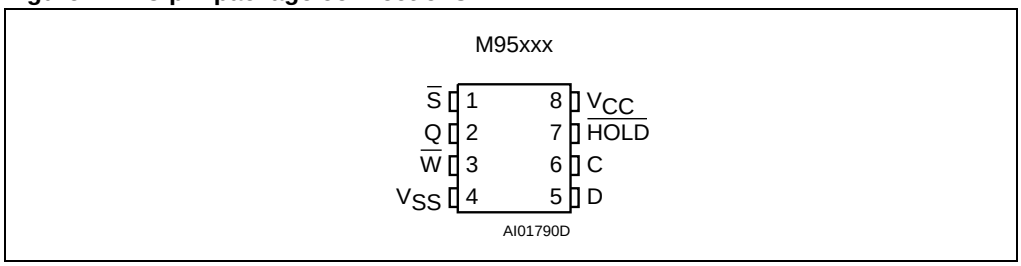


Figure 2. 8-pin package connections



1. See *Section 10: Package mechanical* for package dimensions, and how to identify pin-1.

Table 2. Signal names

C	Serial Clock
D	Serial Data Input
Q	Serial Data Output
$\overline{S}$	Chip Select
$\overline{W}$	Write Protect
$\overline{HOLD}$	Hold
V_{CC}	Supply Voltage
V_{SS}	Ground

2 Signal description

During all operations, V_{CC} must be held stable and within the specified valid range: V_{CC}(min) to V_{CC}(max).

All of the input and output signals can be held High or Low (according to voltages of V_{IH}, V_{OH}, V_{IL} or V_{OL}, as specified in *Table 13* to *Table 17*). These signals are described next.

2.1 Serial Data Output (Q)

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of Serial Clock (C).

2.2 Serial Data Input (D)

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and the data to be written. Values are latched on the rising edge of Serial Clock (C).

2.3 Serial Clock (C)

This input signal provides the timing of the serial interface. Instructions, addresses, or data present at Serial Data Input (D) are latched on the rising edge of Serial Clock (C). Data on Serial Data Output (Q) changes after the falling edge of Serial Clock (C).

2.4 Chip Select ($\overline{S}$)

When this input signal is High, the device is deselected and Serial Data Output (Q) is at high impedance. Unless an internal Write cycle is in progress, the device will be in the Standby Power mode. Driving Chip Select ($\overline{S}$) Low selects the device, placing it in the Active Power mode.

After Power-up, a falling edge on Chip Select ($\overline{S}$) is required prior to the start of any instruction.

2.5 Hold ($\overline{HOLD}$)

The Hold ($\overline{HOLD}$) signal is used to pause any serial communications with the device without deselecting the device.

During the Hold condition, the Serial Data Output (Q) is high impedance, and Serial Data Input (D) and Serial Clock (C) are Don't Care.

To start the Hold condition, the device must be selected, with Chip Select ($\overline{S}$) driven Low.

2.6 Write Protect ($\overline{W}$)

This input signal is used to control whether the memory is write protected. When Write Protect ($\overline{W}$) is held Low, writes to the memory are disabled, but other operations remain enabled. Write Protect ($\overline{W}$) must either be driven High or Low, but must not be left floating.

2.7 V_{SS} ground

V_{SS} is the reference for the V_{CC} supply voltage.

2.8 Supply voltage (V_{CC})

V_{CC} is the supply voltage.

2.8.1 Operating supply voltage V_{CC}

Prior to selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range must be applied (see *Table 8*, *Table 9* and *Table 10*). In order to secure a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually of the order of 10nF to 100nF) close to the V_{CC}/V_{SS} package pins.

This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal write cycle (t_W).

2.8.2 Power-up conditions

When the power supply is turned on, V_{CC} rises from V_{SS} to V_{CC}. During this time, the Chip Select ($\overline{S}$) signal is not allowed to float and must follow the V_{CC} voltage. The $\overline{S}$ line should therefore be connected to V_{CC} via a suitable pull-up resistor.

In addition, the Chip Select ($\overline{S}$) input offers a built-in safety feature, as it is both edge sensitive and level sensitive. Practically this means that after power-up, the device cannot become selected until a falling edge has first been detected on Chip Select ($\overline{S}$). So the Chip Select ($\overline{S}$) signal must first have been High, and then gone Low before the first operation can be started.

2.8.3 Internal device reset

In order to prevent inadvertent Write operations during Power-up, a Power On Reset (POR) circuit is included. At Power-up (continuous rise of V_{CC}), the device will not respond to any instruction until V_{CC} has reached the Power On Reset threshold voltage (this threshold is lower than the minimum V_{CC} operating voltage defined in *Section 9: DC and AC parameters*).

When V_{CC} has passed the POR threshold voltage, the device is reset and in the following state:

- in Standby Power mode
- deselected (at next Power-up, a falling edge is required on Chip Select ($\overline{S}$) before any instruction can be executed)
- not in the Hold Condition Status register state:
  - the Write Enable Latch (WEL) is reset to 0
  - the Write In Progress (WIP) is reset to 0. The SRWD, BP1 and BP0 bits of the Status Register are at the same logic level as when the device was last powered down (they are non-volatile bits)

2.8.4 Power-down

At Power-down (continuous decrease of V_{CC}), as soon as V_{CC} drops from the normal operating voltage to below the Power On Reset threshold voltage, the device stops responding to any instruction sent to it.

At Power-down, the device must be deselected and in Standby Power mode (that is there should be no internal Write cycle in progress). Chip Select ($\overline{S}$) should be allowed to follow the voltage applied on V_{CC}.

3 Connecting to the SPI bus

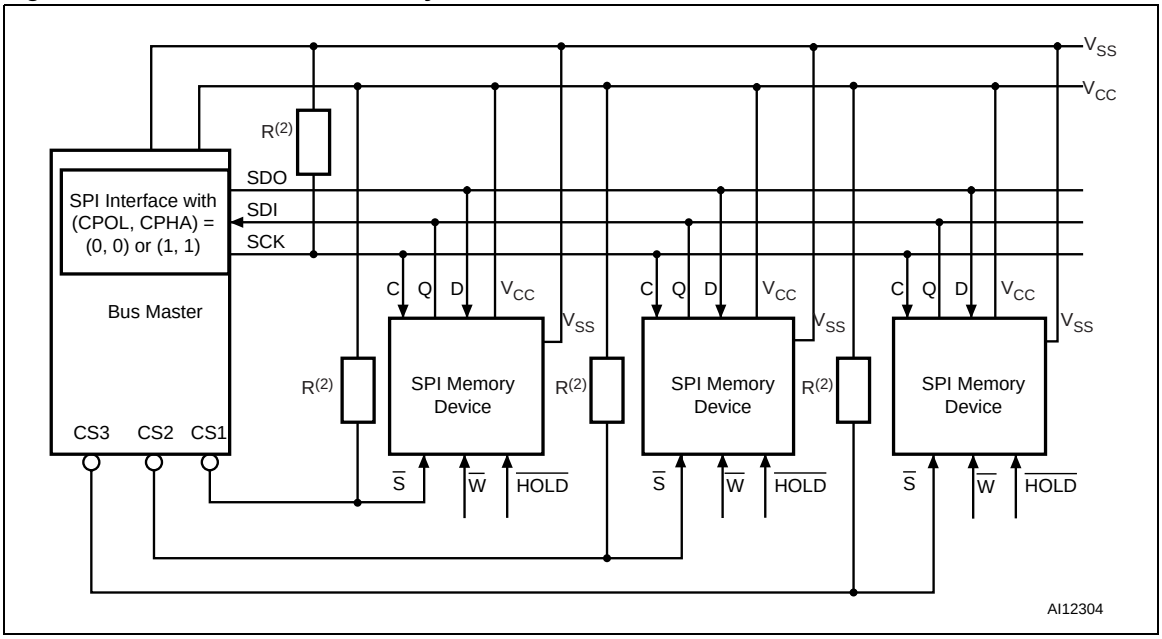
These devices are fully compatible with the SPI protocol.

All instructions, addresses and input data bytes are shifted in to the device, most significant bit first. The Serial Data Input (D) is sampled on the first rising edge of the Serial Clock (C) after Chip Select ($\overline{S}$) goes Low.

All output data bytes are shifted out of the device, most significant bit first. The Serial Data Output (Q) is latched on the first falling edge of the Serial Clock (C) after the instruction (such as the Read from Memory Array and Read Status Register instructions) have been clocked into the device.

Figure 3 shows three devices, connected to an MCU, on a SPI bus. Only one device is selected at a time, so only one device drives the Serial Data Output (Q) line at a time, all the others being high impedance.

Figure 3. Bus master and memory devices on the SPI bus



1. The Write Protect ($\overline{W}$) and Hold ($\overline{HOLD}$) signals should be driven, High or Low as appropriate.
2. These pull-up resistors, R, ensure that the M950x0 are not selected if the Bus Master leaves the $\overline{S}$ line in the high-impedance state. As the Bus Master may enter a state where all inputs/outputs are in high impedance at the same time (that is when the Bus Master is reset), the clock line (C) must be connected to an external pull-down resistor so that, when all inputs/outputs become high impedance, $\overline{S}$ is pulled High while C is pulled Low (thus ensuring that $\overline{S}$ and C do not become High at the same time, and so, that the t_{SHCH} requirement is met).

3.1 SPI modes

These devices can be driven by a microcontroller with its SPI peripheral running in either of the two following modes:

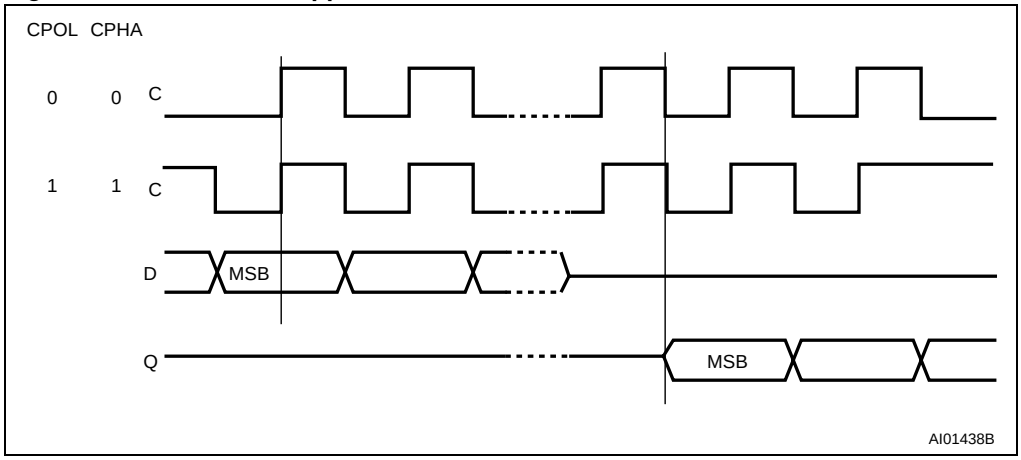
- CPOL=0, CPHA=0
- CPOL=1, CPHA=1

For these two modes, input data is latched in on the rising edge of Serial Clock (C), and output data is available from the falling edge of Serial Clock (C).

The difference between the two modes, as shown in *Figure 4*, is the clock polarity when the bus master is in Stand-by mode and not transferring data:

- C remains at 0 for (CPOL=0, CPHA=0)
- C remains at 1 for (CPOL=1, CPHA=1)

Figure 4. SPI modes supported



4 Operating features

4.1 Hold Condition

The Hold ($\overline{HOLD}$) signal is used to pause any serial communications with the device without resetting the clocking sequence.

During the Hold condition, the Serial Data Output (Q) is high impedance, and Serial Data Input (D) and Serial Clock (C) are Don't Care.

To enter the Hold condition, the device must be selected, with Chip Select ($\overline{S}$) Low.

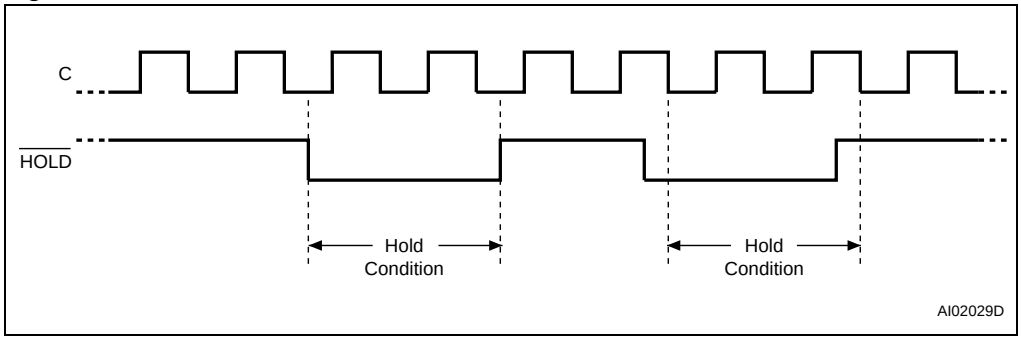
Normally, the device is kept selected, for the whole duration of the Hold condition. Deselecting the device while it is in the Hold condition, has the effect of resetting the state of the device, and this mechanism can be used if it is required to reset any processes that had been in progress.

The Hold condition starts when the Hold ($\overline{HOLD}$) signal is driven Low at the same time as Serial Clock (C) already being Low (as shown in *Figure 5*).

The Hold condition ends when the Hold ($\overline{HOLD}$) signal is driven High at the same time as Serial Clock (C) already being Low.

Figure 5 also shows what happens if the rising and falling edges are not timed to coincide with Serial Clock (C) being Low.

Figure 5. Hold Condition activation



4.2 Status Register

Figure 6 shows the position of the Status Register in the control logic of the device. This register contains a number of control bits and status bits, as shown in *Table 5*. For a detailed description of the Status Register bits, see *Section 6.3: Read Status Register (RDSR)*.

4.3 Data Protection and Protocol control

To help protect the device from data corruption in noisy or poorly controlled environments, a number of safety features have been built in to the device. The main security measures can be summarized as follows:

- The WEL bit is reset at power-up.
- Chip Select ($\overline{S}$) must rise after the eighth clock count (or multiple thereof) in order to start a non-volatile Write cycle (in the memory array or in the Status Register).
- Accesses to the memory array are ignored during the non-volatile programming cycle, and the programming cycle continues unaffected.
- Invalid Chip Select ($\overline{S}$) and Hold ($\overline{HOLD}$) transitions are ignored.

For any instruction to be accepted and executed, Chip Select ($\overline{S}$) must be driven High after the rising edge of Serial Clock (C) that latches the last bit of the instruction, and before the next rising edge of Serial Clock (C).

For this, “the last bit of the instruction” can be the eighth bit of the instruction code, or the eighth bit of a data byte, depending on the instruction (except in the case of RDSR and READ instructions). Moreover, the "next rising edge of CLOCK" might (or might not) be the next bus transaction for some other device on the bus.

When a Write cycle is in progress, the device protects it against external interruption by ignoring any subsequent READ, WRITE or WRSR instruction until the present cycle is complete.

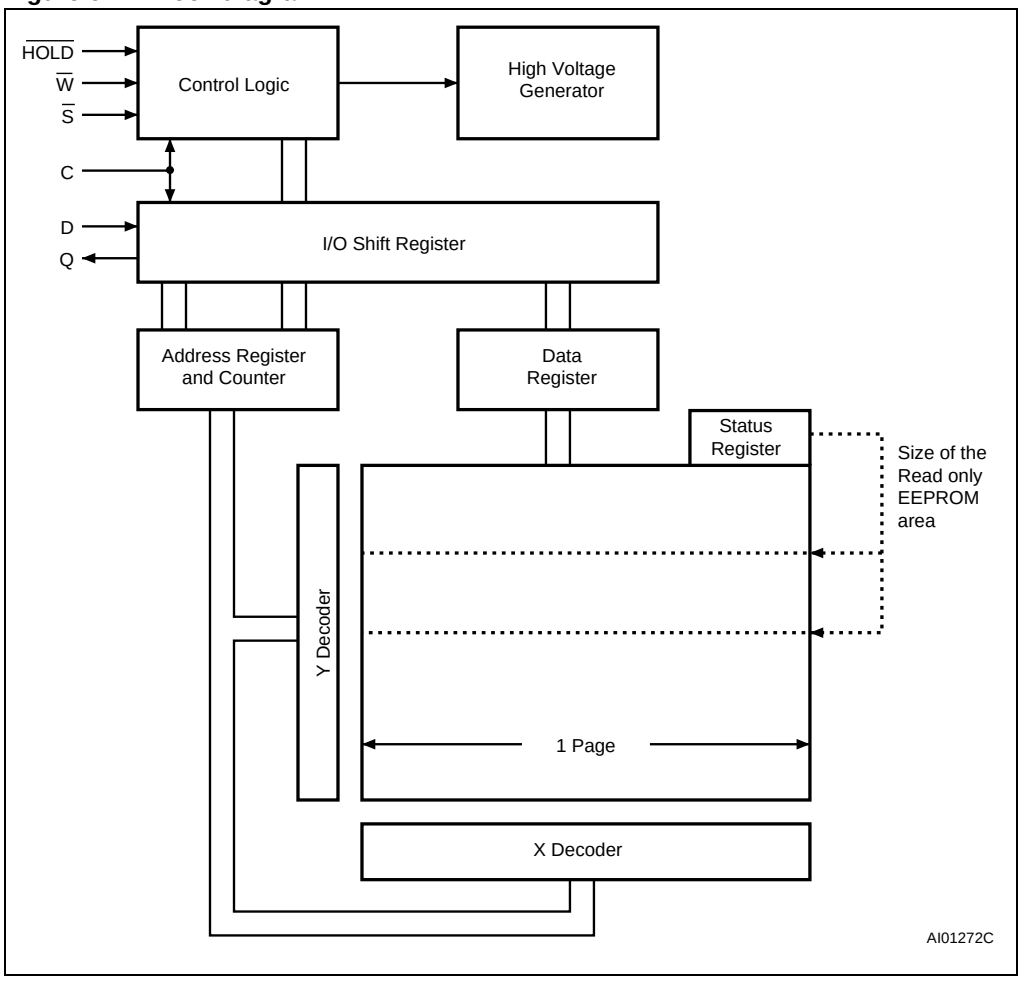
Table 3. Write-Protected block size

Status Register Bits		Protected Block	Array Addresses Protected		
BP1	BP0		M95040	M95020	M95010
0	0	none	none	none	none
0	1	Upper quarter	180h - 1FFh	C0h - FFh	60h - 7Fh
1	0	Upper half	100h - 1FFh	80h - FFh	40h - 7Fh
1	1	Whole memory	000h - 1FFh	00h - FFh	00h - 7Fh

5 Memory organization

The memory is organized as shown in *Figure 6*.

Figure 6. Block diagram



6 Instructions

Each instruction starts with a single-byte code, as summarized in *Table 4*.

If an invalid instruction is sent (one not contained in *Table 4*), the device automatically deselects itself.

Table 4. Instruction set

Instruction	Description	Instruction Format
WREN	Write Enable	0000 X110(1)
WRDI	Write Disable	0000 X100(1)
RDSR	Read Status Register	0000 X101(1)
WRSR	Write Status Register	0000 X001(1)
READ	Read from Memory Array	0000 $A_8$011(2)
WRITE	Write to Memory Array	0000 $A_8$010(2)

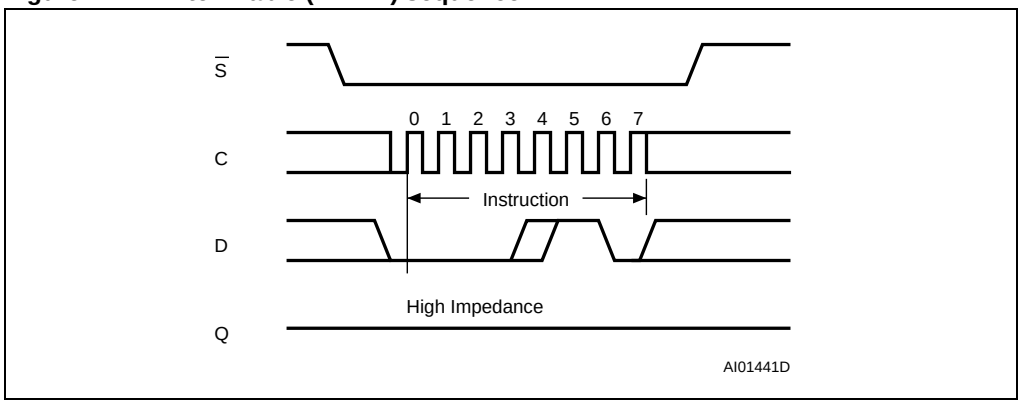
1. X = Don't Care.
2. A8 = 1 for the upper half of the memory array of the M95040, and 0 for the lower half, and is Don't Care for other devices.

6.1 Write Enable (WREN)

The Write Enable Latch (WEL) bit must be set prior to each WRITE and WRSR instruction. The only way to do this is to send a Write Enable instruction to the device.

As shown in *Figure 7*, to send this instruction to the device, Chip Select ($\overline{S}$) is driven Low, and the bits of the instruction byte are shifted in, on Serial Data Input (D). The device then enters a wait state. It waits for a the device to be deselected, by Chip Select ($\overline{S}$) being driven High.

Figure 7. Write Enable (WREN) sequence



6.2 Write Disable (WRDI)

One way of resetting the Write Enable Latch (WEL) bit is to send a Write Disable instruction to the device.

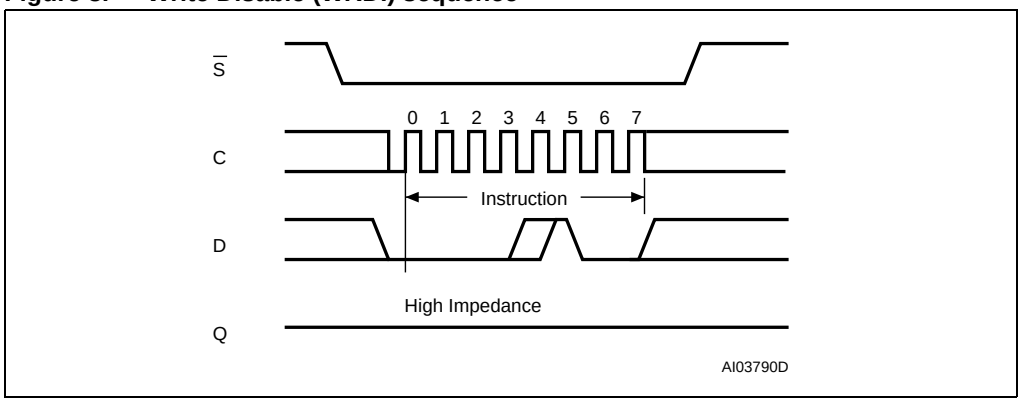
As shown in *Figure 8*, to send this instruction to the device, Chip Select ($\overline{S}$) is driven Low, and the bits of the instruction byte are shifted in, on Serial Data Input (D).

The device then enters a wait state. It waits for a the device to be deselected, by Chip Select ($\overline{S}$) being driven High.

The Write Enable Latch (WEL) bit, in fact, becomes reset by any of the following events:

- Power-up
- WRDI instruction execution
- WRSR instruction completion
- WRITE instruction completion
- Write Protect ($\overline{W}$) line being held Low.

Figure 8. Write Disable (WRDI) sequence



6.3 Read Status Register (RDSR)

One of the major uses of this instruction is to allow the MCU to poll the state of the Write In Progress (WIP) bit. This is needed because the device will not accept further WRITE or WRSR instructions when the previous Write cycle is not yet finished.

As shown in *Figure 9*, to send this instruction to the device, Chip Select ($\overline{S}$) is first driven Low. The bits of the instruction byte are then shifted in, on Serial Data Input (D). The current state of the bits in the Status Register is shifted out, on Serial Data Out (Q). The Read Cycle is terminated by driving Chip Select ($\overline{S}$) High.

The Status Register may be read at any time, even during a Write cycle (whether it be to the memory area or to the Status Register). All bits of the Status Register remain valid, and can be read using the RDSR instruction. However, during the current Write cycle, the values of the non-volatile bits (BP0, BP1) become frozen at a constant value. The updated value of these bits becomes available when a new RDSR instruction is executed, after completion of the Write cycle. On the other hand, the two read-only bits (Write Enable Latch (WEL), Write In Progress (WIP)) are dynamically updated during the on-going Write cycle.

Bits b7, b6, b5 and b4 are always read as 1. The status and control bits of the Status Register are as follows:

6.3.1 WIP bit

The Write In Progress (WIP) bit indicates whether the memory is busy with a Write or Write Status Register cycle. When set to 1, such a cycle is in progress, when reset to 0 no such cycle is in progress.

6.3.2 WEL bit

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write or Write Status Register instruction is accepted.

6.3.3 BP1, BP0 bits

The Block Protect (BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Write instructions. These bits are written with the Write Status Register (WRSR) instruction. When one or both of the Block Protect (BP1, BP0) bits is set to 1, the relevant memory area (as defined in *Table 3*) becomes protected against Write (WRITE) instructions. The Block Protect (BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set.

Table 5. Status Register format

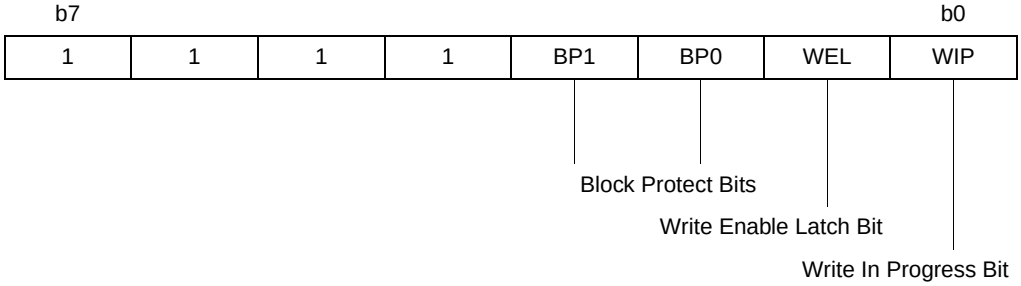
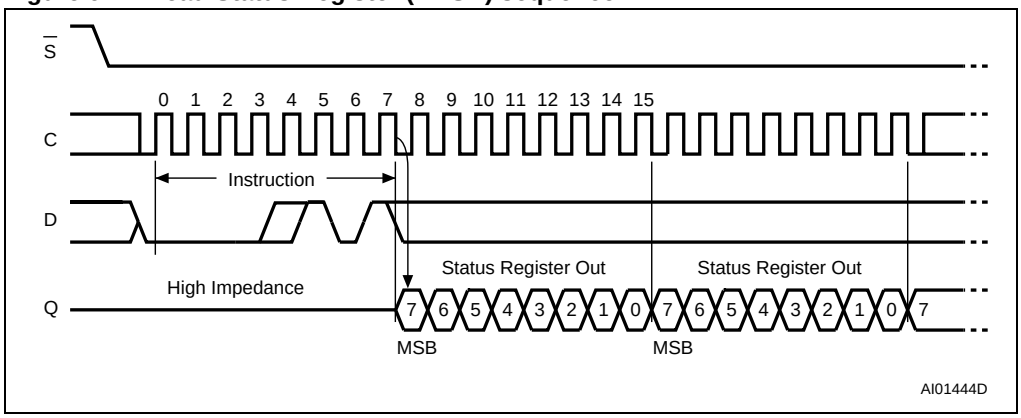


Figure 9. Read Status Register (RDSR) sequence



6.4 Write Status Register (WRSR)

This instruction has no effect on bits b7, b6, b5, b4, b1 and b0 of the Status Register.

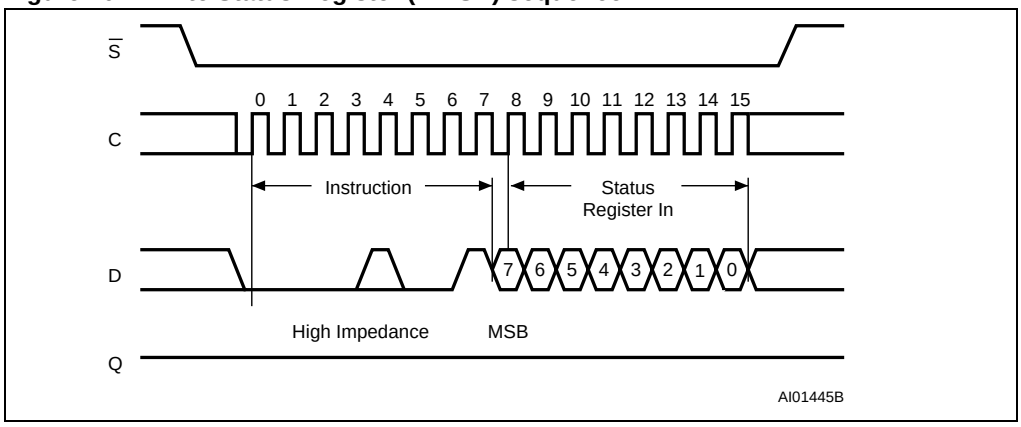
As shown in *Figure 10*, to send this instruction to the device, Chip Select ($\overline{S}$) is first driven Low. The bits of the instruction byte and data byte are then shifted in on Serial Data Input (D).

The instruction is terminated by driving Chip Select ($\overline{S}$) High. Chip Select ($\overline{S}$) must be driven High after the rising edge of Serial Clock (C) that latches the eighth bit of the data byte, and before the next rising edge of Serial Clock (C). If this condition is not met, the Write Status Register (WRSR) instruction is not executed. The self-timed Write Cycle starts, and continues for a period t_W (as specified in *Table 18* to *Table 22*), at the end of which the Write in Progress (WIP) bit is reset to 0.

The instruction is not accepted, and is not executed, under the following conditions:

- if the Write Enable Latch (WEL) bit has not been set to 1 (by executing a Write Enable instruction just before)
- if a Write Cycle is already in progress
- if the device has not been deselected, by Chip Select ($\overline{S}$) being driven High, after the eighth bit, b0, of the data byte has been latched in
- if Write Protect ($\overline{W}$) is Low.

Figure 10. Write Status Register (WRSR) sequence



6.5 Read from Memory Array (READ)

As shown in *Figure 11*, to send this instruction to the device, Chip Select ($\overline{S}$) is first driven Low. The bits of the instruction byte and address byte are then shifted in, on Serial Data Input (D). For the M95040, the most significant address bit, A8, is incorporated as bit b3 of the instruction byte, as shown in *Table 4*. The address is loaded into an internal address register, and the byte of data at that address is shifted out, on Serial Data Output (Q).

If Chip Select ($\overline{S}$) continues to be driven Low, an internal bit-pointer is automatically incremented at each clock cycle, and the corresponding data bit is shifted out.

When the highest address is reached, the address counter rolls over to zero, allowing the Read cycle to be continued indefinitely. The whole memory can, therefore, be read with a single READ instruction.

The Read cycle is terminated by driving Chip Select ($\overline{S}$) High. The rising edge of the Chip Select ($\overline{S}$) signal can occur at any time during the cycle.

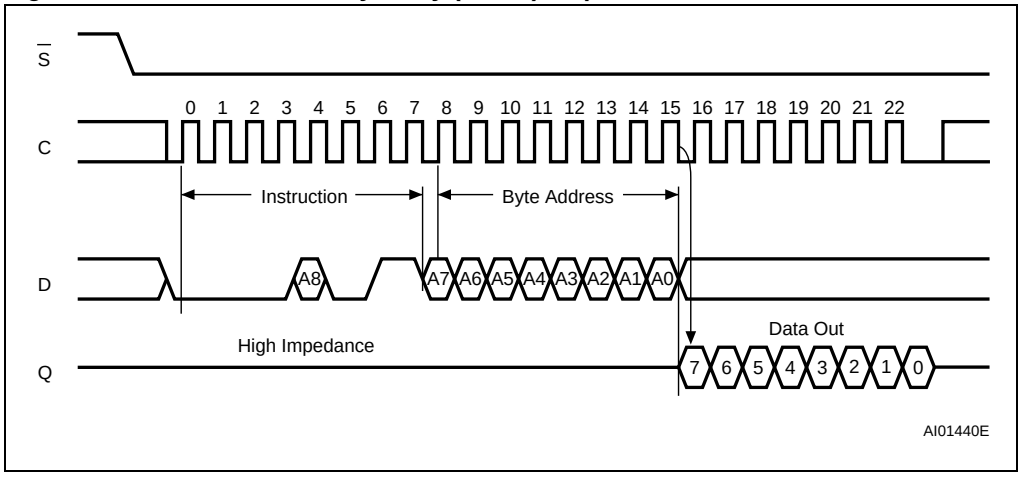
The first byte addressed can be any byte within any page.

The instruction is not accepted, and is not executed, if a Write cycle is currently in progress.

Table 6. Address range bits

Device	M95040	M95020	M95010
Address Bits	A8-A0	A7-A0	A6-A0

Figure 11. Read from Memory Array (READ) sequence



1. Depending on the memory size, as shown in *Table 6*, the most significant address bits are Don't Care.

6.6 Write to Memory Array (WRITE)

As shown in *Figure 12*, to send this instruction to the device, Chip Select ($\overline{S}$) is first driven Low. The bits of the instruction byte, address byte, and at least one data byte are then shifted in, on Serial Data Input (D).

The instruction is terminated by driving Chip Select ($\overline{S}$) High after the rising edge of Serial Clock (C) that latches the last data bit, and before the next rising edge of Serial Clock (C) occurs anywhere on the bus. In the case of *Figure 12*, this occurs after the eighth bit of the data byte has been latched in, indicating that the instruction is being used to write a single byte. The self-timed Write cycle starts, and continues for a period t_{WC} (as specified in *Table 18* to *Table 22*), at the end of which the Write in Progress (WIP) bit is reset to 0.

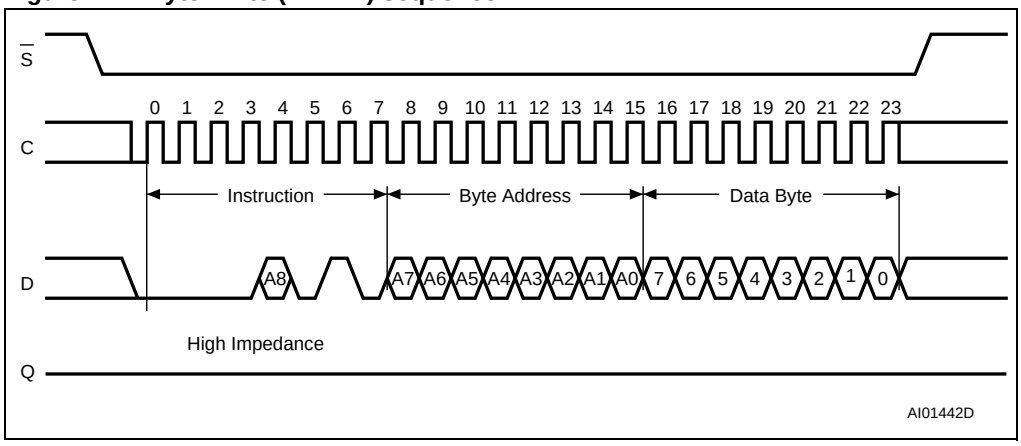
If, though, Chip Select ($\overline{S}$) continues to be driven Low, as shown in *Figure 13*, the next byte of input data is shifted in. In this way, all the bytes from the given address to the end of the same page can be programmed in a single instruction.

If Chip Select ($\overline{S}$) still continues to be driven Low, the next byte of input data is shifted in, and is used to overwrite the byte at the start of the current page.

The instruction is not accepted, and is not executed, under the following conditions:

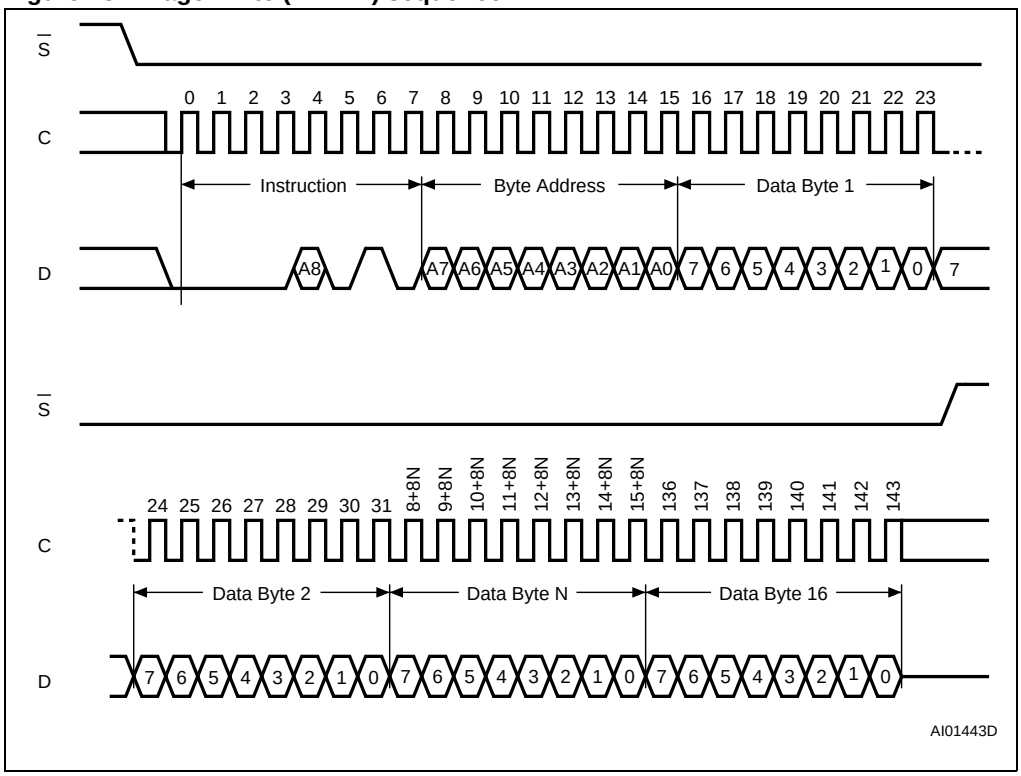
- if the Write Enable Latch (WEL) bit has not been set to 1 (by executing a Write Enable instruction just before)
- if a Write cycle is already in progress
- if the device has not been deselected, by Chip Select ($\overline{S}$) being driven High, at a byte boundary (after the rising edge of Serial Clock (C) that latches the last data bit, and before the next rising edge of Serial Clock (C) occurs anywhere on the bus)
- if Write Protect ($\overline{W}$) is Low or if the addressed page is in the region protected by the Block Protect (BP1 and BP0) bits.

Figure 12. Byte Write (WRITE) sequence



1. Depending on the memory size, as shown in *Table 6*, the most significant address bits are Don't Care.

Figure 13. Page Write (WRITE) sequence



1. Depending on the memory size, as shown in *Table 6*, the most significant address bits are Don't Care.

6.7 Cycling

7 Power-up and delivery states

7.1 Power-up state

After Power-up, the device is in the following state:

- low power Standby Power mode
- deselected (after Power-up, a falling edge is required on Chip Select ($\overline{S}$) before any instructions can be started).
- not in the Hold Condition
- the Write Enable Latch (WEL) is reset to 0
- Write In Progress (WIP) is reset to 0

The BP1 and BP0 bits of the Status Register are unchanged from the previous power-down (they are non-volatile bits).

7.2 Initial delivery state

The device is delivered with the memory array set at all 1s (FFh). The Block Protect (BP1 and BP0) bits are initialized to 0.

8 Maximum rating

Stressing the device outside the ratings listed in *Table 7* may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the Operating sections of this specification, is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 7. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
T_A	Ambient Operating Temperature	–40	130	°C
T_{STG}	Storage Temperature	–65	150	°C
T_{LEAD}	Lead Temperature during Soldering	see note (1)		°C
V_O	Output Voltage	–0.50	V_{CC}+0.6	V
V_I	Input Voltage	–0.50	6.5	V
V_{CC}	Supply Voltage	–0.50	6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model)(2)	–4000	4000	V

1. Compliant with JEDEC Std J-STD-020C (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU.
2. AEC-Q100-002 (compliant with JEDEC Std JESD22-A114A, C1=100pF, R1=1500Ω, R2=500Ω)

9 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC Characteristic tables that follow are derived from tests performed under the Measurement Conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 8. Operating conditions (M950x0)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.5	V
T_A	Ambient Operating Temperature (Device Grade 6)	–40	85	°C
	Ambient Operating Temperature (Device Grade 3)	–40	125	°C

Table 9. Operating conditions (M950x0-W)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	2.5	5.5	V
T_A	Ambient Operating Temperature (Device Grade 6)	–40	85	°C
	Ambient Operating Temperature (Device Grade 3)	–40	125	°C

Table 10. Operating conditions (M950x0-R)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	1.8	5.5	V
T_A	Ambient Operating Temperature	–40	85	°C

Table 11. AC test measurement conditions

Symbol	Parameter	Min.	Max.	Unit
C_L	Load Capacitance	30		pF
	Input Rise and Fall Times		50	ns
	Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$		V
	Input and Output Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$		V

1. Output Hi-Z is defined as the point where data out is no longer driven.

Figure 14. AC test measurement I/O waveform

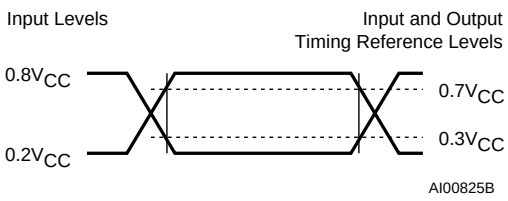


Table 12. Capacitance

Symbol	Parameter	Test Condition	Min.	Max.	Unit
C_{OUT}	Output Capacitance (Q)	V_{OUT} = 0V		8	pF
C_{IN}	Input Capacitance (D)	V_{IN} = 0V		8	pF
	Input Capacitance (other pins)	V_{IN} = 0V		6	pF

1. Sampled only, not 100% tested, at T_A=25°C and a frequency of 5MHz.

Table 13. DC characteristics (M950x0, Device Grade 6)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current	$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output Leakage Current	$\overline{S} = V_{CC}$, $V_{OUT} = V_{SS}$ or V_{CC}		± 2	µA
I_{CC}	Supply Current	C = 0.1V_{CC}/0.9V_{CC} at 10 MHz, V_{CC} = 5 V, Q = open		5	mA
I_{CC1}	Supply Current (Standby Power mode)	$\overline{S} = V_{CC}$, V_{CC} = 5 V, $V_{IN} = V_{SS}$ or V_{CC}		2	µA
V_{IL}	Input Low Voltage		–0.45	0.3 V_{CC}	V
V_{IH}	Input High Voltage		0.7 V_{CC}	V_{CC}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 2 mA, V_{CC} = 5 V		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –2 mA, V_{CC} = 5 V	0.8 V_{CC}		V

Table 14. DC characteristics (M950x0, Device Grade 3)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current	$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output Leakage Current	$\overline{S} = V_{CC}$, $V_{OUT} = V_{SS}$ or V_{CC}		± 2	µA
I_{CC}	Supply Current	C = 0.1V_{CC}/0.9V_{CC} at 5 MHz, V_{CC} = 5 V, Q = open		3	mA
I_{CC1}	Supply Current (Standby Power mode)	$\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC} V_{CC} = 5 V		5	µA
V_{IL}	Input Low Voltage		–0.45	0.3 V_{CC}	V
V_{IH}	Input High Voltage		0.7 V_{CC}	V_{CC}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 2 mA, V_{CC} = 5 V		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –2 mA, V_{CC} = 5 V	0.8 V_{CC}		V

Table 15. DC characteristics (M950x0-W, Device Grade 6)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current	$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output Leakage Current	$\overline{S} = V_{CC}$, $V_{OUT} = V_{SS}$ or V_{CC}		± 2	µA
I_{CC}	Supply Current	C = 0.1V_{CC}/0.9V_{CC} at 5 MHz, V_{CC} = 2.5 V, Q = open		2	mA
I_{CC1}	Supply Current (Standby Power mode)	$\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC} V_{CC} = 2.5 V		1	µA
V_{IL}	Input Low Voltage		–0.45	0.3 V_{CC}	V
V_{IH}	Input High Voltage		0.7 V_{CC}	V_{CC}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 1.5 mA, V_{CC} = 2.5 V		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –0.4 mA, V_{CC} = 2.5 V	0.8 V_{CC}		V

Table 16. DC characteristics (M950x0-W, Device Grade 3)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current	$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output Leakage Current	$\overline{S} = V_{CC}$, $V_{OUT} = V_{SS}$ or V_{CC}		± 2	µA
I_{CC}	Supply Current	C = 0.1V_{CC}/0.9V_{CC} at 5 MHz, V_{CC} = 2.5 V, Q = open		2	mA
I_{CC1}	Supply Current (Standby Power mode)	$\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC} V_{CC} = 2.5 V		2	µA
V_{IL}	Input Low Voltage		–0.45	0.3 V_{CC}	V
V_{IH}	Input High Voltage		0.7 V_{CC}	V_{CC}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 1.5 mA, V_{CC} = 2.5 V		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –0.4 mA, V_{CC} = 2.5 V	0.8 V_{CC}		V

Table 17. DC characteristics (M950x0-R)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current	$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output Leakage Current	$\overline{S} = V_{CC}$, $V_{OUT} = V_{SS}$ or V_{CC}		± 2	µA
I_{CC}	Supply Current	C = 0.1 V_{CC}/0.9. V_{CC} at 2 MHz, V_{CC} = 1.8 V, Q = open		2	mA
I_{CC1}	Supply Current (Standby Power mode)	$\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 1.8 V		1	µA
V_{IL}	Input Low Voltage		–0.45	0.3V_{CC}	V
V_{IH}	Input High Voltage		0.7 V_{CC}	V_{CC}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 0.15 mA, V_{CC} = 1.8 V		0.3	V
V_{OH}	Output High Voltage	I_{OH} = –0.1 mA, V_{CC} = 1.8 V	0.8 V_{CC}		V

Table 18. AC characteristics (M950x0, Device Grade 6)

Test conditions specified in *Table 11* and *Table 8*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SCK}	Clock Frequency	D.C.	10	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ Active Setup Time	15		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ Not Active Setup Time	15		ns
t_{SHSL}	t_{CS}	$\overline{S}$ Deselect Time	40		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ Active Hold Time	25		ns
t_{CHSL}		$\overline{S}$ Not Active Hold Time	15		ns
t_{CH}(1)	t_{CLH}	Clock High Time	40		ns
t_{CL}(1)	t_{CLL}	Clock Low Time	40		ns
t_{CLCH}(2)	t_{RC}	Clock Rise Time		1	µs
t_{CHCL}(2)	t_{FC}	Clock Fall Time		1	µs
t_{DVCH}	t_{DSU}	Data In Setup Time	15		ns
t_{CHDX}	t_{DH}	Data In Hold Time	15		ns
t_{HHCH}		Clock Low Hold Time after $\overline{HOLD}$ not Active	15		ns
t_{HLCH}		Clock Low Hold Time after $\overline{HOLD}$ Active	20		ns
t_{CLHL}		Clock Low Setup Time before $\overline{HOLD}$ Active	0		ns
t_{CLHH}		Clock Low Setup Time before $\overline{HOLD}$ not Active	0		ns
t_{SHQZ}(2)	t_{DIS}	Output Disable Time		25	ns
t_{CLQV}	t_V	Clock Low to Output Valid		35	ns
t_{CLQX}	t_{HO}	Output Hold Time	0		ns
t_{QLQH}(2)	t_{RO}	Output Rise Time		20	ns
t_{QHQL}(2)	t_{FO}	Output Fall Time		20	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ High to Output Valid		25	ns
t_{HLQZ}(2)	t_{HZ}	$\overline{HOLD}$ Low to Output High-Z		35	ns
t_W	t_{WC}	Write Time		5	ms

1. $t_{CH} + t_{CL}$ must never be less than the shortest possible clock period, $1 / f_C$(max)
2. Value guaranteed by characterization, not 100% tested in production.

Table 19. AC characteristics (M950x0, Device Grade 3)

Test conditions specified in *Table 11* and *Table 8*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SCK}	Clock Frequency	D.C.	5	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ Active Setup Time	90		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ Not Active Setup Time	90		ns
t_{SHSL}	t_{CS}	$\overline{S}$ Deselect Time	100		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ Active Hold Time	90		ns
t_{CHSL}		$\overline{S}$ Not Active Hold Time	90		ns
t_{CH}(1)	t_{CLH}	Clock High Time	90		ns
t_{CL}(1)	t_{CLL}	Clock Low Time	90		ns
t_{CLCH}(2)	t_{RC}	Clock Rise Time		1	µs
t_{CHCL}(2)	t_{FC}	Clock Fall Time		1	µs
t_{DVCH}	t_{DSU}	Data In Setup Time	20		ns
t_{CHDX}	t_{DH}	Data In Hold Time	30		ns
t_{HHCH}		Clock Low Hold Time after $\overline{HOLD}$ not Active	70		ns
t_{HLCH}		Clock Low Hold Time after $\overline{HOLD}$ Active	40		ns
t_{CLHL}		Clock Low Setup Time before $\overline{HOLD}$ Active	0		ns
t_{CLHH}		Clock Low Setup Time before $\overline{HOLD}$ not Active	0		ns
t_{SHQZ}(2)	t_{DIS}	Output Disable Time		100	ns
t_{CLQV}	t_V	Clock Low to Output Valid		60	ns
t_{CLQX}	t_{HO}	Output Hold Time	0		ns
t_{QLQH}(2)	t_{RO}	Output Rise Time		50	ns
t_{QHQL}(2)	t_{FO}	Output Fall Time		50	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ High to Output Valid		50	ns
t_{HLQZ}(2)	t_{HZ}	$\overline{HOLD}$ Low to Output High-Z		100	ns
t_W	t_{WC}	Write Time		5	ms

1. $t_{CH} + t_{CL}$ must never be less than the shortest possible clock period, $1 / f_C$(max)
2. Value guaranteed by characterization, not 100% tested in production.

Table 20. AC characteristics (M950x0-W, Device Grade 6)

Test conditions specified in *Table 11* and *Table 9*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SCK}	Clock Frequency	D.C.	5	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ Active Setup Time	90		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ Not Active Setup Time	90		ns
t_{SHSL}	t_{CS}	$\overline{S}$ Deselect Time	100		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ Active Hold Time	90		ns
t_{CHSL}		$\overline{S}$ Not Active Hold Time	90		ns
t_{CH}(1)	t_{CLH}	Clock High Time	90		ns
t_{CL}(1)	t_{CLL}	Clock Low Time	90		ns
t_{CLCH}(2)	t_{RC}	Clock Rise Time		1	µs
t_{CHCL}(2)	t_{FC}	Clock Fall Time		1	µs
t_{DVCH}	t_{DSU}	Data In Setup Time	20		ns
t_{CHDX}	t_{DH}	Data In Hold Time	30		ns
t_{HHCH}		Clock Low Hold Time after $\overline{HOLD}$ not Active	70		ns
t_{HLCH}		Clock Low Hold Time after $\overline{HOLD}$ Active	40		ns
t_{CLHL}		Clock Low Setup Time before $\overline{HOLD}$ Active	0		ns
t_{CLHH}		Clock Low Setup Time before $\overline{HOLD}$ not Active	0		ns
t_{SHQZ}(2)	t_{DIS}	Output Disable Time		100	ns
t_{CLQV}	t_V	Clock Low to Output Valid		60	ns
t_{CLQX}	t_{HO}	Output Hold Time	0		ns
t_{QLQH}(2)	t_{RO}	Output Rise Time		50	ns
t_{QHQL}(2)	t_{FO}	Output Fall Time		50	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ High to Output Valid		50	ns
t_{HLQZ}(2)	t_{HZ}	$\overline{HOLD}$ Low to Output High-Z		100	ns
t_W	t_{WC}	Write Time		5	ms

1. $t_{CH} + t_{CL}$ must never be less than the shortest possible clock period, $1 / f_C$(max)
2. Value guaranteed by characterization, not 100% tested in production.

Table 21. AC characteristics (M950x0-W, Device Grade 3)

Test conditions specified in *Table 11* and *Table 9*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SCK}	Clock Frequency	D.C.	5	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ Active Setup Time	90		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ Not Active Setup Time	90		ns
t_{SHSL}	t_{CS}	$\overline{S}$ Deselect Time	100		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ Active Hold Time	90		ns
t_{CHSL}		$\overline{S}$ Not Active Hold Time	90		ns
t_{CH}(1)	t_{CLH}	Clock High Time	90		ns
t_{CL}(1)	t_{CLL}	Clock Low Time	90		ns
t_{CLCH}(2)	t_{RC}	Clock Rise Time		1	µs
t_{CHCL}(2)	t_{FC}	Clock Fall Time		1	µs
t_{DVCH}	t_{DSU}	Data In Setup Time	20		ns
t_{CHDX}	t_{DH}	Data In Hold Time	30		ns
t_{HHCH}		Clock Low Hold Time after $\overline{HOLD}$ not Active	70		ns
t_{HLCH}		Clock Low Hold Time after $\overline{HOLD}$ Active	40		ns
t_{CLHL}		Clock Low Setup Time before $\overline{HOLD}$ Active	0		ns
t_{CLHH}		Clock Low Set-up Time before $\overline{HOLD}$ not Active	0		ns
t_{SHQZ}(2)	t_{DIS}	Output Disable Time		100	ns
t_{CLQV}	t_V	Clock Low to Output Valid		60	ns
t_{CLQX}	t_{HO}	Output Hold Time	0		ns
t_{QLQH}(2)	t_{RO}	Output Rise Time		50	ns
t_{QHQL}(2)	t_{FO}	Output Fall Time		50	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ High to Output Valid		50	ns
t_{HLQZ}(2)	t_{HZ}	$\overline{HOLD}$ Low to Output High-Z		100	ns
t_W	t_{WC}	Write Time		5	ms

1. $t_{CH} + t_{CL}$ must never be less than the shortest possible clock period, $1 / f_C$(max)
2. Value guaranteed by characterization, not 100% tested in production.

Table 22. AC characteristics (M950x0-R)

Test conditions specified in *Table 11* and *Table 10*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SCK}	Clock Frequency	D.C.	2	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ Active Setup Time	200		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ Not Active Setup Time	200		ns
t_{SHSL}	t_{CS}	$\overline{S}$ Deselect Time	200		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ Active Hold Time	200		ns
t_{CHSL}		$\overline{S}$ Not Active Hold Time	200		ns
t_{CH}(1)	t_{CLH}	Clock High Time	200		ns
t_{CL}(1)	t_{CLL}	Clock Low Time	200		ns
t_{CLCH}(2)	t_{RC}	Clock Rise Time		1	µs
t_{CHCL}(2)	t_{FC}	Clock Fall Time		1	µs
t_{DVCH}	t_{DSU}	Data In Setup Time	40		ns
t_{CHDX}	t_{DH}	Data In Hold Time	50		ns
t_{HHCH}		Clock Low Hold Time after $\overline{HOLD}$ not Active	140		ns
t_{HLCH}		Clock Low Hold Time after $\overline{HOLD}$ Active	90		ns
t_{CLHL}		Clock Low Setup Time before $\overline{HOLD}$ Active	0		ns
t_{CLHH}		Clock Low Setup Time before $\overline{HOLD}$ not Active	0		ns
t_{SHQZ}(2)	t_{DIS}	Output Disable Time		250	ns
t_{CLQV}	t_V	Clock Low to Output Valid		180	ns
t_{CLQX}	t_{HO}	Output Hold Time	0		ns
t_{QLQH}(2)	t_{RO}	Output Rise Time		100	ns
t_{QHQL}(2)	t_{FO}	Output Fall Time		100	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ High to Output Valid		100	ns
t_{HLQZ}(2)	t_{HZ}	$\overline{HOLD}$ Low to Output High-Z		250	ns
t_W	t_{WC}	Write Time		10	ms

1. $t_{CH} + t_{CL}$ must never be less than the shortest possible clock period, $1 / f_C$(max)
2. Value guaranteed by characterization, not 100% tested in production.

Figure 15. Serial input timing

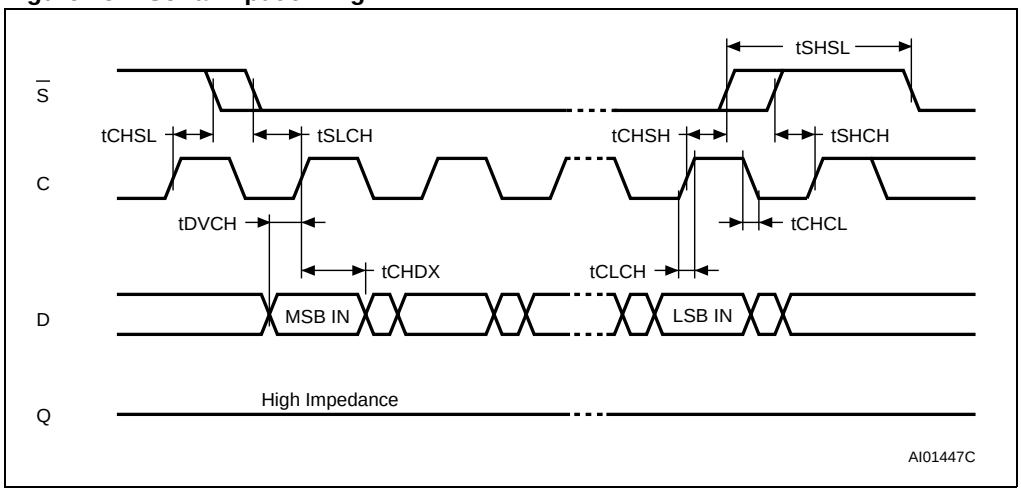


Figure 16. Hold timing

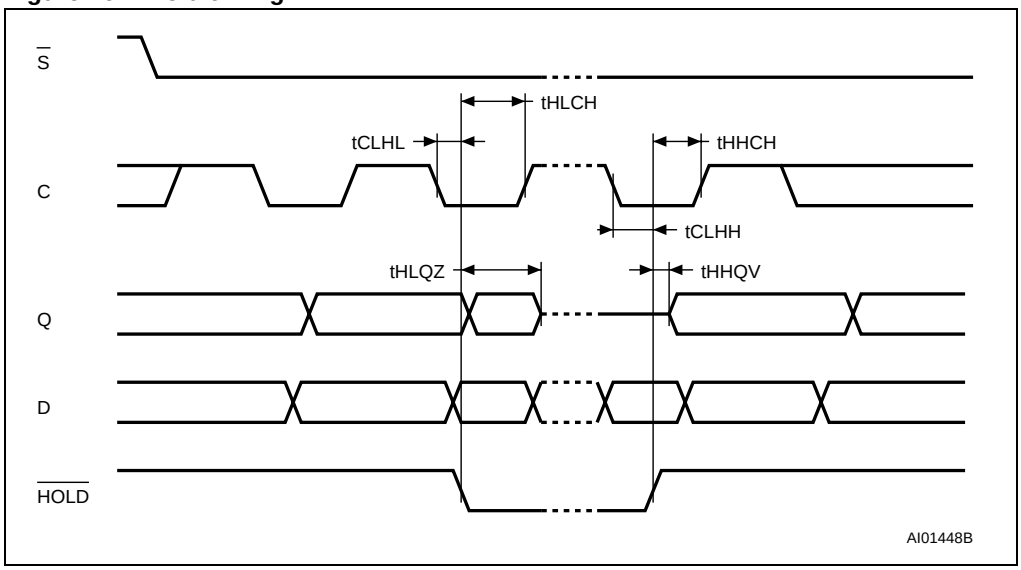
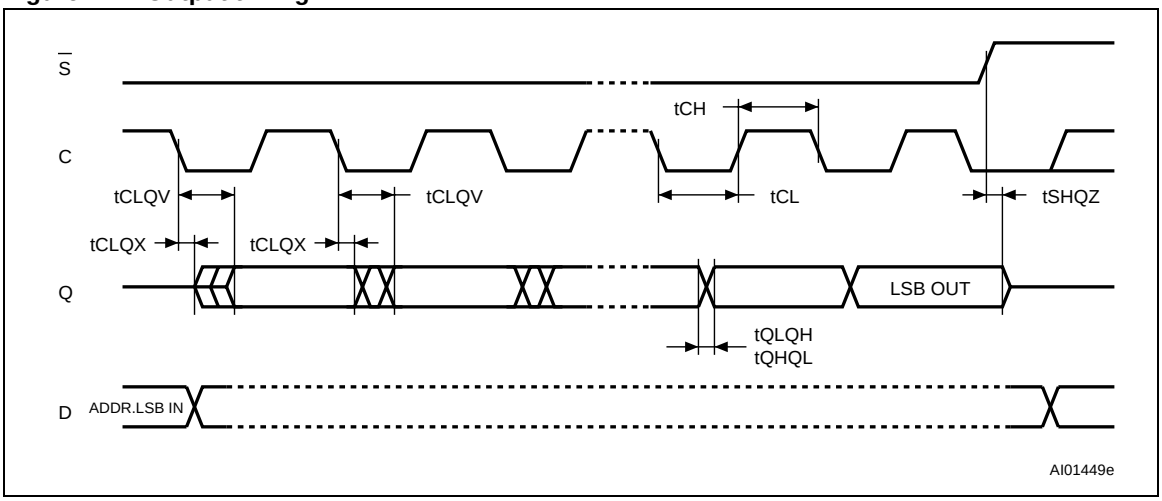
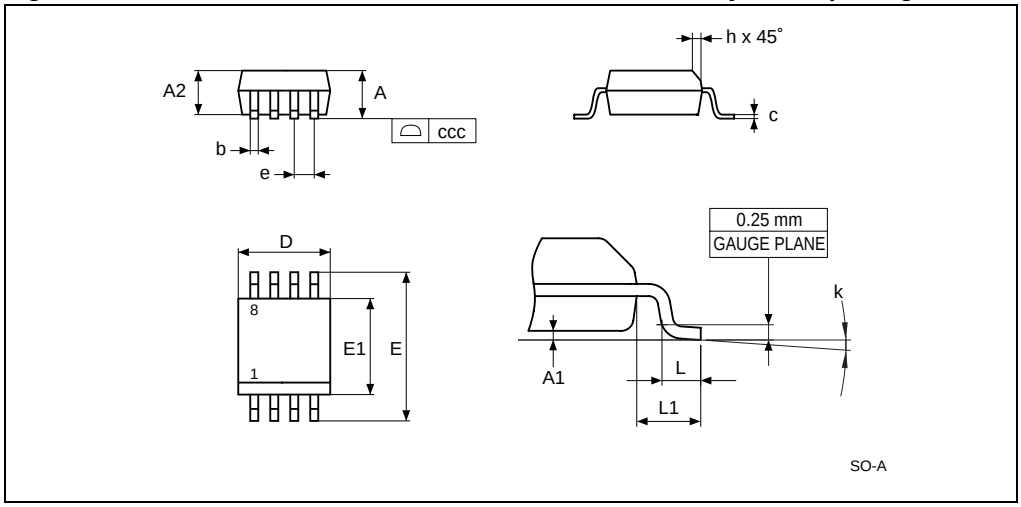


Figure 17. Output timing



10 Package mechanical

Figure 18. SO8N - 8 lead Plastic Small Outline, 150 mils body width, package outline

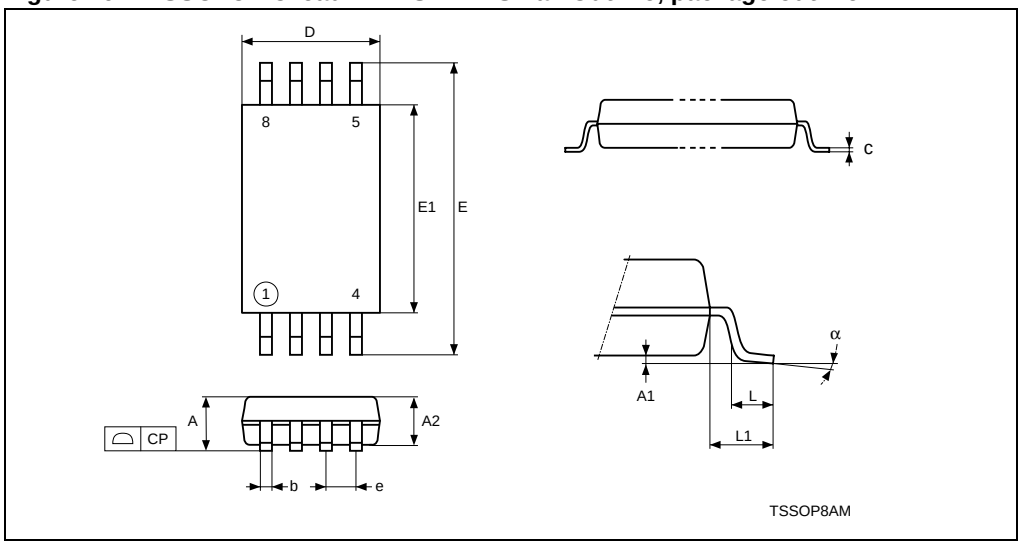


1. Drawing is not to scale.

Table 23. SO8N - 8 lead Plastic Small Outline, 150 mils body width, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.75			0.069
A1		0.10	0.25		0.004	0.010
A2		1.25			0.049	
b		0.28	0.48		0.011	0.019
c		0.17	0.23		0.007	0.009
ccc			0.10			0.004
D	4.90	4.80	5.00	0.193	0.189	0.197
E	6.00	5.80	6.20	0.236	0.228	0.244
E1	3.90	3.80	4.00	0.154	0.150	0.157
e	1.27	–	–	0.050	–	–
h		0.25	0.50		0.010	0.020
k		0°	8°		0°	8°
L		0.40	1.27		0.016	0.050
L1	1.04			0.041		

Figure 19. TSSOP8 – 8 lead Thin Shrink Small Outline, package outline

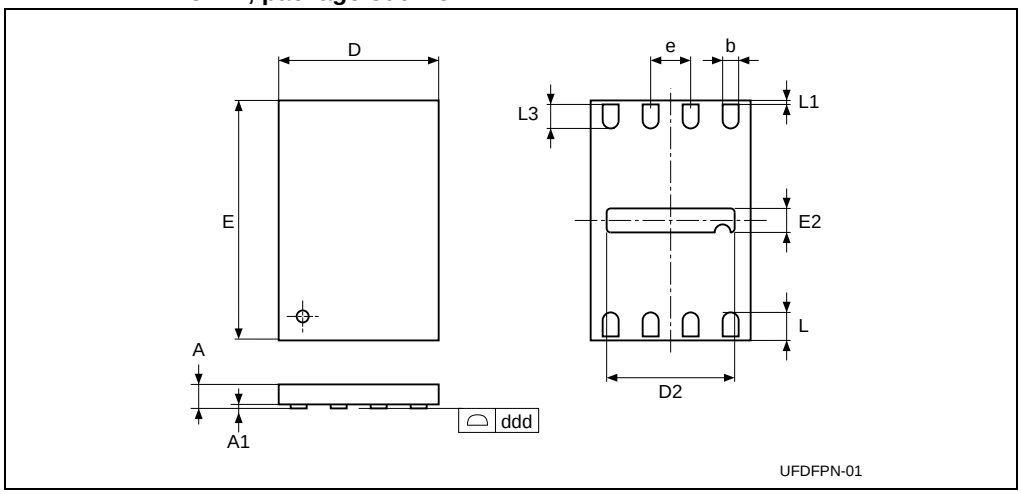


1. Drawing is not to scale.

Table 24. TSSOP8 – 8 lead Thin Shrink Small Outline, package mechanical data

Symbol	millimeters			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			1.200			0.0472
A1		0.050	0.150		0.0020	0.0059
A2	1.000	0.800	1.050	0.0394	0.0315	0.0413
b		0.190	0.300		0.0075	0.0118
c		0.090	0.200		0.0035	0.0079
CP			0.100			0.0039
D	3.000	2.900	3.100	0.1181	0.1142	0.1220
e	0.650	–	–	0.0256	–	–
E	6.400	6.200	6.600	0.2520	0.2441	0.2598
E1	4.400	4.300	4.500	0.1732	0.1693	0.1772
L	0.600	0.450	0.750	0.0236	0.0177	0.0295
L1	1.000			0.0394		
α		0°	8°		0°	8°
N (number of pins)	8			8		

Figure 20. UFDFPN8 (MLP8) - 8-lead Ultra thin Fine pitch Dual Flat Package No lead 2 × 3mm, package outline



1. Drawing is not to scale.

Table 25. UFDFPN8 (MLP8) - 8-lead Ultra thin Fine pitch Dual Flat Package No lead 2 × 3mm, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A	0.55	0.50	0.60	0.022	0.020	0.024
A1		0.00	0.05		0.000	0.002
b	0.25	0.20	0.30	0.010	0.008	0.012
D	2.00			0.079		
D2		1.55	1.65		0.061	0.065
ddd			0.05			0.002
E	3.00			0.118		
E2		0.15	0.25		0.006	0.010
e	0.50	–	–	0.020	–	–
L	0.45	0.40	0.50	0.018	0.016	0.020
L1			0.15			0.006
L3		0.30			0.012	
N (number of pins)	8			8		

11 Part numbering

Table 26. Ordering information scheme

Example: M95040 – W MN 6 T P /W

Device Type
M95 = SPI serial access EEPROM

Device Function
040 = 4 Kbit (512 x 8)
020 = 2 Kbit (256 x 8)
010 = 1 Kbit (128 x 8)

Operating Voltage
blank = V_{CC} = 4.5 to 5.5V
W = V_{CC} = 2.5 to 5.5V
R = V_{CC} = 1.8 to 5.5V

Package
MN = SO8 (150 mil width)
DW = TSSOP8 (169 mil width)
MB = UFDFPN8 (MLP8) 2 × 3mm

Device Grade
6 = Industrial temperature range, –40 to 85 °C.
Device tested with standard test flow
3 = Device tested with High Reliability Certified Flow(1).
Automotive temperature range (–40 to 125 °C)

Option
blank = Standard Packing
T = Tape and Reel Packing

Plating Technology
blank = Standard SnPb plating
P or G = ECOPACK® (RoHS compliant)

Process(2)
/W, /G or /S = F6SP36%

1. ST strongly recommends the use of the Automotive Grade devices for use in an automotive environment. The High Reliability Certified Flow (HRCF) is described in the quality note QNEE9801. Please ask your nearest ST sales office for a copy.
2. Used only for Device Grade 3

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST Sales Office.

The category of second-Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

12 Revision history

Table 27. Document revision history

Date	Version	Changes
10-May-2000	2.2	s/issuing three bytes/issuing two bytes/ in the 2nd sentence of the Byte Write Operation
16-Mar-2001	2.3	Human Body Model meets JEDEC std (Table 2). Minor adjustments to Figs 7,9,10,11 & Tab 9. Wording changes, according to the standard glossary Illustrations and Package Mechanical data updated
19-Jul-2001	2.4	Temperature range '3' added to the -W supply voltage range in DC and AC characteristics
11-Oct-2001	3.0	Document reformatted using the new template
26-Feb-2002	3.1	Description of chip deselect after 8th clock pulse made more explicit
27-Sep-2002	3.2	Position of A8 in Read Instruction Sequence Figure corrected. Load Capacitance C_L changed
24-Oct-2002	3.3	Minimum values for tCHHL and tCHHH changed.
24-Feb-2003	3.4	Description of Read from Memory Array (READ) instruction corrected, and clarified
28-May-2003	3.5	New products, identified by the process letter W, added
25-Jun-2003	3.6	Correction to current products, identified by the process letter K not L. I_{CC} changed in DC characteristics, and t_{CHHL}, t_{CHHH} substituted in AC characteristics Voltage range -S upgraded by removing it, and adding the -R voltage range in its place Temperature range 5 removed.
21-Nov-2003	4.0	Table of contents, and Pb-free options added. V_{IL}(min) improved to -0.45V
02-Feb-2004	4.1	V_{IL}(max) and t_{CLQV}(max) changed
01-Mar-2004	5.0	Absolute Maximum Ratings for V_{IO}(min) and V_{CC}(min) improved. Soldering temperature information clarified for RoHS compliant devices. New 5V and 2.5V devices, with process letter W, promoted from preliminary data to full data. Device Grade 3 clarified, with reference to HRCF and automotive environments

Table 27. Document revision history (continued)

Date	Version	Changes
05-Oct-2004	6.0	Product List summary table added. Process identification letter “G” information added. Order information for Tape and Reel changed to T. AEC-Q100-002 compliance. Device Grade information clarified. tHHQX corrected to tHHQV. Signal Description updated. 10MHz, 5ms Write is now the present product. tCH+tCL<1/fC constraint clarified
06-Nov-2006	7	Document converted to new template, *Table 5: Status Register format* moved to below *Section 6.3: Read Status Register (RDSR)*. PDIP package removed. UFDFPN8 (MB) package added (see *Figure 20* and *Table 25*) and SO8N package specifications updated (see *Figure 18* and *Table 23*). Packages are ECOPACK® compliant. *Section 6.7: Cycling* added. *Section 2.8: Supply voltage (V_{CC})* added and information removed below *Section 4: Operating features*. *Figure 3: Bus master and memory devices on the SPI bus* modified. T_{LEAD} parameter modified, *Note 1* changed, and T_A added to *Table 7: Absolute maximum ratings*. Characteristics of previous product identified by process letter K removed. CL modified in *Table 11: AC test measurement conditions*. Note removed below *Table 13* and *Table 14*. Information in *Table 17* is no longer Preliminary data, I_{CC}, I_{CC1} and V_{IL} modified. End timing line of t_{SHQZ} moved in *Figure 17*. t_{CHHL} and t_{CHHH} changed to t_{CLHL} and t_{CLHH}, respectively in *Figure 16*, *Table 18*, *Table 19*, *Table 20*, *Table 21* and *Table 22*. *Plating Technology* and *Process* updated in *Table 26: Ordering information scheme*.

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