



ISO K Line Serial Link Interface

The 33660 is a serial link bus interface device designed to provide bi-directional half-duplex communication interfacing in automotive diagnostic applications. It is designed to interface between the vehicle's on-board microcontroller, and systems off-board the vehicle via the special ISO K line. The 33660 is designed to meet the Diagnostic Systems ISO9141 specification. The device's K line bus driver's output is fully protected against bus shorts and over-temperature conditions.

The 33660 derives its robustness to temperature and voltage extremes by being built on a SMARTMOS process, incorporating CMOS logic, bipolar/MOS analog circuitry, and DMOS power FETs. Although the 33660 was principally designed for automotive applications, it is suited for other serial communication applications. It is parametrically specified over an ambient temperature range of $-40\text{ }^{\circ}\text{C} \leq T_A \leq 125\text{ }^{\circ}\text{C}$ and $8.0\text{ V} \leq V_{BB} \leq 18\text{ V}$ supply. The economical SO-8 surface-mount plastic package makes the 33660 very cost effective.

Features

- Operates over wide supply voltage of 8.0 to 18 V
- Operating temperature of -40 to $125\text{ }^{\circ}\text{C}$
- Interfaces directly to standard CMOS microprocessors
- ISO K line pin protected against shorts to battery
- Thermal shutdown with hysteresis
- ISO K line pin capable of high currents
- ISO K line can be driven with up to 10 nF of parasitic capacitance
- 8.0 kV ESD protection attainable with few additional components
- Standby mode: no V_{BAT} current drain with V_{DD} at 5.0 V
- Low current drain during operation with V_{DD} at 5.0 V

33660

ISO9141 PHYSICAL INTERFACE



**EF SUFFIX (PB-FREE)
98ASB42564B
8-PIN SOICN**

ORDERING INFORMATION		
Device	Temperature Range (T_A)	Package
MC33660EF/R2	-40 to $125\text{ }^{\circ}\text{C}$	8-SOICN

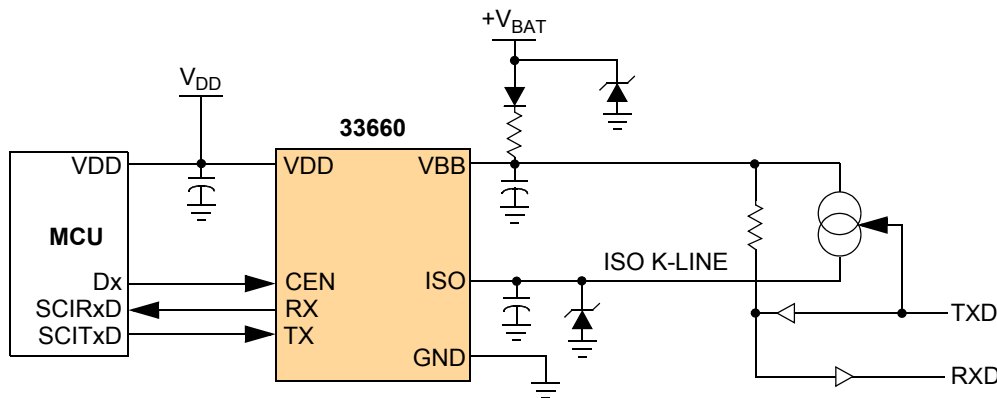


Figure 1. 33660 Simplified Application Diagram

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INTERNAL BLOCK DIAGRAM

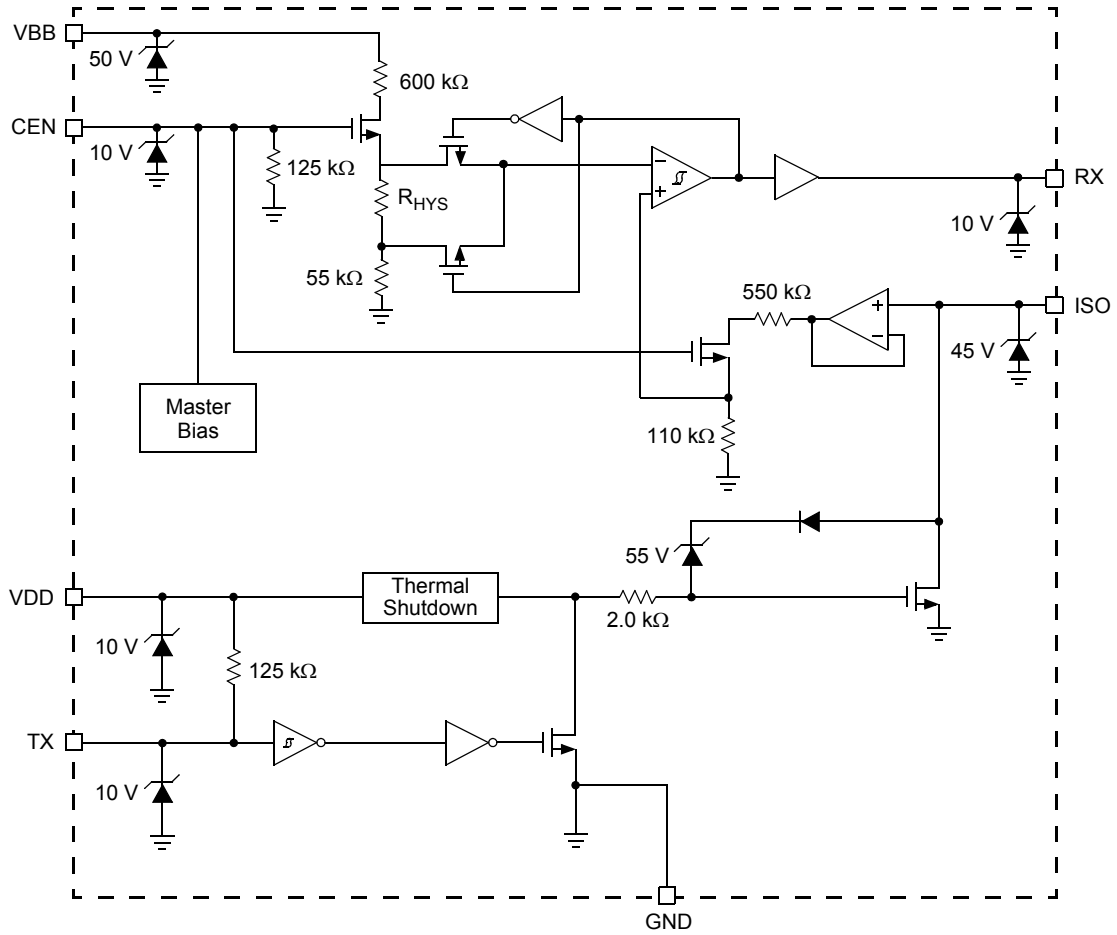


Figure 2. 33660 Simplified Internal Block Diagram

PIN CONNECTIONS

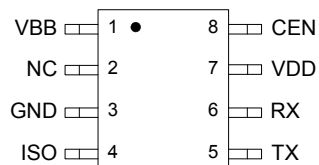


Figure 3. 33660 Pin Connections

Table 1. 33660 Pin Definitions

Pin Number	Pin Name	Definition
1	VBB	Battery power through external resistor and diode.
2	NC	Not to be connected. ⁽¹⁾
3	GND	Common signal and power return.
4	ISO	Bus connection.
5	TX	Logic level input for data to be transmitted on the bus.
6	RX	Logic output of data received on the bus.
7	VDD	Logic power source input.
8	CEN	Chip enable. Logic "1" for active state. Logic "0" for sleep state.

Notes

1. NC pins should not have any connections made to them. NC pins are not guaranteed to be open circuits.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Rating	Symbol	Value	Unit
VDD DC Supply Voltage	V_{DD}	-0.3 to 7.0	V
VBB Load Dump Peak Voltage	$V_{BB(LD)}$	45	V
ISO Pin Load Dump Peak Voltage ⁽²⁾	V_{ISO}	40	V
ESD Voltage ⁽³⁾			V
Human Body Model ⁽⁴⁾	V_{ESD1}	±2000	
Machine Model ⁽⁴⁾	V_{ESD2}	±200	
Charge Device Model ⁽⁴⁾			
Corner Pins	V_{ESD3-1}	±750	
All other Pins	V_{ESD3-2}	±500	
ISO Clamp Energy ⁽⁵⁾	E_{CLAMP}	10	mJ
Storage Temperature	T_{STG}	-55 to +150	°C
Operating Case Temperature	T_C	-40 to +125	°C
Operating Junction Temperature	T_J	-40 to +150	°C
Power Dissipation $T_A = 25\text{ °C}$	P_D	100	mW
Peak Package Reflow Temperature During Reflow ^{(6), (7)}	T_{PPRT}	Note 7.	°C
Thermal Resistance: Junction-to-Ambient	$R_{\theta JA}$	150	°C/W

Notes

- Device will survive double battery jump start conditions in typical applications for 10 minutes duration, but is not guaranteed to remain within specified parametric limits during this duration.
- ESD data available upon request.
- ESD1 testing is performed in accordance with the Human Body Model ($C_{ZAP} = 100\text{ pF}$, $R_{ZAP} = 1500\ \Omega$), ESD2 testing is performed in accordance with the Machine Model ($C_{ZAP} = 200\text{ pF}$, $R_{ZAP} = 0\ \Omega$), ESD3 testing is performed in accordance with the Charge Device Model ($C_{ZAP} = 4.0\text{ pF}$).
- Nonrepetitive clamping capability at 25 °C.
- Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
- Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxx enter 33xxx), and review parametrics.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions of $4.75\text{ V} \leq V_{DD} \leq 5.25\text{ V}$, $8.0\text{ V} \leq V_{BB} \leq 18\text{ V}$, $-40\text{ }^\circ\text{C} \leq T_C \leq 125\text{ }^\circ\text{C}$, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER AND CONTROL					
V_{DD} Sleep State Current $T_X = 0.8 V_{DD}$, $CEN = 0.3 V_{DD}$	$I_{DD(SS)}$	–	–	0.1	mA
V_{DD} Quiescent Operating Current $T_X = 0.2 V_{DD}$, $CEN = 0.7 V_{DD}$	$I_{DD(Q)}$	–	–	1.0	mA
V_{BB} Sleep State Current $V_{BB} = 16\text{ V}$, $T_X = 0.8 V_{DD}$, $CEN = 0.3 V_{DD}$	$I_{BB(SS)}$	–	–	50	μA
V_{BB} Quiescent Operating Current $T_X = 0.2 V_{DD}$, $CEN = 0.7 V_{DD}$	$I_{BB(Q)}$	–	–	1.0	mA
Chip Enable Input High Voltage Threshold ⁽⁸⁾ Input Low Voltage Threshold ⁽⁹⁾	$V_{IH(CEN)}$ $V_{IL(CEN)}$	$0.7 V_{DD}$ –	– –	– $0.3 V_{DD}$	V
Chip Enable Pull-down Current ⁽¹⁰⁾	$I_{PD(CEN)}$	2.0	–	40	μA
T_X Input Low Voltage Threshold $R_{ISO} = 510\ \Omega$ ⁽¹¹⁾	$V_{IL(TX)}$	–	–	$0.3 \times V_{DD}$	V
T_X Input High Voltage Threshold $R_{ISO} = 510\ \Omega$ ⁽¹²⁾	$V_{IH(TX)}$	$0.7 \times V_{DD}$	–	–	V
T_X Pull-up Current ⁽¹³⁾	$I_{PU(TX)}$	-40	–	-2.0	μA
R_X Output Low Voltage Threshold $R_{ISO} = 510\ \Omega$, $T_X = 0.2 V_{DD}$, R_X Sinking 1.0 mA	$V_{OL(RX)}$	–	–	$0.2 V_{DD}$	V
R_X Output High Voltage Threshold $R_{ISO} = 510\ \Omega$, $T_X = 0.8 V_{DD}$, R_X Sourcing 250 μA	$V_{OH(RX)}$	$0.8 V_{DD}$	–	–	V
Thermal Shutdown ⁽¹⁴⁾	T_{LIM}	150	170	–	$^\circ\text{C}$

Notes

8. When I_{BB} transitions to $>100\ \mu\text{A}$.
9. When I_{BB} transitions to $<100\ \mu\text{A}$.
10. Enable pin has an internal current pull-down. Pull-down current is measured with CEN pin at $0.3 V_{DD}$.
11. Measured by ramping T_X down from $0.8 V_{DD}$ and noting T_X value at which ISO falls below $0.2 V_{BB}$.
12. Measured by ramping T_X up from $0.2 V_{DD}$ and noting the value at which ISO rises above $0.9 V_{BB}$.
13. T_X pin has internal current pull-up. Pull-up current is measured with T_X pin at $0.7 V_{DD}$.
14. Thermal Shutdown performance (T_{LIM}) is guaranteed by design, but not production tested.

Table 3. Static Electrical Characteristics (Continued)

Characteristics noted under conditions of $4.75\text{ V} \leq V_{DD} \leq 5.25\text{ V}$, $8.0\text{ V} \leq V_{BB} \leq 18\text{ V}$, $-40^\circ\text{C} \leq T_C \leq 125^\circ\text{C}$, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
ISO I/O					
Input Low Voltage Threshold $R_{ISO} = 510\ \Omega$, $T_X = 0.8\ V_{DD}$	$V_{IL(ISO)}$	–	–	$0.4 \times V_{BB}$	V
Input High Voltage Threshold $R_{ISO} = 510\ \Omega$, $T_X = 0.8\ V_{DD}$	$V_{IH(ISO)}$	$0.7 \times V_{BB}$	–	–	V
Input Voltage Hysteresis	$V_{HYS(ISO)}$	$0.05 \times V_{BB}$	–	$0.1 \times V_{BB}$	V
Internal Pull-up Current $R_{ISO} = \infty\ \Omega$, $T_X = 0.8\ V_{DD}$, $V_{ISO} = 9.0\text{ V}$, $V_{BB} = 18\text{ V}$	$I_{PU(ISO)}$	-5.0	–	-140	μA
Short-circuit Current Limit $R_{ISO} = 0\ \Omega$, $T_X = 0.4\ V_{DD}$, $V_{ISO} = V_{BB}$	$I_{SC(ISO)}$	50	–	200	mA
Output Low Voltage $R_{ISO} = 510\ \Omega$, $T_X = 0.2\ V_{DD}$	$V_{OL(ISO)}$	–	–	$0.1 \times V_{BB}$	V
Output High Voltage $R_{ISO} = \infty\ \Omega$, $T_X = 0.8\ V_{DD}$	$V_{OH(ISO)}$	$0.95 \times V_{BB}$	–	–	V

DYNAMIC ELECTRICAL CHARACTERISTICS**Table 4. Dynamic Electrical Characteristics**

Characteristics noted under conditions of $4.75\text{ V} \leq V_{DD} \leq 5.25\text{ V}$, $8.0\text{ V} \leq V_{BB} \leq 18\text{ V}$, $-40\text{ }^{\circ}\text{C} \leq T_C \leq 125\text{ }^{\circ}\text{C}$, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Fall Time ⁽¹⁵⁾ $R_{ISO} = 510\ \Omega$ to V_{BB} , $C_{ISO} = 10\text{ nF}$ to Ground	$t_{FALL(ISO)}$	–	–	2.0	μs
ISO Propagation Delay ⁽¹⁶⁾ High to Low: $R_{ISO} = 510\ \Omega$, $C_{ISO} = 500\text{ pF}$ ⁽¹⁷⁾ Low to High: $R_{ISO} = 510\ \Omega$, $C_{ISO} = 500\text{ pF}$ ⁽¹⁸⁾	$t_{PD(ISO)}$	– –	– –	2.0 2.0	μs

Notes

15. Time required ISO voltage to transition from $0.8\ V_{BB}$ to $0.2\ V_{BB}$.
16. Changes in the value of C_{ISO} affect the rise and fall time but have minimal effect on Propagation Delay.
17. Step T_X voltage from $0.8\ V_{DD}$ to $0.2\ V_{DD}$. Time measured from $V_{IH(TX)}$ until V_{ISO} reaches $0.3\ V_{BB}$.
18. Step T_X voltage from $0.2\ V_{DD}$ to $0.8\ V_{DD}$. Time measured from $V_{IL(TX)}$ until V_{ISO} reaches $0.7\ V_{BB}$.

ELECTRICAL PERFORMANCE CURVES

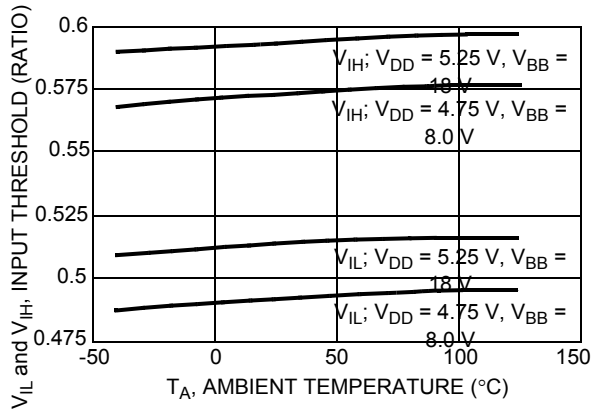


Figure 4. ISO Input Threshold/ V_{BB} vs. Temperature

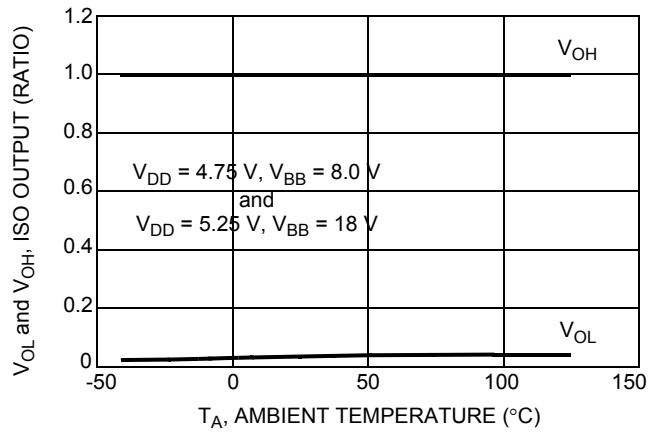


Figure 6. ISO Fall Time vs. Temperature

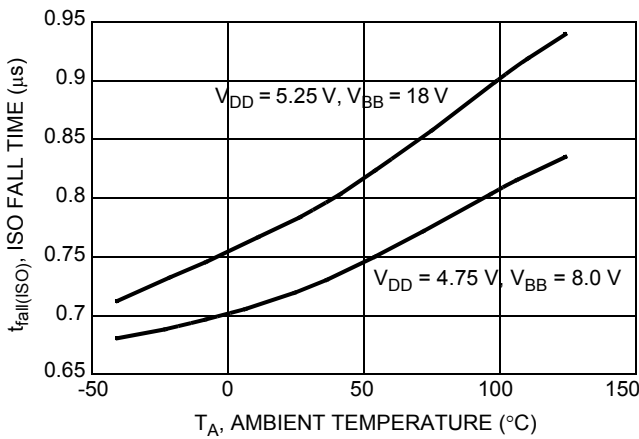


Figure 5. ISO Output/ V_{BB} vs. Temperature

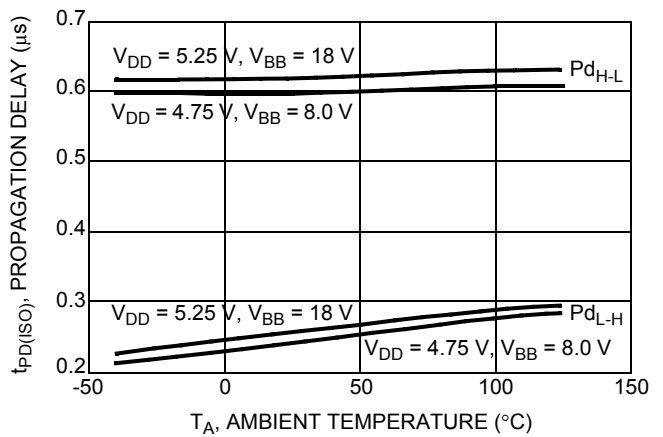
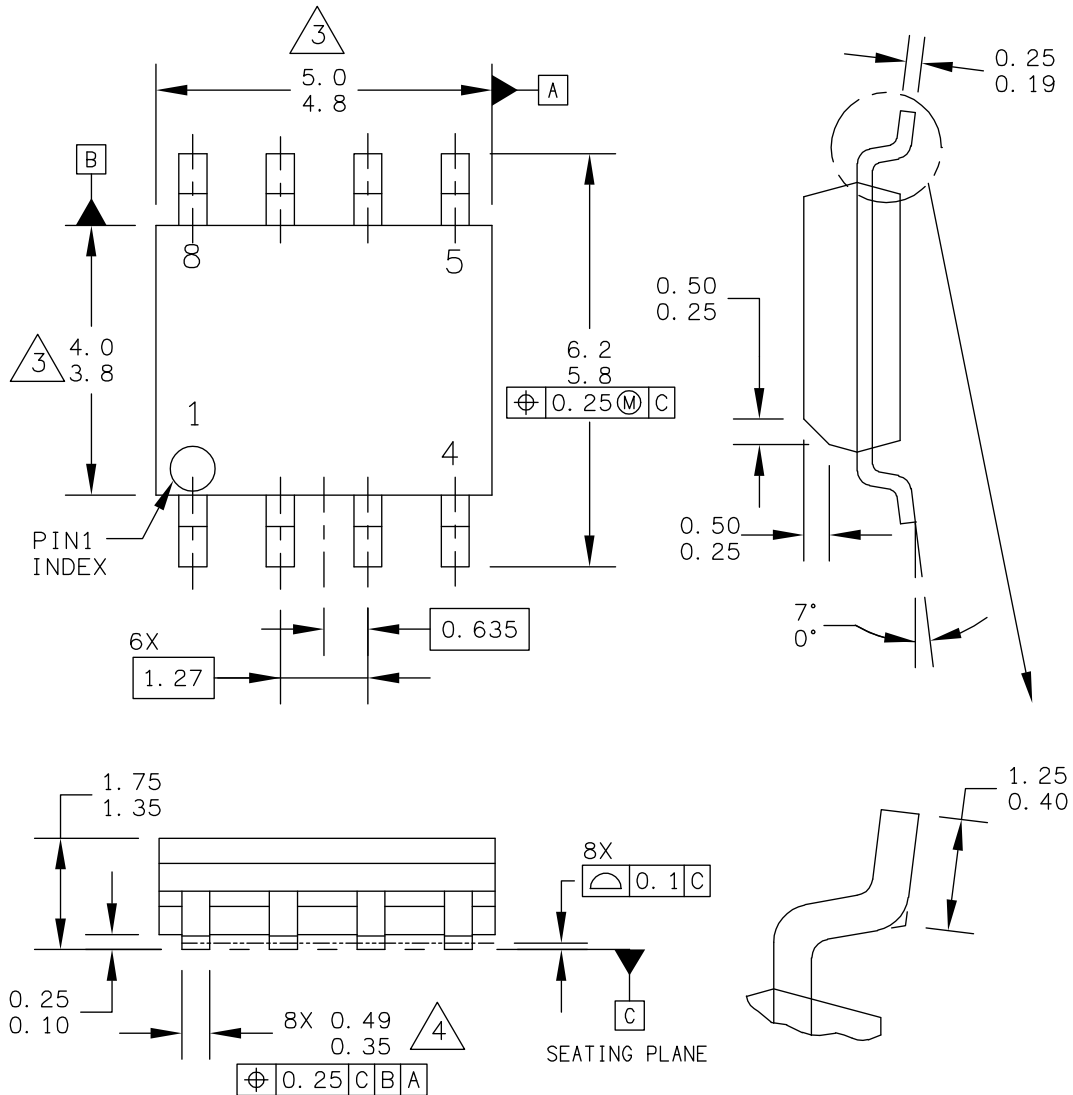


Figure 7. ISO Propagation Delay vs. Temperature

PACKAGING

PACKAGE DIMENSIONS

For the most current package revision, visit www.freescale.com and perform a keyword search using the "98A" listed below.



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TITLE: 8LD SOIC NARROW BODY	DOCUMENT NO: 98ASB42564B	REV: V
	CASE NUMBER: 751-07	20 NOV 2007
	STANDARD: JEDEC MS-012AA	

EF SUFFIX (PB-FREE)
8-PIN
98ASB42564B
REV. V

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
4. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION.

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EF SUFFIX (PB-FREE)
8-PIN
98ASB42564B
REV. V

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
1.0	1/2011	<ul style="list-style-type: none">Initial release
2.0	9/2011	<ul style="list-style-type: none">Adjusted format to meet current compliance standards. No data was altered.
3.0	10/2011	<ul style="list-style-type: none">Updated the PC part number to MC.

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