Multiphase PWM Regulator for VR12 DDR Memory Systems

ISL6353

The ISL6353 is a three-phase PWM buck regulator controller for VR12 DDR memory applications. The multi-phase implementation results in better system performance, superior thermal management, lower component cost and smaller PCB area.

The ISL6353 has two integrated power MOSFET drivers for implementing a cost effective and space saving power management solution.

The PWM modulator of the ISL6353 is based on Intersil's Robust Ripple Regulator™ (R^3) technology. Compared with the traditional multi-phase buck regulator, the R^3 modulator commands variable PWM switching frequency during load transients, achieving faster transient response. R^3 also naturally goes into pulse frequency modulation operation in light load conditions to achieve higher light load efficiency.

The ISL6353 is designed to be completely compliant with VR12 specifications. The ISL6353 has a serial VID (SVID) bus communicating with the CPU. The output can be programmed for 1-, 2- or 3-phase interleaved operation. The output voltage and power state can also be controlled independent of the serial VID bus.

The ISL6353 has several other key features. It supports DCR current sensing with a single NTC thermistor for DCR temperature compensation or accurate resistor current sensing. It also has remote voltage sense, adjustable switching frequency, current monitor, OC/OV protection and power-good. Temperature monitor and thermal alert is available too.

Features

- VR12 Serial Communications Bus
- Precision Voltage Regulation
  - 5mV Steps with VID Fast/Slow Slew Rates
- Supports Two Current Sensing Methods
  - Lossless Inductor DCR Current Sensing
  - Precision Resistor Current Sensing
- Programmable 1, 2 or 3-Phase Operation
- Adaptive Body Diode Conduction Time Reduction
- Superior Noise Immunity and Transient Response
- Pin Programmable Output Voltage and Power State Mode
- Output Current Monitor and Thermal Monitor
- Differential Remote Voltage Sensing
- High Efficiency Across Entire Load Range
- Programmable Switching Frequency
- Resistor Programmable VBOOT, Power State Operation, SVID Address Setting, I_{MAX}
- Excellent Dynamic Current Balance Between Phases
- OCP/WOC, OVP, OT Alert, PGOOD
- Small Footprint 40 Ld 5x5 TQFN Package
- Pb-Free (RoHS Compliant)

Applications

- DDR Memory

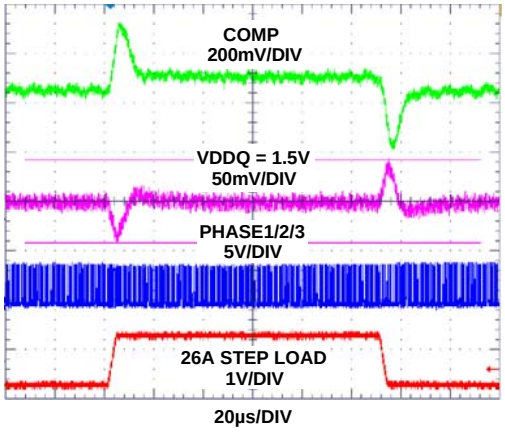


FIGURE 1. FAST TRANSIENT RESPONSE

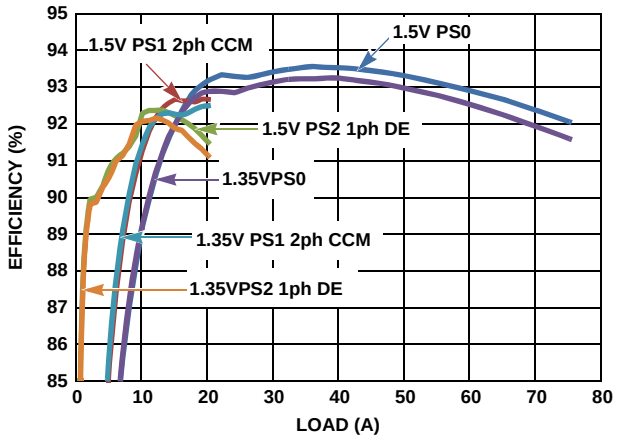
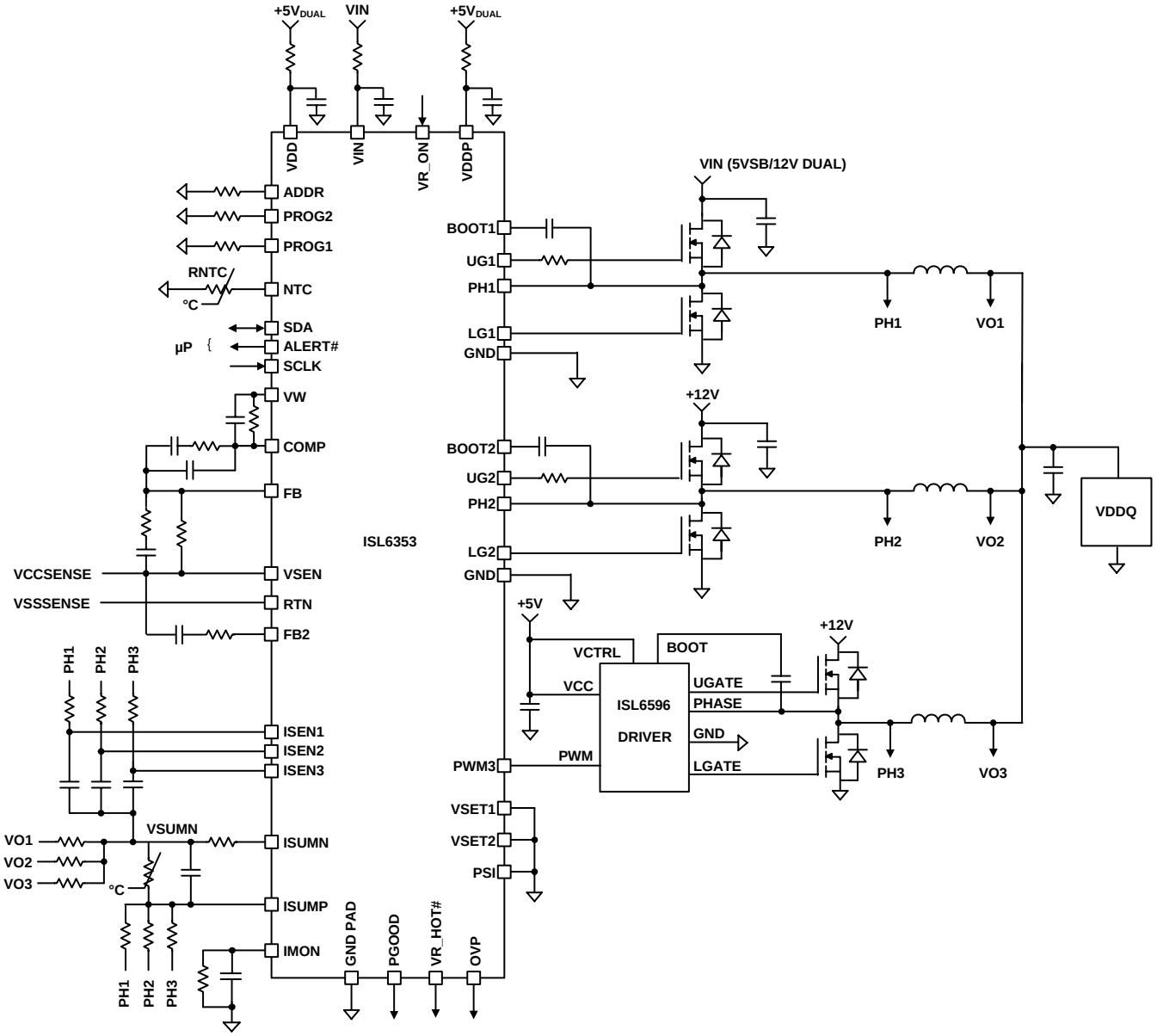
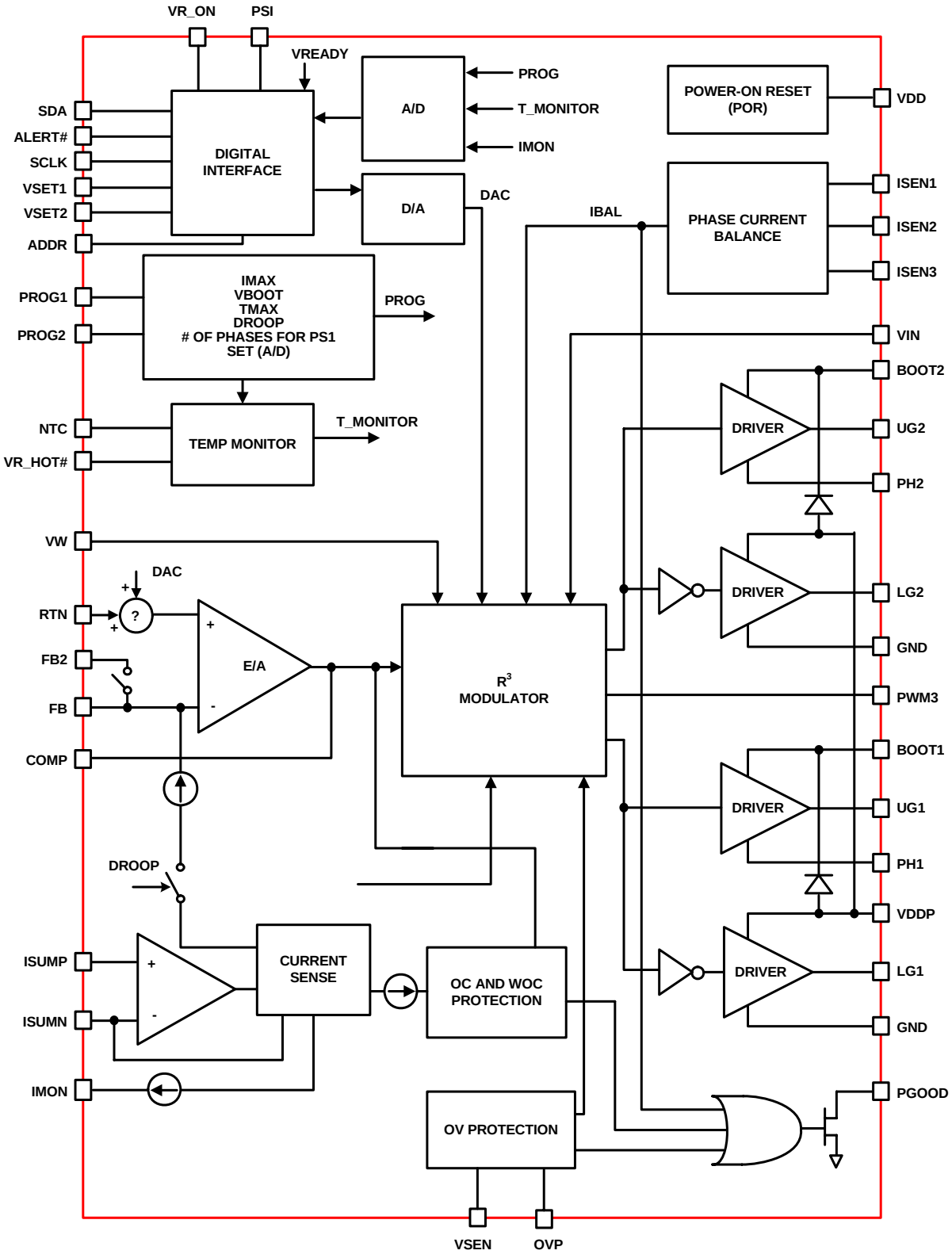


FIGURE 2. ISL6353EVAL1Z EFFICIENCY vs LOAD

Simplified Application Circuit Using Inductor DCR Current Sensing

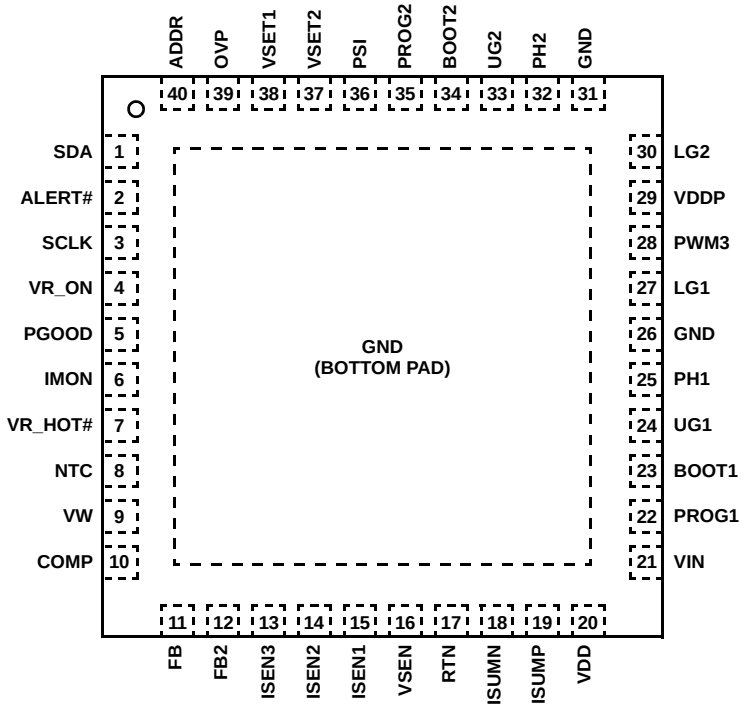


Block Diagram



Pin Configuration

ISL6353
(40 LD TQFN)
TOP VIEW



Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1, 2, 3	SDA, ALERT#, SCLK	Serial communication bus signals connected between the CPU and the voltage regulator.
4	VR_ON	Voltage regulator enable input. A high level logic signal on this pin enables the VR.
5	PGOOD	Open-drain output to indicate the regulator is ready to supply regulated voltage. Use an appropriate external pull-up resistor.
6	IMON	Output current monitor pin. IMON sources a current proportional to the regulator output current. A resistor connected from this pin to ground will set a voltage that is proportional to the load current. This voltage is sampled with an internal ADC to produce a digital IMON signal that can be read through the serial communications bus.
7	VR_HOT#	Thermal overload output indicator.
8	NTC	Thermistor input to the VR_HOT# circuit.
9	VW	Window voltage set pin used to set the switching frequency. A resistor from this pin to COMP programs the switching frequency (18kΩ gives approximately 300kHz).
10	COMP	This pin is the output of the error amplifier.
11	FB	This pin is the inverting input of the error amplifier.
12	FB2	This pin switches in an RC network from VOUT to FB in PS1 and PS2 modes to help improve transient performance and phase margin when dropping phases in low power states. There is a switch between the FB2 pin and the FB pin. The switch is off in the PS0 state and on in the PS1 and PS2 states. If this function is not needed, the pin can be left open.
13	ISEN3	Individual current sensing input for Phase 3. Leave this pin open when ISL6353 is configured in 2-phase mode.
14	ISEN2	Individual current sensing input for Phase 2. When ISEN2 is pulled to 5V VDD, the controller will disable Phase 2, and the controller will run in 1-phase mode.
15	ISEN1	Individual current sensing input for Phase 1.
16	VSEN	Output voltage sense pin. Connect to the output voltage (typically VDDQ) at the desired remote voltage sensing location.

Pin Descriptions (Continued)

PIN NUMBER	SYMBOL	DESCRIPTION
17	RTN	Output voltage sense return pin. Connect to the ground at desired remote sensing location.
18, 19	ISUMN and ISUMP	Inverting and non-inverting input of the transconductance amplifier for current monitoring and OCP.
20	VDD	5V bias power.
21	VIN	Input supply voltage, used for input supply feed-forward compensation.
22	PROG1	The program pin for the voltage regulator I_{MAX} setting. Refer to Table 6.
23	BOOT1	Connect an MLCC capacitor across the BOOT1 and the PH1 pins. The boot capacitor is charged through an internal switch connected from the VDDP pin to the BOOT1 pin.
24	UG1	Output of the Phase 1 high-side MOSFET gate driver. Connect the UG1 pin to the gate of the Phase 1 high-side MOSFET.
25	PH1	Current return path for the Phase 1 high-side MOSFET gate driver. Connect the PH1 pin to the node consisting of the high-side MOSFET source, the low-side MOSFET drain, and the output inductor of Phase 1.
26	GND	This is an electrical ground connection for the IC. Connect this pin to the ground plane of the PCB right next to the controller or to the exposed pad on the back of the IC using a low impedance path.
27	LG1	Output of the Phase 1 low-side MOSFET gate driver. Connect the LG1 pin to the gate of the Phase 1 low-side MOSFET.
28	PWM3	PWM output for Phase 3. When PWM3 is pulled to 5V VDD, the controller will disable Phase 3 and allow other phases to operate.
29	VDDP	Input voltage bias for the internal gate drivers. Connect +5V to the VDDP pin. Decouple with at least 1µF using an MLCC capacitor to the ground plane close to the IC.
30	LG2	Output of the Phase 2 low-side MOSFET gate driver. Connect the LG2 pin to the gate of the Phase 2 low-side MOSFET.
31	GND	This is an electrical ground connection for the IC. Connect this pin to the ground plane of the PCB right next to the controller or to the exposed pad on the back of the IC using a low impedance path.
32	PH2	Current return path for the Phase 2 high-side MOSFET gate driver. Connect the PH2 pin to the node consisting of the high-side MOSFET source, the low-side MOSFET drain, and the output inductor of Phase 2.
33	UG2	Output of the Phase 2 high-side MOSFET gate driver. Connect the UG2 pin to the gate of the Phase 2 high-side MOSFET.
34	BOOT2	Connect an MLCC capacitor across the BOOT2 and the PH2 pins. The boot capacitor is charged through an internal switch connected from the VDDP pin to the BOOT2 pin.
35	PROG2	The program pin for the voltage regulator V_{BOOT} voltage, droop enable/disable and the number of active phases for PS1 mode.
36	PSI	This pin can be used to set the power state of the controller with external logic signals. By connecting this pin to ground, the controller will refer only to the power state indicated by the serial communication bus register. If the pin is connected to a high impedance, the controller will enter the PS1 state. If the pin is connected to a logic high, the controller will enter the PS2 state.
37	VSET2	This pin is a logic input that can be used in conjunction with VSET1 to program the output voltage of the regulator with external logic signals. Refer to Table 9. By connecting VSET1 and VSET2 to ground, the controller will refer to the VID setting indicated by the serial communication bus register.
38	VSET1	This pin is a logic input that can be used in conjunction with VSET2 to program the output voltage of the regulator with external signals. Refer to Table 9. By connecting VSET1 and VSET2 to ground, the controller will refer to the VID setting indicated by the serial communication bus register.
39	OVP	An inverter output, latched high for an overvoltage event. It is reset by POR.
40	ADDR	This pin sets the address offset register, range from 0 to 13 (0h to Dh).
-	GND (Bottom Pad)	Electrical ground of the IC. Unless otherwise stated, all signals are referenced to the GND pin. Connect this ground pad to the ground plane through a low impedance path. Recommend use of at least 5 vias to connect to ground planes in PCB internal layers.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL6353CRTZ	ISL6353 CRTZ	0 to +70	40 Ld 5x5 TQFN	L40.5x5
ISL6353IRTZ	ISL6353 IRTZ	-40 to +85	40 Ld 5x5 TQFN	L40.5x5
ISL6353EVAL1Z	Evaluation Board			

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL6353. For more information on MSL please see techbrief TB363.

Table of Contents

Absolute Maximum Ratings

Supply Voltage, VDD . . . . . -0.3V to +7V
Input Supply Voltage, VIN . . . . . +28V
Boot Voltage (BOOT) . . . . . -0.3V to +33V
Boot to Phase Voltage (BOOT-PHASE) . . . . . -0.3V to +7V(DC)
. . . . . -0.3V to +9V(<10ns)
Phase Voltage (PHASE) . . . . . -7V (<20ns Pulse Width, 10µJ)
UGATE Voltage (UGATE) . . . . . PHASE - 0.3V (DC) to BOOT
. . . . . PHASE-5V (<20ns Pulse Width, 10µJ) to BOOT
LGATE Voltage (LGATE) . . . . . -0.3V (DC) to VDD + 0.3V
. . . . . -2.5V (<20ns Pulse Width, 5µJ) to VDD + 0.3V
All Other Pins . . . . . -0.3V to (VDD +0.3V)
Open Drain Outputs, PGOOD, VR_HOT#, ALERT# . . . . . -0.3V to +7V
ESD Rating
Human Body Model (Tested per JESD22-A114E) 2000V
Machine Model (Tested per JESD22-A115-A) 200V
Charged Device Model (Tested per JESD22-C101A) 750V
Latch Up (Tested per JESD-78B; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
40 Ld TQFN Package (Notes 4, 5)	32	3

Maximum Junction Temperature . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Supply Voltage, VDD . . . . . +5V ±5%
Input Voltage, VIN . . . . . +4.5V to 25V
Ambient Temperature
ISL6353CRTZ . . . . . 0°C to +70°C
ISL6353IRTZ . . . . . -40°C to +85°C
Junction Temperature
ISL6353CRTZ . . . . . 0°C to +125°C
ISL6353IRTZ . . . . . -40°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Operating Conditions: V_{DD} = 5V, T_A = 0°C to +70°C for ISL6353CRTZ and T_A = -40°C to +85°C for ISL6353IRTZ, f_{SW} = 300kHz, unless otherwise noted. **Boldface limits apply over the operating temperature range.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
INPUT POWER SUPPLY						
+5V Supply Current	I_{VDD}	VR_ON = 1V		4	**4.6**	mA
		VR_ON = 0V			**1**	µA
Input Supply Current	I_{VIN}	VR_ON = 0V			**1**	µA
Power-On-Reset Threshold	POR_r	V_{DD} rising		4.35	**4.5**	V
	POR_f	V_{DD} falling	**4.00**	4.15		V
	POR_r	VIN pin rising		4.00	4.35	V
	POR_f	VIN pin falling	**2.8**	3.50		V
SYSTEM AND REFERENCES						
System Accuracy	CRTZ %Error (V_{CC_CORE})	No load; closed loop, active mode range VID = 0.75V to 1.50V,	**-0.5**		**+0.5**	%
		VID = 0.5V to 0.7375V	**-8**		**8**	mV
		VID = 0.3V to 0.4875V	**-15**		**15**	mV
	IRTZ %Error (V_{CC_CORE})	No load; closed loop, active mode range VID = 0.75V to 1.50V,	**-0.8**		**0.8**	%
		VID = 0.5V to 0.7375V	**-10**		**10**	mV
		VID = 0.3V to 0.4875V	**-18**		**18**	mV
Maximum Output Voltage + Offset	$V_{CC\_CORE(max)}$	VID = FFh OFFSET = 7Fh		1.520+ 0.635 = 2.155		V
Minimum Output Voltage	$V_{CC\_CORE(min)}$	VID = 01h OFFSET = 00h		0.25		V

Electrical Specifications Operating Conditions: V_{DD} = 5V, T_A = 0°C to +70°C for ISL6353CRTZ and T_A = -40°C to +85°C for ISL6353IRTZ, f_{SW} = 300kHz, unless otherwise noted. **Boldface limits apply over the operating temperature range. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
CHANNEL FREQUENCY						
Nominal Channel Frequency	$f_{SW(nom)}$	R_{FSET} = 18kΩ, 3-channel operation, V_{COMP} = 1V	**280**	300	**320**	kHz
Adjustment Range			**200**		**500**	kHz
AMPLIFIERS						
Current-Sense Amplifier Input Offset		I_{FB} = 0A	**-0.1**		**+0.1**	mV
Error Amp DC Gain	A_{V0}			119		dB
Error Amp Gain-Bandwidth Product	GBW	C_L = 20pF		17		MHz
ISEN1/2/3						
Input Bias Current				20		nA
POWER GOOD AND PROTECTION MONITORS						
PGOOD Low Voltage	V_{OL}	I_{PGOOD} = 4mA		0.26	**0.4**	V
PGOOD Leakage Current	I_{OH}	PGOOD = 3.3V	**-1**		**1**	µA
ALERT# Pull-Down Resistance				7	**13**	Ω
ALERT# Leakage Current					**1**	µA
VR_HOT# Pull-Down Resistance				7	**13**	Ω
VR_HOT# Leakage Current					**1**	µA
GATE DRIVER						
UGATE Pull-Up Resistance	R_{UGPU}	200mA Source Current		1.0	**1.5**	Ω
UGATE Source Current	I_{UGSRC}	UGATE - PHASE = 2.5V		2.0		A
UGATE Sink Resistance	R_{UGPD}	250mA Sink Current		1.0	**1.5**	Ω
UGATE Sink Current	I_{UGSNK}	UGATE - PHASE = 2.5V		2.0		A
LGATE Pull-Up Resistance	R_{LGPU}	250mA Source Current		1.0	**1.5**	Ω
LGATE Source Current	I_{LGSRC}	LGATE - GND = 2.5V		2.0		A
LGATE Sink Resistance	R_{LGPD}	250mA Sink Current		0.5	**0.9**	Ω
LGATE Sink Current	I_{LGSNK}	LGATE - GND = 2.5V		4.0		A
UGATE to LGATE Deadtime	t_{UGFLGR}	UGATE falling to LGATE rising, no load		23		ns
LGATE to UGATE Deadtime	t_{LGFUGR}	LGATE falling to UGATE rising, no load		28		ns
PROTECTION FUNCTIONS						
Pre-Charge Overvoltage Threshold	OV_P	VSEN rising above setpoint for >1ms	**2.29**	2.35		V
Overvoltage Threshold	OV_H	VSEN rising above setpoint for >1ms	**145**	175	**200**	mV
OVP Pin Sink Current	I_{OVP}	V_{OVP} = VDD - 1V	**20**			mA
Overcurrent Threshold	CRTZ	3/2/1-Phase Config, PS0	**56.5**	60	**64.5**	µA
	IRTZ	3/2/1-Phase Config, PS0	**54.5**	60	**64.5**	µA
	CRTZ	3-Phase Config, PS1 - Drop to 2-Phase	**38.3**	40	**43.2**	µA
	IRTZ	3-Phase Config, PS1 - Drop to 2-Phase	**37**	40	**43.2**	µA
	CRTZ	3-Phase Config, PS1/2 - Drop to 1-Phase	**19**	20	**22.25**	µA
	IRTZ	3-Phase Config, PS1/2 - Drop to 1-Phase	**18.5**	20	**22.25**	µA
	CRTZ	2-Phase Config, PS1/2 - Drop to 1-Phase	**28**	30	**33**	µA
	IRTZ	2-Phase Config, PS1/2 - Drop to 1-Phase	**27**	30	**33**	µA

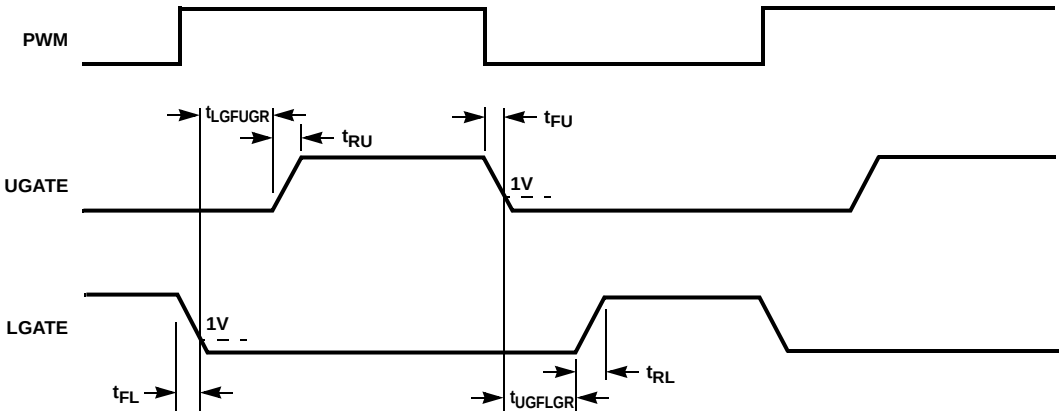
Electrical Specifications Operating Conditions: V_{DD} = 5V, T_A = 0°C to +70°C for ISL6353CRTZ and T_A = -40°C to +85°C for ISL6353IRTZ, f_{SW} = 300kHz, unless otherwise noted. **Boldface limits apply over the operating temperature range. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
Way Overcurrent Threshold	CRTZ	3/2/1-Phase Config, PS0	**76.8**	88	**100**	µA
	IRTZ	3/2/1-Phase Config, PS0	**74**	88	**100**	µA
	CRTZ	3-Phase Config, PS1 - Drop to 2-Phase	**52**	60	**68**	µA
	IRTZ	3-Phase Config, PS1 - Drop to 2-Phase	**50**	60	**68**	µA
	CRTZ	3-Phase Config, PS1/2 - Drop to 1-Phase	**28**	32	**35.8**	µA
	IRTZ	3-Phase Config, PS1/2 - Drop to 1-Phase	**27**	32	**35.8**	µA
	CRTZ	2-Phase Config, PS1/2 - Drop to 1-Phase	**40**	46	**52**	µA
	IRTZ	2-Phase Config, PS1/2 - Drop to 1-Phase	**39.5**	46	**52**	µA
Current Imbalance Threshold		One ISEN above another ISEN for >1.2ms		20		mV
PWM						
PWM3 Output Low	V_{OL_MAX}	Sinking 5mA			**1.0**	V
PWM3 Output High	V_{OH_MIN}	Sourcing 5mA	**3.5**			V
PWM3 Tri-State Leakage		PWM3 = 2.5V		2		µA
THERMAL MONITOR						
NTC Source Current	CRTZ	NTC = 1.3V	**58**	60	**62**	µA
	IRTZ	NTC = 1.3V	**56**	60	**62**	µA
VR_HOT# Trip Voltage		Falling	**0.895**	0.91		V
VR_HOT# Reset Voltage		Rising		0.95	**0.965**	V
ALERT# Trip Voltage		Falling	**0.915**	0.93		V
ALERT# Reset Voltage		Rising		0.97	**0.985**	V
CURRENT MONITOR						
IMON Output Current	I_{IMON}	ISUM- pin current = 50µA	**12.3**	12.45	**12.6**	µA
		ISUM- pin current = 2µA	**400**	500	**600**	nA
IccMAX Alert Trip Voltage	$V_{IMONMAX}$	Rising		1.2	**1.225**	V
IccMAX Alert Reset Voltage		Falling	**1.05**	1.14		V
INPUTS						
VR_ON Input Low	V_{IL_MAX}				**0.3**	V
VR_ON Input High	V_{IH_MIN}		**0.8**			V
VR_ON Leakage Current	I_{VR_ON}	VR_ON = 0V	**-1**	0		µA
		VR_ON = 1V, 300kΩ Typical Pull-Down		3.3		µA
VSET1/2 Input Low	$VSET_{IL\_MAX}$				**1.5**	V
VSET1/2 Input High	$VSET_{IH\_MIN}$		**3.1**			V
PSI Sink/Source Current		PSI Voltage	**12**	16	**20**	µA
PSI Pin State		PS0, V_{DD} = 5V	**0**		**0.51**	V
		PS1, V_{DD} = 5V	**1.06**		**3.91**	V
		PS2, V_{DD} = 5V	**4.47**		**5**	V
PSI High-Z Voltage			**2.12**	2.37	**2.60**	V
SCLK, SDA						
SCLK, SDA Leakage		VR_ON = 0V, SCLK & SDA = 0V & 1V	**-1**		**1**	µA
		VR_ON = 1V, SCLK & SDA = 1V	**-5**		**1**	µA
		VR_ON = 1V, SDA = 0V		20		µA
		VR_ON = 1V, SCLK = 0V		40		µA

NOTE:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Gate Driver Timing Diagram



Theory of Operation

Multiphase R^3 Modulator

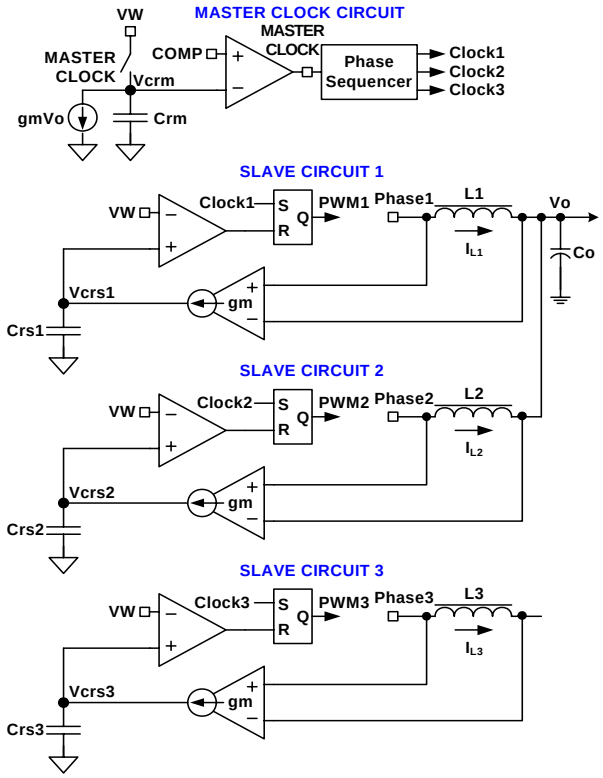


FIGURE 3. R^3 MODULATOR CIRCUIT

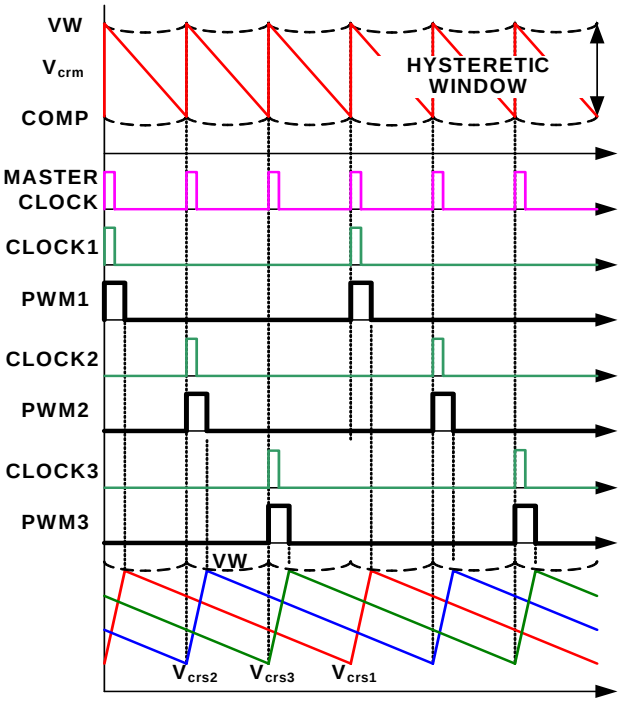


FIGURE 4. R^3 MODULATOR OPERATION PRINCIPLES IN STEADY STATE

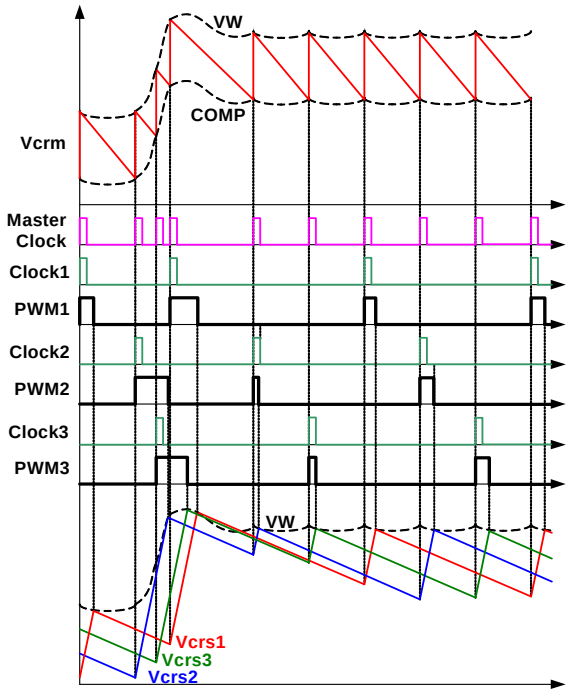


FIGURE 5. R^3 MODULATOR OPERATION DURING A LOAD STEP-UP RESPONSE

The ISL6353 is a multiphase regulator controller implementing the Intel VR12™ protocol primarily intended for use in DDR memory regulator applications. It can be programmed for 1-, 2- or 3-phase operation. It uses Intersil's patented R^3 (Robust Ripple Regulator™) modulator. The R^3 modulator combines the best features of fixed frequency PWM and hysteretic PWM while eliminating many of their respective shortcomings. Figure 3 conceptually shows the ISL6353 multiphase R^3 modulator circuit, and Figure 4 shows the principle of operation.

A current source flows from the VW pin to the COMP pin, creating a voltage window set by the resistor between the two pins. This voltage window is called the VW window in the following discussion.

Inside the IC, the modulator uses the master clock circuit to generate the clocks for the slave circuits. The modulator discharges the ripple capacitor C_{rm} with a current source equal to $g_m V_o$, where g_m is a gain factor. The C_{rm} voltage V_{crm} is a sawtooth waveform traversing between the VW and COMP voltages. It resets to VW when it hits COMP, and generates a one-shot master clock signal. A phase sequencer distributes the master clock signal to the slave circuits. If the ISL6353 is in 3-phase mode, the master clock signal will be distributed to the three phases, and the Clock1~3 signals will be 120° out-of-phase. If the ISL6353 is in 2-phase mode, the master clock signal will be distributed to Phases 1 and 2, and the Clock1 and Clock2 signals will be 180° out-of-phase. If the ISL6353 is in 1-phase mode, the master clock signal will be distributed to Phase 1 only and is the Clock1 signal.

Each slave circuit has its own ripple capacitor C_{rs}, whose voltage mimics the inductor ripple current. A g_m amplifier converts the inductor voltage into a current source to charge and discharge C_{rs}. The slave circuit turns on its PWM pulse upon receiving the clock signal, and the current source charges C_{rs}. When C_{rs} voltage V_{Crs} hits VW, the slave circuit turns off the PWM pulse, and the current source discharges C_{rs}.

Since the ISL6353 individual phase modulators use a large-amplitude and noise-free synthesized signal, V_{crs}, to determine the pulse width, phase jitter is lower than conventional hysteretic mode and fixed PWM mode controllers. Unlike conventional hysteretic mode converters, the ISL6353 has an error amplifier that allows the controller to maintain 0.5% output voltage accuracy.

Figure 5 shows the principle of operation during a load step-up response. The COMP voltage rises after the load step up, generating master clock pulses more quickly, so PWM pulses turn on earlier, increasing the effective switching frequency. This allows for higher control loop bandwidth than conventional fixed frequency PWM controllers. The VW voltage rises as the COMP voltage rises, making the PWM pulses wider as well. During load step-down response, COMP voltage falls. It takes the master clock circuit longer to generate the next clock signal, so the PWM pulse is held off until needed. The VW voltage falls as the COMP voltage falls, reducing the current PWM pulse width. This kind of behavior gives the ISL6353 excellent load transient response.

The fact that all the phases share the same VW window voltage also ensures excellent dynamic current balance among phases.

Diode Emulation and Period Stretching

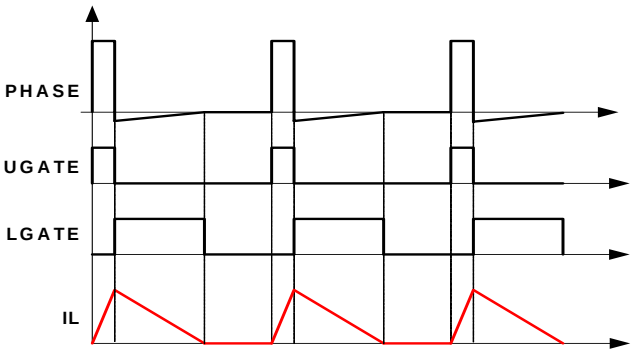


FIGURE 6. DIODE EMULATION OPERATION

ISL6353 can operate in diode emulation (DE) mode to improve light load efficiency. In DE mode, the low-side MOSFET conducts when the current is flowing from source to drain and does not allow reverse current, thus emulating a diode. As Figure 6 shows, when LGATE is on, the low-side MOSFET carries current, creating negative voltage on the phase node due to the voltage drop across the ON-resistance. The ISL6353 monitors the current by monitoring the phase node voltage. It turns off LGATE when the phase node voltage reaches zero to prevent the inductor current from reversing direction and creating unnecessary power loss.

If the load current is light enough, as Figure 6 shows, the inductor current will reach and stay at zero before the next phase node pulse, and the regulator is in discontinuous conduction mode (DCM). If the load current is heavy enough, the inductor current will never reach 0A, and the regulator is in CCM although the controller is in DE mode.

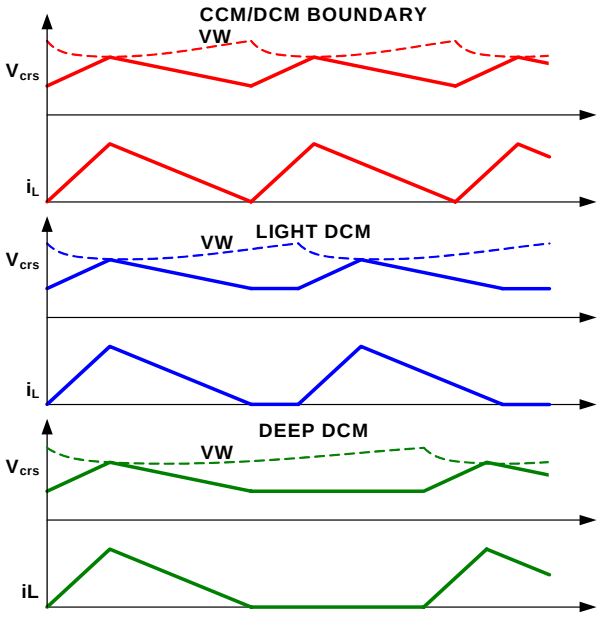


FIGURE 7. PERIOD STRETCHING

Figure 7 shows the principle of operation in diode emulation mode at light load. The load gets incrementally lighter in the three cases from top to bottom. The PWM on-time is determined by the VW window size and therefore it is the same, making the inductor current triangle the same in the three cases. The ISL6353 clamps the ripple capacitor voltage V_{crs} in DE mode to make it mimic the inductor current. It takes the COMP voltage longer to hit V_{crs}, naturally stretching the switching period. The inductor current triangles move further apart from each other such that the inductor current average value is equal to the load current. The reduced switching frequency helps increase light load efficiency.

Start-up Timing

With the controller's V_{DD} voltage above the POR threshold, the start-up sequence begins about 1.3ms after VR_ON exceeds the logic high threshold. The ISL6353 uses digital soft-start to ramp up the DAC to the boot voltage, V_{BOOT}. V_{BOOT} is set by the PROG2 pin resistor and the status of the VSET1/2 pins. The DAC slew rate during soft-start is about 2.5mV/µs. PGOOD is asserted high at the end of the start-up sequence indicating that the output voltage has moved to the V_{BOOT} setting, the VR is operating properly and all phases are switching. Figure 8 shows the typical start-up timing.

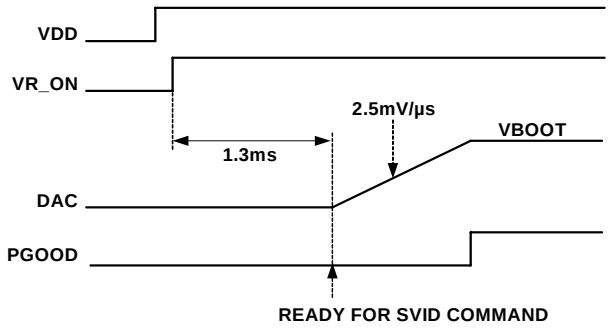


FIGURE 8. SOFT-START WAVEFORMS

Voltage Regulation and Differential Sensing

After the start sequence, the ISL6353 regulates the output voltage to the value set by the SetVID commands through the SVID bus or to the value set by the status of the VSET1/2 pins. The ISL6353 will regulate the output voltage to VID + OFFSET (Register 33h). A differential amplifier allows remote voltage sensing for precise voltage regulation.

VID Table

The ISL6353 will regulate the output voltage to VID+OFFSET (33h). Table 1 shows the output voltage setting based on the VID register setting.

TABLE 1. VID TABLE

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Hex		V_O (V)
0	0	0	0	0	0	0	0	0	0	0.0000
0	0	0	0	0	0	0	1	0	1	0.2500
0	0	0	0	0	0	1	0	0	2	0.2550
0	0	0	0	0	0	1	1	0	3	0.2600
0	0	0	0	0	1	0	0	0	4	0.2650
0	0	0	0	0	1	0	1	0	5	0.2700
0	0	0	0	0	1	1	0	0	6	0.2750
0	0	0	0	0	1	1	1	0	7	0.2800
0	0	0	0	1	0	0	0	0	8	0.2850
0	0	0	0	1	0	0	1	0	9	0.2900
0	0	0	0	1	0	1	0	0	A	0.2950
0	0	0	0	1	0	1	1	0	B	0.3000
0	0	0	0	1	1	0	0	0	C	0.3050
0	0	0	0	1	1	0	1	0	D	0.3100
0	0	0	0	1	1	1	0	0	E	0.3150
0	0	0	0	1	1	1	1	0	F	0.3200
0	0	0	1	0	0	0	0	1	0	0.3250
0	0	0	1	0	0	0	1	1	1	0.3300
0	0	0	1	0	0	1	0	1	2	0.3350
0	0	0	1	0	0	1	1	1	3	0.3400
0	0	0	1	0	1	0	0	1	4	0.3450
0	0	0	1	0	1	0	1	1	5	0.3500

TABLE 1. VID TABLE (Continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Hex		V_O (V)
0	0	0	1	0	1	1	0	1	6	0.3550
0	0	0	1	0	1	1	1	1	7	0.3600
0	0	0	1	1	0	0	0	1	8	0.3650
0	0	0	1	1	0	0	1	1	9	0.3700
0	0	0	1	1	0	1	0	1	A	0.3750
0	0	0	1	1	0	1	1	1	B	0.3800
0	0	0	1	1	1	0	0	1	C	0.3850
0	0	0	1	1	1	0	1	1	D	0.3900
0	0	0	1	1	1	1	0	1	E	0.3950
0	0	0	1	1	1	1	1	1	F	0.4000
0	0	1	0	0	0	0	0	2	0	0.4050
0	0	1	0	0	0	0	1	2	1	0.4100
0	0	1	0	0	0	1	0	2	2	0.4150
0	0	1	0	0	0	1	1	2	3	0.4200
0	0	1	0	0	1	0	0	2	4	0.4250
0	0	1	0	0	1	0	1	2	5	0.4300
0	0	1	0	0	1	1	0	2	6	0.4350
0	0	1	0	0	1	1	1	2	7	0.4400
0	0	1	0	1	0	0	0	2	8	0.4450
0	0	1	0	1	0	0	1	2	9	0.4500
0	0	1	0	1	0	1	0	2	A	0.4550
0	0	1	0	1	0	1	1	2	B	0.4600
0	0	1	0	1	1	0	0	2	C	0.4650
0	0	1	0	1	1	0	1	2	D	0.4700
0	0	1	0	1	1	1	0	2	E	0.4750
0	0	1	0	1	1	1	1	2	F	0.4800
0	0	1	1	0	0	0	0	3	0	0.4850
0	0	1	1	0	0	0	1	3	1	0.4900
0	0	1	1	0	0	1	0	3	2	0.4950
0	0	1	1	0	0	1	1	3	3	0.5000
0	0	1	1	0	1	0	0	3	4	0.5050
0	0	1	1	0	1	0	1	3	5	0.5100
0	0	1	1	0	1	1	0	3	6	0.5150
0	0	1	1	0	1	1	1	3	7	0.5200
0	0	1	1	1	0	0	0	3	8	0.5250
0	0	1	1	1	0	0	1	3	9	0.5300
0	0	1	1	1	0	1	0	3	A	0.5350
0	0	1	1	1	0	1	1	3	B	0.5400
0	0	1	1	1	1	0	0	3	C	0.5450
0	0	1	1	1	1	0	1	3	D	0.5500
0	0	1	1	1	1	1	0	3	E	0.5550
0	0	1	1	1	1	1	1	3	F	0.5600

TABLE 1. VID TABLE (Continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Hex		V_O (V)
0	1	0	0	0	0	0	0	4	0	0.5650
0	1	0	0	0	0	0	1	4	1	0.5700
0	1	0	0	0	0	1	0	4	2	0.5750
0	1	0	0	0	0	1	1	4	3	0.5800
0	1	0	0	0	1	0	0	4	4	0.5850
0	1	0	0	0	1	0	1	4	5	0.5900
0	1	0	0	0	1	1	0	4	6	0.5950
0	1	0	0	0	1	1	1	4	7	0.6000
0	1	0	0	1	0	0	0	4	8	0.6050
0	1	0	0	1	0	0	1	4	9	0.6100
0	1	0	0	1	0	1	0	4	A	0.6150
0	1	0	0	1	0	1	1	4	B	0.6200
0	1	0	0	1	1	0	0	4	C	0.6250
0	1	0	0	1	1	0	1	4	D	0.6300
0	1	0	0	1	1	1	0	4	E	0.6350
0	1	0	0	1	1	1	1	4	F	0.6400
0	1	0	1	0	0	0	0	5	0	0.6450
0	1	0	1	0	0	0	1	5	1	0.6500
0	1	0	1	0	0	1	0	5	2	0.6550
0	1	0	1	0	0	1	1	5	3	0.6600
0	1	0	1	0	1	0	0	5	4	0.6650
0	1	0	1	0	1	0	1	5	5	0.6700
0	1	0	1	0	1	1	0	5	6	0.6750
0	1	0	1	0	1	1	1	5	7	0.6800
0	1	0	1	1	0	0	0	5	8	0.6850
0	1	0	1	1	0	0	1	5	9	0.6900
0	1	0	1	1	0	1	0	5	A	0.6950
0	1	0	1	1	0	1	1	5	B	0.7000
0	1	0	1	1	1	0	0	5	C	0.7050
0	1	0	1	1	1	0	1	5	D	0.7100
0	1	0	1	1	1	1	0	5	E	0.7150
0	1	0	1	1	1	1	1	5	F	0.7200
0	1	1	0	0	0	0	0	6	0	0.7250
0	1	1	0	0	0	0	1	6	1	0.7300
0	1	1	0	0	0	1	0	6	2	0.7350
0	1	1	0	0	0	1	1	6	3	0.7400
0	1	1	0	0	1	0	0	6	4	0.7450
0	1	1	0	0	1	0	1	6	5	0.7500
0	1	1	0	0	1	1	0	6	6	0.7550
0	1	1	0	0	1	1	1	6	7	0.7600
0	1	1	0	1	0	0	0	6	8	0.7650
0	1	1	0	1	0	0	1	6	9	0.7700

TABLE 1. VID TABLE (Continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Hex		V_O (V)
0	1	1	0	1	0	1	0	6	A	0.7750
0	1	1	0	1	0	1	1	6	B	0.7800
0	1	1	0	1	1	0	0	6	C	0.7850
0	1	1	0	1	1	0	1	6	D	0.7900
0	1	1	0	1	1	1	0	6	E	0.7950
0	1	1	0	1	1	1	1	6	F	0.8000
0	1	1	1	0	0	0	0	7	0	0.8050
0	1	1	1	0	0	0	1	7	1	0.8100
0	1	1	1	0	0	1	0	7	2	0.8150
0	1	1	1	0	0	1	1	7	3	0.8200
0	1	1	1	0	1	0	0	7	4	0.8250
0	1	1	1	0	1	0	1	7	5	0.8300
0	1	1	1	0	1	1	0	7	6	0.8350
0	1	1	1	0	1	1	1	7	7	0.8400
0	1	1	1	1	0	0	0	7	8	0.8450
0	1	1	1	1	0	0	1	7	9	0.8500
0	1	1	1	1	0	1	0	7	A	0.8550
0	1	1	1	1	0	1	1	7	B	0.8600
0	1	1	1	1	1	0	0	7	C	0.8650
0	1	1	1	1	1	0	1	7	D	0.8700
0	1	1	1	1	1	1	0	7	E	0.8750
0	1	1	1	1	1	1	1	7	F	0.8800
1	0	0	0	0	0	0	0	8	0	0.8850
1	0	0	0	0	0	0	1	8	1	0.8900
1	0	0	0	0	0	1	0	8	2	0.8950
1	0	0	0	0	0	1	1	8	3	0.9000
1	0	0	0	0	1	0	0	8	4	0.9050
1	0	0	0	0	1	0	1	8	5	0.9100
1	0	0	0	0	1	1	0	8	6	0.9150
1	0	0	0	0	1	1	1	8	7	0.9200
1	0	0	0	1	0	0	0	8	8	0.9250
1	0	0	0	1	0	0	1	8	9	0.9300
1	0	0	0	1	0	1	0	8	A	0.9350
1	0	0	0	1	0	1	1	8	B	0.9400
1	0	0	0	1	1	0	0	8	C	0.9450
1	0	0	0	1	1	0	1	8	D	0.9500
1	0	0	0	1	1	1	0	8	E	0.9550
1	0	0	0	1	1	1	1	8	F	0.9600
1	0	0	1	0	0	0	0	9	0	0.9650
1	0	0	1	0	0	0	1	9	1	0.9700
1	0	0	1	0	0	1	0	9	2	0.9750
1	0	0	1	0	0	1	1	9	3	0.9800

TABLE 1. VID TABLE (Continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Hex		V_O (V)
1	0	0	1	0	1	0	0	9	4	0.9850
1	0	0	1	0	1	0	1	9	5	0.9900
1	0	0	1	0	1	1	0	9	6	0.9950
1	0	0	1	0	1	1	1	9	7	1.0000
1	0	0	1	1	0	0	0	9	8	1.0050
1	0	0	1	1	0	0	1	9	9	1.0100
1	0	0	1	1	0	1	0	9	A	1.0150
1	0	0	1	1	0	1	1	9	B	1.0200
1	0	0	1	1	1	0	0	9	C	1.0250
1	0	0	1	1	1	0	1	9	D	1.0300
1	0	0	1	1	1	1	0	9	E	1.0350
1	0	0	1	1	1	1	1	9	F	1.0400
1	0	1	0	0	0	0	0	A	0	1.0450
1	0	1	0	0	0	0	1	A	1	1.0500
1	0	1	0	0	0	1	0	A	2	1.0550
1	0	1	0	0	0	1	1	A	3	1.0600
1	0	1	0	0	1	0	0	A	4	1.0650
1	0	1	0	0	1	0	1	A	5	1.0700
1	0	1	0	0	1	1	0	A	6	1.0750
1	0	1	0	0	1	1	1	A	7	1.0800
1	0	1	0	1	0	0	0	A	8	1.0850
1	0	1	0	1	0	0	1	A	9	1.0900
1	0	1	0	1	0	1	0	A	A	1.0950
1	0	1	0	1	0	1	1	A	B	1.1000
1	0	1	0	1	1	0	0	A	C	1.1050
1	0	1	0	1	1	0	1	A	D	1.1100
1	0	1	0	1	1	1	0	A	E	1.1150
1	0	1	0	1	1	1	1	A	F	1.1200
1	0	1	1	0	0	0	0	B	0	1.1250
1	0	1	1	0	0	0	1	B	1	1.1300
1	0	1	1	0	0	1	0	B	2	1.1350
1	0	1	1	0	0	1	1	B	3	1.1400
1	0	1	1	0	1	0	0	B	4	1.1450
1	0	1	1	0	1	0	1	B	5	1.1500
1	0	1	1	0	1	1	0	B	6	1.1550
1	0	1	1	0	1	1	1	B	7	1.1600
1	0	1	1	1	0	0	0	B	8	1.1650
1	0	1	1	1	0	0	1	B	9	1.1700
1	0	1	1	1	0	1	0	B	A	1.1750
1	0	1	1	1	0	1	1	B	B	1.1800
1	0	1	1	1	1	0	0	B	C	1.1850
1	0	1	1	1	1	0	1	B	D	1.1900

TABLE 1. VID TABLE (Continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Hex		V_O (V)
1	0	1	1	1	1	1	0	B	E	1.1950
1	0	1	1	1	1	1	1	B	F	1.2000
1	1	0	0	0	0	0	0	C	0	1.2050
1	1	0	0	0	0	0	1	C	1	1.2100
1	1	0	0	0	0	1	0	C	2	1.2150
1	1	0	0	0	0	1	1	C	3	1.2200
1	1	0	0	0	1	0	0	C	4	1.2250
1	1	0	0	0	1	0	1	C	5	1.2300
1	1	0	0	0	1	1	0	C	6	1.2350
1	1	0	0	0	1	1	1	C	7	1.2400
1	1	0	0	1	0	0	0	C	8	1.2450
1	1	0	0	1	0	0	1	C	9	1.2500
1	1	0	0	1	0	1	0	C	A	1.2550
1	1	0	0	1	0	1	1	C	B	1.2600
1	1	0	0	1	1	0	0	C	C	1.2650
1	1	0	0	1	1	0	1	C	D	1.2700
1	1	0	0	1	1	1	0	C	E	1.2750
1	1	0	0	1	1	1	1	C	F	1.2800
1	1	0	1	0	0	0	0	D	0	1.2850
1	1	0	1	0	0	0	1	D	1	1.2900
1	1	0	1	0	0	1	0	D	2	1.2950
1	1	0	1	0	0	1	1	D	3	1.3000
1	1	0	1	0	1	0	0	D	4	1.3050
1	1	0	1	0	1	0	1	D	5	1.3100
1	1	0	1	0	1	1	0	D	6	1.3150
1	1	0	1	0	1	1	1	D	7	1.3200
1	1	0	1	1	0	0	0	D	8	1.3250
1	1	0	1	1	0	0	1	D	9	1.3300
1	1	0	1	1	0	1	0	D	A	1.3350
1	1	0	1	1	0	1	1	D	B	1.3400
1	1	0	1	1	1	0	0	D	C	1.3450
1	1	0	1	1	1	0	1	D	D	1.3500
1	1	0	1	1	1	1	0	D	E	1.3550
1	1	0	1	1	1	1	1	D	F	1.3600
1	1	1	0	0	0	0	0	E	0	1.3650
1	1	1	0	0	0	0	1	E	1	1.3700
1	1	1	0	0	0	1	0	E	2	1.3750
1	1	1	0	0	0	1	1	E	3	1.3800
1	1	1	0	0	1	0	0	E	4	1.3850
1	1	1	0	0	1	0	1	E	5	1.3900
1	1	1	0	0	1	1	0	E	6	1.3950
1	1	1	0	0	1	1	1	E	7	1.4000

TABLE 1. VID TABLE (Continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Hex		V_O (V)
1	1	1	0	1	0	0	0	E	8	1.4050
1	1	1	0	1	0	0	1	E	9	1.4100
1	1	1	0	1	0	1	0	E	A	1.4150
1	1	1	0	1	0	1	1	E	B	1.4200
1	1	1	0	1	1	0	0	E	C	1.4250
1	1	1	0	1	1	0	1	E	D	1.4300
1	1	1	0	1	1	1	0	E	E	1.4350
1	1	1	0	1	1	1	1	E	F	1.4400
1	1	1	1	0	0	0	0	F	0	1.4450
1	1	1	1	0	0	0	1	F	1	1.4500
1	1	1	1	0	0	1	0	F	2	1.4550
1	1	1	1	0	0	1	1	F	3	1.4600
1	1	1	1	0	1	0	0	F	4	1.4650
1	1	1	1	0	1	0	1	F	5	1.4700
1	1	1	1	0	1	1	0	F	6	1.4750
1	1	1	1	0	1	1	1	F	7	1.4800
1	1	1	1	1	0	0	0	F	8	1.4850
1	1	1	1	1	0	0	1	F	9	1.4900
1	1	1	1	1	0	1	0	F	A	1.4950
1	1	1	1	1	0	1	1	F	B	1.5000
1	1	1	1	1	1	0	0	F	C	1.5050
1	1	1	1	1	1	0	1	F	D	1.5100
1	1	1	1	1	1	1	0	F	E	1.5150
1	1	1	1	1	1	1	1	F	F	1.5200

VID OFFSET Table

The ISL6353 will regulate the output voltage to VID+OFFSET (33h). Table 2 shows the output voltage setting based on the VID register setting.

TABLE 2. VID TABLE

OFS7	OFS6	OFS5	OFS4	OFS3	OFS2	OFS1	OFS0	Hex		V_{OFS} (V)
0	0	0	0	0	0	0	0	0	0	0.0000
0	0	0	0	0	0	0	1	0	1	0.005
0	0	0	0	0	0	1	0	0	2	0.010
0	0	0	0	0	0	1	1	0	3	0.015
0	0	0	0	0	1	0	0	0	4	0.020
0	0	0	0	0	1	0	1	0	5	0.025
0	0	0	0	0	1	1	0	0	6	0.030
0	0	0	0	0	1	1	1	0	7	0.035
0	0	0	0	1	0	0	0	0	8	0.040
0	0	0	0	1	0	0	1	0	9	0.045
0	0	0	0	1	0	1	0	0	A	0.050

TABLE 2. VID TABLE (Continued)

OFS7	OFS6	OFS5	OFS4	OFS3	OFS2	OFS1	OFS0	Hex		V_{OFS} (V)
0	0	0	0	1	0	1	1	0	B	0.055
0	0	0	0	1	1	0	0	0	C	0.060
0	0	0	0	1	1	0	1	0	D	0.065
0	0	0	0	1	1	1	0	0	E	0.070
0	0	0	0	1	1	1	1	0	F	0.075
0	0	0	1	0	0	0	0	1	0	0.080
0	0	0	1	0	0	0	1	1	1	0.085
0	0	0	1	0	0	1	0	1	2	0.090
0	0	0	1	0	0	1	1	1	3	0.095
0	0	0	1	0	1	0	0	1	4	0.100
0	0	0	1	0	1	0	1	1	5	0.105
0	0	0	1	0	1	1	0	1	6	0.110
0	0	0	1	0	1	1	1	1	7	0.115
0	0	0	1	1	0	0	0	1	8	0.120
0	0	0	1	1	0	0	1	1	9	0.125
0	0	0	1	1	0	1	0	1	A	0.130
0	0	0	1	1	0	1	1	1	B	0.135
0	0	0	1	1	1	0	0	1	C	0.140
0	0	0	1	1	1	0	1	1	D	0.145
0	0	0	1	1	1	1	0	1	E	0.150
0	0	0	1	1	1	1	1	1	F	0.155
0	0	1	0	0	0	0	0	2	0	0.160
0	0	1	0	0	0	0	1	2	1	0.165
0	0	1	0	0	0	1	0	2	2	0.170
0	0	1	0	0	0	1	1	2	3	0.175
0	0	1	0	0	1	0	0	2	4	0.180
0	0	1	0	0	1	0	1	2	5	0.185
0	0	1	0	0	1	1	0	2	6	0.190
0	0	1	0	0	1	1	1	2	7	0.195
0	0	1	0	1	0	0	0	2	8	0.200
0	0	1	0	1	0	0	1	2	9	0.205
0	0	1	0	1	0	1	0	2	A	0.210
0	0	1	0	1	0	1	1	2	B	0.215
0	0	1	0	1	1	0	0	2	C	0.220
0	0	1	0	1	1	0	1	2	D	0.225
0	0	1	0	1	1	1	0	2	E	0.230
0	0	1	0	1	1	1	1	2	F	0.235
0	0	1	1	0	0	0	0	3	0	0.240
0	0	1	1	0	0	0	1	3	1	0.245
0	0	1	1	0	0	1	0	3	2	0.250
0	0	1	1	0	0	1	1	3	3	0.255
0	0	1	1	0	1	0	0	3	4	0.260

TABLE 2. VID TABLE (Continued)

OFS7	OFS6	OFS5	OFS4	OFS3	OFS2	OFS1	OFS0	Hex		V_{OFS} (V)
0	0	1	1	0	1	0	1	3	5	0.265
0	0	1	1	0	1	1	0	3	6	0.270
0	0	1	1	0	1	1	1	3	7	0.275
0	0	1	1	1	0	0	0	3	8	0.280
0	0	1	1	1	0	0	1	3	9	0.285
0	0	1	1	1	0	1	0	3	A	0.290
0	0	1	1	1	0	1	1	3	B	0.295
0	0	1	1	1	1	0	0	3	C	0.300
0	0	1	1	1	1	0	1	3	D	0.305
0	0	1	1	1	1	1	0	3	E	0.310
0	0	1	1	1	1	1	1	3	F	0.315
0	1	0	0	0	0	0	0	4	0	0.320
0	1	0	0	0	0	0	1	4	1	0.325
0	1	0	0	0	0	1	0	4	2	0.330
0	1	0	0	0	0	1	1	4	3	0.335
0	1	0	0	0	1	0	0	4	4	0.340
0	1	0	0	0	1	0	1	4	5	0.345
0	1	0	0	0	1	1	0	4	6	0.350
0	1	0	0	0	1	1	1	4	7	0.355
0	1	0	0	1	0	0	0	4	8	0.360
0	1	0	0	1	0	0	1	4	9	0.365
0	1	0	0	1	0	1	0	4	A	0.370
0	1	0	0	1	0	1	1	4	B	0.375
0	1	0	0	1	1	0	0	4	C	0.380
0	1	0	0	1	1	0	1	4	D	0.385
0	1	0	0	1	1	1	0	4	E	0.390
0	1	0	0	1	1	1	1	4	F	0.395
0	1	0	1	0	0	0	0	5	0	0.400
0	1	0	1	0	0	0	1	5	1	0.405
0	1	0	1	0	0	1	0	5	2	0.410
0	1	0	1	0	0	1	1	5	3	0.415
0	1	0	1	0	1	0	0	5	4	0.420
0	1	0	1	0	1	0	1	5	5	0.425
0	1	0	1	0	1	1	0	5	6	0.430
0	1	0	1	0	1	1	1	5	7	0.435
0	1	0	1	1	0	0	0	5	8	0.440
0	1	0	1	1	0	0	1	5	9	0.445
0	1	0	1	1	0	1	0	5	A	0.450
0	1	0	1	1	0	1	1	5	B	0.455
0	1	0	1	1	1	0	0	5	C	0.460
0	1	0	1	1	1	0	1	5	D	0.465
0	1	0	1	1	1	1	0	5	E	0.470

TABLE 2. VID TABLE (Continued)

OFS7	OFS6	OFS5	OFS4	OFS3	OFS2	OFS1	OFS0	Hex		V_{OFS} (V)
0	1	0	1	1	1	1	1	5	F	0.475
0	1	1	0	0	0	0	0	6	0	0.480
0	1	1	0	0	0	0	1	6	1	0.485
0	1	1	0	0	0	1	0	6	2	0.490
0	1	1	0	0	0	1	1	6	3	0.495
0	1	1	0	0	1	0	0	6	4	0.500
0	1	1	0	0	1	0	1	6	5	0.505
0	1	1	0	0	1	1	0	6	6	0.510
0	1	1	0	0	1	1	1	6	7	0.515
0	1	1	0	1	0	0	0	6	8	0.520
0	1	1	0	1	0	0	1	6	9	0.525
0	1	1	0	1	0	1	0	6	A	0.530
0	1	1	0	1	0	1	1	6	B	0.535
0	1	1	0	1	1	0	0	6	C	0.540
0	1	1	0	1	1	0	1	6	D	0.545
0	1	1	0	1	1	1	0	6	E	0.550
0	1	1	0	1	1	1	1	6	F	0.555
0	1	1	1	0	0	0	0	7	0	0.560
0	1	1	1	0	0	0	1	7	1	0.565
0	1	1	1	0	0	1	0	7	2	0.570
0	1	1	1	0	0	1	1	7	3	0.575
0	1	1	1	0	1	0	0	7	4	0.580
0	1	1	1	0	1	0	1	7	5	0.585
0	1	1	1	0	1	1	0	7	6	0.590
0	1	1	1	0	1	1	1	7	7	0.595
0	1	1	1	1	0	0	0	7	8	0.600
0	1	1	1	1	0	0	1	7	9	0.605
0	1	1	1	1	0	1	0	7	A	0.610
0	1	1	1	1	0	1	1	7	B	0.615
0	1	1	1	1	1	0	0	7	C	0.620
0	1	1	1	1	1	0	1	7	D	0.625
0	1	1	1	1	1	1	0	7	E	0.630
0	1	1	1	1	1	1	1	7	F	0.635

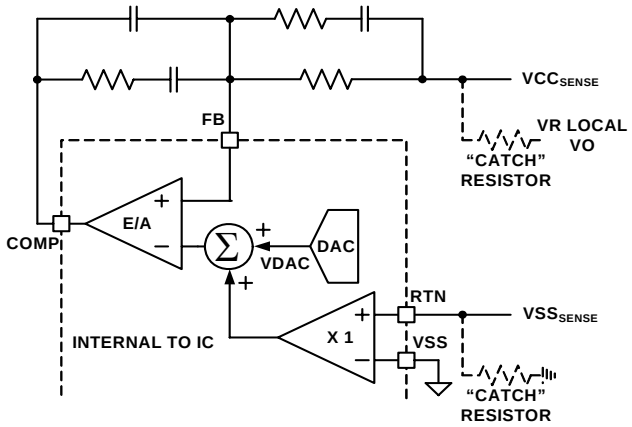


FIGURE 9. DIFFERENTIAL SENSING

Figure 9 shows the differential voltage sensing scheme. VCC_{SENSE} and VSS_{SENSE} are the remote voltage sensing signals from the DDR memory. A unity gain differential amplifier senses the VSS_{SENSE} voltage and adds it to the DAC output. The error amplifier regulates the inverting and the non-inverting input voltages to be equal as shown in Equation 1:

$$VCC_{SENSE} = V_{DAC} + VSS_{SENSE} \quad \text{(EQ. 1)}$$

Rewriting Equation 1 gives Equation 2:

$$VCC_{SENSE} - VSS_{SENSE} = V_{DAC} \quad \text{(EQ. 2)}$$

The VCC_{SENSE} and VSS_{SENSE} signals are routed from the memory socket. In most cases the remote sensing location will be on the PCB right next to one of the DDR memory sockets. If a remote sensing location is used on a module that passes through a socket then the feedback signals will be open circuit in the absence of the module. As shown in Figure 9, a "catch" resistor should be added in this case to feed the local VR output voltage back to the compensator, and another "catch" resistor should be added to connect the local VR output ground to the RTN pin. These resistors, typically 10Ω~100Ω, will provide voltage feedback if the system is powered up without any memory cards installed.

Inductor DCR Current-Sensing Network

The ISL6353 can sense the inductor current through the intrinsic DC Resistance (DCR) of the inductors or through precision resistors in series with the inductors. With both current-sensing methods, the voltage across capacitor C_n represents the total inductor current from all phases. An amplifier converts the C_n voltage, V_{Cn}, into an internal current source, I_{sense}, with the gain set by resistor R_i shown in Equation 3.

$$I_{sense} = \frac{V_{Cn}}{R_i} \quad \text{(EQ. 3)}$$

The sensed current is used for current monitoring and overcurrent protection.

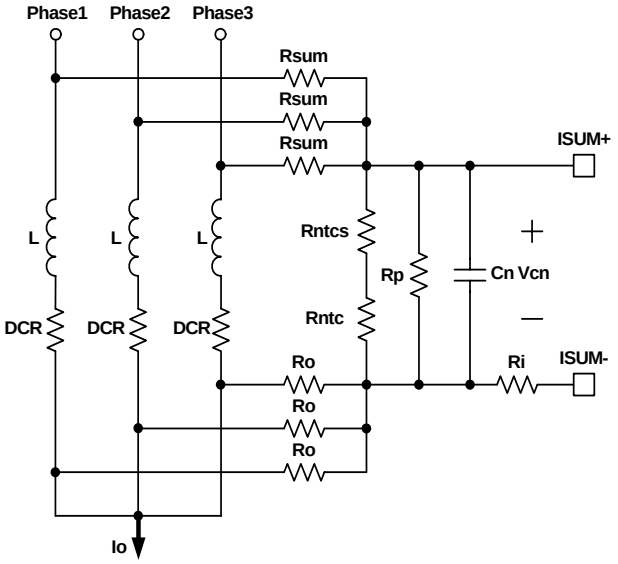


FIGURE 10. DCR CURRENT-SENSING NETWORK

Figure 10 shows the inductor DCR current-sensing network for a 3-phase regulator. Inductor current flows through the DCR and creates a voltage drop. Each inductor has two resistors R_{sum} and R_o connected to the pads to accurately sense the inductor current by sensing the DCR voltage drop. The R_{sum} and R_o resistors are connected in a summing network as shown, and feed the total current information to the NTC network (consisting of R_{ntcs}, R_{ntc} and R_p) and capacitor C_n. R_{ntc} is a negative temperature coefficient (NTC) thermistor, used to compensate for the increase in inductor DCR as temperature increases.

The inductor output pads are electrically shorted in the schematic, but have some parasitic impedance in the actual board layout, which is why the signals cannot simply be shorted together for the current-sense summing network. A resistor from 1Ω~10Ω for R_o is recommended to create quality signals. Since the R_o value is much smaller than the rest of the current sensing circuit, the following analysis will ignore it for simplicity.

The summed inductor current information is represented at capacitor C_n. Equations 4 through 8 describe the frequency-domain relationship between total inductor current $I_o(s)$ and the C_n voltage $V_{Cn}(s)$:

$$V_{Cn}(s) = \left(\frac{R_{ntcnet}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times \frac{DCR}{N} \right) \times I_o(s) \times A_{cs}(s) \quad \text{(EQ. 4)}$$

$$R_{ntcnet} = \frac{(R_{ntcs} + R_{ntc}) \times R_p}{R_{ntcs} + R_{ntc} + R_p} \quad \text{(EQ. 5)}$$

$$A_{cs}(s) = \frac{1 + \frac{s}{\omega_L}}{1 + \frac{s}{\omega_{sns}}} \quad \text{(EQ. 6)}$$

$$\omega_L = \frac{DCR}{L} \quad \text{(EQ. 7)}$$

$$\omega_{sns} = \frac{1}{\frac{R_{ntcnet}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times C_n} \quad \text{(EQ. 8)}$$

where N is the number of phases.

Transfer function $A_{cs}(s)$ always has unity gain at DC. The inductor DCR value increases as the winding temperature increases, giving higher a reading of the inductor DC current. The NTC R_{ntc} values decreases as its temperature increases. Proper selections of R_{sum}, R_{ntcs}, R_p and R_{ntc} parameters ensure that V_{Cn} represents the total inductor DC current over the temperature range of interest.

There are many sets of parameters that can properly temperature-compensate the DCR change. Since the NTC network and the R_{sum} resistors form a voltage divider, V_{cn} is always a fraction of the inductor DCR voltage. A higher ratio of V_{cn} to the inductor DCR voltage is recommended so the current monitor and OCP circuit has a higher signal level to work with.

A typical set of parameters that provide good temperature compensation are: R_{sum} = 3.65kΩ, R_p = 11kΩ, R_{ntcs} = 2.61kΩ and R_{ntc} = 10kΩ (ERT-J1VR103J). The NTC network component values may need to be fine tuned on actual boards. To help fine tune the network apply a full load condition to the regulator and record the IMON pin voltage reading immediately; then record the IMON voltage reading again when the board has reached thermal steady state. A good NTC network can limit the IMON voltage drift to within 1% over the temperature range. If droop is used for the ISL6353 based regulator the output voltage can be used for this test rather than IMON. DDR memory regulators typically do not operate with droop enabled. The Intersil evaluation board layout and current-sensing network parameters can be referred to in order to help minimize engineering time.

$V_{Cn}(s)$ needs to represent real-time $I_o(s)$ for the controller to achieve best OCP and IMON response. The transfer function $A_{cs}(s)$ has a pole ω_{sns} and a zero ω_L. ω_L and ω_{sns} should be matched so $A_{cs}(s)$ is unity gain at all frequencies. By forcing ω_L equal to ω_{sns} and solving for the solution, Equation 9 gives Cn value.

$$C_n = \frac{L}{\frac{R_{ntcnet}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times DCR} \quad \text{(EQ. 9)}$$

For example, given N = 3, R_{sum} = 3.65kΩ, R_p = 11kΩ, R_{ntcs} = 2.61kΩ, R_{ntc} = 10kΩ, DCR = 0.29mΩ and L = 0.22µH, Equation 9 gives C_n = 0.79µF.

C_n is the capacitor used to match the inductor time constant. Sometimes it takes the parallel combination of two or more capacitors to get the desired value. To verify the capacitor value is correct a repetitive load can be placed on the output voltage and the IMON voltage can be monitored. The capacitor in parallel with the IMON resistor needs to be removed for this test. The

IMON voltage should be approximately a square wave with little or no overshoot. In regulators without droop control the capacitor value can be selected to err on the high side to overdamp the current sense input to the controller to avoid overshoots.

Resistor Current-Sensing Network

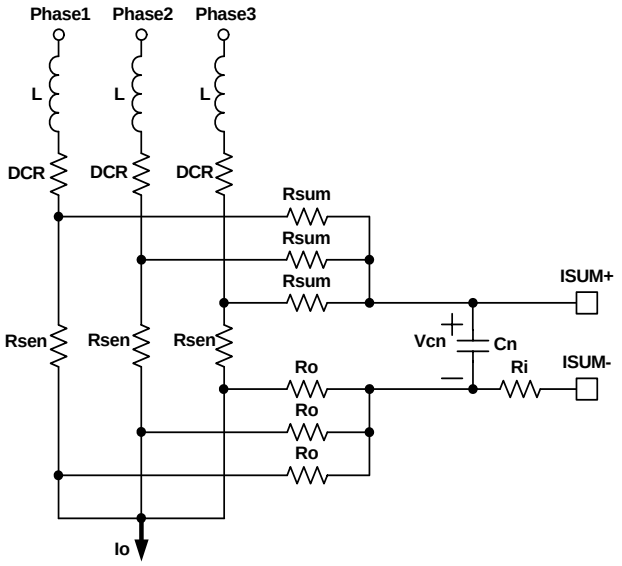


FIGURE 11. RESISTOR CURRENT-SENSING NETWORK

Figure 11 shows the precision resistor current-sensing network for a 3-phase solution. Each inductor has a series current-sensing resistor, R_{sen}. R_{sum} and R_o are connected to the R_{sen} pads to accurately capture the inductor current information. The R_{sum} and R_o resistors are connected to capacitor C_n. R_{sum} and C_n form a filter for noise attenuation. Equations 10 through 12 give $V_{Cn}(s)$ expressions:

$$V_{Cn}(s) = \frac{R_{sen}}{N} \times I_o(s) \times A_{Rsen}(s) \quad \text{(EQ. 10)}$$

$$A_{Rsen}(s) = \frac{1}{1 + \frac{s}{\omega_{sns}}} \quad \text{(EQ. 11)}$$

$$\omega_{Rsen} = \frac{1}{\frac{R_{sum}}{N} \times C_n} \quad \text{(EQ. 12)}$$

Transfer function $A_{Rsen}(s)$ always has unity gain at DC. The current-sensing resistor R_{sen} value will not have a significant variation over temperature, so there is no need for the NTC network.

Recommended values are R_{sum} = 1kΩ and C_n = 5600pF.

Overcurrent Protection

The ISL6353 implements overcurrent protection (OCP) by comparing the average value of the measured current I_{sense} with an internal current source reference. The OCP threshold is 60µA for 3-phase, 2-phase and 1-phase PS0 operation. In PS1/2 mode the OCP threshold is scaled based on the number of active phases in PS1/2 mode divided by the number of active phases in PS0 mode. For example, if the regulator operates in 3-phase mode in PS0, 2-phase in PS1 mode and 1-phase in PS2 mode, the OCP threshold will be 60µA in PS0 mode, 40µA in PS1 mode and 20µA in PS2 mode. For a 2-phase design, the OCP threshold is 60µA in PS0 mode and 30µA in PS1 and PS2 mode. The ISL6353 declares a OCP fault when I_{sense} is above the threshold for 120µs.

Referring to Equation 3 and Figure 10, resistor R_i sets the sensed current I_{sense}. In general, I_{sense} can be set to 40µA at the maximum load current expected in the design. The OCP trip level will be 1.5 times the maximum load current with a threshold at 60µA. The OCP ratio can be set to something other than 1.5 times the maximum load current by setting $I_{sense} = 60\mu A/OCP_{ratio}$.

For inductor DCR sensing, Equation 13 gives the DC relationship of $V_{cn}(s)$ and $I_o(s)$.

$$V_{Cn} = \left(\frac{R_{ntcnet}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times \frac{DCR}{N} \right) \times I_o \quad \text{(EQ. 13)}$$

Substitution of Equation 13 into Equation 3 gives Equation 14:

$$II_{sense} = \frac{1}{R_i} \times \frac{R_{ntcnet}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times \frac{DCR}{N} \times I_o \quad \text{(EQ. 14)}$$

Therefore:

$$R_i = \frac{R_{ntcnet} \times DCR \times I_o}{N \times \left(R_{ntcnet} + \frac{R_{sum}}{N} \right) \times I_{sense}} \quad \text{(EQ. 15)}$$

Substitution of Equation 5 and application of the full load condition in Equation 15 gives Equation 16:

$$R_i = \frac{\frac{(R_{ntcs} + R_{ntc}) \times R_p}{R_{ntcs} + R_{ntc} + R_p} \times DCR \times I_{omax}}{N \times \left(\frac{(R_{ntcs} + R_{ntc}) \times R_p}{R_{ntcs} + R_{ntc} + R_p} + \frac{R_{sum}}{N} \right) \times I_{sensemax}} \quad \text{(EQ. 16)}$$

where I_{omax} is the full load current, and $I_{sensemax}$ is the corresponding sensed current based on the desired OCP to I_{omax} ratio.

For resistor sensing, Equation 17 gives the DC relationship of $V_{cn}(s)$ and $I_o(s)$.

$$V_{Cn} = \frac{R_{sen}}{N} \times I_o \quad \text{(EQ. 17)}$$

Substitution of Equation 17 into Equation 3 gives Equation 18:

$$I_{sense} = \frac{1}{R_i} \times \frac{R_{sen}}{N} \times I_o \quad \text{(EQ. 18)}$$

Therefore:

$$R_i = \frac{R_{sen} \times I_o}{N \times I_{sense}} \quad \text{(EQ. 19)}$$

Application of the full load condition gives Equation 20:

$$R_i = \frac{R_{sen} \times I_{omax}}{N \times I_{sensemax}} \quad \text{(EQ. 20)}$$

where I_{omax} is the full load current, and $I_{sensemax}$ is the corresponding sensed current.

Current Monitor

The ISL6353 provides a current monitor function. The IMON pin outputs a high-speed analog current source that is 1/4 times the I_{sense} current.

$$I_{IMON} = \frac{1}{4} \times I_{sense} \quad \text{(EQ. 21)}$$

A resistor R_{imon} is connected to the IMON pin to convert the IMON pin current to a voltage. The voltage across R_{imon} is expressed in Equation 22:

$$V_{Rimon} = \frac{1}{4} \times I_{sense} \times R_{imon} \quad \text{(EQ. 22)}$$

Substitution of Equation 14 into Equation 22 gives Equation 23:

$$V_{Rimon} = \frac{1}{4R_i} \times \frac{R_{ntcnet}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times \frac{DCR}{N} \times I_o \times R_{imon} \quad \text{(EQ. 23)}$$

Rewriting Equation 23 gives Equation 24:

$$R_{imon} = \frac{V_{Rimon} \times R_i \times (NR_{ntcnet} + R_{sum})}{\frac{1}{4}R_{ntcnet} \times DCR \times I_o} \quad \text{(EQ. 24)}$$

Substitution of Equation 5 and application of the full load condition in Equation 24 gives Equation 25:

$$R_{imon} = \frac{V_{Rimon} \times R_i \times \left(N\frac{(R_{ntcs} + R_{ntc}) \times R_p}{R_{ntcs} + R_{ntc} + R_p} + R_{sum}\right)}{\frac{1}{4}\frac{(R_{ntcs} + R_{ntc}) \times R_p}{R_{ntcs} + R_{ntc} + R_p} \times DCR \times I_{omax}} \quad \text{(EQ. 25)}$$

where I_{omax} is the full load current.

A capacitor C_{imon} can be paralleled with R_{imon} to filter the IMON pin voltage. The $R_{imon}C_{imon}$ time constant is the user's choice. The time constant should be long enough such that switching frequency ripple is removed.

Phase Current Balancing

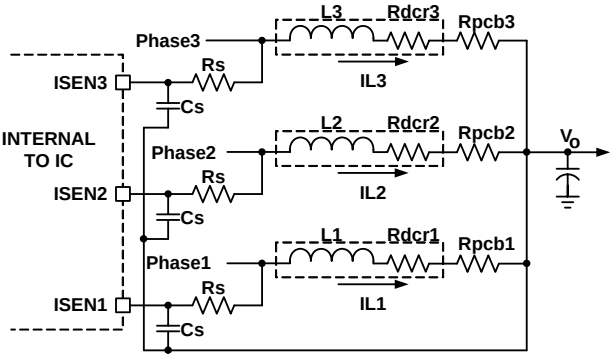


FIGURE 12. CURRENT BALANCING CIRCUIT

The ISL6353 monitors individual phase current by monitoring the ISEN1, ISEN2, and ISEN3 pin voltages. Figure 12 shows the current balancing circuit recommended for the ISL6353. Each phase node voltage is averaged by a low-pass filter consisting of R_S and C_S, and presented to the corresponding ISEN pin. A long time constant for R_SC_S should be used such that the ISEN voltages have minimal ripple and represent the DC current flowing through the inductors. Recommended values are $R_S = 10k\Omega$ and $C_S = 0.22\mu F$.

R_S should be routed to the inductor phase-node pad in order to help eliminate the effect of phase node parasitic PCB DCR. Equations 26 through 28 give the ISEN pin voltages:

$$V_{ISEN1} = (R_{dcr1} + R_{pcb1}) \times I_{L1} \quad \text{(EQ. 26)}$$

$$V_{ISEN2} = (R_{dcr2} + R_{pcb2}) \times I_{L2} \quad \text{(EQ. 27)}$$

$$V_{ISEN3} = (R_{dcr3} + R_{pcb3}) \times I_{L3} \quad \text{(EQ. 28)}$$

where R_{dcr1}, R_{dcr2} and R_{dcr3} are inductor DCR; R_{pcb1}, R_{pcb2} and R_{pcb3} are parasitic PCB DCR between the inductor output pad and the output voltage rail; and I_{L1}, I_{L2} and I_{L3} are inductor average currents.

The ISL6353 will adjust the phase pulse-width relative to the other phases to make $V_{ISEN1} = V_{ISEN2} = V_{ISEN3}$, thus to achieve $I_{L1} = I_{L2} = I_{L3}$, when $R_{dcr1} = R_{dcr2} = R_{dcr3}$ and $R_{pcb1} = R_{pcb2} = R_{pcb3}$.

Using the same components for L1, L2 and L3 will provide a good match of R_{dcr1}, R_{dcr2} and R_{dcr3}. Board layout will determine R_{pcb1}, R_{pcb2} and R_{pcb3}. Each phase should be as symmetric as possible in the PCB layout for the power delivery path between each inductor and the output voltage load, such that $R_{pcb1} = R_{pcb2} = R_{pcb3}$.

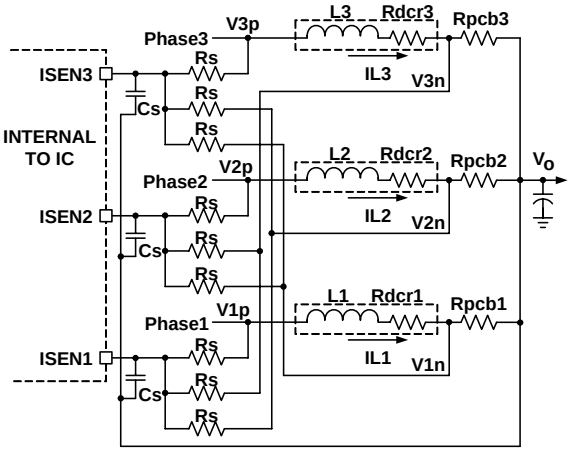


FIGURE 13. DIFFERENTIAL-SENSING CURRENT BALANCING CIRCUIT

Sometimes, it is difficult to implement a symmetric layout. For the circuit shown in Figure 12, an asymmetric layout causes different R_{pcb1}, R_{pcb2} and R_{pcb3} resulting in phase current imbalance. Figure 13 shows a differential-sensing current balancing circuit recommended for the ISL6353. The current sensing traces should be routed to the inductor pads so they only pick up the inductor DCR voltage. Each ISEN pin sees the average voltage of three sources: its own phase inductor phase-node pad,

and the other two phases inductor output pads. Equations 29 through 31 give the ISEN pin voltages:

$$V_{ISEN1} = V_{1p} + V_{2n} + V_{3n} \quad \text{(EQ. 29)}$$

$$V_{ISEN2} = V_{1n} + V_{2p} + V_{3n} \quad \text{(EQ. 30)}$$

$$V_{ISEN3} = V_{1n} + V_{2n} + V_{3p} \quad \text{(EQ. 31)}$$

The ISL6353 will make $V_{ISEN1} = V_{ISEN2} = V_{ISEN3}$ as in Equations 32 and 33:

$$V_{1p} + V_{2n} + V_{3n} = V_{1n} + V_{2p} + V_{3n} \quad \text{(EQ. 32)}$$

$$V_{1n} + V_{2p} + V_{3n} = V_{1n} + V_{2n} + V_{3p} \quad \text{(EQ. 33)}$$

Rewriting Equation 32 gives Equation 34:

$$V_{1p} - V_{1n} = V_{2p} - V_{2n} \quad \text{(EQ. 34)}$$

and rewriting Equation 33 gives Equation 35:

$$V_{2p} - V_{2n} = V_{3p} - V_{3n} \quad \text{(EQ. 35)}$$

Combining Equations 34 and 35 gives Equation 36:

$$V_{1p} - V_{1n} = V_{2p} - V_{2n} = V_{3p} - V_{3n} \quad \text{(EQ. 36)}$$

Therefore:

$$R_{dcr1} \times I_{L1} = R_{dcr2} \times I_{L2} = R_{dcr3} \times I_{L3} \quad \text{(EQ. 37)}$$

Current balancing ($I_{L1} = I_{L2} = I_{L3}$) is achieved when $R_{dcr1} = R_{dcr2} = R_{dcr3}$. R_{pcb1}, R_{pcb2} and R_{pcb3} will not have any effect.

Since the slave ripple capacitor voltages mimic the inductor currents, the R^3™ modulator can naturally achieve excellent current balancing during steady-state and dynamic operation. The inductor currents follow the load current dynamic change, with the output capacitors supplying the difference. The inductor currents can track the load current well at low rep rate, but cannot keep up when the rep rate gets into the hundred-kHz range, where it is out of the control loop bandwidth. The controller achieves excellent current balancing in all cases.

CCM Switching Frequency

The resistor connected between the COMP pin and the VW pin sets the VW windows size, therefore setting the steady state PWM switching frequency. When the ISL6353 is in continuous conduction mode (CCM), the switching frequency is not absolutely constant due to the nature of the R^3 modulator. As explained in the “Multiphase R3 Modulator” on page 11, the effective switching frequency will increase during load step-up and will decrease during load step-down to achieve fast transient response. On the other hand, the switching frequency is relatively constant at steady state. Equation 38 gives an estimate of the frequency-setting resistor R_{fset} value. 20kΩ R_{fset} gives approximately 300kHz switching frequency. Lower resistance yields higher switching frequency.

$$R_{fset}(\Omega) = 1.293 \cdot 10^{-7} \cdot F_{SW}^{\ 2} - 0.1445 \cdot F_{SW} + 52055 \quad \text{(EQ. 38)}$$

Phase Count Configurations

The ISL6353 can be configured for 1, 2 or 3-phase operation.

For 2-phase configuration, tie the PWM3 pin to VDD. Phase 1 and Phase 2 PWM pulses are 180° out-of-phase. Leave the ISEN3 pin open for 2-phase configuration.

For 1-phase configuration, tie the PWM3 and ISEN2 pins to VDD. In this configuration, only Phase 1 is active. The ISEN3, ISEN2, ISEN1, and FB2 pins are not used because there is no need for current balancing or the FB2 function.

Modes of Operation

TABLE 3. ISL6353 MODES OF OPERATION

CONFIGURATION	PS#	OPERATIONAL MODE
3-phase Configuration	PS0	3-phase CCM
	PS1	2-phase CCM or 1-phase CCM
	PS2	1-phase DE
	PS3	1-phase DE
2-phase Configuration	PS0	2-phase CCM
	PS1	1-phase CCM
	PS2	1-phase DE
	PS3	1-phase DE
1-phase Configuration	PS0	1-phase CCM
	PS1	1-phase CCM
	PS2	1-phase DE
	PS3	1-phase DE

Table 3 shows the modes of operation for the various power states programmed using the SetPS command through the SVID bus or by changing the state of the PSI pin. Table 3 is used in conjunction with the status of the PROG2 pin. Refer to Table 7 for the PROG2 programming options.

Dynamic Operation

The controller responds to VID changes by slewing to the new voltage at a slew rate indicated in the SetVID command. There are three SetVID slew rates SetVID_fast, SetVID_slew and SetVID_decay.

The SetVID_fast command prompts the controller to enter CCM and to actively drive the output voltage to the new VID value at a minimum 10mV/µs slew rate.

The SetVID_slow command prompts the controller to enter CCM and to actively drive the output voltage to the new VID value at a minimum 2.5mV/µs slew rate.

The SetVID_decay command prompts the controller to enter DE mode. The output voltage will decay down to the new VID value at a slew rate determined by the load. If the voltage decay rate is

too fast, the controller will limit the voltage slew rate at the SetVID_slow slew rate.

ALERT# will be asserted low at the end of SetVID_fast and SetVID_slow VID transitions.

When the ISL6353 is in DE mode, it will actively drive the output voltage up when the VID changes to a higher value. DE operation will resume after reaching the new voltage level. If the load is light enough to warrant DCM, it will enter DCM after the inductor current has crossed zero for four consecutive cycles. The ISL6353 will remain in DE mode when the VID changes to a lower value. The output voltage will decay to the new value and the load will determine the slew rate.

Protection Functions

The ISL6353 provides overcurrent, current-balance, overvoltage, and over-temperature protection.

OVERCURRENT PROTECTION

The ISL6353 determines overcurrent protection (OCP) by comparing the average value of the measured current I_{sense} with an internal current source threshold. ISL6353 declares OCP when I_{sense} is above the threshold for 120µs.

The way-overcurrent protection threshold is significantly above the standard overcurrent protection threshold. The way-overcurrent function is intended to provide a fast overcurrent detection and action mechanism in a short circuit output condition. Once the way-overcurrent condition is detected, the PWM outputs will immediately shut off and PGOOD will go low to maximize protection.

CURRENT BALANCE FAULT

The ISL6353 monitors the ISEN pin voltages to detect severe phase current imbalances. If any ISEN pin voltage is more than 20mV different than the average ISEN voltage for 1ms, the controller will declare a fault and latch off.

OVERVOLTAGE PROTECTION

The ISL6353 will declare an OVP fault if the output voltage exceeds 175mV above the VID set value + positive offset. In the event of an OVP condition, the OVP pin is pulled high. OVP is blanked during dynamic VID events to prevent false trigger. During soft-start, the OVP threshold is set at 2.33V to avoid a false trigger due to turn on into a precharged output capacitor bank.

POWER GOOD INDICATOR

The ISL6353 takes the same actions for all of the above fault protection functions: PGOOD is set low and the high-side and low-side MOSFETs are turned off. Any residual inductor current will decay through the MOSFET body diodes. These fault conditions can be reset by bringing VR_ON low or by bringing V_{DD} below the POR threshold. When VR_ON and V_{DD} return to their high operating levels, a soft-start will occur.

THERMAL MONITOR

The ISL6353 has a thermal throttling feature. If the voltage on the NTC pin goes below the 0.91V threshold, the VR_HOT# pin is pulled low indicating the need for thermal throttling to the system. The VR_HOT# pin will be pulled back high if the voltage on the NTC pin goes above 0.95V.

If the voltage on the NTC pin goes below 0.93V the ALERT# pin will be pulled low indicating a thermal alert. ALERT# is reset by checking the status register. ALERT# will be pulled low again if the NTC pin voltage goes above 0.97V.

All the above fault conditions can be reset by bringing VR_ON low or by bringing V_{DD} below the POR threshold. When VR_ON and V_{DD} return to their high operating levels, a soft-start will occur.

VR_HOT#/ALERT# BEHAVIOR

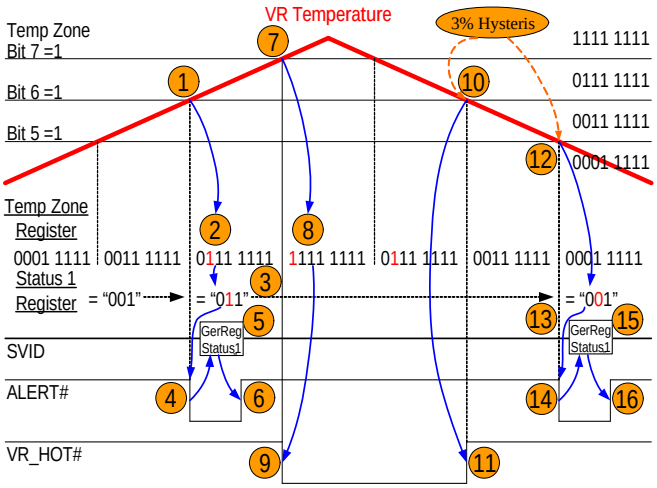


FIGURE 14. VR_HOT#/ALERT# BEHAVIOR

The controller drives a 60µA current source out of the NTC pin. The current source flows through the NTC resistor network on the pin and creates a voltage that is monitored by the controller through an A/D converter (ADC) to generate the Tzone value. Table 4 shows the typical programming table for Tzone. The user needs to scale the NTC a network resistance such that it generates the NTC pin voltage that corresponds to the left-most column.

TABLE 4. TZONE TABLE

VNTC (V)	TMAX (%)	TZONE
0.86	>100	FFh
0.88	100	FFh
0.92	97	7Fh
0.96	94	3Fh
1.00	91	1Fh
1.04	88	0Fh
1.08	85	07h
1.12	82	03h
1.16	79	01h
1.20	76	01h
>1.20	<76	00h

Figure 14 shows the how the NTC network should be designed to get correct VR_HOT#/ALERT# behavior when the system temperature rises and falls, manifested as the NTC pin voltage falling and rising. The series of events are:

1. The temperature rises so the NTC pin voltage drops. Tzone value changes accordingly.
2. The temperature crosses the threshold where Tzone register Bit 6 changes from 0 to 1.
3. The controller changes Status_1 register bit 1 from 0 to 1.
4. The controller asserts ALERT#.
5. The CPU reads Status_1 register value to know that the alert assertion is due to Tzone register bit 6 flipping.
6. The controller clears ALERT#.
7. The temperature continues rising.
8. The temperature crosses the threshold where Tzone register Bit 7 changes from 0 to 1.
9. The controllers asserts VR_HOT# signal. The CPU throttles back and the system temperature starts dropping eventually.
10. The temperature crosses the threshold where Tzone register bit 6 changes from 1 to 0. This threshold is 1 ADC step lower than the one when VR_HOT# gets asserted, to provide 3% hysteresis.
11. The controllers de-asserts VR_HOT# signal.
12. The temperature crosses the threshold where Tzone register bit 5 changes from 1 to 0. This threshold is 1 ADC step lower than the one when ALERT# gets asserted during the temperature rise to provide 3% hysteresis.
13. The controller changes Status_1 register bit 1 from 1 to 0.
14. The controller asserts ALERT#.
15. The CPU reads Status_1 register value to know that the alert assertion is due to Tzone register bit 5 flipping.
16. The controller clears ALERT#.

Table 5 summarizes the fault protection functionality.

TABLE 5. FAULT PROTECTION SUMMARY

FAULT TYPE	FAULT DURATION BEFORE PROTECTION	PROTECTION ACTION	FAULT RESET
Overcurrent	120µs	PWM tri-state, PGOOD latched low	VR_ON toggle or VDD toggle
Phase Current Unbalance	1ms		
Way-Overcurrent (1.5xOC)	Immediately		
Overvoltage +175mV		PGOOD latched low. Actively pulls the output voltage to below VID value, then tri-state.	

FB2 Function

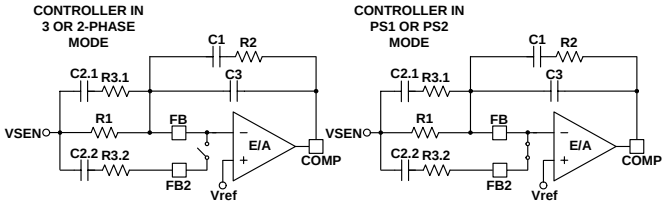


FIGURE 15. FB2 FUNCTION IN 2-PHASE MODE

Figure 15 shows the FB2 function. In order to improve transient response and stability when phases are disabled in PS1 or PS2 mode, the ISL6353 FB2 function allows a second type 3 compensation network to be connected from the output voltage to the FB pin.

In PS0 mode of operation the FB2 switch is open (off). In PS1 or PS2 mode of operation the FB2 switch closes (on).

The FB2 function ensures excellent transient response in both PS0 mode and PS1/2 mode. If the FB2 function is not needed C2.2 and R3.2 can be unpopulated and the FB2 pin can be left unconnected.

Adaptive Body Diode Conduction Time Reduction

In DCM, the controller turns off the low-side MOSFET when the inductor current approaches zero. During the on-time of the low-side MOSFET, the phase voltage is negative and the amount is the MOSFET $r_{DS(ON)}$ voltage drop, which is proportional to the inductor current. A phase comparator inside the controller monitors the phase voltage during on-time of the low-side MOSFET and compares it with a threshold to determine the zero-crossing point of the inductor current. If the inductor current has not reached zero when the low-side MOSFET turns off, it will flow through the low-side MOSFET body diode, causing the phase node to have a larger voltage drop until it decays to zero. If the inductor current has crossed zero and reversed the direction when the low-side MOSFET turns off, it will flow through the high-side MOSFET body diode, causing the phase node to have a spike until the current decays to zero. The controller continues monitoring the phase voltage after turning off the low-side MOSFET and adjusts the phase comparator threshold voltage accordingly in iterative steps such that the low-side MOSFET body diode conducts for approximately 40ns to minimize the body diode-related loss.

System Parameter Programming PROG1/2 Pins

ISL6353 has two system parameter programming pins PROG1 and PROG2. Some system parameters, such as maximum output current, boot voltage, number of phases for PS1 state, can be programmed by changing the resistors connected to these three pins.

Table 6 shows the definition of PROG1. PROG1 defines the maximum output current setting in the IMAX register of the ISL6353.

TABLE 6. DEFINITION OF PROG1

R_{PROG1} (Ω)	I_{MAX} 3-PHASE MODE (A)	I_{MAX} 2-PHASE MODE(A)	I_{MAX} 1-PHASE MODE (A)
158	99	66	33
475	90	60	30
787	84	56	28
1100	81	54	27
1430	75	50	25
1740	69	46	23
2050	66	44	22
2370	60	40	20
2870	54	36	18
3480	51	34	17
4120	45	30	15
4750	39	26	13

Table 7 shows the definition of PROG2. PROG2 defines the boot voltage, enable/disable droop and the working mode for PS1.

TABLE 7. DEFINITION OF PROG2

R_{PROG2} (Ω)	DROOP	WORKING MODE AT PS1	V_{BOOT} (V)
158	Enabled	1-phase CCM	0
475	Enabled	1- phase CCM	1.20
787	Enabled	1-phase CCM	1.35
1100	Enabled	1- phase CCM	1.50
1430	Enabled	2-Phase CCM (3-Phase Configuration) 1-Phase CCM (2-phase configuration)	1.50
1740	Enabled	2-Phase CCM (3-Phase Configuration) 1-Phase CCM (2-phase configuration)	1.35
2050	Enabled	2-Phase CCM (3-Phase Configuration) 1-Phase CCM (2-phase configuration)	1.20
2370	Enabled	2-Phase CCM (3-Phase Configuration) 1-Phase CCM (2-Phase configuration)	0
2870	Disabled	2-Phase CCM (3-Phase Configuration) 1-Phase CCM (2-Phase configuration)	0
3480	Disabled	2 phase CCM (3-phase Configuration) 1-Phase CCM (2-phase configuration)	1.20
4120	Disabled	2 phase CCM (3-phase Configuration) 1-Phase CCM (2-phase configuration)	1.35
4750	Disabled	2 phase CCM (3-phase Configuration) 1-Phase CCM (2-phase configuration)	1.50
5360	Disabled	1 phase CCM	1.50
6040	Disabled	1 phase CCM	1.35
6650	Disabled	1 phase CCM	1.20
7500	Disabled	1 phase CCM	0

SVID ADDRESS Setting

The SVID address of ISL6353 can be programmed by changing the resistor connected to the ADDR pin. Table 8 shows the SVID address definition.

TABLE 8. SVID ADDRESS DEFINITION

R_{ADDR} (Ω)	ADDRESS
158	0
475	1
787	2
1100	3
1430	4
1740	5
2050	6
2370	7
2870	8
3480	9
4120	A
4750	B
5360	C
6040	D

External Control of VOUT and Power State VSET1/2, PSI

For additional design flexibility, the ISL6353 has 3 pins that can be used to set the output voltage and power state of the regulator with external signals independent of the serial communication bus register settings.

VSET1 and VSET2 can be used to set the output voltage of the regulator. Table 9 shows the available options. If VSET1 and VSET2 are connected to ground, the controller will refer only to the SVID register setting to program the output voltage. If any other logic combination is used on VSET1/2, the controller will ignore the SVID register setting and program the output voltage based on Table 8 for soft-start and steady state.

TABLE 9. VSET1/2 PIN DEFINITION

V_{BOOT} from PROG2 (V)	VSET1	VSET2	OUTPUT VOLTAGE
1.5	0	0	SVID Setting
1.5	0	1	1.35V
1.5	1	0	1.6V
1.5	1	1	1.65V
1.35	0	0	SVID Setting
1.35	0	1	1.2V
1.35	1	0	1.4V
1.35	1	1	1.45V
1.2	0	0	SVID Setting
1.2	0	1	1.1V
1.2	1	0	1.25V
1.2	1	1	1.3V
0	0	0	SVID Setting
0	0	1	1.05V
0	1	0	1.55V
0	1	1	1.15V

The PSI pin can be used to set the power state of the regulator as indicated on Table 10. If PSI is connected to ground the controller will refer only to the SVID register contents to set the power state. If PSI is pulled high, the controller will enter the PS2 state. If PSI is connected to a high impedance, the controller will enter the PS1 state.

TABLE 10. PSI PIN DEFINITION

PSI	ADDRESS
0	Internal SVID Power State
High-Z	PS1
1	PS2

Supported Serial VID Data And Configuration Registers

The controller supports the following data and configuration registers.

TABLE 11. SUPPORTED DATA AND CONFIGURATION REGISTERS

INDEX	REGISTER NAME	DESCRIPTION	DEFAULT VALUE
00h	Vendor ID	Uniquely identifies the VR vendor. Assigned by Intel.	12h
01h	Product ID	Uniquely identifies the VR product. Intersil assigns this number.	35h
02h	Product Revision	Uniquely identifies the revision of the VR control IC. Intersil assigns this data.	
05h	Protocol ID	Identifies which revision of SVID protocol the controller supports.	01h
06h	Capability	Identifies the SVID VR capabilities and which of the optional telemetry registers are supported.	81h
10h	Status_1	Data register read after ALERT# signal; indicating if a VR rail has settled, has reached VRHOT condition or has reached ICC max.	00h
11h	Status_2	Data register showing Status_2 communication.	00h
12h	Temperature Zone	Data register showing temperature zones that have been entered.	00h
15h	IOUT	Data register showing output current information. The voltage at the IMON pin is digitized and stored in this register.	00h
1Ch	Status_2_ LastRead	This register contains a copy of the Status_2 data that was last read with the GetReg (Status_2) command.	00h
21h	ICC max	Data register containing the ICC max the platform supports; set at start-up by resistor on PROG1 pin. The platform design engineer programs this value during the design process. Binary format in amps, for example 100A = 64h.	Refer to Table 6
24h	SR-fast	Slew Rate Normal. The fastest slew rate the platform VR can sustain. Binary format in mV/µs. i.e. 0Ah = 10mV/µs.	0Ah
25h	SR-slow	Is 4x slower than normal. Binary format in mV/µs. i.e. 02h = 2.5mV/µs	02h

TABLE 11. SUPPORTED DATA AND CONFIGURATION REGISTERS (Continued)

INDEX	REGISTER NAME	DESCRIPTION	DEFAULT VALUE
26h	Vboot	If programmed by the platform, the VR supports V_{BOOT} voltage during start-up ramp. The VR will ramp to V_{BOOT} and hold at V_{BOOT} until it receives a new SetVID command to move to a different voltage.	Refer to Table 6
30h	Vout max	This register is programmed by the master and sets the maximum VID the VR will support. If a higher VID code is received, the VR will respond with “not supported” acknowledge.	FBh
31h	VID Setting	Data register containing currently programmed VID voltage. VID data format.	00h
32h	Power State	Register containing the programmed power state.	00h

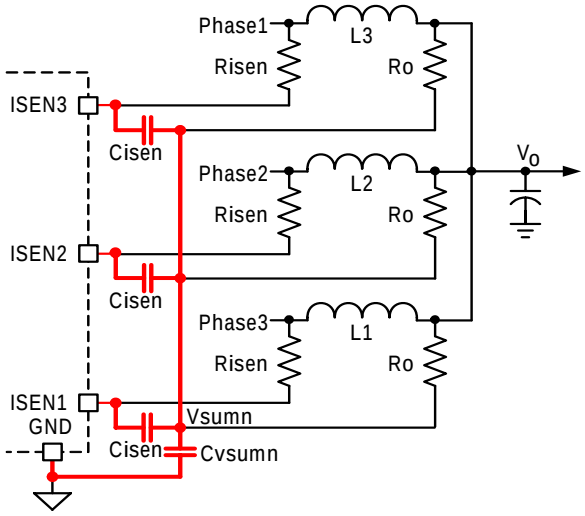
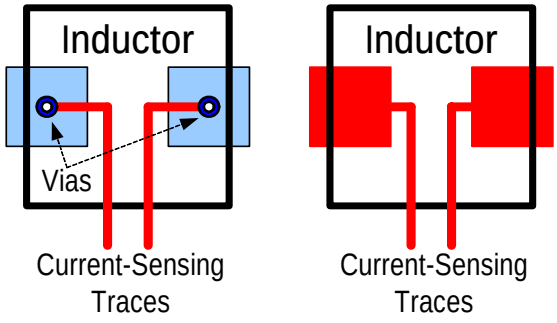
33h	Voltage Offset	Sets offset in VID steps added to the VID setting for voltage margining. Bit 7 is a sign bit,
		0 = positive margin,
		1 = negative margin.
		Remaining 7 bits are # VID steps for the margin.
		00h = no margin,
		01h = +1 VID step
		02h = +2 VID steps...
			00h

34h	Multi VR Config	Data register that configures multiple VRs behavior on the same SVID bus.	VR1: 00h VR2: 01h

Layout Guidelines

ISL6353 PIN NUMBER	SYMBOL	LAYOUT GUIDELINES
BOTTOM PAD	GND	Connect this ground pad to the ground plane through low impedance path. Recommend use of at least 5 vias to connect to ground planes in PCB internal layers.
1, 2, 3	SDA, ALERT#, SCLK	Follow Intel recommendations.
4, 5, 6, 7, 22, 28, 36, 37, 38, 39	VR_ON, PGOOD, IMON, VR_HOT#, PROG1, PWM3, PSI, VSET1, VSET2, OVP	No special consideration.
8	NTC	The NTC thermistor needs to be placed close to the thermal source that is monitored to determine the desired VR_HOT# and thermal ALERT# toggling. Recommend placing it at the hottest spot of the ISL6353 based regulator.
9	VW	Place the resistor and capacitor from VW to COMP in close proximity of the controller.

Layout Guidelines (Continued)

ISL6353 PIN NUMBER	SYMBOL	LAYOUT GUIDELINES
10, 11, 12	COMP, FB, FB2	Place the compensator components in general proximity of the controller
13, 14, 15	ISEN3, ISEN2, ISEN1	Each ISEN pin has a capacitor (Cisen) decoupling it to VSUMN, then through another capacitor (Cvsumn) to GND. Place Cisen capacitors as close as possible to the controller and keep the following loops small: 1. Any ISEN pin to another ISEN pin 2. Any ISEN pin to GND The red traces in the following drawing show the loops that need to minimized. 
16, 17	VSEN, RTN	Place the VSEN/RTN filter in close proximity of the controller for good decoupling. Route these signals differentially from the remote sense location back to the controller.
18, 19	ISUMN, ISUMP	Place the current sensing circuit in general proximity of the controller. Place capacitor Cn very close to the controller. Place the NTC thermistor next to the phase 1 inductor so it senses the inductor temperature correctly. Each phase of the power stage sends a pair of VSUMP and VSUMN signals to the controller. Run these two signals traces in parallel fashion. IMPORTANT: Sense the inductor current by routing the sensing circuit to the inductor pads. If possible, route the traces on a different layer from the inductor pad layer and use vias to connect the traces to the center of the pads. If no via is allowed on the pad, consider routing the traces into the pads from the inside of the inductor. The following drawings show the two preferred ways of routing current sensing traces. If possible connect the traces to the inductor pad in only one place and isolate this connection from other planes of the same net that may be present on other layers. Also make the connections a symmetric as possible for all phases. 
20	VDD	Place the decoupling capacitor a close as possible to this pin.
21	VIN	Place the decoupling capacitor a close as possible to this pin.

Layout Guidelines (Continued)

ISL6353 PIN NUMBER	SYMBOL	LAYOUT GUIDELINES
23	BOOT1	Use a fairly wide trace (>30mil). Avoid routing or crossing any sensitive analog signals near this trace.
24, 25	UG1, PH1	Run these two traces in parallel with fairly wide traces (>30mil). Avoid routing or crossing any sensitive analog signals near this trace. Recommend routing the PH1 trace to the phase 1 high-side MOSFET source pins instead of general copper.
26	GND	Connect this pin to ground right next to the controller or to the exposed pad underneath the controller.
27	LG1	Use a fairly wide trace (>30mil). Avoid routing or crossing any sensitive analog signals near this trace.
29	VDDP	Place the decoupling capacitor a close as possible to this pin.
30	LG2	Use a fairly wide trace (>30mil). Avoid routing or crossing any sensitive analog signals near this trace.
31	GND	Connect this pin to ground right next to the controller or to the exposed pad underneath the controller.
32, 33	PH2, UG2	Run these two traces in parallel with fairly wide traces (>30mil). Avoid routing or crossing any sensitive analog signals near this trace. Recommend routing the PH1 trace to the phase 1 high-side MOSFET source pins instead of general copper.
34	BOOT2	Use fairly wide trace (>30mil). Avoid routing or crossing any sensitive analog signals near this trace.
35	PROG2	Place resistor close to the controller.
40	ADDR	Place resistor close to the controller.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
09/15/2011	FN6897.0	Initial Release.

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL6353

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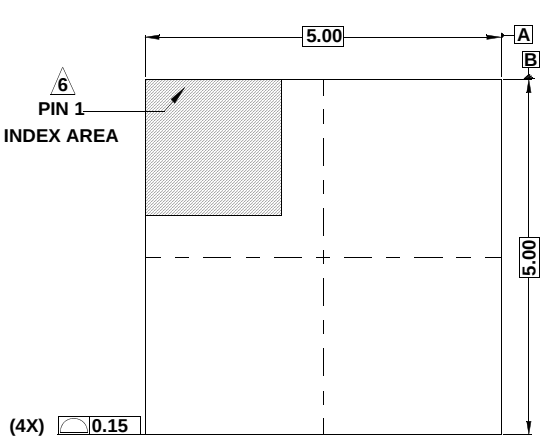
FITs are available from our website at http://rel.intersil.com/reports/search.php

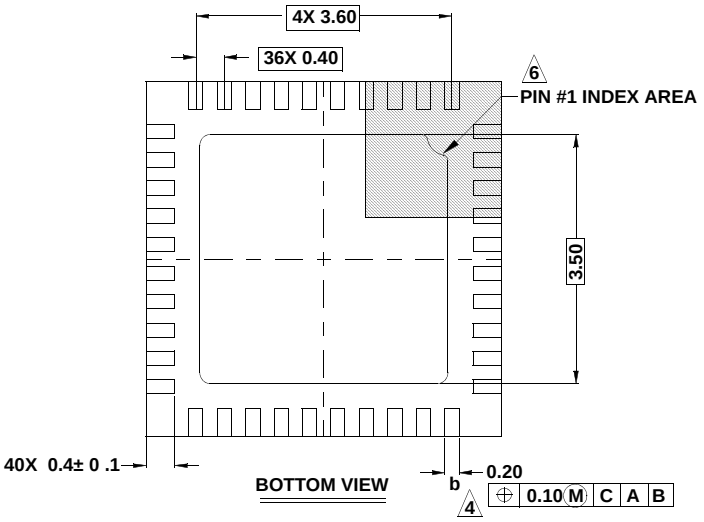
Package Outline Drawing

L40.5x5

40 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 1, 9/10

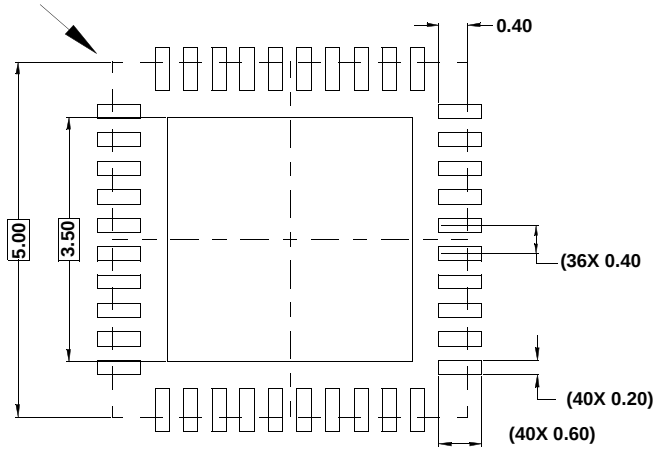


TOP VIEW

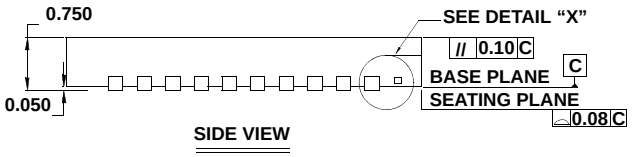


BOTTOM VIEW

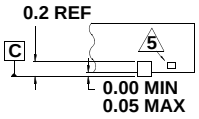
PACKAGE OUTLINE



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.27mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.
7. JEDEC reference drawing: MO-220WHHE-1