DATA SHEET

MICRONAS

VSP 94x2A
PRIMUS
Powerful Scan-Rate Converter
including Multistandard Color
Decoder

Version B13/B14

Edition Aug. 16, 2004
6251-552-1DS

◆ **MICRONAS**

Contents

Aug. 16, 2004; 6251-552-1DS

Contents, continued

VSP 94x2A

**Powerful Scan-Rate Converter
including Multistandard Color Decoder**

Release Note: Revision bars indicate significant changes to the previous edition.

1. Introduction

The VSP 94x2A (PRIMUS) is a new component of the Micronas MEGAVISION® IC set in a CMOS embedded DRAM technology. The VSP 94x2A comprises all main functions of a digital featurebox in one monolithic IC. The number of features is limited in favor of a low-cost solution, but no trade-off has been made concerning picture quality.

The family is ideally suited to work in conjunction with the deflection processors SDA 9380 (9402/32) and DDP 3315C (9412/42). In combination with the 'digital TV decoder' MDE 9500, double-scan iDTV is possible.

The package is upward pin-compatible to other medium-range and high-end devices of the VSP 94xy family. A 50/60 Hz derivative is also available (9432, 9442). The device comprises a digital multistandard color decoder, an RGB interface with fast-blank capability (SCART), digital ITU656 input, scaling units including panorama, embedded DRAM for upconversion, picture improvements, temporal noise reduction, as well as A/D and D/A converters.

Table 1–1: PRIMUS' versions

Version	Scan Rate Conversion	Digital Input	Digital Output	Analog Output
9402A (B13)	100i/120i	$(\checkmark)^{1)}$	$(\checkmark)^{1)}$	✓
9412A (B14)	100i/120i	✓	✓	
$^{1)}$ Input and output cannot be used at same time (pin sharing)				

Table 1–2: Hardware Compatibility and Suited Backend ICs

Hardware Compatible $^{1)}$	Suited Backend IC	
	DDP 3315C	SDA 9380
VSP 94**02A**, VSP 94**05B**, VSP 94**35B** VSP 94**07B,** VSP 94**37B**	✓ (No ITU656 input possible)	✓
VSP 94**12A,** VSP 94**15B**, VSP 94**45B** VSP 94**17B**, VSP 94**47B**	✓	
VSP 94**25B,** VSP 94**27B**	✓	✓
$^{1)}$ With some restrictions. Please refer to pin description and/or respective application note		

1.1. Features

– Integrated video matrix switch
  • Up to seven CVBS inputs, up to two Y/C inputs,
  • Three CVBS outputs (Y/C inputs signals are combined to CVBS output format)
  • 9 bit amplitude resolution for CVBS, Y/C A/D converter
  • AGC (Automatic Gain Control)

– Multi-standard color decoder
  • PAL/NTSC/SECAM including all substandards
  • Automatic recognition of chroma standard
  • Only one crystal necessary for all standards

– RGB-FBL or YUV-H-V input
  • 8 bit amplitude resolution for RGB or YUV
  • 8 bit amplitude resolution for FBL or H

– ITU656 support (version dependent, refer to next chapter)
  • ITU656 input/output
  • DS656 output (double-scan '656-like' output)

– Letterbox detection

– Noise reduction
  • Temporal noise reduction
  • Field-based temporal noise reduction for luminance and chrominance
  • Different motion detectors for luminance and chrominance or identical
  • Flexible programming of the temporal noise reduction parameters
  • Automatic measurement of the noise level

– Horizontal scaling of the $1f_H$ signal
  • Split-screen possible with additional PiP or Text processor

– Flexible digital horizontal scaling of the $2f_H$ signal
  • Scaling factors: 3, ..., 0.75 including 16:9 compatibility
  • 5 zone panorama generator

– Embedded memory
  • On-chip memory controller
  • Embedded DRAM core for field memory
  • SRAM for PAL/SECAM delay line

– Data format 4:2:2

– Flexible clock and synchronization concept
  • Horizontal line-locked or free-running mode
  • Vertical locked or free-running mode

– Scan-rate-conversion
  • Simple interlaced modes (100/120 Hz): AABB, AAAA, BBBB (9402A/9412A only)
  • No scan-rate-conversion modes (50/60 Hz): AB, AA, BB (9432A/9442A only)

– Flexible output sync controller
  • Flexible positioning of the output signal
  • Flexible programming of the output sync raster
  • 'Blank signal' generation

– Signal manipulations
  • Still field
  • Insertion of colored background
  • Windowing
  • Vertical chrominance shift for improved VCR picture quality

– Sharpness improvement
  • Digital color transition improvement (DCTI)
  • Peaking (luminance)

– Three D/A converters
  • 9 bit amplitude resolution for Y, -(R-Y), -(B-Y) output
  • 72 MHz clock frequency
  • Two-fold oversampling for anti-imaging
  • Simplification of external analog postfiltering

– 1920 active pixel/per line in default configuration

– I^2C-bus control (400 kHz)
  • Selectable I^2C address

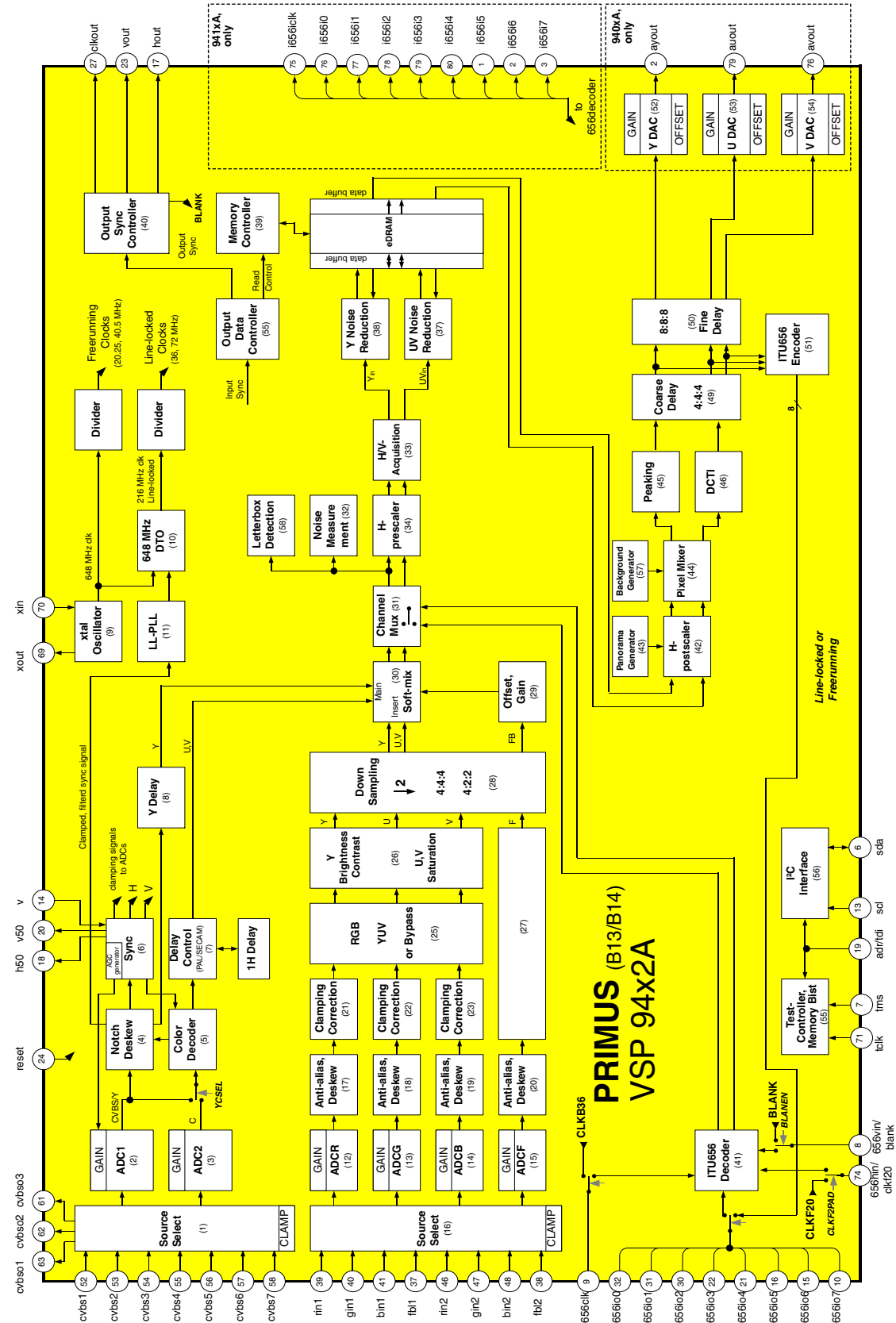– 1.8 V ±5% and 3.3 V ±5% supply voltages

– PMQFP80-1 package

Fig. 1–1: Block Diagram

2. Functional Description

All I^{2}C bus registers mentioned are printed in bold and italics (e.g. **YCDEL**).

2.1. CVBS Front-end

The CVBS front-end consists of the color decoding circuit itself, a sync processing circuit for generation of H/V signals out of the CVBS signal, and the luminance processing. The main task of the luminance processing is to remove the color carrier by means of a notch filter. For PAL and SECAM operation a baseband delay line is used for U and V signals. This can be used as comb filter in NTSC operation (only for chrominance). The RGB input can either be used as an overlay for the CVBS channel (RGB+FBL) or as a full master channel (RGB+H/V). The overlay is done by means of a soft-mix and can be used e.g. for 'SCART' connector. This block contains a matrix (for RGB signals) which is switched off for YUV (e.g. YPbPr) input signals. A CBS (contrast, brightness, saturation) control makes the input signal adjustable.

2.1.1. Source Select

Fig. 2–1 shows the analog front-end. The analog CVBS signal can be fed to the inputs CVBS1...7 of VSP 94x2A (amplitude 0.5...1.5 V$_{pp}$). One signal is selected via **CVBSEL1** and fed to the first ADC. A second signal is selected via **CVBSEL2** and fed to the other ADC. CVBS4&5 or CVBS6&7 are intended to be use as separate Y/C inputs (**YCSEL**). After clamping to the back porch both signals are AD-converted with an amplitude resolution of 9 bit. The AD conversion is done using a 20.25 MHz freerunning stable crystal clock. Before the A to D conversion the signals are lowpass filtered to avoid antialias effects. Three inputs

can be looped back to output CVBSO1-3 (**CVBOSEL1**, **CVBOSEL2**, **CVBOSEL3**). A signal addition is performed to output a CVBS signal even when separate Y/C signals are used at input. Inputs that are not used are roughly clamped to fit in the allowed voltage region. For stand-by operation (power-down mode), A/D and D/A converter are switched off by **STANDBY** keeping the source-selector operational.

2.1.2. Signal Levels and Gain Control

To adjust to different CVBS input voltages a digitally working automatic gain control is implemented. Input voltages in the range between 0.6 to 1.8 V$_{pp}$ can be applied to the CVBS inputs.

For best signal-to-noise ratio the maximum available CVBS amplitude is recommended.

The AGC behavior can be chosen from four possible modes (**AGCMD**) (see Table 2–1).

Table 2–1: AGC Modes

AGCMD	AGC Operation Mode
00	AGC uses the height of the sync pulse as a reference and additionally reduces amplification when ADC overflows
01	AGC uses the height of the sync pulse as a reference
10	AGC uses only ADC overflows
11	AGC is disabled and the ADC fits to the values given in **AGCADJ1**
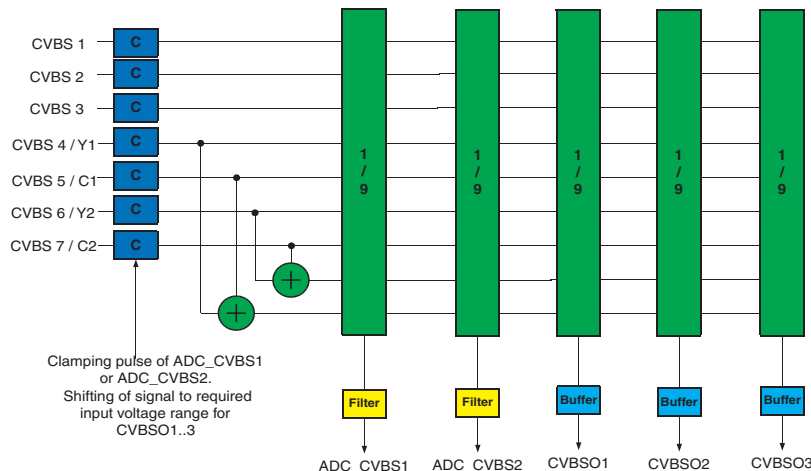
Fig. 2–1: Input Selection
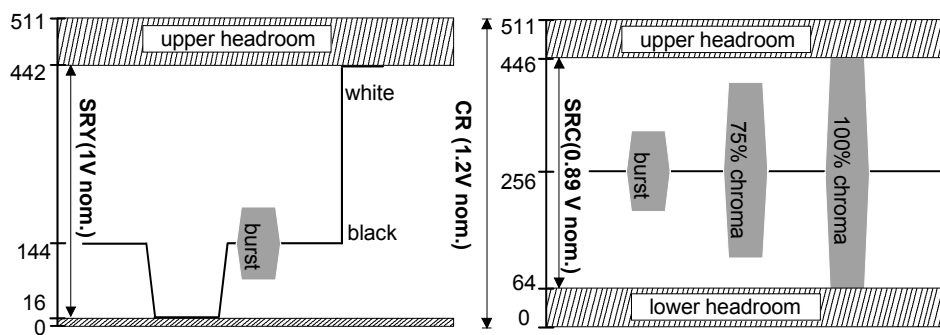
Fig. 2–2: CVBS, Y and C Amplitude Characteristics.

When using the sync height based AGC mode, the A/D gain increases or decreases depending on the incoming signal. When using overflow detection only, the gain is set to maximum and is reduced whenever an 'overflow' occurs.

The signal is low pass filtered so that chrominance and noise are not used for detection. The threshold can be adjusted by **PWTHD**. A setting of '11' equals 511 and means an overflow of the ADC. Other settings react for a lower level. The gain only becomes higher when a change of the channel is detected or is manually reset by **AGCRES**. **AGCFRZE** holds the current AGC value.

A manual setting of the ADCs gain control is possible using the parameters **AGCADJ1** and **AGCADJ2**.

The conversion range (CR) is bigger than the signal range (SRY, SRC) leaving a headroom for overshoots (see Fig. 2–2).

.

2.1.3. Clamping

The timing of the clamping (pulse) control signals for the analog inputs are derived from its corresponding CVBS input signal. The clamping algorithm works with a split *measurement* pulse and a *clamping* pulse. The measurement pulse is used to detect the clamping error. The clamping pulse is used to enable current sources for reducing the detected clamping errors. The start and length of the measurement signals are independently adjustable for both channels (**CLMPST1**, **CLMPD1**, **CLMPST2**, **CLMPD2**).

The same applies for the clamping signals (**CLMPST1S**, **CLMPD1S**, **CLMPST2S**, **CLMPD2S**). Clamping and measurement signals for RGB channel are not separate. Clamping for these ADC are controlled by **CLMPST2S** and **CLMPD2S** only. Clamping can be suppressed for some lines by **CLMPLOW** and **CLMPHIGH** to ignore copyprotection information. No external sync signals are required.

Fig. 2–3: CVBS ADC Characteristic
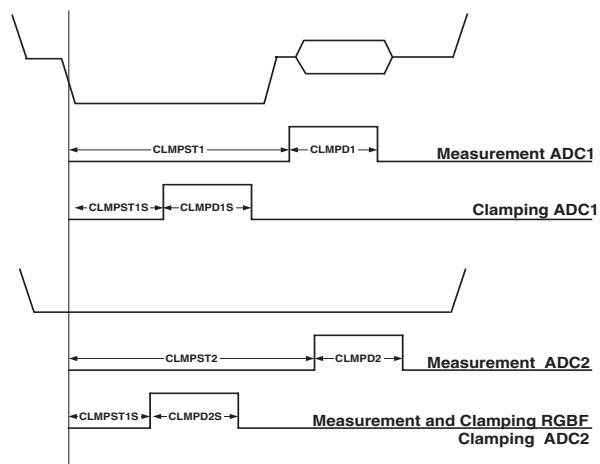
Fig. 2–4: Clamping Signals

Table 2–2: Clamping Adjustment

Signal	Description
CLMPST1	Measurement pulse start for ADC1
CLMPD1	Measurement pulse duration for ADC1
CLMPST1S	Clamping pulse start for ADC1
CLMPD1S	Clamping pulse duration for ADC1
CLMPST2	(Measurement pulse start for ADC2)
CLMPD2	(Measurement pulse duration for ADC2)
CLMPST2S	Measure and clamp start for RGBF-ADC (clamping start for ADC2)
CLMPD2S	Measure and clamp duration for RGBF-ADC (clamping duration for ADC2

2.1.4. Synchronization

After elimination of the high frequent components of the CVBS signal by a low pass filter, horizontal and vertical sync pulses are separated. Horizontal sync pulses are generated by a digital phase locked loop. The time constant can be adjusted between fast and slow behavior in four steps (*PLLTC*) to accommodate different input sources (e.g. VCR). The time-constant can be changed during normal operation without visible picture degradation. A fine tuning of the PLL time constant can be done by *NSRED*.

Additional weak input signals from a satellite dish ('fish') become more stable when *SATNR* is enabled. Vertical sync pulses are separated by integration of equalizing pulses. A vertical flywheel mode improves vertical sync separation for weak signals (*VFLYWHL, VFLYWHLMD*).

Additionally, v-syncs may be gated by *VTHRL* and *VTHRH* to reject invalid v-syncs (independently adjustable for 50 and 60 Hz sources) if no input signal is connected the device switches to a freeruning mode. The device can be configured to switch-on background color when no or only a weak signal is applied (*NOSIGB*). 50 Hz or 60 Hz operation for sync separation may be forced separately or selected to work automatically (*FLNSTRD*).

2.1.5. Chroma Decoder

The digital multistandard chroma decoder is able to decode NTSC and PAL signals with a subcarrier frequency of 3.58 MHz and 4.43 MHz (PAL B[*]/N/ 60[†],NTSC M/4.4) as well as SECAM signals with automatic standard detection. Alternatively a standard can be forced. The demodulation is done with a regenerated color-carrier. To enable a factory adjustment of the crystal frequency, the frequency of the regenerated subcarrier can be adjusted via *SCADJ*. For this purpose the crystal deviation (*SCDEV*) can be read out via I^2C after chroma PLL locking (indicated by *SCOUTEN*) and can be stored in μC ROM for *SCADJ*. For test purposes, *CPLLOF* allows the opening of the chroma PLL loop.

For adjustment to the specific operational area an automatic norm detection is selectable. Available 50 Hz color standards are PAL B, PAL N and SECAM. Available 60 Hz color standards are NTSC M, PAL M, PAL60 and NTSC44. For each line standard, one or more color standards can be enabled for automatic chroma standard detection. Please refer to **Table 2–3:** and **Table 2–4:** for allowed combinations.

The standard detection process can be set to slow or fast behavior **(LOCKSP).** In slow behavior, 25 fields are used to detect the standard, whereas 15 fields are used in fast behavior. If the detection was not successful during this time frame, the system will switch to the next enabled TV Standard.

---

* PAL B is representative for PAL B/G/H/I/N
† PAL60 and NTSC44 are nonstandard signals which are generated by some VCR or DVD player

Table 2–3: Allowed combinations for color-standard search (50 Hz)

Standard	CSTAND		
(50 Hz)	**D2**	**D1**	**D0**
None	0	0	0
PAL N	0	0	1
PAL B	0	1	0
SECAM	1	0	0
Automatic PAL BG / SECAM	1	1	0

Table 2–4: Allowed combinations for color-standard search (60 Hz)

Standard	CSTAND			
(60 Hz)	**D6**	**D5**	**D4**	**D3**
PAL M	0	0	1	0
NTSC M	0	1	0	0
NTSC44	1	0	0	0
Automatic PAL M / NTSC M	0	1	1	0
Automatic NTSC M / NTSC44/PAL60	1	1	0	0(!)

In addition, a standard can be forced as well. **AMSTD50** selects whether PAL B or SECAM is tried first in the automatic routine. **AMSTD60** selects whether NTSC44/PAL60 or NTSC M is tried first. Both bits can also be set for automatic detection, then the last detected chroma standard will be used. For SECAM detection, a choice between different recognition levels is possible (**SCMIDL, SCMREL**) and the evaluated burst position is shiftable (**BGPOS**).

Color standard (**STDET**), line standard (**LNSTDRD**) and color killer status (**CKSTAT**) can be read out.

An Automatic Chroma Control (ACC) produces a stable output for input chroma variations from (approximately) -30 dB to +6 dB compared to nominal burst value. The ACC reference value is programmable for NTSC and PAL independently (**NTSCREF, PALREF**) to ensure correct color saturation. With **ACCFIX**, the ACC is disabled and a constant value (dependent on **NTSCREF** and **PALREF**) is used instead.

ACCFRZ holds the current ACC value. The maximum amplification of the ACC can be limited by **ACCLIM.**

This results a smooth attenuation of color intensity for weak color carrier (see Fig. 2–5).
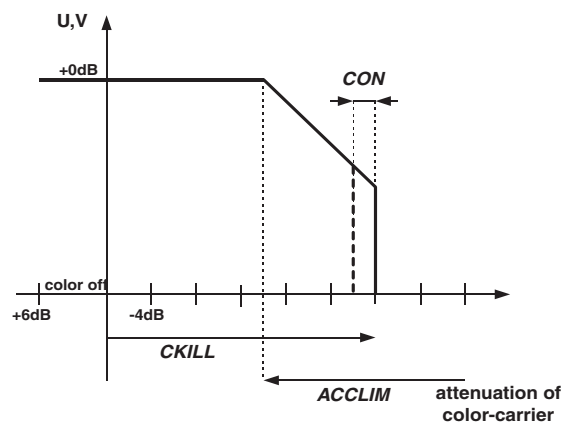
PAL, NTSC operation
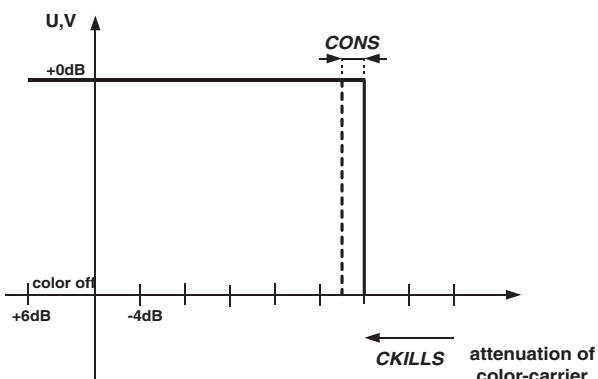
SECAM operation

Fig. 2–5: Color Killer Adjustment

If the chrominance signal is below an adjustable threshold (**CKILL** (PAL; NTSC) or **CKILLS** (SECAM)) the color is switched off. To prevent on / off switching, a hysteresis is given by **CON** or **CONS** which is the value of switching on the color. **COLON** switches on the color under any circumstance.

The output of the color decoder can be set to UV or CrCb data by **CRCB.** For NTSC only, the color impression (tint) can be adjusted by the Hue Control between -88° and 90° in steps of 0.7° (**HUE**). Low chrominance values (+/- 1...3 LSB) may be deleted by UV-coring (**UVCOR**). The Chroma bandwidth can be adjusted by **CHRF**. The setting value of CHRF has no linear impact to the chroma bandwidth. The frequency response of the Chroma bandfilter are shown in Figure 2-7. Also a filter with asymmetrical characteristic around the color carrier is available (**IFCOMP**) (Figure 2–7). For SECAM mode, the de-emphasis filter can be adjusted by **DEEMPFIR** and **DEEMPIIR**. The bell filter can be adjusted by **BELLFIR** and **BELLIIR**.

The delay between Y and C is well aligned and can also be adjusted in steps of 50 ns (**YCDEL**). No picture shifting occurs when switching between different color standards (e.g. SECAM -> PAL). A delay-line is implemented for PAL and SECAM signals. It acts as a simple chrominance comb-filter for NTSC and can be disabled by **COMB.** This improves the vertical chroma resolution, but cross-color remains.
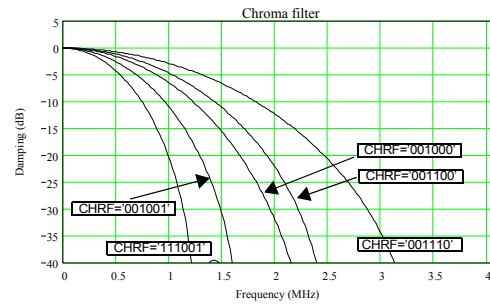
Fig. 2–6: Chroma Filter Characteristics
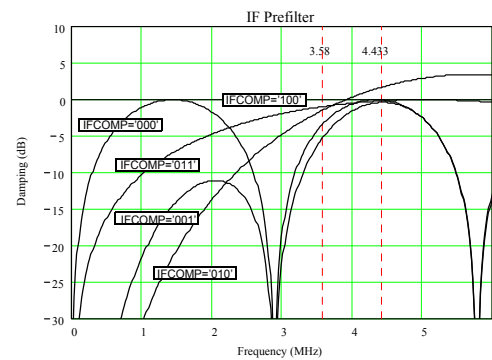
Fig. 2–7: IF Prefilter

2.1.6. Luminance Processing

A luminance notch filter is implemented to separate the chroma information from the luminance. Depending on the color standard, one out of three different notch characteristics is chosen ('PAL', 'NTSC', 'SECAM') automatically.

For PAL and Secam the respective notch filters have 5 different characteristics each. The luminance notch filter for NTSC can be set to 4 different filter response curves. They can be selected by **NTCHSEL**. Alternatively, no notch should be used for Y/C input (**NOTCHOFF**). The filter characteristics can be found in Figure 2–8. In SECAM operation, the notch filter can be fixed to one frequency or toggle between 4.4 MHz and 4.25 MHz depending on the transmitted color (Dr, Db) (**SECNTCH**).

A simple lowpass-filter can be enabled by **LPPOST** to further reduce high-frequency noise component from the CVBS signal.

characteristic for NTSC
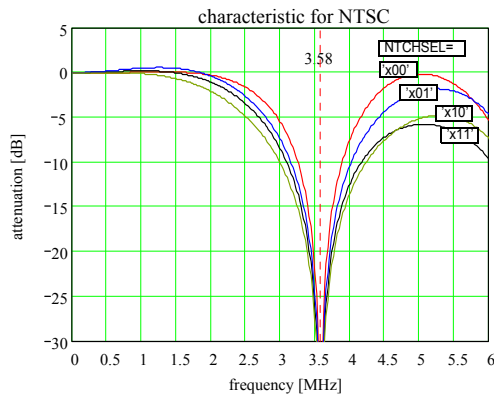
Fig. 2–8: Filter Characteristics for NTSC, PAL M and PAL N

characteristic for PAL
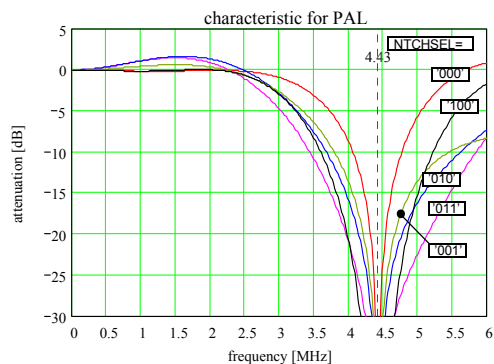
Fig. 2–9: Filter Characteristics for PAL B/G, NTSC44, PAL60

characteristic for SECAM (4.25 MHz)
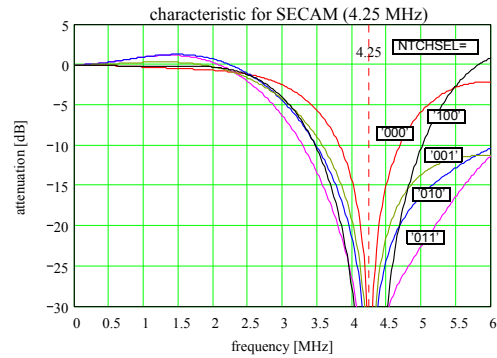
Fig. 2–10: Filter Characteristics for SECAM (*SECNTCH*='01', 4.25 MHz)

characteristic for Y/C
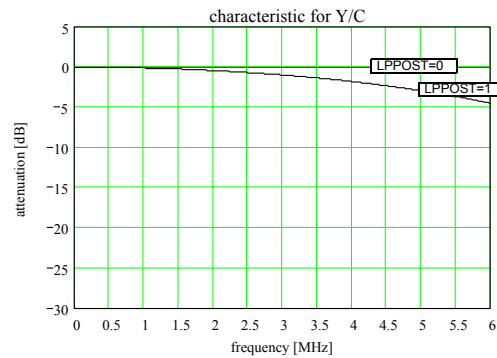
Fig. 2–11: Filter Characteristics for Y/C mode.

The black level can be shifted by the parameter **LMOFST**. This is required to compensate 7.5 IRE offsets in some input signals (e.g. NTSC) The positive or negative offset is added to the Y signal before scaling.

BLANKING BLACK
LMOFST='10'
LMOFST='00'
LMOFST='11'
LMOFST='01'

BLANKING BLACK
LMOFST='10'
LMOFST='00'
LMOFST='11'
LMOFST='01'

Input signals without 7.5IRE offset

Input signals with 7.5IRE offset
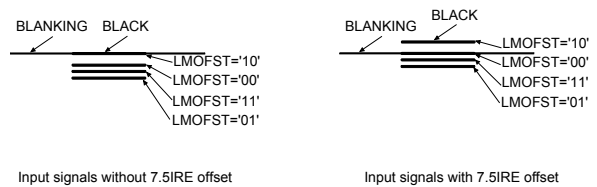
Fig. 2–12: Adjustment of 'Black' to 'Blankingvalue' at Analog Output.

2.2. RGB Front-end

An analog RGB input port for an external RGB or YUV source is available. The incoming signal is clamped to the back porch by a clamping pulse. As the memory is only able to store a 4:2:2 picture, the YUV input signal is downconverted to 4:2:2. There are two operation modes available. The first one uses this input as an overlay input (soft mix). The RGB or YUV signal must then be synchronized to the main CVBS/YC signal. The second so called independent mode uses RGB /

YUV including sync or H/V signals. This can be used, for example, for a DVD player or set-top-box. When using H sync from a non CVBS input (e.g. separate H-sync) this must be indicated by *HINP*. The usage of separate V sync must be set by *VINP*.

The delay of luminance and fast-blank can be adjusted by *YFDEL*, and chrominance can be delay adjusted by *UVDEL*. If necessary, a fine adjustment of the fast blank can be set by the parameter *FBLDEL*.

Table 2–5: Possible input signals for RGB Front-end

Input Signal	FBL_{IN}	V_{IN}	Sync Separation	Remark	Hinp	Vinp
RGB	CVBS[1]		Sync on CVBS		1	0
YUV	CVBS[1]		Sync on CVBS		1	0
RGB	H[1]	V	Sync on H	E.g. set-top-box	1	1
YUV	H[1]	V	Sync on H	E.g. set-top-box	1	1
RGB	FBL		Synchron to CVBS/YC	Soft mix	0	0
YUV	FBL		Synchron to CVBS/YC	Soft mix	0	0
RGB (incl. sync)			Sync on G (maybe on R/B)	No external sync	1	0
YUV (incl. sync)			Sync on Y	No external sync e.g. DVD	1	0
[1] Instead of FBL input, CVBS input can be used when Hinp=0						
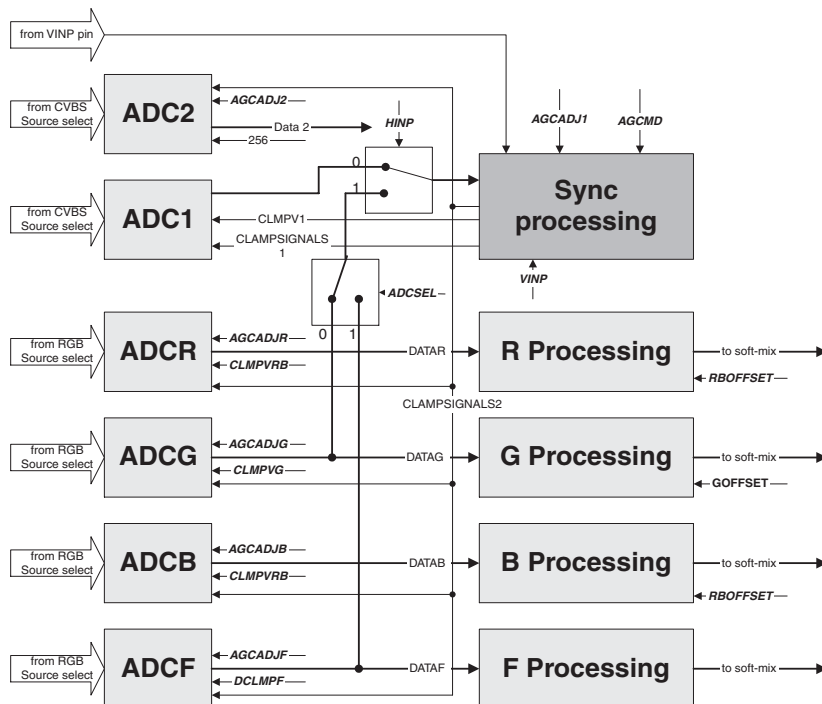
Fig. 2–13: Signal and Clamping Organization

2.2.1. Source Select

Two inputs are available. The choice between the first or second input is made by **RGBSEL**.

2.2.2. Signal Magnitudes and Gain Control

The gain adjustment of the four ADCs can be done with the parameters **AGCADJR**, **AGCADJG**, **AGCADJB**, **AGCADJF**
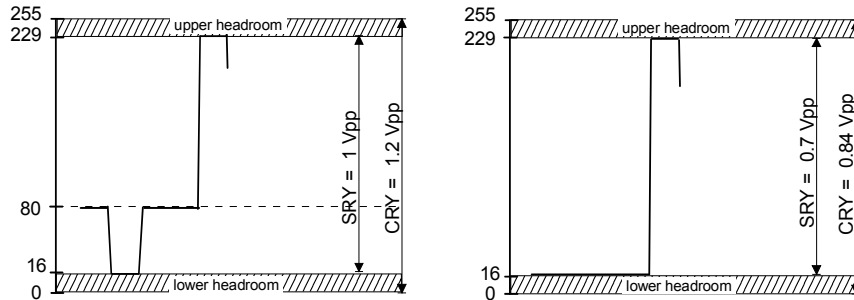
Fig. 2–14: Y/RGBF Amplitude Characteristics (with or without sync)
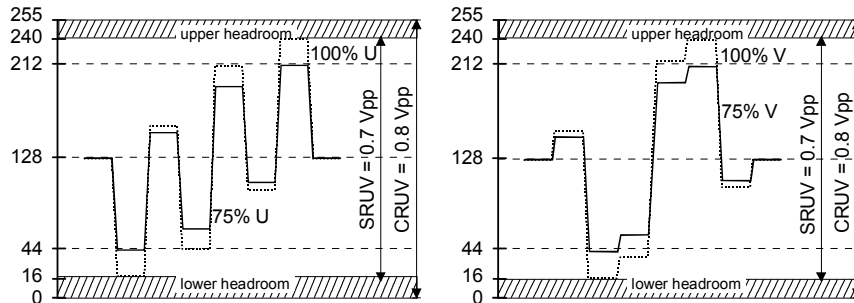
Fig. 2–15: UV Amplitude Characteristics
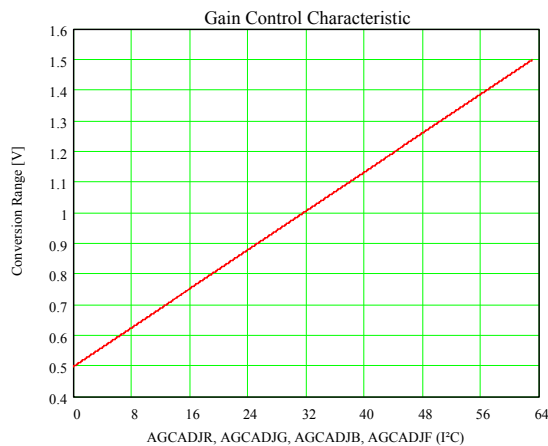
Fig. 2–16: RGB ADC Characteristic, Fast-blank ADC with Clamping (*DCLMPF*=0)
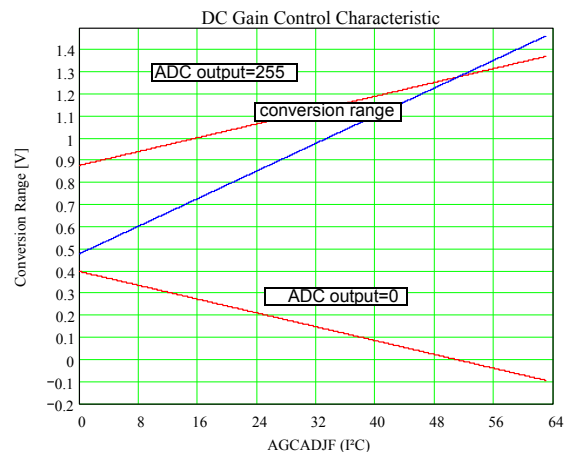
Fig. 2–17: Fast-blank ADC Characteristic without Clamping (*DCLMPF*=1)

Table 2–6: Configurations of input signals

Mode	CLMPVG	CLMPVRB	GOFST	RBOFST	DCLMPF
YUV, sync on Y	80	128	64	128	Don't care
YUV, sync on H,V	16	128	0	128	0 (clamping enabled)
RGB, sync on G	80	16	64	0	Don't care
RGB, sync on RGB	80	80	64	64	Don't care
RGB, sync on H,V	16	16	0	0	0 (clamping enabled)
RGB with fast-blank, synchron to CVBS	16	16	0	0	1 (clamping disabled)
YUV with fast-blank, synchron to CVBS	16	128	0	128	1 (clamping disabled)

2.2.3. Clamping

When using the dynamic softmix-mode with fast-blank, clamping of fast-blank input must be disabled by **DCLMPF**. The analog clamping value of red and blue input (V and U resp.) can be adjusted by **CLMPVRB**. The analog clamping value of green input (Y resp.) can be adjusted by **CLMPVG**. Depending on the input signal format (YUV, RGB, sync signal or not) these bits must be set accordingly. On the digital side, a correction of the analog clamping value must be performed to reconstruct the blacklevel. This is achieved by **RBOFST** and **GOFST**. (see Table 2–6 on page 15)

2.2.4. Digital Prefiltering

A digital prefiltering can be enabled. A band limitation is required, because the following deskewing filter performs best at frequencies of below 14 MHz. The filtering is performed in all four channels and can be disabled by **AABYP**. For signal conversion to 4:2:2, an additional chrominance lowpass can be enabled by **CHRSF**. The deskewing filter can be disabled by **SKEWSEL**. This is necessary when using the H50-pin in connection with a Micronas picture-in-picture device (e.g. SDA 938x, SDA 948x, SDA 958x). In this application, the RGB input (in1, in2, in3) of the PiP can not be used for other RGB/YUV signals (e.g. 'SCART' is not possible). As there is a pixel skew on H50, this pin is NOT suited to synchronize any IC, except for the above mentioned PiP ICs
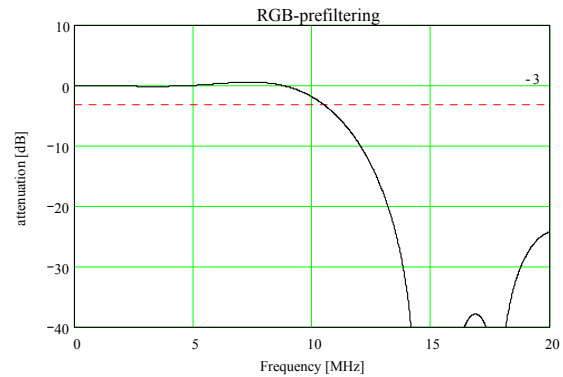
Fig. 2–18: Digital Prefiltering of RGB Input

2.2.5. RGB → YUV Matrix

RGB or YUV signals are selected by **YUVSEL**. The matrix coefficients are set according to ITU recommendations.

$$\begin{bmatrix} Y \\ U \\ V \end{bmatrix} = \begin{bmatrix} R \\ G \\ B \end{bmatrix} \cdot \begin{bmatrix} 0{,}299 & 0{,}587 & 0{,}114 \\ -0{,}147 & -0{,}289 & 0{,}436 \\ 0{,}615 & -0{,}515 & -0{,}100 \end{bmatrix}$$

Fig. 2–19: RGB to YUV Matrix

2.2.6. Contrast, Brightness and Saturation Control of Input Signal

The YUV signal can be manipulated in order to fit to the main channel. The contrast can be adjusted between 0 and 1.97 in 64 steps (**CONADJ**). The brightness is adjustable in 255 steps (**BRTADJ**). Due to the independent chroma adjustment of U and V (64 steps each, **USATADJ**, **VSATADJ**), UV as well as CrCb input signals can both be displayed correctly.

2.2.7. Soft Mix

The soft-mixer circuit consists of a Fast Blank (FB) processing block supplying a mixing factor k (0... 128) achieving the output function:

$$YUVmix = \frac{YUV_{main} \cdot (128 - k) + YUV_{inserted} \cdot k}{128}$$

k= '0' means that only the main signal is fed through to the output. k= '128' means that only the inserted signal becomes visible. The soft mixer supports four modes that are selected by **MIXOP** and **SMOP.**

Table 2–7: RGB operation modes

MIXOP	SMOP	Soft Mix mode
00	0	Dynamic Soft Mix (**DECTWO** must be set to '1')
00	1	Static Soft Mix (**DECTWO** must be set to '1')
01	x	Only RGB/YUV path visible
10	x	Only CVBS path visible
11	x	(Reserved)

2.2.8. Static Switch mode

In its simplest and most common application the soft-mixer is used as a static switch between YUVmain and YUVinsert. This for instance the adequate way to handle a DVD component signal. By using **MIXOP**, k is internally set to 0 or 128 respectively.

2.2.9. Static Mixer mode

The signal YUVmain and the component signal YUVinsert may also be statically mixed. In this environment, k is manually controlled via **FBLOFFSET** and **MIXGAIN**.

$$k = MIXGAIN \cdot (31 - FBLOFFST) + 32$$

All necessary limitation and rounding operations are built-in to fit the range: $0 \leq k \leq 128$

Considering **MIXGAIN**=3, k is obtained by

$$k = 158 - 3 \cdot FBLOFFST$$
[κ limited to 0 and 128]

The mixing is only controlled by **FBLOFFST**.

In the static mixer mode as well as in the previously mentioned static switch mode, the softmixer operates independently of the analog fast blank input.

2.2.10. Dynamic Mixer mode

In the dynamic mixer mode, the mixer is controlled by the Fast Blank signal. The VSPA provides a linear mixing coefficient

$$k = \frac{MIXGAIN(FB - FBLOFFST \cdot 2)}{2} + 64$$

The dynamic mode is used for mixing which is dependent on FB input. FB is the preprocessed digitized fast-blank input in the range from 0...127. FBL manipulation is done both for luminance and chrominance FBL signal.

Fast blank is delay adjustable by **FBLDEL** in the range of -2...4 clock cycles.

2.2.11. FBL Activity and Overflow Detection

It is important to know whether the FBL input is used or not. Therefore a detection circuit gives information via the I^{2}C bus to the microcontroller. The circuit uses the FBL value as input. If it is greater than a threshold for one or five clock cycles (**FBLCONF**), the I^{2}C register **FBLACTIVE** is set. This register is reset after a read access by the microcontroller. **PFBL**, **PG**, **PR**, **PB** indicate an overflow of the corresponding ADC (upper limit: ADC= 255) exceeding 5 clock cycles duration.

2.3. Input Processing
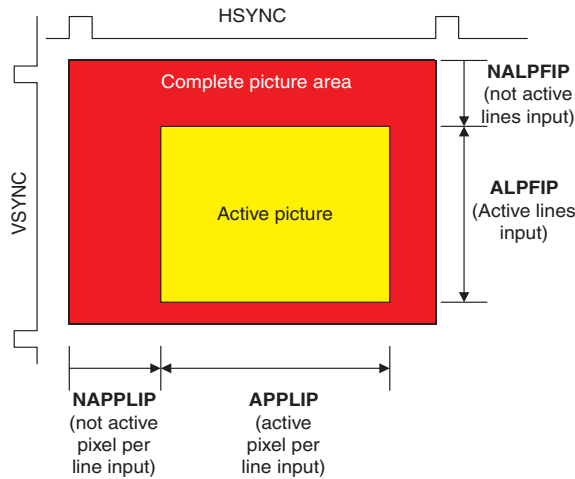
Fig. 2–20: Image Format before Memory

2.3.1. Horizontal Prescaler

The main application of the horizontal prescaler is the conversion of the number of pixels coming form the 40.5/20.25 MHz pixel clock domain down to the number of pixels stored in the memory (factor 2/3). Generally the number of incoming pixels can be decimated by a factor between 1 and 64 in a granularity of 2 output pixels. The horizontal scaler reduces the number of incoming pixels by subsampling. To prevent the introduction of alias distortion low pass filters are used for luminance and chrominance processing (Fig. 2–22). In case of ITU656 input, the lowpass filter must be disabled by **HAAPRESC**.

The horizontal prescaler consists of two main subsampling stages. The first stage is a scaler for rational decimation factors in a range of 1 to 2, controlled by **HSCPRESC**. The second stage decimates in integer steps (1,2,3,4...32), controlled by **HDCPRESC**.

Fig. 2–21: Y-decimation Filter Characteristics for Standard Operation (Decimation=1.5)

Fig. 2–22: UV-decimation Filter Characteristic for Standard Operation (Decimation=1.5)

2.3.2. Noise Reduction

The Fig. 2–23 shows a block diagram of the temporal noise reduction. The structure of the temporal motion adaptive noise reduction is the same for luminance as for chrominance signal. Noise reduction is enabled by **NRON**.

The output of the motion detector is weighted using the parameters **TNRCLC** and **TNRCLY**. The look-up table input value range is separated into 8 segments. It is possible to freely program different behavior of the noise reduction by using predefined curve characteristic for each segment. The curve characteristics can be programmed by the parameters **TNRSxY** for luminance and **TNRSxC** for chrominance. The curve-start is defined by **TNRSSY** (**TNRSSC**) at the end of the last segment (Figure 2–24). The overall curve is now constructed by connecting the end of segment 6 to the beginning of segment 7 and so on. Negative values of Ky (Kc) are not possible and clipped to zero.

For chrominance, the result of the luminance motion detector or a separate chorminance motion detector can be used (**TNRSEL**).

Fig. 2–23: Temporal Noise Reduction
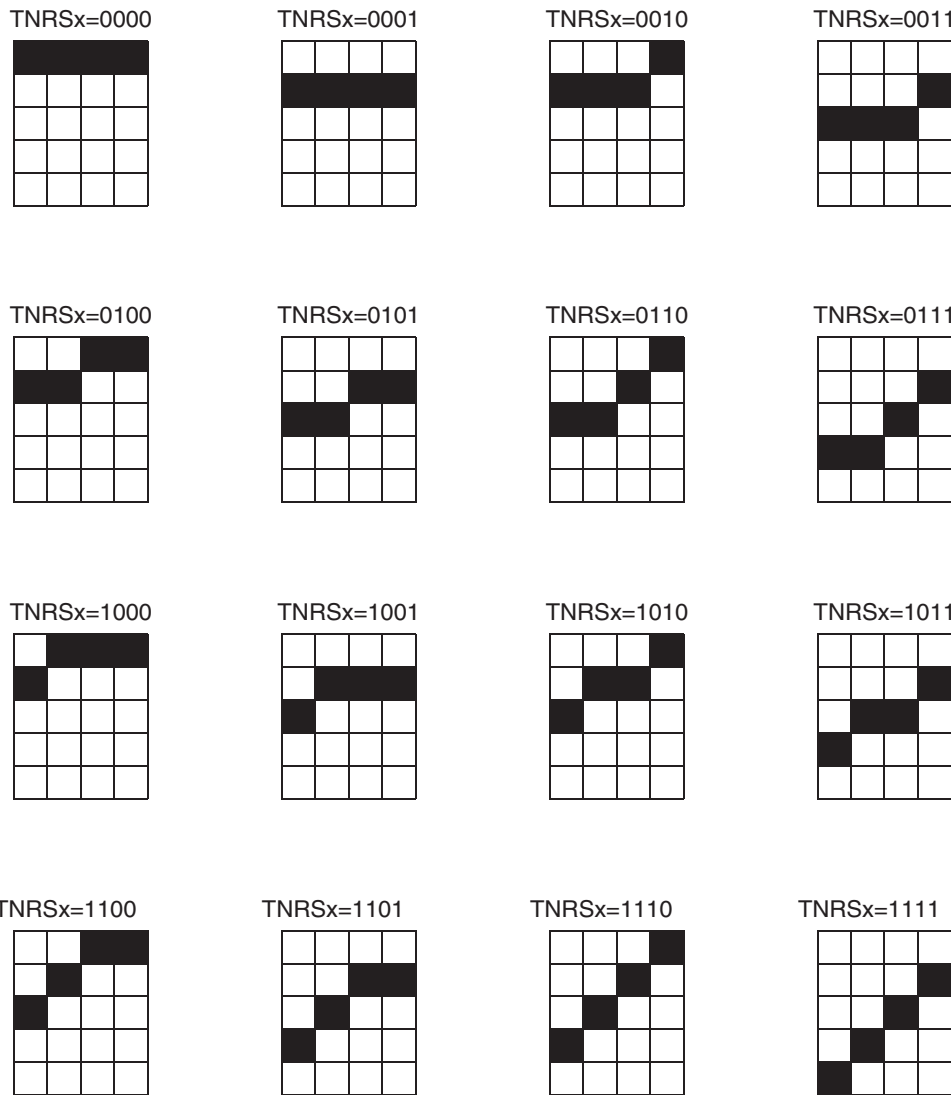
Fig. 2–24: Segments of LUT
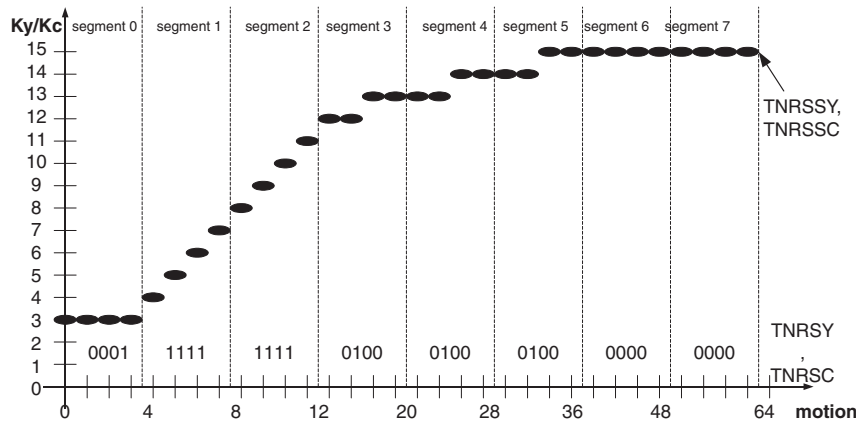
Fig. 2–25: Predefined Curve Characteristics for LUT

2.3.3. Noise Measurement

The noise measurement algorithm can be used to change the parameters of the temporal noise reduction processing depending on the actual noise level of the input signal. This is done by the TV- microcontroller which reads the noise level (**NOISEME**), and sends different parameter sets to the temporal noise reduction registers of the VSP 94x2A depending on this value (0 = no noise, 126 = strong noise). Value 127 indicates an overflow status which means that the measurement failed. The value is determined by averaging over several fields. The line taken for noise measurement is selected by **NMLINE**. When **NOISEME** contains updated data which were not read so far, **NMSTATUS** is set. **NMSTATUS** is reset when read. The measurement position can be adjusted (**NMPOS**) as well as the sensitivity (**NMSENSE**).

2.3.4. Letterbox Detection

A drawback of wide screen 16:9 TV sets are the black bars at the left and the right side on the screen, if displaying a 4:3 source on a 16:9 screen with correct aspect ratio. In case of letterbox source material also

black bars at the top and bottom exist. With the help of an expansion algorithm it is possible to expand the letterbox picture vertically and horizontally in such a way, that the letterbox picture will fill the complete screen without loosing information. To do so, the information about the active part of the letterbox picture is necessary. Active part means the information about the first active line and the last active line of the letterbox picture. The figure below shows the principle of this idea.

The WSS (Wide Screen Signal) signal contains some information about the picture format (4:3 or 14:9 or 16:9), but not all existing formats are covered and not all signals contain WSS. Therefore a separate algorithm is necessary which delivers the necessary information. The figure below shows the concept of the letterbox detection algorithm. One part of the algorithm is dedicated hardware and located in the VSP 94x2A another part is software and located in the RAM of the TV microcontroller. The part located in VSP 94x2A is called measurement part. The measurement part delivers 5 signals to the controller part.Based on the delivered information the controller part calculates an expansion and a vertical pan factor and sends these values back to the VSP 94x2A for manipulation of the video signal.

4:3 Letterbox Picture

Expanded Letterbox Picture
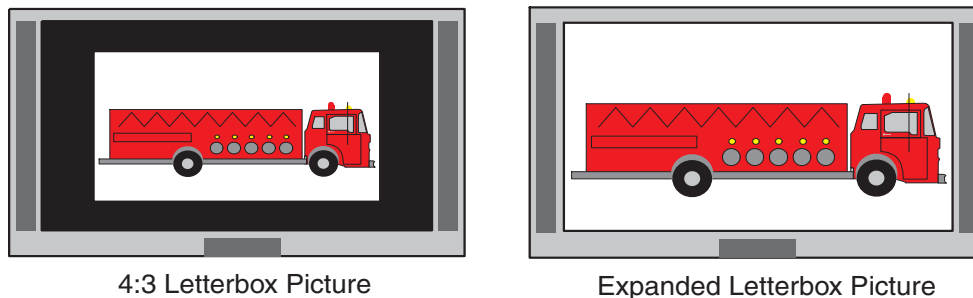
Fig. 2–26: Handling of Letterbox Pictures on 16:9 Tubes
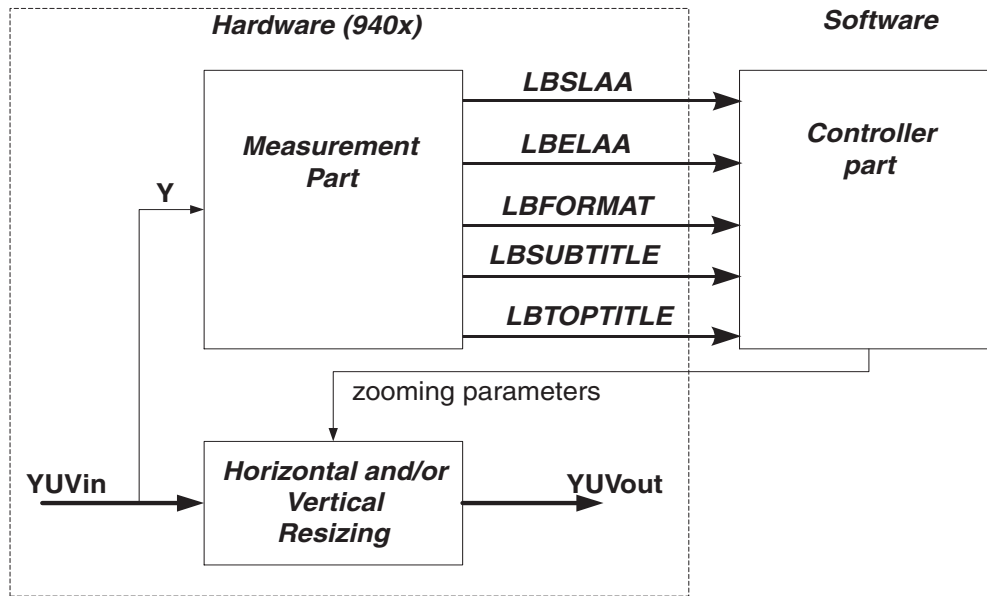
Fig. 2–27: HW/SW Partitioning

The letterbox detection block works only at a data rate of 13.5 MHz. Due to the fact, that the input data rate at channel-mux output can be 13.5 MHz, 20.25 MHz or 40.5 MHz, the input signal has to be downsampled. Depending on the I^2C bus register **LBSUB** different modes are possible (Downsample 1, 1.5, 3). As digital 656input data are already in 13.5 MHz format, no downsampling should be used (**LBSUB**=0). For CVBS, YUV and RGB signals (if **DECTWO**=1) a downsampling of 1.5 (**LBSUB**=2) is required.

In principle the input picture is separated in one upper and one lower part. The measurement windows are defined by the parameters **LBVWSTUP**, **LBVWENDUP** (upper vertical measurement window), **LBVWSTLO**, **LBVWENDLO** (lower measurement window) and **LBHWST**, **LBHWEND** (horizontal measurement window).

A controller software and its description is available upon request.
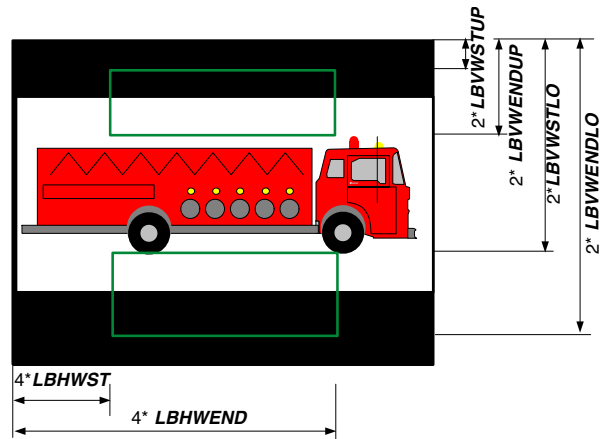
Fig. 2–28: Measurement Windows

2.4. Output Processing

2.4.1. Horizontal Postscaler

After main memory, the display processing is performed using a different clock. In this way a decoupling of input and output clocks is achieved. The conversion to the display clock is done by an interpolation filter. This can be used for horizontal expansion in the range of 1...4 in steps of 2 pixels (**HSCPOSC**). Due to increased clock frequency in the backend part, the realized horizontal scaling factor depends on backend clock frequency. Usually (36 MHz operation), the horizontal expansion factors result as 0.75...16. This ensures that the factor 0.75 gives no loss of resolution (to show a 4:3 picture on a 16:9 tube). When using DS656 output, neither horizontal compression nor horizontal panorama is possible due to 27 MHz clock.

Table 2–8: Horizontal expansion factors

HSCPOSC	Horizontal Filter Expansion	Overall Expansion	
		CLKB36= 27 MHz	CLKB36= 36 MHz
1024 (min.)	4	4	3
3072	1.33	1.33	1
4095	1	1	0.75

Because of the nonlinear characteristic and integer number of pixel, sometimes different **HSCPOSC** values result in the same decimation factors.
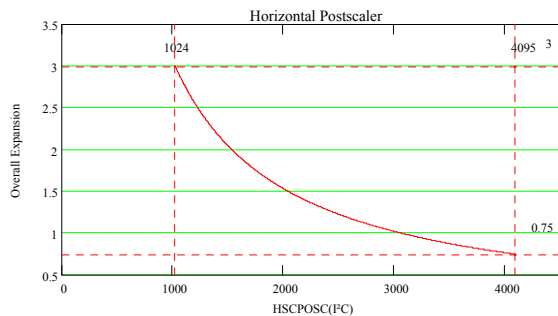
Fig. 2–29: Expansion Factor of Horizontal Postscaler Dependent on *HSCPOSC*

2.4.1.1. Panorama Mode

The picture can be geometrically distorted in horizontal direction for an improved impression in the case of expansions of 4:3 pictures to a 16:9 ratio tube. It is enabled by **HPANON**. The idea behind this panorama mode is to keep the middle part of the picture in a 4:3 ratio and to stretch the left and the right to fill the entire width of the 16:9 screen. For the adjustment of the expansion process, the picture is divided into 5 segments. For each of these segments the increment value for the expansion factor can be defined separately. Each end of a segment can be defined individually in a granularity of two output pixels. For every segment an increment value can be defined (**HINC0**...**HINC4**) which indicates the amount of decimation/expansion. One LSB is equivalent to an offset of 0.125 to **HSCPRESC** per double pixel. This means that with **HINC**, **HSCPRESC** is altered in the range from −32...31.875 per double pixel. The segments are distributed among the maximum number of pixels, which is adjusted by **PPLOP**. The first four segments are defined by (**HSEG1**...**HSEG4**). The last one goes from **HSEG4** to **PPLOP.**
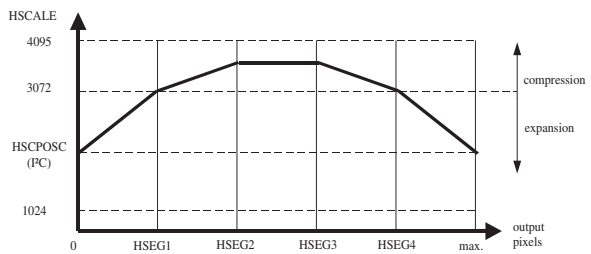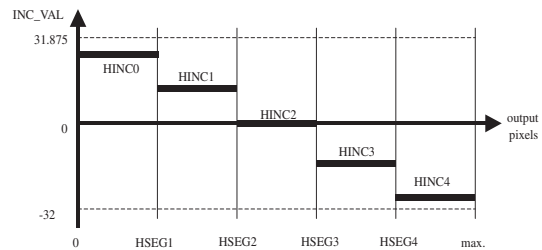
Fig. 2–30: Visualization of Panorama Segments

Table 2–9: Examples of Panorama Mode

Function	Panorama	Extreme Pan.	Lens
HSCPOSC	2099_d	1023_d	3999_d
HSEG1	96_d	96_d	96_d
HSEG2	192_d	192_d	192_d
HSEG3	288_d	288_d	288_d
HSEG4	384_d	384_d	384_d
HINC0	40_d	85_d	472_d
HINC1	20_d	43_d	492_d
HINC2	000_d	000_d	000_d
HINC3	492_d	469_d	20_d
HINC4	472_d	427_d	40_d
APPLOP	960_d	960_d	960_d

2.4.2. Operation Modes

There are four operation modes defined. The first mode is simple AABB, where each stored field in the memory is displayed double times on the TV screen. The second and third mode are AAAA and BBBB, in which only one field phase will be displayed on the TV screen. There is also a fourth mode AAAA mode with $\alpha\beta\alpha\beta$ raster possible. Fig. 2–31 explains the picture and the display raster.

The interlaced input signal (e.g. 50 Hz PAL or 60 Hz NTSC) is composed of a field A (odd lines) and a field B (even lines).

A^n - Input signal, field A at time n,

B^n - Input signal, field B at time n

The field information describes the picture content. The output signal, which could contain different picture contents (e.g. field A, field B), can be displayed with the display raster α or β.

(A^n,α) - Output signal, field A at time n, displayed as raster α,

(A^n,β) - Output signal, field A at time n, displayed as raster β,

Table 2–9 on page 22) describes the different scan rate conversion algorithms of VSP 94x2A and the corresponding raster sequences.

Fig. 2–32 on page 23 explains the 50/60 Hz interlaced to the 100/120 Hz interlaced conversion including the field signal, the raster organization and the memory timing for AABB.

A still field can be displayed using **FREEZE** command. For the improvement of VCR signals, the chrominance can be shifted one line upwards by **CHRSHFT**

FRAME/FIELD

DISPLAY LINE-SCANNING PATTERN
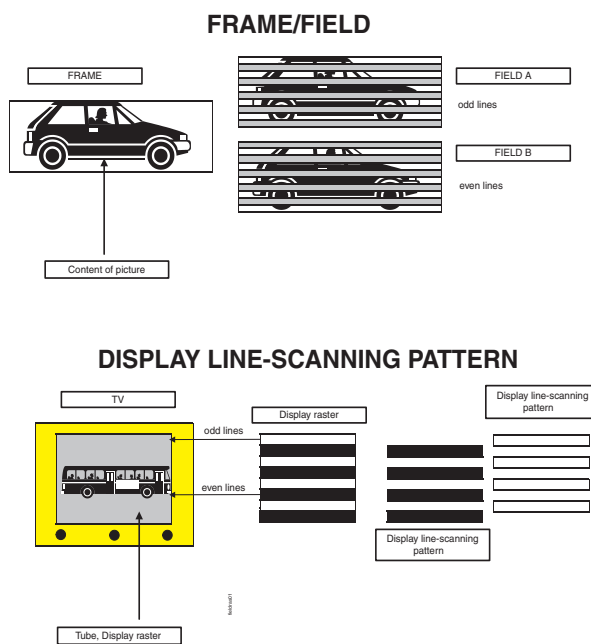
Fig. 2–31: Explanation of Field and Display Line-scanning Pattern

Table 2–10: Operation modes for scan-rate conversion

		Input Field A		Input Field B	
STOPMODE	**Scan-Rate Conversion**	**Output Field Phase 0**	**Output Field Phase 1**	**Output Field Phase 2/0**	**Output Field Phase 3/1**
00	AABB mode	A^n,α	A^n,α	B^n,β	B^n,β
01	AAAA mode	A^n,α	A^n,α	A^n,α	A^n,α
10	AAAA mode	A^n,α	A^n,β	A^n,α	A^n,β
11	BBBB mode	B^{n-1},β	B^{n-1},β	B^n,β	B^n,β
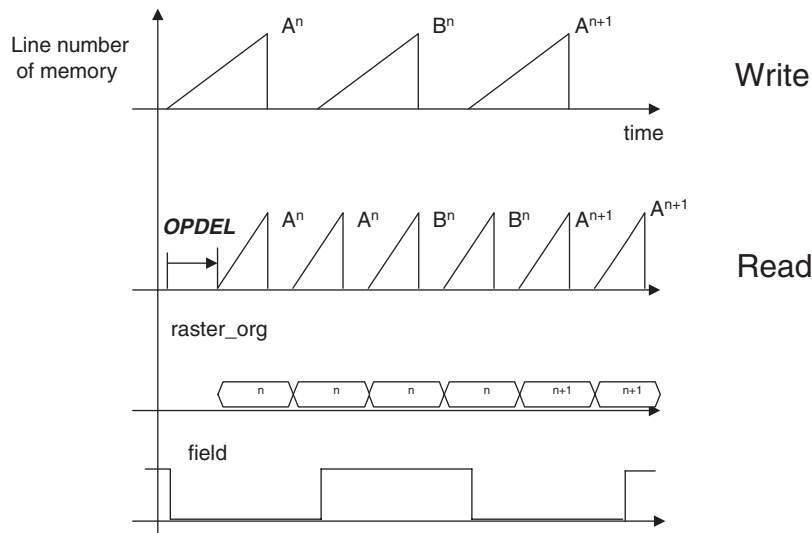
Fig. 2–32: 50/60 Hz Interlaced to 100/120 Hz Interlaced Conversion (AABB)

2.5. Display Processing

The display processing part contains an integrated triple 9-bit DAC and performs digital enhancements and manipulations of the digital video component signal. Fig. 2–35 shows the block diagram of the display processing part.

2.5.1. Peaking

The luminance peaking filter improves the overall frequency response of the luminance channel. It consists of two filters working in parallel. They have high pass (HP) and band pass (BP) characteristics. Their gain factors are programmable separately (**BCOF**, **HCOF**). Values greater than 4 peak the signal, whereas values less than 4 attenuate the signal. The high pass and the band pass filters are equipped with a common coring algorithm. It is optimized to achieve a smooth display of grey scales, not to improve the signal-to-noise ratio. Therefore no artifacts are produced. Coring can be switched off (**YCOR**). The Fig. 2–34 shows the block diagram of the peaking block.

The peaking filter clock frequency is CLKB36=36 MHz (27 MHz). The maximum signal frequency of the picture stored in the memory is 6.75 MHz. Due to a peaking after postscaler, the frequency range of the peaking filter varies with the expansion factor of the postscaler.
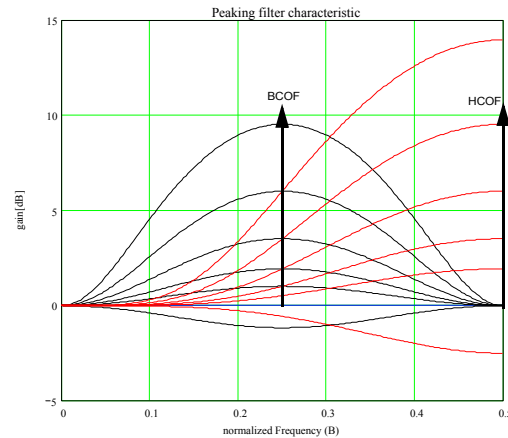
Fig. 2–33: Peaking Filter: Bandpass and Highpass filter
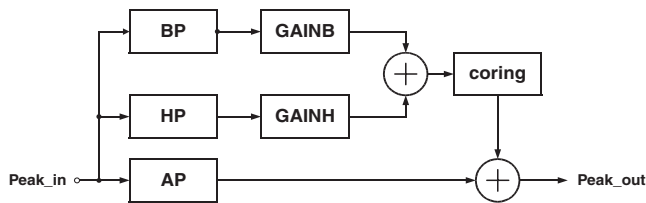
Fig. 2–34: Block Diagram Peaking
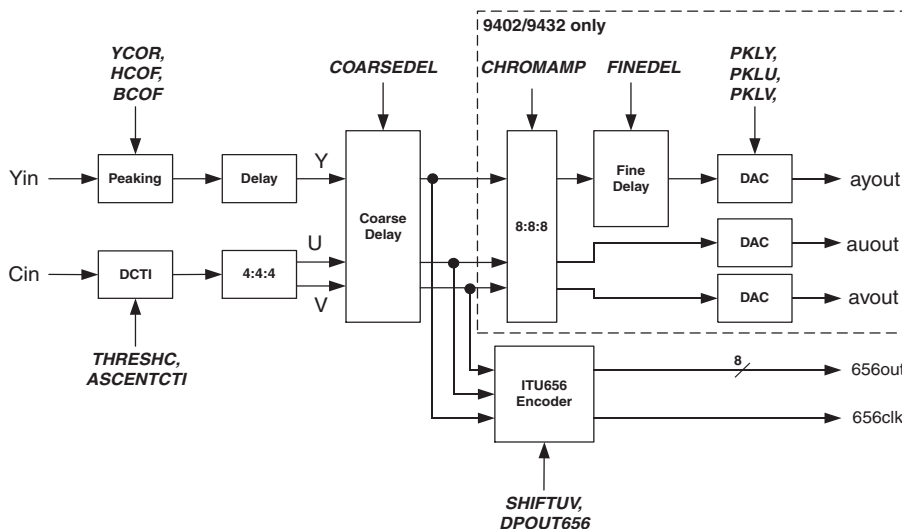
Fig. 2–35: Block Diagram of Display Processing

Table 2–11: Conversion table between HCOF/BCOF and GAINHP/GAINBP

BCOF	GAINBP	HCOF	GAINHP
0	−1	0	−1
1	−0.75	1	−0.75
2	−0.50	2	−0.50
3	−0.25	3	−0.25
4	0.00	4	0.00
5	0.25	5	0.25
6	0.50	6	0.50
7	0.75	7	0.75
8	1.00	8	1.00
9	1.25	9	1.25
10	1.50	10	1.50
11	1.75	11	1.75
12	2.00	12	2.00
13	2.50	13	2.50
14	3.00	14	3.00
15	4.00	15	4.00

2.5.2. Digital Color Transition Improvement (DCTI)

A digital algorithm is implemented to improve horizontal transitions of the chrominance signals resulting in a better picture sharpness. A correction signal proportional to the slope of the detected horizontal transition of the input signal is added to the original input signal. The amplitude of the correction signal is adjustable by the I^{2}C bus parameter **ASCENTCTI**.

The I²C bus parameter **THRESHC** modifies the sensitivity of the DCTI circuit. High values of **THRESHC** result in an improvement of significant color transitions only.

Table 2–12: Peaking filter adaption for 36 MHz or 27 MHz operation

Expansion Factor of Postscaler	Corresponding Frequency of Input Signal for Center Frequency Bandpass (B=0.25) CLKB36=36 MHz/27 MHZ	Corresponding Frequency of Input Signal for Center Frequency Highpass (B=0.5) CLKB36=36 MHz/27 MHZ
0.75	3.375 MHz / 2.5 MHz	6.75 MHz / 5.06 MHz
...	...	...
1	4.5 MHz / 3.375 MHz	9 MHz / 6.75 MHz
...	...	...
3	13.5 MHz / 10.125 MHz	27 MHz / 20.25 MHz

2.5.3. Coarse and Fine Delay

Before digital-to-analog conversion an adjustment of the phase of the luminance is performed. A coarse delay from −8 to +7 in steps of 1 pixel CLKB36 (~28 ns) is possible (**COARSEDEL**). **FINEDEL** shifts the luminance one CLKB72 (~14 ns) pixel. This can be used to compensate delays, if the external processing of Y and UV produces different delays (e.g. external lowpass filtering).

2.5.4. Oversampling and DAC

After conversion into 8:8:8 format (CLKB72=72 MHz), three 9-bit digital-to-analog converters are used for analog YUV output. This twofold-oversampling generates 1920 active pixels per line (when using recommended settings) and simplifies the external postfiltering. The output voltage is determined by **PKLY**, **PKLU** and **PKLV** and can be set in a range of 0.4 V ...1.9 V (fullscale).

8 bits of the luminance D/A converter are used for the entire signal. The 9th bit is used for over- and undershoots caused by the peaking to prevent or reduce clipping artifacts. As the CTI block seldomly produces such overshoots, a full-scale operation can be activated by **CHROMAMP**. The output voltages may be calculated by:

$$Voltage\,Y = \left(1.56\text{V} \cdot \frac{PKLY}{256} + 0.36\text{V}\right) \cdot signal\,Y$$

$$signal\,Y = \frac{160....400}{512}$$

[for unpeaked signals max.]

$$signal\,Y = \frac{0....511}{512}$$

[for peaked signals max.]

$$Voltage\,U,V = \left(1.56\text{V} \cdot \frac{PKLU,V}{256} + 0.36\text{V}\right) \cdot CHROMAMP \cdot signal\,UV$$

$$signal\,UV = \frac{128....384}{512}$$
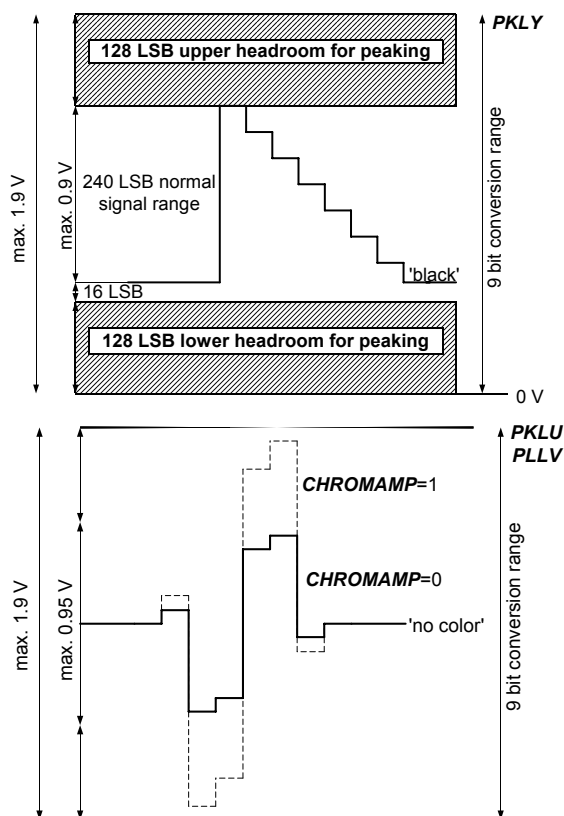
Fig. 2–36: DAC Output Signals

2.5.5. Output-Sync Controller

The output sync controller generates horizontal and vertical synchronization signals for the scanrate-converted output signal.

The number of pixels per line is 4***PPLOP**. The default value of 288 results in 1152 pixels/line. With CLKB= 36 MHz, the horizontal output frequency is 31.25 kHz, which is twice the PAL horizontal frequency. Out of these pixels, 16***APPLOP** are displayed as active picture area, which are 960 by default. The position on the screen depends on the **NAPPLOP**. It marks the picture area not active in horizontal direction and moves the active picture in horizontal direction. The number of lines per field is 2***LPFOP.** This value is only used in the vertical freeruning mode. In vertical locked mode, the number of lines per field is derived from the CVBS signal itself and not adjustable. The active and non-active picture areas are marked by **ALPFOP** and **NALPFOP**, respectively.

Both generators have a so called 'locked-mode' and 'freeruning-mode'. Not all combinations of these modes make sense. Table 2–13 on page 27 shows ingenious configurations.
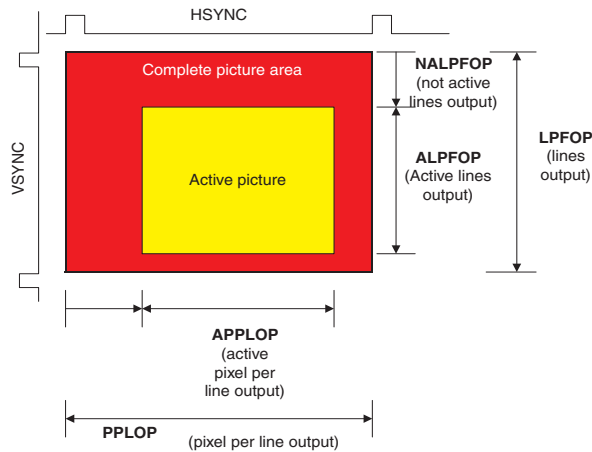
Fig. 2–37: Image Format behind Memory

For freerun mode the backend part works stand alone without analyzing the input signals. The clock domains, input data part and output data part of the IC, are not synchronized to each other. If the output processing works in the freerun mode, the output signals of the OSC are generated depending on I^{2}C-bus settings. For locked mode the backend part works with a line locked clock. This means that the front-end and the backend of the IC are synchronized to each other. The generation of the controlling signals depends on output signals from the front-end. This mode will be the default and the most used mode for standard TV applications.

With activated vertical freerun mode the phase of the generated vsync signal has no correlation to the incoming vsync signal. A hard switch from freerun mode to locked mode would therefore cause visible synchronization problems in the deflection unit of the TV set concerning the vertical picture positioning. To avoid these problems a circuit is implemented which synchronizes the freerunning vsync signal to the vsync

derived from the CVBS signal, to enable a soft transition to locked mode (**PDGSR**, **LPFOPFF**). This synchronization is only possible when the number of CVBS input lines corresponds to the programmed value of **LPFOP**.

When no or very weak signal is connected to the CVBS input, the IC can be configured to automatically switch into freerunning mode. This stabilizes the display which may contain OSD information, e.g. during channel-tune. The configuration, whether the IC switches to H-freerun, V-freerun or both can be configured by **AUTOFRRN**

2.5.5.1. HOUT Generator

The HOUT generator has two operation modes, which can be selected by the parameter **HOUTFR**. The HOUT signal is active high for 64 clock cycles (CLKB36). In the freerunning-mode the HOUT signal is generated depending on the **PPLOP** parameter. In the locked-mode the HOUT signal is locked on the incoming H-Sync signal derived from CVBS. The polarity of the HOUT signal is programmable by the parameter **HOUTPOL**.

2.5.5.2. VOUT Generator

The VOUT generator has two operation modes, which can be selected by the parameter **VOUTFR**. In the freerunning-mode (**VOUTFR**=1) the VOUT signal is generated depending on the **LPFOP** parameter.

In the locked-mode the VOUT signal is synchronized by the incoming V-Sync signal derived from CVBS, delayed by some lines (**OPDEL**). During one incoming V-Sync signal, two VOUT pulses have to be generated. The polarity of the VOUT signal is programmable by the parameter **VOUTPOL**. The VOUT signal is active high for two output lines..

Table 2–13: Ingenious configurations of the HOUT and VOUT generator

Mode	HOUTFR	VOUTFR
'H-and-V-locked' mode	0	0
'H-freerunning / V-locked' mode	1	0
'H-and V freerunning' mode	1	1

2.5.5.3. BLANK Generator

The BLANK signal is used to horizontally and vertically mark active picture area. It is enabled by **BLANEN** and its polarity can be chosen by **BLANPOL** and **VBLAN-POL**. Referred to hsync, the start is given by **BLAN-DEL** and its length is given by **BLANLEN**, both adjustable with 4 pixel resolution. Referred to vsync, the start is given by **VBLANDEL** and its length is given by **VBLANLEN**, both adjustable in 1 lines resolution.

2.5.5.4. Background Generator

This generator is able to realize an automatic closing and opening of the displayed picture. This means that with every picture the displayed colored background, defined by **UBORDER**, **VBORDER** and **YBORDER** will get bigger or smaller. The original picture data will

be replaced by the background values and vice versa. There is also the possibility to realize a fixed border via the I²C bus (**BORDPOSH** and **BORDPOSV**). 4096 different colors are available.

BORDPOSH and **BORDPOSV** also influence the window generation. This means the automatic opening and closing of the picture will start or end at the position which is defined with these values. The border is calculated with the following formula: The horizontal border on the left side of the TV screen is 2***BORDPOSH** and 2***BORDPOSH** on the right side of the TV screen. This means, that 4***BORDPOSH** pixels are overwritten with border values. The same applies to the vertical direction. 4***BORDPOSV** lines in total are overwritten with background values. **BORDERV** decides whether upper or lower or both borders are displayed. **BORDERH** decides whether left or right or both borders are displayed.

Table 2–14: Display line scanning pattern sequence

Display Line Scanning Pattern Sequence	1. to 2.	2. to 3.	3. to 4.	4. to 5.(1.)
a a a a	312	313	312	313
b b b b	313	312	313	312
a a b b	312	312.5	313	312.5
a b a b	312.5	312.5	312.5	312.5

2.5.5.5. Window Function

Fig. 2–38 shows the functionality of the horizontal window function. The window can be closed or opened.

The windowing feature can be enabled by the *WINDHON* parameter. The *WINDHST* and the *WINDHDR* parameter determine, what status (opened or closed) the window has, and what can be done with the window (open or close). With each enabling of the window function by the *WINDHON* parameter, the status of the window will be as defined by *WINDHST* and *WINDHDR*. To change from „close" to „open" or vice versa only the *WINDHDR* parameter has to be toggled. The speed of the window can be defined by the *WINDHSP* parameter. Fig. 2–39 shows the functionality of the vertical window function.

All settings are also available in vertical direction. All I^2C parameters exist for both directions (e.g. *WINDHON* and *WINDVON* for horizontal and vertical window enabling). Combinations of both window functions (horizontal and vertical) are also possible.
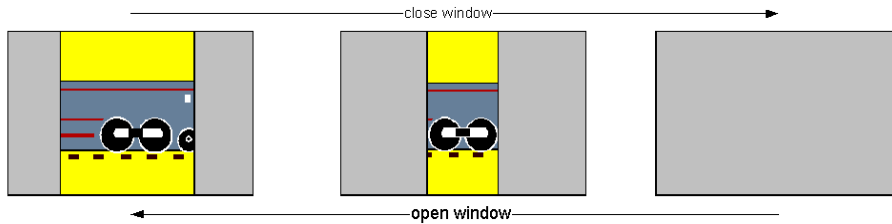
Fig. 2–38: Horizontal Windowing
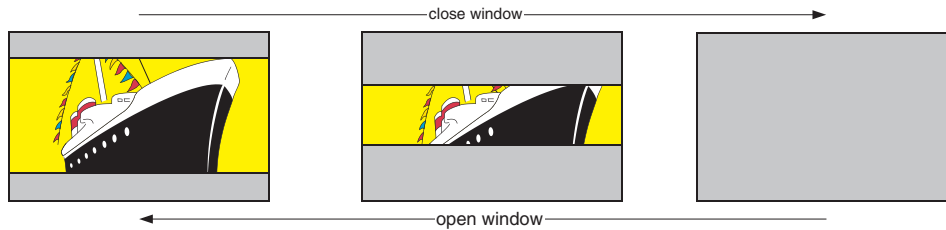
Fig. 2–39: Vertical Windowing
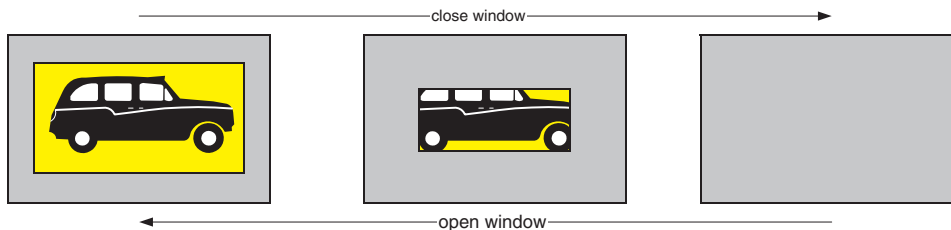
Fig. 2–40: Horizontal and Vertical Windowing

2.5.6. Digital 656 Input

The IC decodes a digital 8 bit@27 MHz data stream according to ITU.BT656 standard. The configuration is set by **EN_656**. and **DPOUT656**.

Table 2–15: 656 input / output selection

EN_656	DPOUT656	656 Operation
0	0	Input disabled/ output disabled
0	1	Input disabled/ output enabled
1	0	Input enabled/ output disabled
1	1	Input enabled/ output disabled (9412A only)

Four input modes are supported:

Table 2–16: 656 modes

IMODE	656 Operation
00	Full ITU mode (automatic) Information about active picture is taken from data-stream
01	Full ITU mode (manual) Information about active picture is taken from **APPLIPI**, **NAPPLIPI**, **ALPFIPI**, **NALPFIPI**
10	ITU656 only data, H/V-sync according PAL/NTSC
11	ITU656 only data, H/V-sync according ITU656

To adjust the input to sources, which deviate from the standard, the field information may be inverted (**F_POL**) and the chrominance format can be chosen between unsigned and 2's complement format (**CFORMAT**). The polarity of H an V can be inverted by **H_POL** and **V_POL** respectively. Dependent on version, the digital input must be selected by **ITUPRTSEL** (pins i656i or 656io).

2.5.7. Digital 656 Output

Dependent on version (single- or double-scan), the output data format corresponds to CCIR 656 (8-bit bus at a data rate of 27 MHz) or has double-scan format (8-bit bus at a data rate of 54 MHz). There all frequencies and data-rates are doubled compared to standard CCIR656 specification. Double scan format is intended to be used with a suited backend device, e.g. DDP3315C. Timing reference codes (SAV, EAV) are inserted according to the specification. The output can be enabled by **DPOUT656**. The output should be set to 720 pixels per line (**APPLOP**) and the display clock should be set to 27/54 MHz (refer to **Chapter 2.6.**). The chrominance information can be inverted by **CHRMSIG656**. HOUT and VOUT pins may be used in parallel.

2.6. Clock Concept

A single 20.25 MHz crystal at fundamental mode is used as clock reference. All other clocks are derived from this source. The CVBS front-end works with 20.25 MHz, the RGB front-end works with 40.5 MHz, the oversampling DACs use CLKB72 and the memory and all parts behind the memory are clocked with CLKB36. The frequency of CLKB36 and CLKB72 is adjustable and depends on application. With analog output, CLKB72 is usually 72 MHz and with digital output, CLKB72 is usually 54 MHz. CLKB72 is always twice of CLKB36.

Three different clock concepts are supported. The difference is the behavior in clocking the memory output. The front-end part of the VSP 94x2A uses a freeruning but crystal-stable clock (CLKF). After deskewing, an orthogonal picture is written into the memory. The read out is done using the (CLKB) clock.

The horizontal sync-signal output (HOUT) is derived from a counter running with CLKB. The VOUT is directly derived from the input vertical signal, which is generated by the sync-separation block. This '*H-freerunning-V-locked mode*' is only possible together with a DC coupled deflection controller.

In '*H-and-V-locked mode*' CLKB is line-locked to the incoming signal. The freerunning YUV picture data and the internal H signal are converted to the line-locked domain. Now HOUT and the sync signal in the $1f_H$ domain are directly coupled.

In case of '*H-and-V-freerunning mode*' the HOUT and VOUT signals are derived from counters running with CLKB. There is no connection to the incoming signal. This mode can be used for stable pictures when no signal is applied (e.g. channel search with OSD insertion).

The selection between freerunning and locked clocks may be forced or selected to be dependent on PLL conditions. Please refer to Fig. 2–41

A clock output of 27 MHz (single-scan version:13.5 MHz) is possible (pin 27:*clkout*). This clock is 3/4 of CLKB36. HOUT and VOUT are in line with this sampling clock. The clock output can be disabled by **CLKOUTON**. Additionally a 20.25 MHz clock can be output to pin 74 (*656hin/clkf20*) to supply other ICs (e.g. PiP) with the same clock (**CLKF2PAD**). When enabled, 656-input with separate H/V-sync is not possible. For 656-output operation, CLKB36 is given to pin 9 (*656clk*).

Table 2–17: Clock system

Name	Clock	Nominal Frequency	'H-/V-locked' Mode	'H-freerunning-V-locked' Mode	'H-/V-freerunning' Mode
CLKF20	CVBS front-end	20.25 MHz	FR	FR	FR
CLKF40	RGB front-end, input processing	40.5 MHz	FR	FR	FR
CLKB36	Output and display processing	9402: 36 MHz (analog out) 9412: 27 MHz (digital out)	LL	FR	FR
CLKB72	Oversampling, DAC	9402: 72 MHz 9412: 54 MHz	LL	FR	FR
CLKB27	CLKOUT-pin	9402: 27 MHz 9412: 20.25 MHz	LL	FR	FR
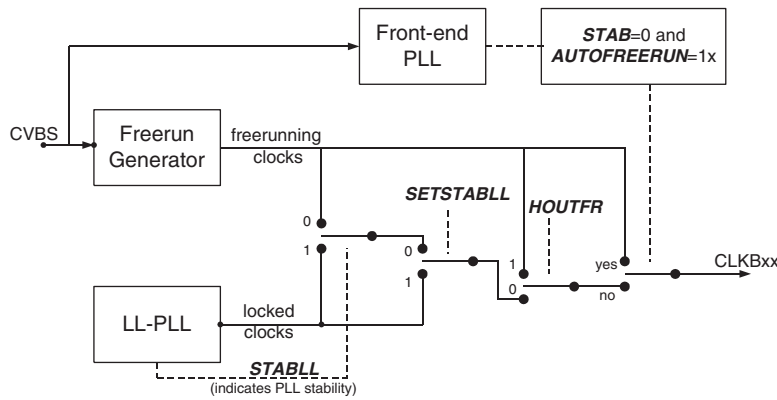
Fig. 2–41: Conditions for Freerunning/Locked Switching

2.6.1. Line-locked Clock Generator

The clock generation system derives all clocks from one 20.25 MHz crystal oscillator clock source. An internal PLL multiplies this oscillator frequency by 32, generating a clock of 648 MHz which is used as reference for all clocks needed.

Line-locked horizontal sync pulses are generated by a digital phase locked loop. The time constant can be adjusted between fast and slow behavior (**KPL, KIL**) to accommodate different backend ICs. The PLL control can be frozen up to 15 lines before V-sync (**FION**) for a duration up to 15 lines (**FILE**). This may be used to reduce disturbances by h-phase errors which are produced by VCR's. The output frequency for the 100/120 Hz version dependent on **IICINCR** is

$$f_{displayll} = IICINCR \cdot 103Hz$$

A freerunning frequency is also generated which may be selected alternatively. The freerunning frequency for the 100/120 Hz version dependent on **FRINC** is

$$f_{displayfr} = FRINC \cdot 103Hz$$

Normally, **IICINCR** and **FRINC** are equal or nearly the same. The value is internally divided by two for the 50/60 Hz versions.

The number of pixels generated by the PLL is given by **PPLIP**. For line-locked clock generation the following equation must be fulfilled:

$$PPLIP = 2 \cdot PPLOP$$
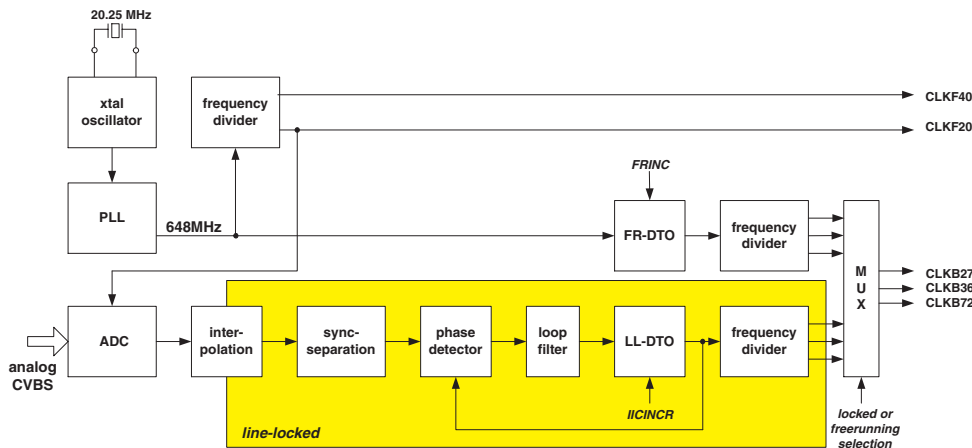
Fig. 2–42: Line-locked Clock Ceneration
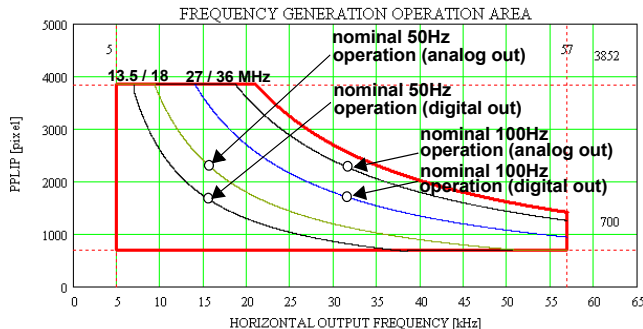
Fig. 2–43: Allowed Operation Area for Clock Generation

The PLL settings for different operation modes can be seen in Table 2–18.

Dependent on input signal (50 Hz or 60 Hz), the line-locked clock is changing slightly (e.g. from 27 MHz to 27.18 MHz). To have no artifacts when switching between locked and freerun operation, it is possible to change the *FRINC* parameter, after the input TV standard has been detected safely. In case the IC is operating in horizontal locked OR freerunning mode only, this adaptivity is not required.

Table 2–18: Recommended LL-PLL settings for normal TV-application

Operation	Input	PPLIP*4	PPLOP*4	IICINCR	FRINCR	CLKB36 [MHz]	f_H[kHz]
100/120 Hz (analog out)	50 Hz	2304	1152	349525	349525	36	31.250
	60 Hz				351953	36.25	31.468
100/120 Hz (digital out)	50 Hz	1728	864	262144	262144	27	31.250
	60 Hz				263892	27.18	31.468
50/60 Hz (analog out)	50 Hz	2304	1152	349525	349525	18	15.625
	60 Hz				351953	18.125	15.734
50/60 Hz (digital out)	50 Hz	1728	864	262144	262144	13.5	15.625
	60 Hz				263892	13.59	15.734

3. I^{2}C Bus Interface

3.1. I^{2}C Bus Slave Address

When pin 19 (adr/tdi) is connected to Vss, the VSP 94x2A reacts on the first I^{2}C address (B0h for write access and B1h for read access). The second address (B2h and B3h) is active, when pin 19 is connected to Vdd.

Table 3–1: I^{2}C bus slave addresses B0h and B1h

Write Address1: B0h								Read Address1: B1h							
1	0	1	1	0	0	0	0	1	0	1	1	0	0	0	1

Table 3–2: I^{2}C bus slave addresses B2h and B3h

Write Address2: B2h								Read Address2: B3h							
1	0	1	1	0	0	1	0	1	0	1	1	0	0	1	1

3.1.1. I^{2}C Bus Format

The VSP 94x2A I^{2}C bus interface acts as a slave receiver and a slave transmitter and provides two different access modes (write, read). All modes run with a subaddress auto increment. The interface supports the normal 100 kHz transmission speed as well as the high speed 400 kHz transmission.

The transmitted data is internally stored in registers. The registers are located in four different clock domains. The Table 3–5 on page 35 shows the four different clock domains of the VSP 94x2A. The clock domains are called CP - CVBS processing block (20.25 MHz domain, clkf20), FP - Front end processing block (40.5 MHz domain, clkf40), BP - Back end processing block (36.0 MHz domain, clkb36) and PP - PLL processing block (36.0 MHz domain, clkf36).

The registers themselves are grouped in an I^{2}C bus interface block, one in each domain. The transmitted data is received by the I^{2}C bus kernel. The I^{2}C bus kernel itself is located in the CP domain. This means that the working frequency is 20.25 MHz. The data is transmitted to the I^{2}C bus interface blocks via an internal serial bus.

For the write process, the I2C bus master has to write a 'don't care' byte to the subaddress FFh (store command). This makes the register values available to the four I2C bus interface blocks (except for the not-take-over registers, which are used immediately).

In order to have a defined time step for the several blocks in the different domains, the data are made valid with internal V-syncs, depending on the different clock domains.

The subaddresses, where the data are made valid with the V-sync signal of the 20.25 MHz domain are indicated in the overview of the subaddresses with "V20". The others are called "V40", "V36F" and "V36B" accordingly.

Table 3–3: Write

S	1	0	1	1	0	0	x	0	A	Subaddress	A	Data Byte	A	*****	A	P

S: Start condition
SR: Repeated Start condition
A: Acknowledge
P: Stop condition
NA: Not Acknowledge

Table 3–4: Read

S	1	0	1	1	0	0	x	0	A	Subaddress	A	SR	1	0	1	1	0	0	x	1	A	Data Byte	A	Data Byte	NA	P

Table 3–5: I²C bus clock domains

Domain		Description	Clock
CP	CP-CD	CVBS frontend	CLKF20
	CP-PP	LL-PLL	CLKF20
	CP-I2C	I²C read	CLKF20
FP	FP-PRE	Prescaler	CLKF40
	FP-MC	Memory-controller	CLKF40
	FP-RGB	RGB Frontend	CLKF40
	FP-TNR	Temporal noise reduction	CLKF40
	FP-I2C	I²C read	CLKF40
PP	PP	LL-PLL	CLKF36
	PP-I2C	I²C read	CLKF36
BP	BP-DP	Display processing	CLKB36
	BP-PM	Pixel-Mixer	CLKB36
	BP-ODC	Output data control	CLKB36
	BP-ODC/MC	Output data control/ memory-controller	CLKB36
	BP-POS	Postscaler	CLKB36
	BP-DAC	DAC processing	CLKB72
	BP-I2C	I²C read	CLKB36

The I2C parameter V20STAT, V40STAT and V36BSTAT reflect the state of the register values.

If these bits are read as '1', then the store command was sent, but the data is not made available yet.

If these bits are '0' then the data was made valid and a new write or read cycle can start.

The bits **V20STAT**, **V40STAT** and **V36BSTAT** may be checked before writing or reading new data, otherwise data can be lost by overwriting. No *V36FSTAT* register exist. To make the register values available to the four I²C bus interface immediately after sending, the I²C bus master has to write a 'don't care' byte to the sub-address **FEh** (store command).

For the read process, the I²C bus master must not send a store command. In order to have a defined time step for the I²C bus interface blocks in the different domains, where the data will be available from the dif-

ferent blocks, the data is made valid with the same V-Sync related signals mentioned above for the write process.

The VSP 94x2A distinguishes between two different types of read-registers. The behavior of the "normal" read registers does not differ from the behavior of the write registers. Only the direction of the data flow is opposite.

The "rs typ" read registers behave differently. They can be only set (means value 1) by the internal blocks using the rising edge of a corresponding signal. After reading by the I²C bus master, the registers will be automatically reset (means value 0) by the I²C bus kernel/interface. For example the register **NMSTATUS** belongs to the "rs typ" read registers. **NMSTATUS** signalizes a new value for **NOISEME**. So if **NMSTATUS** is read as '0' the current noise measurement has not been updated. If the **NMSTATUS** is read as '1' a new noise measurement value can be read. All other "rs typ" read registers work in the same way. The "rs typ" read registers will be marked in the overview with the short cut "rstyp" or will have the additional hint "Note: reset automatically when read/write" in the detailed I²C bus command description.

By default all registers are made valid by the internal V-Sync related signals and, in addition, a store command has to be sent for write registers. The registers, which should also be made available immediately as for writing and reading, are marked with the short cut NTO (No take over mechanism).

Registers which need a hand-shake mechanism between the I²C bus interface and the different blocks are marked with the shortcut HS (Hand shake mechanism). This means that all bits of the registers are used when the last register is written. After PPLIP9-2 is written, PPLIP1-0 must be written to allow these bits to have effect.

The registers for the write parameter **STOPMODE** are directly connected to the read registers of the parameter **SMMIRROR**. So it is possible to check the I²C bus protocol by writing and reading to the register **STOPMODE** and **SMMIRROR**, respectively.

The transmitted data is internally stored in registers. Writing to or reading from a non-existant register is permitted and does not generate a fault by the IC.

After switching on the IC, all bits of the VSP 94x2A are set to defined states, (refer to Table 3–6). **POR** is set after reset to pin 24. It stays '1', until it is cancled via software **PORCNCL**. This can be used to decide during TV operation, whether to program all registers (e.g. after power failure reset) or only altered ones (normal TV operation).
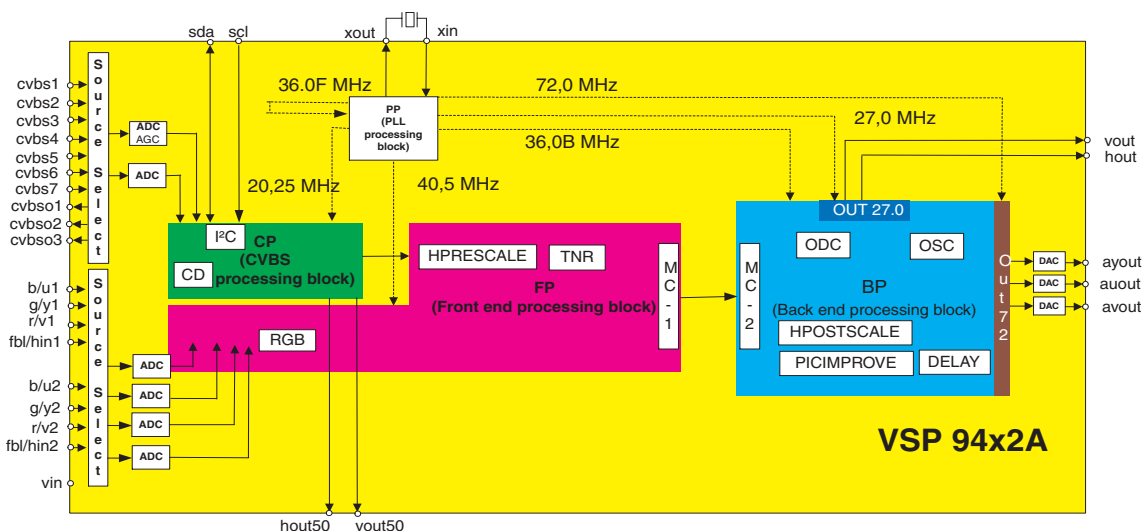
Fig. 3–1: I²C Bus Clock Domains

Table 3–6: I²C bus characterization

Subaddress	Default	R/W	Take-over	Subaddress	Default	R/W	Take-over
00h	AAh	W	V40	1Dh	44h	W	V40
01h	CAh	W	V40	1Eh	00h	W	V40
02h	B0h	W	V40	1Fh	FFh	W	V40
03h	C8h	W	V40	20h	1Fh	W	V40
04h	16h	W	V40	21h	F4h	W	V40
05h	10h	W	V40	22h	44h	W	V40
06h	20h	W	V40	23h	00h	W	V40
07h	01h	W	V40	24h	FFh	W	V40
08h	F0h	W	V40	25h	AAh	W	NTO
09h	3Eh	W	V40	26h	AAh	W	NTO
0Ah	00h	W	V40	27h	05h	W	NTO/HS
0Bh	A0h	W	V40	28h	00h	W	NTO/rstyp
0Ch	00h	W	V40	29h	60h	W	NTO
0Dh	90h	W	V40	2Ah	60h	W	NTO
0Eh	80h	W	V40	2Bh	90h	W	NTO
0Fh	00h	W	V40	2Ch	00h	W	NTO/HS
10h	20h	W	V40	2Dh	04h	W	NTO

VSP 94x2A

Table 3–6: I^{2}C bus characterization, continued

Subaddress	Default	R/W	Take-over	Subaddress	Default	R/W	Take-over
11h	20h	W	V40	2Eh	00h	W	NTO
12h	00h	W	V40	2Fh	00h	W	V36B
13h	00h	W	V40	30h	2Dh	W	V36B
14h	00h	W	V40	31h	44h	W	V36B
15h	00h	W	V40	32h	94h	W	V36B
16h	00h	W	V40	33h	20h	W	V36B
17h	00h	W	V40	34h	00h	W	V36B
18h	16h	W	V40	35h	00h	W	V36B
19h	00h	W	V40	36h	01h	W	V36B
1Ah	03h	W	V40	37h	00h	W	V36B
1Bh	1Fh	W	V40	38h	E0h	W	V36B
1Ch	F4h	W	V40	39h	01h	W	V36B
3Ah	00h	W	V36B	58h	80h	W	V36B
3Bh	00h	W	V36B	59h	80h	W	V36B
3Ch	26h	W	V36B	5Ah	80h	W	V36B
3Dh	3Ch	W	V36B	5Bh	44h	W	V20
3Eh	01h	W	V36B	5Ch	40h	W	V20
3Fh	00h	W	V36B	5Dh	C0h	W	V20
40h	04h	W	V36B	5Eh	5Ch	W	V20
41h	40h	W	V36B	5Fh	66h	W	V20
42h	20h	W	V36B	60h	40h	W	V20
43h	9Ch	W	V36B	61h	40h	W	V20
44h	AAh	W	V36B	62h	00h	W	V20
45h	00h	W	V36B	63h	00h	W	V20
46h	18h	W	V36B	64h	A5h	W	V20
47h	0Bh	W	V20	65h	5Fh	W	V20
48h	00h	W	V36B	66h	0Fh	W	V20
49h	00h	W	V36B	67h	00h	W	V20
4Ah	00h	W	V36B	68h	00h	W	V20
4Bh	00h	W	V36B	69h	3Ch	W	V20
4Ch	00h	W	V36B	6Ah	03h	W	V20

Table 3–6: I^{2}C bus characterization, continued

Subaddress	Default	R/W	Take-over	Subaddress	Default	R/W	Take-over
4Dh	00h	W	V36B	6Bh	07h	W	V20
4Eh	55h	W	V36B	6Ch	07h	W	V20
4Fh	0Bh	W	V36B	6Dh	1Ch	W	V20
50h	00h	W	V36B	6Eh	5Ch	W	V20
51h	00h	W	V36B	6Fh	00h	W	V20
52h	00h	W	V36B	70h	00h	W	V20
53h	00h	W	V36B	71h	E4h	W	V20
54h	00h	W	V36B	72h	00h	W	V20
55h	00h	W	V36B	73h	00h	W	V20
56h	3Fh	W	V36B	74h	00h	W	V20
57h	3Fh	W	V36B	75h	7Fh	W	V20
76h	00h	W	V20	B2h	40h	W	V20
77h	00h	W	V20	B3h	00h	W	V20
78h	1Ch	W	V20	B4h	FFh	W	V20
79h	1Ch	W	V20	B5h (no autoincrement)	43h	W	V20
7Ah	FCh	W	V20	B6h	(spare)		
7Bh	77h	W	V20	B7h	00h	W	V40
7Ch	02h	W	V20	B8h	00h	W	V40
7Dh	6Ch	W	V20	B9h	00h	W	V40
7Eh	00h	W	V20	BAh	00h	W	V40
7Fh	15h	W	V20	BBh	(spare)		
80h	00h	W	V20	BCh	AAh	W	NTO
81h	00h	W	V20	BDh	AAh	W	NTO
82h (no autoincrement)	00h	W	V20	BEh	05h	W	NTO
83h		R	NTO	BFh	(spare)		
84h (no autoincrement)		R	NTO	C0h	00h	W	V40
85h		R	no/rstyp	C1h	00h	W	V40
86-93h		R	NTO	D0h	00h	W	V36
94h-95h	(spare)			D1h	00h	W	V36
96h		R	V40	D2h	00h	W	V36
97h	(spare)			E0h	00h	W	V40

Table 3–6: I^{2}C bus characterization, continued

Subaddress	Default	R/W	Take-over	Subaddress	Default	R/W	Take-over
98h		R	V36B	E1h	00h	W	V40
99h		R	V20	E2h	00h	W	V40
A0h	00h	W	NTO	E3h	00h	W	V40
A1h	00h	W	NTO	E4h	00h	W	V40
A2h	FFh	W	NTO	E5h	00h	W	V40
A3h	FFh	W	NTO	E6h	00h	W	V40
A4h	00h	W	NTO	E7h	00h	W	V40
B0h	10h	W	V20	E8h	00h	W	V40
B1h	00h	W	V20	E9h	00h	W	V40
EAh	00h	W	V40				
EBh	00h	W	V40				
ECh	00h	W	V40				
EDh	00h	W	V40				
EEh	00h	W	V40				
EFh	00h	W	V40				
F0-F6h		R	NTO				
F7h-FDh	(spare)						
FEh		W					
FFh		W					
Take-over mechanism					Register types		
NTO	No take-over mechanism				W	Write register	
V20	Take-over with V-sync in 20 MHz domain				R	Read register	
V40	Take-over with V-sync in 40 MHz domain				Rrstyp	Reset register after reading	
V36B	Take-over with V-sync in back-end 36.0 MHz domain						
HS	Handshake mechanism required						

3.1.2. I²C Bus List in Alphabetical Order

Name	Subaddress
AABYP	0Ch
ACCFIX	5Bh
ACCFRZ	5Bh
ACCLIM	7Ah
ADCSEL	0Ch
ADLCK	81h
ADLCKCC	81h
ADLCKSEL	81h
AFPROC	4Dh
AGCADJ1	67h
AGCADJ2	68h
AGCADJB	16h
AGCADJCV	90h
AGCADJF	17h
AGCADJG	15h
AGCADJR	14h
AGCFRZE	68h
AGCMD	67h
AGCRES	68h
AGCTHD	B0h
ALPFIP	05h
ALPFIPI	B8h
ALPFOP	32h
AM50O	90h
AM60O	90h
AMSTD50	B1h
AMSTD60	B1h
APENSEL	05h
APPLIP	01h
APPLIPI	B9h
APPLOP	3Dh
ASCENTCTI	30h
AUTOFRRN	32h

Name	Subaddress
BCOF	31h
BELLFIR	7Dh
BELLIIR	7Dh
BGPOS	47h
BLANDEL	07h
BLANEN	36h
BLANLEN	08h
BLANPOL	36h
BORDERH	45h
BORDERV	45h
BORDPOSH	35h
BORDPOSV	34h
BRTADJ	0Ah
CDELHPOS	4Fh
CFORMAT	18h
CHRF	5Eh
CHRMSIG656	55h
CHROMAMP	57h
CHROMSIGN	57h
CHRSF	0Bh
CHRSHFT	3Dh
CKILL	60h
CKILLS	61h
CKSTAT	88h
CLKF2PAD	16h
CLKOUTINV	4Fh
CLKOUTON	30h
CLKOUTSEL	4Fh
CLKOUTSEL72	4Dh
CLKT	2Eh
CLMPD1	6Bh
CLMPD1S	7Bh
CLMPD2	6Ch
CLMPD2S	7Bh

Name	Subaddress
CLMPHIGH	69h
CLMPLOW	6Ah
CLMPST1	6Dh
CLMPST1S	78h
CLMPST2	6Eh
CLMPST2S	79h
CLMPVG	10h
CLMPVRB	0Dh
CLPSTGY	6Bh
CLRANGE	5Dh
COARSEDEL	32h
COLON	5Bh
COMB	5Fh
CON	5Ch
CONADJ	0Bh
CONS	5Bh
CPLLOF	82h
CPLLRES	80h
CRCB	5Bh
CSTAND	5Fh
CVBOSEL1	6Ah
CVBOSEL2	70h
CVBOSEL3	70h
CVBSEL1	6Fh
CVBSEL2	6Fh
DCLMPF	10h
DECTWO	0Bh
DEEMPFIR	B5h
DEEMPIIR	B5h
DEEMPSTD	82h
DETHPOL	88h
DETVPOL	88h
DISALLRES	80h
DISCHCH	6Ch

Name	Subaddress
DISRES	27h
DPOUT656	56h
EIA770	7Ch
EN_656	18h
ENLIM	7Eh
F_POL	18h
FBLACTIVE	83h
FBLCONF	0Dh
FBLDEL	0Dh
FBLOFFST	0Ch
FEMAG	B1h
FHDET	6Ch
FHFRRN	71h
FIELDBINV	54h
FILE	2Eh
FINEDEL	32h
FIOFFOFF	54h
FION	2Dh
FKOI	2Ch
FKOIHYS	2Ch
FLDINV	6Bh
FLINE	6Bh
FLNSTRD	7Eh
FMOD	29h
FOFFST	C1h
FREEZE	3Fh
FREQSEL	7Ch
FRFIX	1Ah
FRINC	BCh
FSWFTL	D0h
GOFST	0Eh
GRADELAA	F3h
GRADISSTABLE	F2h
H_POL	18h

Name	Subaddress
HAAPRESC	09h
HCOF	31h
HDCPRESC	05h
HDTOTEST	2Eh
HINC0	48h
HINC1	49h
HINC2	4Ah
HINC3	4Bh
HINC4	4Ch
HINCREXT	29h
HINP	6Dh
HORPOS	3Ah
HORWIDTH	38h
HOUTDEL	3Eh
HOUTFR	41h
HOUTPOL	41h
HPANON	4Fh
HPOL	6Ch
HRES	28h
HSCPOSC	4Eh
HSCPRESC	01h
HSEG1	50h
HSEG2	51h
HSEG3	52h
HSEG4	53h
HSPPL	C0h
HSWIN	29h
HTESTW	2Ah
HUE	63h
HWID	2Eh
IFCOMP	7Ah
IFCOMSTR	82h
IICINCR	25h
IMODE	18h

Name	Subaddress
INT	89h
ISHFT	7Eh
ITUPRTSEL	16h
KD2	29h
KIL	A1h
KINL	A1h
KOIH	2Ah
KOIWID	2Ah
KPL	A0h
KPNL	A0h
LB43SENS	E9h
LBACTIVITY	ECh
LBASDEL	EFh
LBELAA	F0h
LBFORMAT	F2h
LBFS	E6h
LBGFBDEL	EDh
LBGRADDET	E0h
LBGRADRST	EAh
LBGSDEL	EEh
LBHISTBLA	E4h
LBHIWHITE	E3h
LBHSDEL	EAh
LBHWEND	E2h
LBHWST	E7h
LBNGFEN	E9h
LBSLAA	F0h
LBSTABILITY	E9h
LBSTATUS	85h
LBSUB	EAh
LBSUBTITLE	F2h
LBTHDNBNG	E9h
LBTHDNBNHA	EBh
LBTOPTITLE	F2h

Name	Subaddress
LBVWENDLO	E1h
LBVWENDUP	E6h
LBVWSTLO	E5h
LBVWSTUP	E8h
LIMEN	2Ch
LIMII	A3h
LIMIP	A2h
LIMLR	A4h
LMOD	29h
LMOFST	5Dh
LNL	2Dh
LNSTDRD	89h
LOCKSP	47h
LPBLACK	F5h
LPCDEL	72h
LPFIPMD	2Fh
LPFLD	8Ah
LPFOP	43h
LPFOPFF	3Ch
LPPOST	62h
LPWHITE	F5h
MINV	92h
MIXGAIN	0Fh
MIXOP	0Dh
MLL	09h
MVP	B2h
MVPG	B2h
NALPFIP	04h
NALPFIPI	BAh
NALPFOP	45h
NAPIPPHI	17h
NAPPLIP	02h
NAPPLIPI	B7h
NAPPLOP	3Fh

Name	Subaddress
NMLINE	19h
NMPOS	1Ah
NMSENSE	1Ah
NMSTATUS	85h
NOGRADFOUND	F2h
NOISEME	84h
NOSIGB	6Dh
NOSYNC	3Ch
NOTCHOFF	5Ch
NRON	1Ah
NRPIXEL	8Bh
NSRED	72h/7Eh
NTCHSEL	80h
NTSCREF	64h
OPDEL	44h
OSCPD	7Ch
PALDEL	47h
PALDET	8Ch
PALID	88h
PALIDL0	75h
PALIDL1	74h
PALIDL2	82h
PALINC1	82h
PALINC2	82h
PALREF	65h
PB	85h
PDGSR	3Fh
PFBL	85h
PG	85h
PKLU	59h
PKLV	5Ah
PKLY	58h
PLLTC	6Eh
POR	8Ch

Name	Subaddress
PORCNCL	80h
PPLIP	2Bh
PPLOFF	3Ch
PPLOP	41h
PR	85h
PWADJCNT	93h
PWTHD	5Dh
RBOFST	0Eh
RDCTRLDIS	45h
REFRON	41h
REFRPER	41h
REFTRIM	76h
REFTRIMCV	77h
REFTRIMCVRD	8Eh
REFTRIMEN	72h
REFTRIMRD	8Dh
REFTRIMRGB	77h
REFTRIMRGBRD	8Eh
REV	F6h
RGBSEL	0Fh
SATNR	72h
SCADJ	66h
SCDEV	89h
SCMIDL	79h
SCMREL	7Fh
SCOUTEN	88h
SDB	B2h
SDR	5Eh
SECACC	7Fh
SECACCL	81h
SECDIV	7Fh
SECINC1	7Fh
SECINC2	7Fh
SECNTCH	5Ch

Name	Subaddress
SETSTABLL	2Ch
SHAPERDIS	7Ch
SHIFTUV	56h
SKEWSEL	0Eh
SLLTHD	66h
SLLTHDV	B1h
SLLTHDVP	78h
SLS	8Fh/F6h
SMMIRROR	87h
SMOP	0Eh
STAB	8Ch
STABLL	86h
STANDBY	11h
STDET	88h
STOPMODE	3Fh
SUBTITLE	F2h
SWITCHTO43	F2h
SYNFTHD	82h
THRESHC	30h
THRSEL	78h
TNRABS	1Ah
TNRCLC	24h
TNRCLY	24h
TNRS0C	20h
TNRS0Y	1Bh
TNRS1C	20h
TNRS1Y	1Bh
TNRS2C	21h
TNRS2Y	1Ch
TNRS3C	21h
TNRS3Y	1Ch
TNRS4C	22h
TNRS4Y	1Dh
TNRS5C	22h

VSP 94x2A

Name	Subaddress
TNRS5Y	1Dh
TNRS6C	23h
TNRS6Y	1Eh
TNRS7C	23h
TNRS7Y	1Eh
TNRSEL	1Ah
TNRSSC	1Fh
TNRSSY	1Fh
TOPTITLE	F2h
TRAPBLU	80h
TRAPRED	80h
TSTSHAPERI	7Ch
UBORDER	37h
UPBLACK	F5h
UPWHITE	F5h
USATADJ	10h
UVCOR	5Ch
UVDEL	13h
V_POL	18h
V20STAT	99h
V36BSTAT	98h
V40STAT	96h
V656DEL	4Dh
VBLANDEL	D0h
VBLANLEN	D0h
VBLANPOL	D0h
VBORDER	37h
VDEL_EN	55h
VDELF_EN	03h
VDETIFS	5Dh
VDETITC	B2h
VERSION	8Fh/F6h
VFLYMD	8Ch
VFLYWHL	7Dh

Name	Subaddress
VFLYWHLMD	81h
VINMTHD	2Fh
VINP	72h
VLENGTH	91h
VLP	7Eh
VOUTFR	41h
VOUTPOL	41h
VPOL	62h
VSATADJ	11h
VSHIFT	73h
VSIGNAL	18h
VSLPF	C1h
VTHRH50	75h
VTHRH60	B4h
VTHRL50	74h
VTHRL60	B3h
WINDHDR	3Bh
WINDHON	3Bh
WINDHSP	3Bh
WINDHST	3Bh
WINDVDR	39h
WINDVON	39h
WINDVSP	39h
WINDVST	39h
WRCTRLDIS	09h
Y2RGB	12h
YBORDER	36h
YCDEL	62h
YCOR	30h
YCSEL	6Bh
YFDEL	12h
YUVSEL	0Eh

3.1.3. I²C Bus Command Table

Table 3–7: I²C register overview

Sub add (Hex)	Data Byte							
	D7	D6	D5	D4	D3	D2	D1	D0
Input Processing								
00h	APPLIP[8:1]							
01h	APPLIP[0]	HSCPRESC [11:5]						
02h	HSCPRESC[4:0]					NAPPLIP[9:7]		
03h	VDELF_EN	NAPPLIP6[6:0]						
04h	NALPFIP							
05h	APENSEL	NALPFIP8	ALPFIP[9:8]		HDCPRESC			
06h	ALPFIP[7:0]							
07h	BLANDEL							
08h	BLANLEN							
09h		WRCTRLDIS	HAAPRESC		MLL			
RGB Front-end								
0Ah	BRTADJ							
0Bh	DECTWO	CHRSF	CONADJ					
0Ch	ADCSEL	AABYP	FBLOFFST					
0Dh	CLMPVRB1	CLMPVRB0	FBLDEL			MIXOP		FBLCONF
0Eh	YUVSEL	SMOP	SKEWSEL	RBOFST			GOFST	
0Fh	RGBSEL	MIXGAIN						
10h	CLMPVG	DCLMPF	USATADJ					
11h	STANDBY1	STANDBY0	VSATADJ					
12h	Y2RGB		YFDEL					
13h			UVDEL					
14h			AGCADJR					
15h			AGCADJG					
16h	ITUPRTSEL	CLKF2PAD	AGCADJB					
17h	NAPIPPHI1	NAPIPPHI0	AGCADJF					
18h	IMODE		VSIGNAL	CFORMAT	F_POL	H_POL	V_POL	EN_656
Noise Reduction								
19h	NMLINE [7:0]							
1Ah	NMPOS		NMSENSE		NMLINE [8]	TNRABS	NRON	TNRSEL
1Bh	TNRS0Y				TNRS1Y			
1Ch	TNRS2Y				TNRS3Y			
1Dh	TNRS4Y				TNRS5Y			
1Eh	TNRS6Y				TNRS7Y			
1Fh	TNRSSY				TNRSSC			

Table 3–7: I^{2}C register overview, continued

Sub add (Hex)	Data Byte							
	D7	D6	D5	D4	D3	D2	D1	D0
20h	TNRS0C				TNRS1C			
21h	TNRS2C				TNRS3C			
22h	TNRS4C				TNRS5C			
23h	TNRS6C				TNRS7C			
24h	TNRCLY				TNRCLC			
Line-locked Clock PLL								
25h	IICINCR[18:11]							
26h	IICINCR[10:3]							
27h					DISRES	IICINCR[2:0]		
28h								HRES
29h	HSWIN				KD2	HINCREXT	LMOD	FMOD
2Ah	KOIWID		KOIH		HTESTW			
2Bh	PPLIP[9:2]							
2Ch	SETSTABLL	FRFIX		LIMEN	FKOI	FKOIHYS	PPLIP[1:0]	
2Dh	FION							LNL
2Eh	CLKT		HWID	HDTOTEST	FILE			
2Fh							LPFIPMD	VINMTHD
Display Processing								
30h	YCOR		CLKOUTON	THRESHC			ASCENTCTI	
31h	HCOF				BCOF			
32h	AUTOFRRN		ALPFOP[9:8]		FINEDEL	COARSEDEL		
33h	ALPFOP[7:0]							
34h	BORDPOSV							
35h	BORDPOSH [7:0]							
36h	BLANPOL	BLANEN	BORDPOSH[9:8]		YBORDER			
37h	UBORDER				VBORDER			
38h	HORWIDTH[7:0]							
39h	WINDVSP		WINDVST	WINDVDR	WINDVON	HORWIDTH[10:8]		
3Ah	HORPOS							
3Bh	WINDHSP1	WINDHSP0	WINDHST	WINDHDR	WINDHON	HORPOS[10:8]		
3Ch	NOSYNC	PPLOFF			LPFOPFF			
3Dh	CHRSHFT	APPLOP						
3Eh	HOUTDEL							
3Fh	NAPPLOP[9:8]		PDGSR	FREEZE	STOPMODE		HOUTDEL[9:8]	
40h	NAPPLOP							
41h	PPLOP[9:8]		REFRPER	REFRON	HOUTPOL	VOUTPOL	HOUTFR	VOUTFR
42h	PPLOP[7:0]							
43h	LPFOP							

Table 3–7: I^{2}C register overview, continued

Sub add (Hex)	Data Byte							
	D7	D6	D5	D4	D3	D2	D1	D0
44h	OPDEL[7:0]							
45h	BORDERV		BORDERH		RDCTRLDIS	LPFOP8	NALPFOP8	OPDEL[8]
46h	NALPFOP							
Panorama Scaler								
47h		PALDEL.1	PALDEL.0	LOCKSP		BGPOS		
48h	HINC0 [7:0]							
49h	HINC1 [7:0]							
4Ah	HINC2 [7:0]							
4Bh	HINC3 [7:0]							
4Ch	HINC4 [7:0]							
4Dh	V656DEL	AFPROC	CLKOUTSEL272	HINC4 [8]	HINC3 [8]	HINC2 [8]	HINC1 [8]	HINC0 [8]
4Eh	HSCPOSC [7:0]							
4Fh	CDELHPOS	CLKOUTSEL	CLKOUTINV	HPANON	HSCPOSC [11:8]			
50h	HSEG1							
51h	HSEG2							
52h	HSEG3							
53h	HSEG4							
54h	FIOFFOFF	FIELDBINV	HSEG2 [10:8]			HSEG1 [10:8]		
55h	CHRMSIG656	VDEL_EN	HSEG4 [10:8]			HSEG3 [10:8]		
DAC Control								
56h	SHIFTUV	DPOUT656						
57h	CHROMSIGN	CHROMAMP						
58h	PKLY							
59h	PKLU							
5Ah	PKLV							
CVBS Front-end								
5Bh	CONS			COLON	CRCB		ACCFIX	ACCFRZ
5Ch	CON			UVCOR		NOTCHOFF	SECNTCH	
5Dh	PWTHD		CLRANGE		LMOFST		VDETIFS	
5Eh	SDR		CHRF					
5Fh	COMB	CSTAND						
60h	CKILL							
61h	CKILLS							
62h	VPOL		LPPOST	YCDEL				
63h	HUE							
64h	NTSCREF							
65h	PALREF							
66h	SLLTHD		SCADJ					

Table 3–7: I^{2}C register overview, continued

Sub add (Hex)	Data Byte							
	D7	D6	D5	D4	D3	D2	D1	D0
67h	AGCMD		AGCADJ1					
68h	AGCRES	AGCFRZE	AGCADJ2					
69h	CLMPHIGH							
6Ah	CVBOSEL1				CLMPLOW			
6Bh	FLINE	FLDINV	CLPSTGY	YCSEL	CLMPD1			
6Ch	HPOL1	HPOL0	FHDET	DISCHCH	CLMPD2			
6Dh	NOSIGB	HINP	CLMPST1					
6Eh	PLLTC		CLMPST2					
6Fh	CVBSEL2				CVBSEL1			
70h	CVBOSEL2				CVBOSEL3			
71h	FHFRRN							
72h	REFTRIMEN	SATNR	VINP	NSRED		LPCDEL		
73h	VSHIFT							
74h	PALIDL1	VTHRL50						
75h	PALIDL0	VTHRH50						
76h	REFTRIM							
77h	REFTRIMCV				REFTRIMRGB			
78h	SLLTHDVP	THRSEL	CLMPST1S					
79h	SCMIDL		CLMPST2S					
7Ah	ACCLIM					IFCOMP		
7Bh	CLMPD2S				CLMPD1S			
7Ch			EIA770	SHAPERDIS	OSCPD	TSTSHAPERI	FREQSEL1	FREQSEL0
7Dh		BELLFIR			BELLIIR			VFLYWHL
7Eh	FLNSTRD		ENLIM	ISHFT		NSRED2	VLP	
7Fh	SECACC	SECDIV	SECINC1		SECINC2		SCMREL	
80h	PORCNCL	NTCHSEL			CPLLRES	DISALLRES	TRAPBLU	TRAPRED
81h	ADLCK	ADLCKSEL	ADLCKCC	VFLYWHLMD		SECACCL		
82h	SYNFTHD		IFCOMSTR	PALIDL2	CPLLOF	DEEMPSTD	PALINC1	PALINC2
Read Register								
83h								FBLACTIVE
84h		NOISEME						
85h			LBSTATUS	PFBL	PG	PB	PR	NMSTATUS
86h								STABLL
87h							SMMIRROR	
88h	DETHPOL	DETVPOL	STDET			SCOUTEN	PALID	CKSTAT
89h	LNSTDRD	INT	SCDEV					
8Ah	LPFLD							
8Bh	NRPIXEL							

Table 3–7: I^{2}C register overview, continued

Sub add (Hex)	Data Byte							
	D7	D6	D5	D4	D3	D2	D1	D0
8Ch	POR				VFLYMD	STAB		PALDET
8Dh	REFTRIMRD							
8Eh	REFTRIMCVRD				REFTRIMRGBRD			
8Fh					SLS	VERSION		
90h	AM50O	AM60O	AGCADJCV					
91h		VLENGTH						
92h	MINV							
93h				PWADJCNT				
96h								V40STAT
97h								
98h								V36BSTAT
99h								V20STAT
PP								
A0h	KPNL[3:0]				KPL[3:0]			
A1h	KINL[3:0]				KIL[3:0]			
A2h	LIMIP							
A3h	LIMII							
A4h	KPNL[4]	KPL[4]	KINL[4]	KIL[4]	LIMLR			
CVBS Front-end								
B0h		AGCTHD		FEMAG				
B1h		SLLTHDV			AMSTD60		AMSTD50	
B2h	SDB			MVPG	MVP	VDETITC		
B3h		VTHRL60						
B4h		VTHRH60						
B5h	DEEMPIIR				DEEMPFIR			
ITU Input								
B7h	NAPPLIPI							
B8h	ALPFIPI							
B9h	APPLIPI [7:0]							
BAh	APPLIPI[8]	NALPFIPI						
LL-PLL								
BCh	FRINC[18:11]							
BDh	FRINC[10:3]							
BEh						FRINC[2:0]		
C0h	HSPPL							
C1h	FOFFST	VSLPF						

Aug. 16, 2004; 6251-552-1DS

Table 3–7: I²C register overview, continued

Sub add (Hex)	Data Byte							
	D7	D6	D5	D4	D3	D2	D1	D0
D0h	VBLANDEL [9:8]		VBLANPOL			FSWFTL	VBLANLEN [9:8]	
D1h	VBLANDEL [7:0]							
D2h	VBLANLEN [7:0]							
	Letterbox Detection							
E0h	LBGRADDET							
E1h	LBVWENDLO							
E2h	LBHWEND							
E3h	LBHIWHITE							
E4h	LBHISTBLA							
E5h	LBMASLA	LBVWSTLO						
E6h	LBFS	LBVWENDUP						
E7h	LBVISUON	LBHWST						
E8h			LBVWSTUP					
E9h	LBSTABILITY	LB43SENS	LBNGFEN	LBTHDNBNG				
EAh	LBSUB1	LBSUB0	LBGRADRST	LBHSDEL				
EBh				LBTHDNBNHA				
ECh				LBACTIVITY				
EDh				LBGFBDEL				
EEh				LBGSDEL				
EFh				LBASDEL				
	Letterbox Read							
F0h	LBSLAA							
F1h	LBELAA							
F2h	LBFORMAT	LBSUBTITLE	LBTOPTITLE	GRADISSTABLE	TOPTITLE	SUBTITLE	NOGRADFOUND	SWITCHTO43
F3h	GRADELAA[8]	GRADSLAA						
F4h	GRADELAA[7:0]							
F5h					LPBLACK	UPBLACK	LPWHITE	UPWHITE
F6h	VERSION			SLS	REV			
FEh	take-over-indication (immediately)							
FFh	take-over-indication (after V-pulse)							

3.1.4. I²C Bus Command Description

Underlined values are initialized at power-on. Some bits are intended to not be user adjustable. Mandatory and recommended settings are available from Micronas in a separate document (Application Note: I²C Settings).

Table 3–8: I²C bus command description

Bit	Name	Description
Subaddress 00h		
D7-D0	APPLIP8-1 [FP-PRE]	**Active Pixel Per Line** Number of pixels to be stored in memory Granularity: 2 pixel '000000000': 0 pixel '<u>101010101': 682 pixel</u> '111111111': 1022 pixel
Subaddress 01h		
D7	APPLIP0 [FP-PRE]	Belongs to 00h
D6-D0	HSCPRESC11-5 [FP-PRE]	**Control Signal For HSCALE In Horizontal Pre-scaler** '000000000000': subsampling factor by scaler stage is 1 '100000000000': subsampling factor is 1.5 (720 pixel) '<u>100101010110': subsampling factor is 1.583 (682 pixel)</u> '111111111111': subsampling factor is 2 (540 pixel)
Subaddress 02h		
D7-D3	HSCPRESC4-0 [FP-PRE]	Belongs to 01h
D2-D0	NAPPLIP9-7 [FP-PRE]	**Not Active Pixel Per Line** Granularity: 2 clock cycles (~50 ns) '0000000000': 0 clock cycles '<u>0001001000': 144 clock cycles (~7.2 µs)</u> '1111111111': 2046 clock cycles (~51 µs)
Subaddress 03h		
D7	VDELF_EN [FP-PRE]	**Vertical pulse delay frontend** '0': no delay '<u>1': delayed</u>
D6-D0	NAPPLIP6-0 [FP-PRE]	Belongs to 02h
Subaddress 04h		
D7-D0	NALPFIP7-0 [FP-PRE]	**Not Active Lines Per Field (Input Processing)** '000000000': 0 lines '<u>000010110':</u> 22 lines '111111111': 511 lines

Table 3–8: I^{2}C bus command description, continued

Bit	Name	Description
Subaddress 05h		
D7	APENSEL [FP-PRE]	**Active Pixel Enable Select** 0: count clock cycles (recommended for CVBS/RGB input) 1: count active pixels (recommended for ITU656 input)
D6	NALPFIP8 [FP-PRE]	Belongs to 04h
D5-D4	ALPFIP9-8 [FP-PRE]	**Active Lines Per Field** '0000000000': no active line '0100100000': 288 active lines '1111111111': 1023 active lines
D3-D0	HDCPRESC	**Horizontal Pre-Scaler Decimates By** '0000': 1 '0001': 2 '0010': 3 '0011': 4 '0100': 6 '0101': 8 '0110': 12 '0111': 16 '1000': 24 '1001': 32
Subaddress 06h		
D7-D0	ALPFIP7-0	Belongs to 05h
Subaddress 07h		
D7-D0	BLANDEL	**Blanking signal delay** Delay in pixels from hsync to active edge of blank signal: Blank_start=4*__BLANDEL__ '00000000': no delay '00000001': 4 pixel delay '11111111': 1020 pixel delay
Subaddress 08h		
D7-D0	BLANLEN	**Blanking signal length** Length in pixels from start of active blank signal: Blank_length=4*__BLANLEN__ '00000000': no pixel '11110000': 960 pixel '11111111': 1020 pixel length

Table 3–8: I^{2}C bus command description, continued

Bit	Name	Description
Subaddress 09h		
D6	WRCTRLDIS [FP-MC]	**Memory Write Control Circuit Disable** '0': enabled '1': disabled
D5-D4	HAAPRESC [FP-MC]	**Horizontal Anti Alias Filter** '00': filter bypassed '01': force characteristic weak '10': force characteristic strong '11': automatic characteristic (weak or strong) *Note: For normal CVBS/RGB full-screen, filter should be set to weak or automatic characteristic. For ITU656 full-screen input, filter should be bypassed. Strong characteristic is for split-screen and PiP only.*
D3-D0	MLL [FP-MC]	**Minimum Line Length** effective number of clock periods: 600 + MLL*128 1110: corresponds to 2392 clock periods
Subaddress 0Ah		
D7-D0	BRTADJ [FP-RGB]	**Brightness Adjustment of RGB/YUV input** '10000000': −128 LSB (darkest picture) '00000000': 0 '01111111': +127 LSB (brightest picture)
Subaddress 0Bh		
D7	DECTWO [FP-RGB]	**Decimation by 2** decimation of RGB/YUV signal before soft-mix '0': no decimation '1': decimation by 2
D6	CHRSF [FP-RGB]	**Additional Chroma subsampling filter** '0': disabled '1': enabled
D5-D0	CONADJ [FP-RGB]	**Contrast Adjustment of RGB/YUV input** '000000': 0 '000001': 1/32 '100000': 1 '111111': 63/32
Subaddress 0Ch		
D7	ADCSEL [FP-RGB]	**Select ADC for sync signal conversion** '0': use ADC_G '1': use ADC_FBL
D6	AABYP [FP-RGB]	**Bypass RGB/YUV Antialiasfilter** '0': use filter '1': bypass
D5-D0	FBLOFFST [FP-RGB]	**Fast Blank Offset Correction** '000000': 0 LSB offset '111111': 63 LSB offset

Micronas

Table 3–8: I^{2}C bus command description, continued

Bit	Name	Description
Subaddress 0Dh		
D7-D6	CLMPVRB [FP-RGB]	**Clamping Value Red and Blue ADC** '00': 16 (B/R signal without sync) '01': 80 (B/R signal with sync) <u>'10': 128 (U/V signal)</u> '11': (reserved)
D5-D3	FBLDEL [FP-RGB]	**Fast Blank Delay vs. RGB/YUV Input** granularity: 25 ns '000': −50 ns delay <u>'010': no delay</u> '110': +100 ns delay '111': (reserved)
D2-D1	MIXOP [FP-RGB]	**Mixing Configuration** <u>'00': enable Soft-Mix</u> '01': only RGB path visible '10': only CVBS path visible '11': (reserved)
D0	FBLCONF [FP-RGB]	**Configuration of FBLACTIVE signal** <u>'0': react after one clock (25 ns) active FBL input</u> '1': react after 5 clock (125 ns) active FBL input
Subaddress 0Eh		
D7	YUVSEL [FP-RGB]	**YUV or RGB Input Selection** '0': YUV expected <u>'1': RGB expected</u>
D6	SMOP [FP-RGB]	**Softmix Operation Mode** <u>'0': dynamic</u> '1': static
D5	SKEWSEL [FP-RGB]	**SKEW Correction for RGB/YUV Channel** <u>'0': SKEW correction enabled</u> '1': SKEW correction disabled (for PiP3, PiP4 only)
D4-D2	RBOFST [FP-RGB]	**Clamping Correction for R/B ADC** <u>'000': 0 (R/B, no pedestal offset visible)</u> '001': 16 '010': 64 (R/B with sync, no pedestal offset visible) '011': 80 '100': 127 (UV negative pedestal offset) '101': 128 (UV) '110': 129 (UV positive pedestal offset) '111': (reserved)
D1-D0	GOFST [FP-RGB]	**Clamping correction for G ADC** <u>'00': 0 (G/Y, no pedestal offset visible)</u> '01': 16 '10': 64 (G/Y with sync, no pedestal offset visible) '11': 80

Table 3–8: I^{2}C bus command description, continued

Bit	Name	Description
Subaddress 0Fh		
D7	RGBSEL [FP-RGB]	**Input selection** '0': use RGB/YUV input1 '1': use RGB/YUV input2
D6-D0	MIXGAIN [FP-RGB]	**Gain of Fast Blank Signal** '1000000': −64 '0000000': 0 '0111111': +63 *Note: For proper operation in dynamic softmix mode, absolute value of* **MIX-GAIN** *must be bigger than 2 (e.g. 3)*
Subaddress 10h		
D7	CLMPVG [FP-RGB]	**Clamping Value G ADC** '0': 16 '1': 80
D6	DCLMPF [FP-RGB]	**Clamping Fast Blank input** '0': enable clamping '1': disable clamping (DC coupling)
D5-D0	USATADJ [FP-RGB]	**U Saturation Adjustment** '000000': 0 '000001': 1/32 '100000': 1 '111111': 63/32
Subaddress 11h		
D7-D6	STANDBY [FP-RGB]	**Standby Mode** '00': all analog cores active '01': RGB/FBL ADCs in Stand-By mode '10': RGB/FBL and CVBS ADCs and DACs in Stand-By mode '11': DACs in Stand-By mode
D5-D0	VSATADJ [FP-RGB]	**V Saturation Adjustment** '000000': 0 '000001': 1/32 '100000': 1 '111111': 63/32
Subaddress 12h		
D7	Y2RGB [FP-RGB]	**Y to RGB (for YUV mode)** 0: use Y from green ADC 1: use Y from CVBS ADC
D5-D0	YFDEL [FP-RGB]	**Y/FBL Delay Adjustment** Granularity: 50 ns '000000': no delay '111111': 3.15 μs

Table 3–8: I^{2}C bus command description, continued

Bit	Name	Description
Subaddress 13h		
D5-D0	UVDEL [FP-RGB]	**UV Delay Adjustment** Granularity: 50 ns '000000': no delay '111111': 3.15 μs
Subaddress 14h		
D5-D0	AGCADJR [FP-RGB]	**Conversion Range Adjustment Red** '000000': 0.5 V input signal '111111': 1.5 V input signal
Subaddress 15h		
D5-D0	AGCADJG [FP-RGB]	**Conversion Range Adjustment Green** '000000': 0.5 V input signal '111111': 1.5 V input signal
Subaddress 16h		
D7	ITUPRTSEL [FP-RGB]	**ITU port selection** 0: first input (656io) 1: second input (i656i)
D6	CLKF2PAD [FP-RGB]	**Frontend clock is given to pin 74** '0' pin 74 is used as h-input for ITU656 '1': CLKF20 (20.25 MHz) is given to pin 74
D5-D0	AGCADJB [FP-RGB]	**Conversion Range Adjustment Blue** '000000': 0.5 V input signal '111111': 1.5 V input signal
Subaddress 17h		
D7-D6	NAPIPPHI [FP-RGB]	**CbYCrY-phase shift** '0': no phase shift
D5-D0	AGCADJF [FP-RGB]	**Conversion Range Adjustment Fast Blank** '000000': 0.5 V input signal '111111': 1.5 V input signal

Table 3–8: I^{2}C bus command description, continued

Bit	Name	Description
Subaddress 18h		
D7-D6	IMODE [FP-RGB]	**Input format** '00': full ITU mode (automatic) '01': full ITU mode (manual) '10': ITU656 only data, H/V-sync according PAL/NTSC '11': ITU656 only data, H/V-sync according ITU656
D5	VSIGNAL [FP-RGB]	**Input signal** '0': interlaced '1': non interlaced
D4	CFORMAT [FP-RGB]	**Chrominance data format** '0': unsigned '1': 2s complement
D3	F_POL [FP-RGB]	**Field polarity** '0': Field A=0, Field B=1 '1': Field A=1, Field B=0
D2	H_POL [FP-RGB]	**H656 polarity** '0': H656 active low '1': H656 active high
D1	V_POL [FP-RGB]	**V656 polarity** '0': V656 active low '1': V656 active high
D0	EN_656 [FP-RGB]	**ITU656-Input Interface** '0': analog input enabled (CVBS/RGB) '1': ITUI enabled
Subaddress 19h		
D7-D0	NMLINE7-0 [FP-TNR]	**Line For Noise Measurement** 0_d: line 2 1_d: line 3 311_d: line 1 (PAL) 261_d: line 1 (NTSC) lines 3-260 are not standard dependent

Table 3–8: I^{2}C bus command description, continued

Bit	Name	Description
Subaddress 1Ah		
D7-D6	NMPOS [FP-TNR]	**Noise Measurement analyze window position** 00: 6.3 μs 01: 12.6 μs 10: 18.9 μs 11: 23.7 μs
D5-D4	NMSENSE [FP-TNR]	**Noise Measurement sensitivity** 00: *1 01: *2 10: *4 11: *8
D3	NMLINE8 [FP-TNR]	Belongs to 19h
D2	TNRABS [FP-TNR]	**Motion Detector Works on Absolute Values:** '0': absolute values not calculated '1': absolute values calculated
D1	NRON [FP-TNR]	**Temporal Noise Reduction** '0': disabled '1': enabled
D0	TNRSEL [FP-TNR]	**Chrominance Motion Values From:** '0': luminance motion detector '1': separate chrominance motion detector
Subaddress 1Bh		
D7-D4	TNRS0Y [FP-TNR]	**TNR Curve Characteristic of Luma Segment 0** default value: 0001
D3-D0	TNRS1Y [FP-TNR]	**TNR Curve Characteristic of Luma Segment 1** default value: 1111
Subaddress 1Ch		
D7-D4	TNRS2Y [FP-TNR]	**TNR Curve Characteristic of Luma Segment 2** default value: 1111
D3-D0	TNRS3Y [FP-TNR]	**TNR Curve Characteristic of Luma Segment 3** default value: 0100
Subaddress 1Dh		
D7-D4	TNRS4Y [FP-TNR]	**TNR Curve Characteristic of Luma Segment 4** default value: 0100
D3-D0	TNRS5Y [FP-TNR]	**TNR Curve Characteristic of Luma Segment 5** default value: 0100
Subaddress 1Eh		
D7-D4	TNRS6Y [FP-TNR]	**TNR Curve Characteristic of Luma Segment 6** default value: 0000
D3-D0	TNRS7Y [FP-TNR]	**TNR Curve Characteristic of Luma Segment 7** default value: 0000

Table 3–8: I^{2}C bus command description, continued

Bit	Name	Description
Subaddress 1Fh		
D7-D4	TNRSSY [FP-TNR]	**TNR Start Value of Luma LUT** <u>default value: 1111</u>
D3-D0	TNRSSC [FP-TNR]	**TNR Start Value of Chroma LUT** <u>default value: 1111</u>
Subaddress 20h		
D7-D4	TNRS0C [FP-TNR]	**TNR Curve Characteristic of Chroma Segment 0** <u>default value: 0001</u>
D3-D0	TNRS1C [FP-TNR]	**TNR Curve Characteristic of Chroma Segment 1** <u>default value: 1111</u>
Subaddress 21h		
D7-D4	TNRS2C [FP-TNR]	**TNR Curve Characteristic of Chroma Segment 2** <u>default value: 1111</u>
D3-D0	TNRS3C [FP-TNR]	**TNR Curve Characteristic of Chroma Segment 3** <u>default value: 0100</u>
Subaddress 22h		
D7-D4	TNRS4C [FP-TNR]	**TNR Curve Characteristic of Chroma Segment 4** <u>default value: 0100</u>
D3-D0	TNRS5C [FP-TNR]	**TNR Curve Characteristic of Chroma Segment 5** <u>default value: 0100</u>
Subaddress 23h		
D7-D4	TNRS6C [FP-TNR]	**TNR Curve Characteristic of Chroma Segment 6** <u>default value: 0000</u>
D3-D0	TNRS7C [FP-TNR]	**TNR Curve Characteristic of Chroma Segment 7** <u>default value: 0000</u>
Subaddress 24h		
D7-D4	TNRCLY [FP-TNR]	**TNR Luminance Classification** '0000': strong noise reduction <u>'1111': slight noise reduction</u>
D3-D0	TNRCLC [FP-TNR]	**TNR Chrominance Classification** '0000': strong noise reduction <u>'1111': slight noise reduction</u>
Subaddress 25h		
D7-D0	IICINCR18-11 [PP]	**Set HDTO frequency** Granularity=103 Hz 33981_d (minimum: nominal pixel clock= 3.5 MHz) <u>349525_d (nominal pixel clock= 36 MHz)</u> 388362_d (maximum: nominal pixel clock= 40 MHz)

Table 3–8: I^2C bus command description, continued

Bit	Name	Description
Subaddress 26h		
D7-D0	IICINCR10-3 [PP]	Belongs to 25h
Subaddress 27h		
D3	DISRES [PP]	**Reset of LL-PLL watchdog** '0': reset disabled '1': reset enabled
D2-D0	IICINCR2-0 [PP]	Belongs to 25h
Subaddress 28h		
D0	HRES [PP]	**Reset of LL-HPLL** '0': no reset '1': reset *Note: reset automatically when written*
Subaddress 29h		
D7-D4	HSWIN [PP]	**Width of Noise Suppression Window of LL-HPLL** '0000': ±28 µs '0001': ±24 µs '0010': ±20 µs '0011': ±16 µs '0100': ±12 µs '0101': ±8 µs '0110': ±4 µs '0111': dynamic windowing. '1000': ±30 µs '1001': ±27 µs '1010': ±26 µs '1011': ±22 µs '1100': ±18 µs '1101': ±14 µs '1110': ±10 µs '1111': ±6 µs
D3	KD2 [PP]	**Phase Detector Steepness** '0': steepness for normal TV operation mode '1': steepness for operations where PPLIP is less than 288_d
D2	HINCREXT [PP]	**HDTO testmode** '0': normal mode '1': line-locked-clocks derived from frontend line-length
D1	LMOD [PP]	**Selects line locked mode** '0': line locked-clocks derived from HPLL '1': line-locked-clocks derived from frontend line-length
D0	FMOD [PP]	**Selects freerun mode** '0': freerun-clocks derived from crystal '1': freerun-clocks derived from HDTO Adjustable frequency is only possible when set to '1'. When set to '0', Backend clock is always 36 MHz (9432/42: 18 MHz)

Table 3–8: I^{2}C bus command description, continued

Bit	Name	Description
Subaddress 2Ah		
D7-D6	KOIWID [PP]	**Window-Width of coincidence detector** '00': ±32 pixel (= ±0.9 μs for TV application) <u>'01': ±64 pixel (= ±1.8 μs for TV application)</u> '10': ±128 pixel (= ±3.6 μμs for TV application) '11': ±256 pixel (= ±7.2 μs for TV application)
D5-D4	KOIH [PP]	**Hysteresis of coincidence detector** '00': 0 lines '01': 8 lines <u>'10': 16 lines</u> '11': 32 lines
D3-D0	HTESTW [PP]	**Test bits for HPLL** <u>00: default</u>
Subaddress 2Bh		
D7-D0	PPLIP9-2 [PP]	**Pixel per Line Input (Input-Processing)** Granularity=4 pixel '175$_d$': 700 (minimum) <u>'576$_d$': 2304</u> '963$_d$': 3852 (maximum)
Subaddress 2Ch		
D7	SETSTABLL [PP]	**Stability Signal of LL_HPLL** <u>'0': STABLL is generated by the HPLL</u> '1': STABLL is forced to 1
D6	FRFIX [PP]	**Freerunning clocks** <u>'0': from fixed clock divider</u> '1': from freerunning DTO (adjustable clocks)
D4	LIMEN [PP]	**Limiter enable** <u>'0': A32 behavior for *LIMIP* and *LIMII*</u> '1': normal *LIMII* and *LIMIP* characteristic
D3	FKOI [PP]	**Force Coincidence Bit** <u>'0': coincidence bit dynamically changed</u> '1': coincidence bit forced to 1
D2	FKOIHYS [PP]	**Force coincidence hysteresis bit** <u>'0': coincidence hysteresis bit dynamically changed</u> '1': coincidence hysteresis bit forced to 1
D1-D0	PPLIP1-0 [PP]	Belongs to 2Bh
Subaddress 2Dh		
D7-D4	FION [PP]	**Increment Freeze before V-sync** <u>'0': no freeze</u> '15': freeze starts 15 lines before V-sync
D0	LNL [PP]	**Dynamic Time Constant Control** <u>'0': linear mode</u> '1': non linear mode

Table 3–8: I^{2}C bus command description, continued

Bit	Name	Description
Subaddress 2Eh		
D7-D6	CLKT [PP]	**Switch clkf20 and clkf40 to pads *cvbs1* or *bin2* (test only)** '00': no clock '01': cvbs1 is output of clkf40 '10': *bin2* is output of clkf20 '11': *cvbs1* is output of clkf40 and *bin2* is output of clkf20
D5	HWID [PP]	**Minimum width of H-sync** '0': 60*T$_{clkllf36}$ '1': 15*T$_{clkllf36}$
D4	HDTOTEST [PP]	**Test-bit for HPLL** '0': normal mode '1': test mode
D3-D0	FILE [PP]	**Increment Freeze duration** '0': no freeze '15': increment is frozen for 15 lines
Subaddress 2F		
D1	LPFIPMD [BP-DP]	**Lines per field method** 0: backend 1: frontend
D0	VINMTHD [BP-DP]	**Vertical ODC line counting** 0: field delay 1: frame delay
Subaddress 30h		
D7-D6	YCOR [BP-DP]	**Luminance Coring** '00': off '01': 2 '10': 4 '11': 8
D5	CLKOUTON [BP-DP]	**Clkout Pad:** '0': off (tristate) '1': on
D4-D2	THRESHC [BP-DP]	**Slope of DCTI function** '000': 255 (DCTI off) '001': 2 '010': 3 '011': 4 '100': 6 '101': 8 '110': 10 '111': 12
D1-D0	ASCENTCTI [BP-DP]	**Gain of DCTI function** '00': 1/4 '01': 1/2 '10': 1 '11': 2

Table 3–8: I^{2}C bus command description, continued

Bit	Name	Description
Subaddress 31h		
D7-D4	HCOF [BP-DP]	**Peaking: High-Pass Filter Adjustments** '0000': 0 '0001': 1/4 ... '0100': 1 ... '1100': 12/4 '1101': 14/4 '1110': 16/4 '1111': 20/4
D3-D0	BCOF [BP-DP]	**Peaking: Band-Pass Filter Adjustments** '0000': 0 '0001': 1/4 ... '0100': 1 ... '1100': 12/4 '1101': 14/4 '1110': 16/4 '1111': 20/4
Subaddress 32h		
D7-D6	AUTOFRRN [BP-DP]	**Automatic freerun** when sync-separartion not stable '00': disabled (keep H/V locked, if selected) '01': use vertical freerun '10': use horizontal freerun '11': use horizontal and vertical freerun
D5-D4	ALPFOP9-8 [BP-DP]	**Active Lines Per Field Output** '0000000000': 0 (minimum) '0100100000': 288 (default) '1111111111': 1023 (maximum)
D3	FINEDEL [BP-DP]	**Luminance Fine Delay output** '0': no delay '1': +1 CLKB72 (13.9 ns for TV signal)
D2-D0	COARSEDEL [BP-DP]	**Luminance Coarse Delay output** Granularity: 1 CLKB36 (27.8 ns for TV signal) '000': −4 CLKB36 '100': no delay '111': +3 CLKB36
Subaddress 33h		
D7-D0	ALPFOP7-0 [BP-PM]	Belongs to 32h
Subaddress 34h		
D7-D0	BORDPOSV [BP-PM]	**Borderposition Vertical** Granularity: 2 lines '00000000': no border '11111111': border at 512 lines at top and bottom

Aug. 16, 2004; 6251-552-1DS
Micronas

Table 3–8: I^{2}C bus command description, continued

Bit	Name	Description
Subaddress 35h		
D7-D0	BORDPOSH7-0 [BP-PM]	**Borderposition Horizontal** Granularity: 2 pixel '0000000000': no border '1111111111': border at 2048 pixel on left and right
Subaddress 36h		
D7	BLANPOL [BP-PM]	**Blanking signal polarity** '0': active high '1': active low
D6	BLANEN [BP-PM]	**Blanking signal enable** '0': disabled (pin 8 can be used as 656vin) '1': enabled
D5-D4	BORDPOSH 9-8 [BP-PM]	Belongs to 35h
D3-D0	YBORDER [BP-PM]	**Luminance Value for Border** '0000': sub black '0001': black '1111': white
Subaddress 37h		
D7-D4	UBORDER [BP-PM]	**Chrominance (U) Value for Border** '1000': '0000': 'no color' U '0111':
D3-D0	VBORDER [BP-PM]	**Chrominance (V) Value for Border** '1000': '0000': 'no color' V '0111':
Subaddress 38h		
D7-D0	HORWIDTH7-0 [BP-PM]	**Horizontal Picture Width** Granularity: 2 pixel '00000000000': no display '00111100000': 960 pixel '11111111111': 4094 pixel *Note: Should be set equal to APPLOP (3Dh)*

Table 3–8: I^{2}C bus command description, continued

Bit	Name	Description
Subaddress 39h		
D7-D6	WINDVSP [BP-PM]	**Vertical Windowing: Speed** '<u>00</u>': slow '01': medium '10': fast '11': very fast
D5	WINDVST [BP-PM]	**Vertical Windowing: Start** '<u>0</u>': window is closed '1': window is open
D4	WINDVDR [BP-PM]	**Vertical Windowing: Direction** '<u>0</u>': open the vertical window '1': close the vertical window
D3	WINDVON [BP-PM]	**Vertical Windowing: Enable** '<u>0</u>': off '1': on
D2-D0	HORWIDTH 10-8 [BP-PM]	Belongs to 38h
Subaddress 3Ah		
D7-D0	HORPOS7-0 [BP-PM]	**Horizontal Position inside active picture area** Granularity: 2 pixel '<u>00000000000</u>': most left display position '11111111111': most right display position
Subaddress 3Bh		
D7-D6	WINDHSP [BP-PM]	**Horizontal Windowing: Speed** '<u>00</u>': slow '01': medium '10': fast '11': very fast
D5	WINDHST [BP-PM]	**Horizontal Windowing: Start** '<u>0</u>': window is closed '1': window is open
D4	WINDHDR [BP-PM]	**Horizontal Windowing: Direction** '<u>0</u>': open the horizontal window '1': close the horizontal window
D3	WINDHON [BP-PM]	**Horizontal Windowing: Enable** '<u>0</u>': off '1': on
D2-D0	HORPOS10-8 [BP-PM]	Belongs to 3Ah

Table 3–8: I^{2}C bus command description, continued

Bit	Name	Description
Subaddress 3Ch		
D7	NOSYNC [BP-ODC]	**No horizontal synchronization** '0': horizontal synchronization '1': no horizontal synchronization
D6-D4	PPLOFF [BP-ODC]	**Synchronization offset** (for switching from hor. freerun mode to locked mode) Granularity: 4 pixel '000': 0 (disabled) '010': 8 '111': 28
D3-D0	LPFOPFF [BP-ODC]	**Lines per field offset:** (for switching from vertical freerun mode to locked mode) Granularity: 2 lines '0000': 0 (disabled) '0110':12 '1111': 31
Subaddress 3Dh		
D7	CHRSHFT [BP-O/M]	**Chrominance Shift** shifts the chrominance signal '0': no shift '1': one line upward
D6-D0	APPLOP [BP-O/M]	**Active Pixel Per Line Output:** Granularity: 16 pixel '0000000': 0 pixel '0111100': 960 pixel '1111111': 2032 pixel
Subaddress 3Eh		
D7-D0	HOUTDEL7-0 [BP-ODC]	**H Sync output Delay:** Granularity: 4 pixel '0000000000': no delay '0000000001': 4 pixel delay '1111111111': 4092 pixel delay

Table 3–8: I^{2}C bus command description, continued

Bit	Name	Description
Subaddress 3Fh		
D7-D6	NAPPLOP9-8 [BP-O/M]	**Not Active Pixel Per Line Output:** Granularity: 4 pixel '0000000100': 16 not active pixel '1111111111': 4092 not active pixel
D5	PDGSR [BP-O/M]	**Switch for Vsync transfer algorithm:** '0': Vsync transfer algorithm is enabled '1': Vsync transfer algorithm is disabled
D4	FREEZE [BP-O/M]	**Freeze picture** '0': live '1': frozen (data writing disabled)
D3-D2	STOPMODE [BP-O/M]	**Operation mode for scan rate conversion:** '00': AABB (Raster $\alpha\alpha\beta\beta$) '01': AAAA (Raster $\alpha\alpha\alpha\alpha$) '10': AAAA (Raster $\alpha\beta\alpha\beta$) '11': BBBB (Raster $\beta\beta\beta\beta$)
D1-D0	HOUTDEL9-8 [BP-O/M]	Belongs to 3Eh
Subaddress 40h		
D7-D0	NAPPLOP7-0 [BP-ODC]	Belongs to 3Fh

Table 3–8: I^{2}C bus command description, continued

Bit	Name	Description
Subaddress 41h		
D7-D6	PPLOP9-8 [BP-O/M]	**Pixel Per Line Output:** Granularity:4 '0000000000': 0 pixel '0100100000': 1152 pixel '1111111111': 4092 pixel
D5	REFRPER [BP-O/M]	**Refresh period of the memory** '0': ~5 ms '1': ~2,5 ms
D4	REFRON [BP-O/M]	**Refresh on** '0': no memory refresh '1': memory refresh active
D3	HOUTPOL [BP-O/M]	**HOUT polarity:** '0': high active '1': low active
D2	VOUTPOL [BP-O/M]	**VOUT polarity:** '0': high active '1': low active
D1	HOUTFR [BP-O/M]	**HOUT freerun** '0': locked mode '1': freerun mode
D0	VOUTFR [BP-O/M]	**VOUT freerun** '0': locked mode '1': freerun mode
Subaddress 42h		
D7-D0	PPLOP7-0 [BP-O/M]	Belongs to 41h
Subaddress 43h		
D7-D0	LPFOP7-0 [BP-ODC]	**Lines Per Field Output:** Only used for freerun mode Granularity: 2 lines '000000000': no lines '010011100': 312 lines '111111111:' 1022 lines
Subaddress 44h		
D7-D0	OPDEL7-0 [BP-ODC]	**V delay for output operation:** '000000000': no delay '010101010': 170 lines '111111111': 511 lines

Table 3–8: I^{2}C bus command description, continued

Bit	Name	Description
Subaddress 45h		
D7-D6	BORDERV [BP-O/M]	**Border V** '00': both borders are displayed '01': only lower border is displayed '10': only upper border is displayed '11': (reserved)
D5-D4	BORDERH [BP-O/M]	**Border H** '00': both borders are displayed '01': only right border is displayed '10': only left border is displayed '11': (reserved)
D3	RDCTRLDIS [BP-O/M]	**Memory read control circuit disable** '0': enabled '1': disabled
D2	LPFOP8 [BP-O/M]	Belongs to 43h
D1	NALPFOP8 [BP-O/M]	**Not Active Lines Output** NALPFOP-1 lines are not active lines. '000000001': all lines active '000011001': 24 lines not active '111111111': 510 lines not active
D0	OPDEL8 [BP-O/M]	Belongs to 44h
Subaddress 46h		
D7-D0	NALPFOP7-0 [BP-ODC]	Belongs to 45h
Subaddress 47h		
D6-D5	PALDEL [CP-CD]	**PAL/NTSC delay vs. SECAM (chrominance)** '00': PAL/NTSC most left '11': PAL/NTSC most right
D4-D3	LOCKSP [CP-CD]	**Duration Of Chroma PLL Search** '00': 25 fields '01': 20 fields '10': 17 fields '11': 15 fields
D2-D0	BGPOS [CP-CD]	**Burstgate Delay (SECAM only)** Granularity: 200 ns '000': most left (−400 ns) '011': 200 s delay '111': most right (+1 us)
Subaddress 48h		
D7-D0	HINC0_7-0 [BP-POS]	**Horizontal Post-Scaler Increment 0** '100000000': −32 pixel '000000000': 0 pixel '011111111': 31.875 pixel

Aug. 16, 2004; 6251-552-1DS Micronas

VSP 94x2A

Table 3–8: I^{2}C bus command description, continued

Bit	Name	Description
Subaddress 49h		
D7-D0	HINC1_7-0 [BP-POS]	**Horizontal Post-Scaler Increment 1** '100000000': −32 pixel '000000000': 0 pixel '011111111': 31.875 pixel
Subaddress 4Ah		
D7-D0	HINC2_7-0 [BP-POS]	**Horizontal Post-Scaler Increment 2** '100000000': −32 pixel '000000000': 0 pixel '011111111': 31.875 pixel
Subaddress 4Bh		
D7-D0	HINC3_7-0 [BP-POS]	**Horizontal Post-Scaler Increment 3** '100000000': −32 pixel '000000000': 0 pixel '011111111': 31.875 pixel
Subaddress 4Ch		
D7-D0	HINC4_7-0 [BP-POS]	**Horizontal Post-Scaler Increment 4** '100000000': -32 pixel '000000000': 0 pixel '011111111': 31.875 pixel
Subaddress 4Dh		
D7	V656DEL [BP-POS]	**V656 delay** 0: identical delay for modification 1: field 0 is one line shorter Note: has only effect when **AFPROC**=1
D6	AFPROC [BP-POS]	**Active Field Processing for 656V generation** 0: inverted active field used as v-sync output 1: v-sync modifies end of active video
D5	CLKOUTSEL72 [BP-POS]	**Output clock select** 0: CLKOUT depends on **CLKOUTSEL** 1: CLKOUT is identical to clkb72
D4	HINC4_8 [BP-POS]	Belongs to 4Ch
D3	HINC3_8 [BP-POS]	Belongs to 4Bh
D2	HINC2_8 [BP-POS]	Belongs to 4Ah
D1	HINC1_8 [BP-POS]	Belongs to 49h
D0	HINC0_8 [BP-POS]	Belongs to 48h

Table 3–8: I^{2}C bus command description, continued

Bit	Name	Description
Subaddress 4Eh		
D7-D0	HSCPOSC7-0 [BP-POS]	**Horizontal Scaling Factor For Post Scaler** '010000000000': factor is 4 '<u>101101010101</u>': factor is 1.407 (682 → 960) '110000000000': factor is 4/3 (720 → 960) '111111111111': factor is 1
Subaddress 4Fh		
D7	CDELHPOS [BP-POS]	**Chrominance delay** <u>0: no delay</u> 1: half-pixel delay
D6	CLKOUTSEL [BP-POS]	**Output clock select** <u>0: CLKOUT is identical to clkb27</u> 1: CLKOUT is identical to clkb36 *Note: HSYNC, VSYNC, BLANK are transferred to selected clock*
D5	CLKOUTINV [BP-POS]	**CLKOUT inversion** <u>0: no inverted CLKOUT</u> 1: inverted CLKOUT
D4	HPANON [BP-POS]	**Panorama Mode enable** '<u>0': panorama mode disabled</u> '1': panorama mode enabled
D3-D0	HSCPOSC 11-8 [BP-POS]	Belongs to 4Eh
Subaddress 50h		
D7-D0	HSEG1_7-0 [BP-POS]	**Beginning of Segment 1 for Panorama Mode** Granularity: 2 pixel '<u>00000000000': 0 pixel behind picture start</u> '11111111111': 4094 pixel behind picture start
Subaddress 51h		
D7-D0	HSEG2_7-0 [BP-POS]	**Beginning of Segment 2 for Panorama Mode** Granularity: 2 pixel '<u>00000000000': 0 pixel behind picture start</u> '11111111111': 4094 pixel behind picture start
Subaddress 52h		
D7-D0	HSEG3_7-0 [BP-POS]	**Beginning of Segment 3 for Panorama Mode** Granularity: 2 pixel '<u>00000000000': 0 pixel behind picture start</u> '11111111111': 4094 pixel behind picture start
Subaddress 53h		
D7-D0	HSEG4_7-0 [BP-POS]	**Beginning of Segment 4 for Panorama Mode** Granularity: 2 pixel '<u>00000000000': 0 pixel behind picture start</u> '11111111111': 4094 pixel behind picture start

Table 3–8: I²C bus command description, continued

Bit	Name	Description
Subaddress 54h		
D7	FIOFFOFF [BP-POS]	**Fieldoffset for ITU656 NTSC signals** '0': disabled '1': enabled
D6	FIELDBINV [BP-POS]	**Backend field inversion** '0': no inversion '1': inversion
D5-D3	HSEG2_10-8 [BP-POS]	Belongs to 51h
D2-D0	HSEG1_10-8 [BP-POS]	Belongs to 50h
Subaddress 55h		
D7	CHRMSIG656 [BP-POS]	**Chrominance format for 656 output** '0': (R−Y), (B−Y) output '1': −(R−Y), −(B−Y) output
D6	VDEL_EN [BP-POS]	**Vertical pulse delay backend (test only)** '0': no delay '1': delayed
D5-D3	HSEG4_10-8 [BP-POS]	Belongs to 53h
D2-D0	HSEG3_10-8 [BP-POS]	Belongs to 52h
Subaddress 56h		
D7	SHIFTUV [BP-DAC]	**Shift UV subsampling at digital output** '0': take first UV couple '1': take second UV couple VSP9432/42 only
D6	DPOUT656 [BP-DAC]	**Enable digital 656 Output** '0': disable output '1': enable output
Subaddress 57h		
D7	CHROMSIGN [BP-DAC]	**Chrominance sign** '0': (R−Y), (B−Y) output '1': −(R−Y), −(B−Y) output
D6	CHROMAMP [BP-DAC]	**Chrominance amplification** '0': amplification=1 '1': amplification=2
Subaddress 58h		
D7-D0	PKLY [BP-DAC]	**Voltage Level for Y DAC Output** '00000000': 0.4 V '10000000': 1.0 V '11111111': 1.9 V including peaking overshoots. 0.9 V for white max.

Table 3–8: I^{2}C bus command description, continued

Bit	Name	Description
Subaddress 59h		
D7-D0	PKLU [BP-DAC]	**Voltage Level for U DAC Output** '00000000': 0.4 V '<u>10000000': 1.0 V</u> '11111111': 1.9 V
Subaddress 5Ah		
D7-D0	PKLV [BP-DAC]	**Voltage Level for V DAC Output** '00000000': 0.4 V '<u>10000000': 1.0 V</u> '11111111': 1.9 V
Subaddress 5Bh		
D7-D5	CONS [CP-CD]	**Color Switched On (SECAM)** at level=CKILLS+CONS '000': min value '<u>010': default</u> '111': max value
D4	COLON [CP-CD]	**Force Color On** '<u>0': color depends on color decoder status</u> '1': color always on
D3-D2	CRCB [CP-CD]	**Choice of UV or CrCb output** 00: UV color space <u>01: CrCb color space</u> 10: modified CrCb color space (SECAM only; PAL & NTSC: same as setting '01')
D1	ACCFIX [CP-CD]	**Fix ACC to Nominal Value** '<u>0': ACC is working</u> '1': ACC is fixed
D0	ACCFRZ [CP-CD]	**Freeze ACC** '<u>0': ACC is working</u> '1': ACC is frozen

Table 3–8: I^{2}C bus command description, continued

Bit	Name	Description
Subaddress 5Ch		
D7-D5	CON [CP-CD]	**Color Switched On (PAL/NTSC)** at level=CKILL+CON '000': min value <u>'010': default</u> '111': max value
D4-D3	UVCOR [CP-CD]	**Chrominance coring** <u>'00': off</u> '01': ±1LSB '10': ± 2LSB '11': ± 3LSB
D2	NOTCHOFF [CP-CD]	**Luminance notch-filter** <u>'0': notch-filter enabled</u> '1': notch-filter bypassed
D1-D0	SECNTCH [CP-CD]	**Selection of Notch filter behavior in SECAM mode** <u>'00': 4.406 MHz</u> '01': 4.250 MHz '10': 4.33 MHz '11': 4.406 / 4.25 dependent on transmitted color
Subaddress 5Dh		
D7-D6	PWTHD [CP-CD]	**Selection Of 'Peak-White' Threshold** '00': 448 '01': 470 '10': 500 <u>'11': 511</u>
D5-D4	CLRANGE [CP-CD]	**Chroma lock-range** <u>'00': ± 425 Hz</u> '01': ± 463 Hz '10': ± 505 Hz '11': ± 550 Hz
D3-D2	LMOFST [CP-CD]	**Luminance Offset in color decoder during visible picture** <u>'00': no offset</u> '01': −32 LSB (−7.5 IRE) '10':+32 LSB (+7.5 IRE) '11': −16 LSB (−3.75 IRE) *Note: A 7.5 IRE offset is added during blanking in display processing. When choosing '10', the luminance offset is equal to the offset of the CVBS input as in both picture and blanking the same 7.5 IRE offset is used.*
D1	VDETIFS [CP-CD]	**Vertical Sync-Detection Slope** <u>'0': normal</u> '1': slow

Table 3–8: I^{2}C bus command description, continued

Bit	Name	Description
Subaddress 5Eh		
D7-D6	SDR [CP-CD]	**Secam Dr adjustment** 00: 191 <u>01: 194</u> 10: 197 11: 200
D5-D0	CHRF [CP-CD]	**Chroma Bandwidth** selects chroma bandwidth <u>'011100': nominal bandwidth</u>
Subaddress 5Fh		
D7	COMB [CP-CD]	**Delay Line** <u>'0': use delay line</u> '1': do not use delay line (only suited for NTSC)
D6-D0	CSTAND [CP-CD]	**Color Standard Assignment** '0000000': no color standard chosen '0000001': PAL N '0000010': PAL B '0000100': SECAM '0001000': PAL 60 '0010000': PAL M '0100000': NTSC M '1000000': NTSC 44 For allowed combinations please refer to chapter (see Section 2.1.5. on page 9) <u>'1100110': PALB/SECAM/NTSCM/NTSC44/PAL60</u>
Subaddress 60h		
D7-D0	CKILL [CP-CD]	**Chroma Level For Color Off (PAL/NTSC)** '00000000': high burst amplitude <u>'01000000': default</u> '11111111': low burst amplitude
Subaddress 61h		
D7-D0	CKILLS [CP-CD]	**Chroma Level For Color Off (SECAM)** '00000000': low burst amplitude <u>'01000000': default</u> '11111111': high burst amplitude

Aug. 16, 2004; 6251-552-1DS   **Micronas**

Table 3–8: I^{2}C bus command description, continued

Bit	Name	Description
Subaddress 62h		
D7-D6	VPOL [CP-CD]	**V Polarity at VINP** '<u>00': use Vsync</u> '01': use inverted Vsync '10': autodetect polarity '11': (reserved)
D5	LPPOST [CP-CD]	**Additional Filtering of Luminance** '<u>0': no filtering</u> '1': filtering
D4-D0	YCDEL [CP-CD]	**Luminance Delay** '10000': 800 ns '<u>0000': no delay</u> '01111': −700 ns
Subaddress 63h		
D7-D0	HUE [CP-CD]	**Hue Control (Tint)** '10000000': −89° '<u>00000000': 0°</u> '01111111': +88°
Subaddress 64h		
D7-D0	NTSCREF [CP-CD]	**ACC Reference Adjustment (NTSC)** '00000000': low reference value '<u>10100101': nominal value</u> '11111111': high reference value
Subaddress 65h		
D7-D0	PALREF [CP-CD]	**ACC Reference Adjustment (PAL)** '00000000': low reference value '<u>01011111': nominal value</u> '11111111': high reference value
Subaddress 66h		
D7-D6	SLLTHD [CP-CD]	**Slicing Level Threshold H** '<u>00': no offset</u> '01': small negative '10': small positive '11': large positive (adaptive)
D5-D0	SCADJ [CP-CD]	**Subcarrier Adjustment** '000000': −262 ppm '<u>001111': 0 ppm</u> '111111': 840 ppm

Table 3–8: I^{2}C bus command description, continued

Bit	Name	Description
Subaddress 67h		
D7-D6	AGCMD [CP-CD]	**AGC method** '00': sync amplitude and peak white '01': sync amplitude only '10': peak white only '11': fixed to value AGCADJ1
D5-D0	AGCADJ1 [CP-CD]	**Automatic Gain Adjustment ADC1** '000000': 0.6 V input signal '111111': 1.8 V input signal
Subaddress 68h		
D7	AGCRES [CP-CD]	**AGC reset** '0': no reset '1': reset
D6	AGCFRZE [CP-CD]	**freeze AGC (ADC_CVBS)** '0': normal operation '1': freeze AGC at current value
D5-D0	AGCADJ2 [CP-CD]	**Automatic Gain Adjustment ADC2** '000000': 0.6 V input signal '111111': 1.8 V input signal
Subaddress 69h		
D7-D0	CLMPHIGH [CP-CD]	**Vertical End Of Clamping Pulse** Granularity: 2 '00000000': line 256 '00111100': line 376 '11111111': line 766
Subaddress 6Ah		
D7-D4	CVBOSEL1 [CP-CD]	**Output select 1 for pin cvbso1** '0000': CVBS1 '0001': CVBS2 '0010': CVBS3 '0011': CVBS4 or Y1 '0100': CVBS5 or C1 '0101': CVBS6 or Y2 '0110': CVBS7 or C2 '0111': Y1 + C1 '1000': Y2 + C2
D3-D0	CLMPLOW [CP-CD]	**Vertical Start Of Clamping Pulse** '0000': line 0 '0011': line 6 '1111': line30

Table 3–8: I^{2}C bus command description, continued

Bit	Name	Description
Subaddress 6Bh		
D7	FLINE [CP-CD]	**Mode Selection** '0': interlace input '1': progressive input
D6	FLDINV [CP-CD]	**Field Inversion** '0': no inversion '1': inversion
D5	CLPSTGY [CP-CD]	**Clamping strategy** '0': back-porch clamping '1': sync-tip-clamping
D4	YCSEL [CP-CD]	**Y/C select** '0': CVBS input '1': Y/C input
D3-D0	CLMPD1 [CP-CD]	**Measurement duration ADC1** Granularity: 200 ns '0000': 0 μs '0111': 1.4 μs '1111': 3 μs
Subaddress 6Ch		
D7-D6	HPOL [CP-CD]	**H Polarity at HINP** '00': use Hsync '01': use inverted Hsync '10': autodetect polarity '11': (reserved)
D5	FHDET [CP-CD]	**Automatic Multisync capability** '0': disabled '1': enabled
D4	DISCHCH [CP-CD]	**Channel-change signal for color decoder** '0': color-decoder not reset after channel-change '1': color-decoder reset after channel-change
D3-D0	CLMPD2 [CP-CD]	**Measurement duration ADC2** Granularity: 200 ns '0000': 0 μs '0111': 1.4 μs '1111': 3 μs

Table 3–8: I^{2}C bus command description, continued

Bit	Name	Description
Subaddress 6Dh		
D7	NOSIGB [CP-CD]	**No signal behavior** '0': noisy screen when out of sync '1': colored background insertion instead
D6	HINP [CP-CD]	**Horizontal Pulse Detection** '0': from CVBS ADC1 '1': from RGBF ADC
D5-D0	CLMPST1 [CP-CD]	**Measurement start ADC1** '000000': 0 μs '011100': 5.6 μs '111111': 12.8 μs
Subaddress 6Eh		
D7-D6	PLLTC [CP-CD]	**Time constant HPLL (VCR...TV)** '00': very fast '01': fast '10': slow '11': very slow
D5-D0	CLMPST2 [CP-CD]	**Measurement start ADC2** '000000': 0 μs '011100': 5.6 μs '111111': 12.8 μs
Subaddress 6Fh		
D7-D4	CVBSEL2 [CP-CD]	**Input select for ADC2** '0000': CVBS1 '0001': CVBS2 '0010': CVBS3 '0011': CVBS4 or Y1 '0100': CVBS5 or C1 '0101': CVBS6 or Y2 '0110': CVBS7 or C2 '0111': Y1 + C1 '1000': Y2 + C2 '1111': disabled
D3-D0	CVBSEL1 [CP-CD]	**Input select for ADC1** '0000': CVBS1 '0001': CVBS2 '0010': CVBS3 '0011': CVBS4 or Y1 '0100': CVBS5 or C1 '0101': CVBS6 or Y2 '0110': CVBS7 or C2 '0111': Y1 + C1 '1000': Y2 + C2 '1111': disabled

Table 3–8: I^{2}C bus command description, continued

Bit	Name	Description
Subaddress 70h		
D7-D4	CVBOSEL2 [CP-CD]	**Output select for pin cvbso2** '0000': CVBS1 '0001': CVBS2 '0010': CVBS3 '0011': CVBS4 or Y1 '0100': CVBS5 or C1 '0101': CVBS6 or Y2 '0110': CVBS7 or C2 '0111': Y1 + C1 '1000': Y2 + C2
D3-D0	CVBOSEL3 [CP-CD]	**Output select for pin cvbso3** '0000': CVBS1 '0001': CVBS2 '0010': CVBS3 '0011': CVBS4 or Y1 '0100': CVBS5 or C1 '0101': CVBS6 or Y2 '0110': CVBS7 or C2 '0111': Y1 + C1 '1000': Y2 + C2
Subaddress 71h		
D7-D0	FHFRRN [CP-CD]	**Free Running Frequency Of Horizontal PLL** '00000000': 384 clocks (52.7 kHz) '11100100': 1296 clocks (15.625 kHz) '11111111': 1404 clocks (14.423 kHz)

Table 3–8: I^{2}C bus command description, continued

Bit	Name	Description
Subaddress 72h		
D7	REFTRIMEN [CP-CD]	**Reference Value enable** '0': use fuses '1': uses programmed value
D6	SATNR [CP-CD]	**Noise reduction for satellite signal** '0': disabled '1': enabled
D5	VINP [CP-CD]	**Vertical Pulse Detection** '0': from CVBS signal '1': from V-input pin
D4-D3	NSRED1-0 [CP-CD]	**Noise Reduction For Horizontal PLL** '000': 1/16 '001': 1/8 '010': 1/4 '011': 1/2 '100': 1 '101': 2 '110': 4 '111': 8 MSB is at address 7Eh, D2
D2-D0	LPCDEL [CP-CD]	**Window Shift For Fine Error Calculation** '100': −4 clock cycles '000': no offset '011': +3 clock cycles
Subaddress 73h		
D7-D0	VSHIFT [CP-CD]	**Field Detection Window Shift** '00000000': no shift '11111111': shifted by 2048
Subaddress 74h		
D7	PALIDL1 [CP-CD]	**PAL/NTSC Identification Level 1** '0': less sensitive (192) '1': more sensitive (64)
D6-D0	VTHRL50 [CP-CD]	**Vertical Window Noise Suppression Opening** Opening= 4*$VTHRL50$ 0000000: opening in first line 1111111: opening in line 508
Subaddress 75h		
D7	PALIDL0 [CP-CD]	**PAL/NTSC Identification Level 0** '0': less sensitive '1': more sensitive
D6-D0	VTHRH50 [CP-CD]	**Vertical Window Noise Suppression Closing** Closing= 312+4*$VTHRH50$ 0000000: closing in line 312 1111111: closing in line 820 When VINP (72h) is set, 50 Hz values are taken for opening and closing values.

Table 3–8: I^{2}C bus command description, continued

Bit	Name	Description
Subaddress 76h		
D7-D0	REFTRIM [CP-CD]	**Reference Value Bandgap** '01000000': low reference <u>'00000000': medium reference</u> '01111111': high reference '1XXXXXXX': reference disabled, resistor used
Subaddress 77h		
D7-D4	REFTRIMCV [CP-CD]	**Reference Value ADC CVBS (antialiasfilter)** <u>'0000': narrow</u> '1111': wide
D3-D0	REFTRIMRGB [CP-CD]	**Reference Value ADC RGBF (antialiasfilter)** <u>'0000': narrow</u> '1111': wide
Subaddress 78h		
D7	SLLTHDVP [CP-CD]	**Vertical Slicing Level Threshold Polarity** <u>'0': positive</u> '1': negative
D6	THRSEL [CP-CD]	**H Slicing level threshold** <u>'0': 50 %</u> '1': 37 %
D5-D0	CLMPST1S [CP-CD]	**Clamping start for ADC1** '000000': 0 μs <u>'011100': 5.6 μs</u> '111111': 12.8 μs
Subaddress 79h		
D7-D6	SCMIDL [CP-CD]	**SECAM identification level** <u>'00': 128</u> '01': 64 '10': 96 '11': 80
D5-D0	CLMPST2S [CP-CD]	**Clamping start ADC2** '000000': 0 μs <u>'011100': 5.6 μs</u> '111111': 12.8 μs

Table 3–8: I^{2}C bus command description, continued

Bit	Name	Description
Subaddress 7Ah		
D7-D3	ACCLIM [CP-CD]	**ACC-limitation for weak signals** '00000': strong limitation '<u>11111': no limitation</u>
D2-D0	IFCOMP [CP-CD]	**IF compensation filter** '000': pal prefiltering '001': pal prefiltering + IF '010': prefiltering '011': IF 6dB '<u>100': flat</u> *Note: '000' or '001' are not suited for 3.58 MHz subcarrier color standards (PAL M, PAL N, NTSC M)*
Subaddress 7Bh		
D7-D4	CLMPD2S [CP-CD]	**Clamping duration for ADC2** Granularity: 200 ns '0000': 0 μs '<u>0111': 1.4 μs</u> '1111': 3.0 μs
D3-D0	CLMPD1S [CP-CD]	**Clamping duration for ADC1** Granularity: 200 ns '0000': 0 μs '<u>0111': 1.4 μs</u> '1111': 3.0 μs
Subaddress 7Ch		
D5	EIA770 [CP-CD]	**EIA 770 support** '<u>0': standard TV signals expected</u> '1': progressive signals expected timing according to EIA 770.1 or EIA 770.2 when '1'
D4	SHAPERDIS [CP-PP]	**Power Down Of Crystal Oscillator Shaper** '<u>0': normal operation</u> '1': power down active
D3	OSCPD [CP-PP]	**Power Down Of Crystal Oscillator Amplifier** '<u>0': normal mode</u> '1': power down mode
D2	TSTSHAPERI [CP-PP]	**Testmode Control Of Crystal Oscillator** '<u>0': normal operation (shaper active)</u> '1': external clock input (shaper replaced)
D1-D0	FREQSEL [CP-PP]	**Amplifier Current Setting Of Oscillator Pad** '00': 100 μA '01': 590 μA '<u>10': 235 μA</u> '11': 1730 μA

Table 3–8: I^{2}C bus command description, continued

Bit	Name	Description
Subaddress 7Dh		
D6-D4	BELLFIR [CP-CD]	**Bell filter FIR component** '000': −116 '001': −113 '010': −110 '011': −108 '100': −106 '101': −104 '110': −102 '111': −100
D3-D1	BELLIIR [CP-CD]	**Bell filter IIR component** '000': 8 '001': 9 '010': 10 '011': 11 '100': 12 '101': 13 '110': 14 '111': 16
D0	VFLYWHL [CP-CD]	**Vertical Flywheel** '0': disabled '1': enabled
Subaddress 7Eh		
D7-D6	FLNSTRD [CP-CD]	**Force line standard at CVBS/RGB frontend** '00': automatic '01': force 50 Hz '10': force 60 Hz '11': (reserved)
D5	ENLIM [CP-CD]	**Enable limiter** '0': disabled '1': enabled
D4-D3	ISHFT [CP-CD]	**I-adjustment for horizontal PLL** '00': *1 '01': *2 '10': *4 '11': *8
D2	NSRED2 [CP-CD]	Belongs to 72h
D1-D0	VLP [CP-CD]	**Lowpass for vertical sync-separation** '00': none '01': weak '10': medium '11': strong

Table 3–8: I^{2}C bus command description, continued

Bit	Name	Description
Subaddress 7Fh		
D7	SECACC [CP-CD]	**Secam acceptance** '0': disabled '1': enabled
D6	SECDIV [CP-CD]	**Secam Divider** '0': divide by 4 '1': divide by 2
D5-D4	SECINC1 [CP-CD]	**Secam increment 1** '00': 2 '01': 3 '10': 4 '11': 5
D3-D2	SECINC2 [CP-CD]	**Secam increment 2** '00': 1 '01': 2 '10': 3 '11': 4
D1-D0	SCMREL [CP-CD]	**Secam rejection level** '00': 320 '01': 384 '10': 352 '11': 1024

Table 3–8: I^{2}C bus command description, continued

Bit	Name	Description
Subaddress 80h		
D7	PORCNCL [CP-CD]	**Reset control bit cancel** '0': no operation '1': reset **POR** bit (8Ch) after use, **PORCNCL** must be set to '0' again
D6-D4	NTCHSEL [CP-CD]	**Luminance Notch selection** '000': sharp notch '001': medium 1 '010': medium 2 '011': broad notch '100': broad steep notch (PAL, SECAM only)
D3	CPLLRES [CP-CD]	**Force Chroma PLL reset** '0': no reset '1': reset chroma PLL after use, **CPLLRES** must be set to '0' again
D2	DISALLRES [CP-CD]	**Disable all chroma resets** '0': resets allowed '1': resets disabled may only be used if ONE color standard is selected
D1	TRAPBLU [CP-CD]	**Notchfrequency for 4,250 MHz** '0': 4.25 MHz '1': 4.2 MHz has only effect in SECAM mode
D0	TRAPRED [CP-CD]	**Notchfrequency for 4,406 MHz** '0': 4.406 MHz '1': 4.356 MHz has only effect in SECAM mode

Table 3–8: I^{2}C bus command description, continued

Bit	Name	Description
Subaddress 80h		
D7	PORCNCL [CP-CD]	**Reset control bit cancel** '0': no operation '1': reset **POR** bit (8Ch) after use, **PORCNCL** must be set to '0' again
D6-D4	NTCHSEL [CP-CD]	**Luminance Notch selection** '000': sharp notch '001': medium 1 '010': medium 2 '011': broad notch '100': broad steep notch (PAL, SECAM only)
D3	CPLLRES [CP-CD]	**Force Chroma PLL reset** '0': no reset '1': reset chroma PLL after use, **CPLLRES** must be set to '0' again
D2	DISALLRES [CP-CD]	**Disable all chroma resets** '0': resets allowed '1': resets disabled may only be used if ONE color standard is selected
D1	TRAPBLU [CP-CD]	**Notchfrequency for 4,250 MHz** '0': 4.25 MHz '1': 4.2 MHz *Note: has only effect in SECAM mode*
D0	TRAPRED [CP-CD]	**Notchfrequency for 4,406 MHz** '0': 4.06 MHz '1': 4.356 MHz *Note: has only effect in SECAM mode*

Table 3–8: I^{2}C bus command description, continued

Bit	Name	Description
Subaddress 81h		
D7	ADLCK [CP-CD]	**Additional lock-detection** '0': no used '1': used
D6	ADLCKSEL [CP-CD]	**Additional lock-detection selection** '0': PALID '1': PALDET
D5	ADLCKCC [CP-CD]	**Additional lock-detection color-killer** '0': do not use lock signal '1': use lock-signal
D4-D3	VFLYWHLMD[CP-CD]	**Vertical Flywheel Mode** '00': CHECK FOR CORRECT STANDARD '01': 3 lines deviation allowed '10': 4 lines deviation allowed, no check for interlace '11': 5 lines deviation allowed, no check for interlace
D2-D0	SECACCL [CP-CD]	**Secam Acceptance level** '000': 100 '001': 84 '010': 64 '011': 32 '100': 70 '101': 76 '110': 90 *Note: must be enabled by* **SECACC** *(7Fh) to have an effect*

Table 3–8: I^{2}C bus command description, continued

Bit	Name	Description
Subaddress 82h (no auto-increment)		
D7-D6	SYNCFTHD [CP-CD]	**SYNCF threshold** 00: 4 lines 01: 3 lines 10: 2 lines 11: 1 line
D5	IFCOMPSTR [CP-CD]	**2nd IF compensation filter** '0': disabled '1': enabled
D4	PALIDL2 [CP-CD]	**PAL/NTSC identifikation level 2** '0': less sensitive '1': more sensitive
D3	CPLLOF [CP-CD]	**Chroma PLL Open** '0': normal operation '1': chroma PLL opened
D2	DEEMPSTD [CP-CD]	**Deemphase Filtering For Standard Detection** '0': weak '1': strong
D1	PALINC1 [CP-CD]	**PAL/NTSC Detection: Increment 1** '0': +3 '1': +2
D0	PALINC2 [CP-CD]	**PAL/NTSC Detection: Increment 2** '0': −1 '1': −2 do not use PALINC2=1 in combination with PALINC1=1
Subaddress 83h (Read-only)		
D0	FBLACTIVE [CP-I2C]	**Activity At FBL Input** '0': no activity '1': activity reset automatically when read
Subaddress 84h (Read-only, no auto-increment))		
D6-D0	NOISEME [FP-TNR]	**Noise level of the input signal** 0000000: no noise 1111110: strong noise 1111111: strong noise or measurement failed *Note: no autoincrement possible*

 Micronas

Table 3–8: I^{2}C bus command description, continued

Bit	Name	Description
Subaddress 85h (Read-only)		
D5	LBSTATUS [FP-TNR]	**Status bit for letter box detection:** 0: No new value available 1: New value from Letter Box Detection available *Note: reset automatically when read*
D4	PFBL [FP-TNR]	**Indicates Overflow at FBL Input** '0': no overflow '1': overflow *Note: reset automatically when read*
D3	PG [FP-TNR]	**Indicates Overflow at GREEN Input** '0': no overflow '1': overflow *Note: reset automatically when read*
D2	PB [FP-TNR]	**Indicates Overflow at BLUE Input** '0': no overflow '1': overflow *Note: reset automatically when read*
D1	PR [FP-TNR]	**Indicates Overflow at RED Input** '0': no overflow '1': overflow *Note: reset automatically when read*
D0	NMSTATUS [FP-TNR]	**Indicates New Value of the Noise Measurement** 0: NOISEME has not been updated 1: New value of NOISEME available <u>Note: reset automatically when read</u>
Subaddress 86h (Read-only)		
D0	STABLL [PP]	**Shows LL-HPLL Lock Status** '0': LL_HPLL is not locked '1': LL_HPLL is locked
Subaddress 87h (Read-only)		
D1-D0	SMMIRROR [BP-O/M]	**Operation mode for scan rate conversion:** '00': AABB (Raster $\alpha\alpha\beta\beta$) '01': AAAA (Raster $\alpha\alpha\alpha\alpha$) '10': AAAA (Raster $\alpha\beta\alpha\beta$) '11': BBBB (Raster $\beta\beta\beta\beta$)

Table 3–8: I^{2}C bus command description, continued

Bit	Name	Description
Subaddress 88h (Read-only)		
D7	DETHPOL [CP-CD]	**Detected Polarity Of HSync** '0': negative '1': positive
D6	DETVPOL [CP-CD]	**Detected Polarity Of V Sync** '0': negative '1': positive
D5-D3	STDET [CP-CD]	**Detected Color Standard** '000': non standard or standard not detected '001': NTSC M '010': PAL M '011': NTSC44 '100': PAL60 '101': PAL N '110': SECAM '111': PAL B/G
D2	SCOUTEN [CP-CD]	**SCDEV valid indication** '0': SCDEV not valid '1': SCDEV valid
D1	PALID [CP-CD]	**PAL identification (algorithm 1)** '0': not PAL '1': PAL
D0	CKSTAT [CP-CD]	**Colorkill status** '0': color off '1': color on
Subaddress 89h (Read-only)		
D7	LNSTDRD [CP-CD]	**Line Standard detection** '0': 60 Hz '1': 50 Hz
D6	INT [CP-CD]	**Interlace Detection** '0': progressive input '1': interlace input
D5-D0	SCDEV [CP-CD]	**Deviation Of Clock System or Color Carrier** '100000': max. negative deviation '000000': no deviation '011111': max. positive deviation
Subaddress 8Ah (Read-only)		
D7-D0	LPFLD [CP-CD]	**Nr. of lines per field for input signal** lines= 256+**LPFLD***2 '00000000': 256 lines or less '11111111': 766 lines or more

Table 3–8: I^{2}C bus command description, continued

Bit	Name	Description
Subaddress 8Bh (Read-only)		
D7-D0	NRPIXEL [CP-CD]	**Pixel number of input signal** Granularity: 4 '00000000': 384 or less '11111111': 1404 or more PIXEL=4*__NRPIXEL__+384
Subaddress 8Ch (Read-only)		
D7	POR [CP-CD]	**Reset indication** a reset at pin 24 (reset) sets **POR**. **POR** is reset with **PORCNCL** (80h) '0': no reset appeared '1': reset appeared
D3	VFLYMD [CP-CD]	**Vertical Flywheel mode locked** 0: unlocked 1: locked **VFLYWHL** must be enabled to give a result
D2	STAB [CP-CD]	**Status of horizontal synchronization** '0': sync separation not locked '1': sync separation locked and stable
D0	PALDET [CP-CD]	**PAL identification (algorithm 2)** '0': not PAL '1': PAL
Subaddress 8Dh (Read-only)		
D7-D0	REFTRIMRD [CP-CD]	**Reference Value Bandgap** '01000000': low reference '00000000': medium reference '01111111': high reference '1XXXXXXX': reference disabled, resistor used *Note: contains fused value only when REFTRIMEN (72h)=0.*
Subaddress 8Eh (Read-only)		
D7-D4	REFTRIMCVRD [CP-CD]	**Reference Value CVBS ADC** '0000': narrow '1111': wide *Note: contains fused value only when REFTRIMEN (72h)=0.*
D3-D0	REFTRIMRGBRD [CP-CD]	**Reference Value RGB ADC** '0000': narrow '1111': wide *Note: contains fused value only when REFTRIMEN (72h)=0.*

Table 3–8: I²C bus command description, continued

Bit	Name	Description
Subaddress 8Fh (Read-only, <u>NOT</u> compatible to 940X family)		
D3	SLS [CP-I2C]	**Line Standard At Device Output** '0': 100 Hz (VSP 9402A, VSP 9412A) '1': 50 Hz (VSP 9432A, VSP 9442A)
D2-D0	VERSION [CP-I2C]	**Version Of VSP 94XX Family** '001': VSP 94x5B '010': VSP 94x2A '011': VSP 94x7B '101': VSP 94x9C others: reserved
Subaddress 90h (Read-only)		
D7	AM50O [CP-I2C]	**Last detected Standard 50 Hz** '0': PAL or none '1': SECAM
D6	AM60O [CP-I2C]	**Last detected Standard 60 Hz** '0': NTSC M or none '1': NTSC44 or PAL60
D5-D0	AGCADJCV [CP-I2C]	**AGC value for ADC1** 000000: smallest input range 111111: biggest input range
Subaddress 91h (Read-only)		
D6-D0	VLENGTH [CP-I2C]	**Length of vertical pulse** 0000000: short v 1111111: long v
Subaddress 92h (Read-only)		
D7-D0	MINV [CP-I2C]	**Measured sync amplitude** 00000000: smallest sync 11111111: largest sync
Subaddress 93h (Read-only)		
D4-D0	PWADJCNT [CP-I2C]	**Peak White adjust counter** 00000: no PW reduction 11111: largest PW reduction
Subaddress 96h (Read-only)		
D0	V40STAT [FP-I2C]	**V Status bit of 40.5 MHz domain** '0': New write or read cycle can start '1': No new write or read cycle can start
Subaddress 98h (Read-only)		
D0	V36BSTAT [BP-I2C]	**V Status bit of backend 36 MHz domain** '0': New write or read cycle can start '1': No new write or read cycle can start

Table 3–8: I^{2}C bus command description, continued

Bit	Name	Description
Subaddress 99h (Read-only)		
D0	V20STAT [CP-I2C]	**V Status bit of 20.25 MHz domain** '0': New write or read cycle can start '1': No new write or read cycle can start
Subaddress A0h		
D7-D4	KPNL [PP]	**Proportional factor for loop filter if HPLL is not locked same values as in locked condition (KPL)**
D3-D0	KPL [PP]	**Proportional factor for loop filter if HPLL is locked**) <u>00000</u>: 0 00001: 1 00010: 2 00011: 4 00100: 8 00101: 16 00110: 32 00111: 64 01000: 128 01001: 256 01010: 512 01011: 1024 01100: 2048 01101: 4096 01110: 8192 01111:16384 10000: 0.5 10001: 1.5 10010: 2.5 10011: 3 10100: 3.5 10101: 4.5 10110: 5 10111: 6 11000: 7

Table 3–8: I^{2}C bus command description, continued

Bit	Name	Description
Subaddress A1h		
D7-D4	KINL [PP]	**Integrational factor for loop filter if HPLL is not locked** same values as in locked condition (KIL)
D3-D0	KIL [PP]	**Integrational factor for loop filter if HPLL is locked** <u>00000</u>: 0 00001: 1 00010: 2 00011: 4 00100: 8 00101: 16 00110: 32 00111: 64 01000: 128 01001: 256 01010: 512 01011: 1024 01100: 2048 01101: 4096 01110: 8192 01111:16384 10000: 0.5 10001: 1.5 10010: 2.5 10011: 3 10100: 3.5 10101: 4.5 10110: 5 10111: 6 11000: 7
Subaddress A2h		
D7-D0	LIMIP [PP]	**Limiter Control for P-part for increased dynamic range** LIMIT_P= ±16*LIMIP '00000000': ±0 '11111110': ±4064 '<u>11111111</u>': <u>no limitation</u>
Subaddress A3h		
D7-D0	LIMII [PP]	**Limiter Control for I-part for increased dynamic range** LIMIT_I= ±16*LIMII '00000000': ±0 '11111110': ±4064 '<u>11111111</u>': <u>no limitation</u>

Table 3–8: I^{2}C bus command description, continued

Bit	Name	Description
Subaddress A4h		
D7	KPNL4 [PP]	Refer to A0h
D6	KPL4 [PP]	Refer to A0h
D5	KINL4 [PP]	Refer to A1h
D4	KIL4 [PP]	Refer to A1h
D3-D0	LIMLR [PP]	**Limit LL-PLL lock-in range** 0000: full lock-in range of ±5.85 % 0001: lock in range limited to ±3.8 % 0010: lock in range limited to ±2.55 % 0011: lock in range limited to ±1.27 % 0100: ock in range limited to ±0.63 % 0101: lock in range limited to ±0.32 % 0110: lock in range limited to ±0.19 % 0111: lock in range limited to ±0.13 % 1000: lock in range limited to ±5 % 1001: lock in range limited to ±4.5 % 1010: lock in range limited to ±3.1 % 1011: lock in range limited to ±2.1 % 1100: lock in range limited to ±1.5 % 1101: lock in range limited to ±1 % 1110: (reserved) 1111: (reserved)
Subaddress B0		
D6-D5	AGCTHD [CP-CD]	**AGC hysterisys** 00: broad 01: medium 1 10: medium 2 11: small
D4-D0	FEMAG [CP-CD]	**Fine Error characteristic** 00000: smallest gain 10000: default (equal to A32 version) 11111: largest gain

Table 3–8: I^{2}C bus command description, continued

Bit	Name	Description
Subaddress B1		
D6-D4	SLLTHDV [CP-CD]	**Slicing Level Threshold V** '000': no offset '001': 4 '010': 8 '011':12 '101': adaptive (limited to ±4) '110': adaptive (limited to ±8) '111': adaptive (limited to ±12) polarity is selected by **SLLTHDVP** (78h)
D3-D2	AMSTD60 [CP-CD]	**Automatic standard detection priority 60 Hz** 00: NTSC M 01: NTSC44/PAL60 10: (reserved) 11: automatic
D1-D0	AMSTD50 [CP-CD]	**Automatic standard detection priority 50 Hz** 00: PAL B 01: SECAM 10: (reserved) 11: automatic
Subaddress B2		
D7-D6	SDB [CP-CD]	**Secam Db adjustment** 00: −55 01: −58 10: −61 11: −64
D4	MVPG [CP-CD]	**Vertical Pulse gating** 0: disabled 1: enabled
D3	MVP [CP-CD]	**Vertical length measurement with vertical pulse detection** 0: disabled 1: enabled
D2-D0	VDETITC [CP-CD]	**Vertical Detection Integration Time Constant** 000: 400 clock cycles 001: 375 clock cycles 010: 350 clock cycles 011: 300 clock cycles 100: 250 clock cycles 101: 225 clock cycles 110: 200 clock cycles 111: automatic
Subaddress B3		
D6-D0	VTHRL60 [CP-CD]	**Vertical Window Noise Suppression Opening** Opening=4***VTHRL60M** 0000000: opening in first line 1111111: opening in line 508

Table 3–8: I^{2}C bus command description, continued

Bit	Name	Description
Subaddress B4		
D6-D0	VTHRH60 [CP-CD]	**Vertical Window Noise Suppression Closing** Closing=262+4*$\textbf{VTHRH60M}$ <u>0000000: closing in line 262</u> 1111111: closing in line 770
Subaddress B5		
D7-D5	DEEMPIIR [CP-CD]	**Deemphase filter IIR component** '000': 5 <u>'001': 6</u> '010': 7 '011': 8 '100': 9 '101': 10 '110': (reserved) '111': (reserved)
D3-D0	DEEMPFIR [CP-CD]	**Deemphase filter FIR component** '0000': 16 <u>'0101': 21</u> '1111': 31
Subaddress B7		
D7-D0	NAPPLIPI [FP-RGB]	**Not active pixels from HSYNC to input data for ITU** Delay=$\textbf{NAPPLIPI}$ * 2 + $\textbf{NAPIPPHI}$
Subaddress B8		
D7-D0	ALPFIPI [FP-RGB]	**Active lines per field for ITU** Active lines=ALPFIPI * 2 <u>(int) 144: 288 active lines</u>
Subaddress B9		
D7-D0	APPLIPI [FP-RGB]	**Active pixels per line for ITU** Active pixels=$\textbf{APPLIPI}$ * 2 <u>(int) 360=720 lines</u>
Subaddress BA		
D7	APPLIPI[8] [FP-RGB]	**Active pixels per line for ITU** Active pixels=$\textbf{APPLIPI}$ * 2 <u>(int) 360=720 lines</u>
D6	NALPFIPI [FP-RGB]	**Not active lines per field for ITU** <u>(int) 20= 20 lines</u>
Subaddress BCh		
D7-D0	FRINC18-11 [PP]	**Set HDTO freerunning frequency** Granularity=103 Hz 33981_d (minimum: nominal pixel clock= 3.5 MHz) <u>349525_d (nominal pixel clock= 36 MHz)</u> 388362_d (maximum: nominal pixel clock= 40 MHz)

Table 3–8: I^{2}C bus command description, continued

Bit	Name	Description
Subaddress BD		
D7-D0	FRINC10-3 [PP]	Belongs to BCh
Subaddress BE		
D2-D0	FRINC2-0 [PP]	Belongs to BCh
Subaddress C0		
D7-D0	HSPPL [FP-RGB]	**Hsync shift** shift=HSPPL * 4 <u>00000000: default</u>
Subaddress C1		
D7	FOFST [FP-RGB]	**Offset of active field at interlaced mode (line offset):** <u>0: NALPFIPI+1 at field A, NALPFIPI at field B</u> 1: NALPFIPI at field A, NALPFIPI+1 at field B
D2-D0	VSLPF [FP-RGB]	**Vsync shift** shift=VSLPF * 4 <u>0000000: default</u>
Subaddress D0		
D7-D6	VBLANDEL [BP-PM]	Refer to D1h
D5	VBLANPOL [BP-PM]	**Vertikal Blank Signal Polarity** <u>0: positive</u> 1: negative
D2	FSWFTL [BP-PM]	**Stability Signal of LL_HPLL** <u>'0': STABLL is generated accoding to **SETSTABLL**</u> '1': STABLL is forced to 1 (hout synchronization enabled)
D1-D0	VBLANLEN [BP-PM]	Refer to D2h
Subaddress D1		
D7-D0	VBLANDEL[7:0] [BP-PM]	**Vertical Delay in lines from vsync to active edge of blank signal:** Blank_start=1***VBLANDEL** <u>'0000000000': no delay</u> '1111111111': 1023 lines delay
Subaddress D2		
D7-D0	VBLANLEN [BP-PM]	**Vertical Length in lines from start of active blank signal:** Blank_length=4***VBLANLEN** <u>'00000000': no line</u> '11111111': 1020 lines
Subaddress E0		
D7-D0	LBGRADDET [FP-RGB]	**Threshold for gradient detected** <u>(int) 50: default</u>

Micronas

Table 3–8: I^{2}C bus command description, continued

Bit	Name	Description
Subaddress E1		
D7-D0	LBVWENDLO [FP-RGB]	**Vertical measure window lower end** (int) 150: default, [in lines (*2) related to VSYNC]
Subaddress E2		
D7-D0	LBHWEND [FP-RGB]	**Horizontal measure window end** (int) 180: default, [in active pixels (*4) related to HSYNC]
Subaddress E3		
D7-D0	LBHIWHITE [FP-RGB]	**Histogram white** (int) 50: default
Subaddress E4		
D7-D0	LBHISTBLA [FP-RGB]	**Histogram black** (int) 25: default
Subaddress E5		
D7	LBMASLA [FP-RGB]	Set to 1
D6-D0	LBVWSTLO [FP-RGB]	**Vertical measure window lower start** (int) 96: default], [in lines (*2) related to VSYNC]
Subaddress E6		
D7	LBFS [FP-RGB]	**Field subsampling mode** 0: A+B fields 1: only A field
D6-D0	LBVWENDUP [FP-RGB]	**Vertical measure window upper end** (int) 73: default], [in lines (*2) related to VSYNC]
Subaddress E7		
D7	LBVISUON [FP-RGB]	**Visualisation of letter box results** 0: disabled 1: enabled
D6-D0	LBHWST [FP-RGB]	**Horizontal measure window start** (int) 36: default, [in active pixels (*4) related to HSYNC]
Subaddress E8		
D5-D0	LBVWSTUP [FP-RGB]	**Vertical measure window upper start** (int) 20: default], [in lines (*2) related to VSYNC]

Table 3–8: I^{2}C bus command description, continued

Bit	Name	Description
Subaddress E9		
D7	LBSTABILITY [FP-RGB]	**Stability flag** 0: continuous format update 1: Format update only once
D6	LB43SENS [FP-RGB]	**Sensitivity to 4:3 switch** 0: off 1: on
D5	LBNGFEN [FP-RGB]	**No gradient found** 0: disabled 1: enabled
D4-D0	LBTHDNBNG [FP-RGB]	**Threshold for darkness-brightness, gradient only** (int) 15: default]
Subaddress EA		
D7-D6	LBSUB [FP-RGB]	**Subsampling mode** 0x: 13.5 MHz (1, e.g. digital 656 input) 10: 20.25 MHz source (1.5, for CVBS, YUV and RGB) 11: 40.5 MHz source (3)
D5	LBGRADRST [FP-RGB]	**Reset of gradient method** 0: no reset 1: reset
D4-D0	LBHSDEL [FP-RGB]	**Histogram stability delay** (int)10=default
Subaddress EB		
D4-D0	LBTHDNBNHA [FP-RGB]	**Threshold for darkness-brightness, histogram, activity** (int)30=default
Subaddress EC		
D4-D0	LBACTIVITY [FP-RGB]	**Activity** (int) 5: default]
Subaddress ED		
D4-D0	LBGFBDEL [FP-RGB]	**Gradient fall back delay value** (int) 11: default]
Subaddress EE		
D4-D0	LBGSDEL [FP-RGB]	**Gradient stability delay value** (int) 10: default]
Subaddress EF		
D4-D0	LBASDEL [FP-RGB]	**Activity stability delay** (int) 10: default]

Table 3–8: I^{2}C bus command description, continued

Bit	Name	Description
Subaddress F0 (read only)		
D7	LBELAA [FP-RGB]	Refer to F1h
D6-D0	LBSLAA [FP-RGB]	**Letter box detection: Start line of active area** *LBSLAA* is measured in relation to VSYNC
Subaddress F1 (read only)		
D7-D0	LBELAA [FP-RGB]	**Letter box detection: End line of active area** *LBELAA* is measured in relation to VSYNC
Subaddress F2 (read only)		
D7	LBFORMAT [FP-RGB]	**Letter box detection: Format** 0: 4:3 format 1: other format (letter box)
D6	LBSUBTITLE [FP-RGB]	**Letter box detection: Subtitle flag** 0: no subtitle 1: subtitle available
D5	LBTOPTITLE [FP-RGB]	**Letter box detection: Toptitle flag** 0: no toptitle 1: toptitle available
D4	GRADISSTABLE [FP-RGB]	**Letter box detection: gradient is stable** internal value, only for test purposes
D3	TOPTITLE [FP-RGB]	**LBD: upper area contains high activity** internal value, only for test purposes
D2	SUBTITLE [FP-RGB]	**LBD: lower area contains high activity** internal value, only for test purposes
D1	NOGRADFOUND [FP-RGB]	**LBD: no gradient found** internal value, only for test purposes
D0	SWITCHTO43 [FP-RGB]	**LBD: switch to 4:3 format** internal value, only for test purposes
Subaddress F3 (read only)		
D7	GRADELAA [FP-RGB]	Refer to F4h
D6-D0	GRADSLAA [FP-RGB]	**LBD: Gradient start line of active area** internal value, only for test purposes
Subaddress F4 (read only)		
D7-D0	GRADELAA [FP-RGB]	**LBD: Gradient end line of active area** internal value, only for test purposes

Table 3–8: I^{2}C bus command description, continued

Bit	Name	Description
Subaddress F5 (read only)		
D3	LPBLACK [FP-RGB]	**LBD: lower area contains medium brightness level** internal value, only for test purposes
D2	UPBLACK [FP-RGB]	**LBD: upper area contains medium brightness level** internal value, only for test purposes
D1	LPWHITE [FP-RGB]	**LBD: lower area contains high brightness level** internal value, only for test purposes
D0	UPWHITE [FP-RGB]	**LBD: upper area contains high brightness level** internal value, only for test purposes
Subaddress F6h (Read-only, compatible to 940X family)		
D7-D5	VERSION [CP-I2C]	**Version Of VSP 94xxX Family:** '001': VSP 94x5B '010': VSP 94x2A '011': VSP 94x7B '101': VSP 94x9C others: reserved
D4	SLS [CP-I2C]	**Line Standard At Device Output** '0': 100 Hz (VSP 9402A, VSP 9412A) '1': 50 Hz (VSP 9432A, VSP 9442A)
D3-D1	REV [CP-I2C]	**Revision of VSP94x2A** '000': A23 or below '001': A31 or A32 '010': B13 or B14
Subaddress FEh		
	FE	Any value to this subaddress executes previous I^{2}C protocolls immediately
Subaddress FFh		
	FF	Any value to this subaddress executes previous I^{2}C protocolls according to the take-over-mechanism (dedicated v-pulse, V20, V40, V36)

4. Specifications

4.1. Outline Dimensions

UNIT	L2	Θ
mm	1.60	0°-7°

* does not include dambar protrusion of 0.08 max. per side

UNIT	A	A1	A2	aaa	b	Bd	c	CO	D	D1	E	E1	e	L	L1
mm	2.45 max	0.25 0.00	2.2 1.8	0.25	0.40 0.22	0.13	0.23 0.11	0.10	17.2	14.0	17.2	14.0	0.65	1.03 0.73	0.25

JEDEC STANDARD		ANSI	ISSUE DATE YY-MM-DD	DRAWING-NO.	SPZG-NO.
ISSUE	ITEM NO.				
B	MS-022		03-05-08	06626.0001.4	SPZG001026_001_01
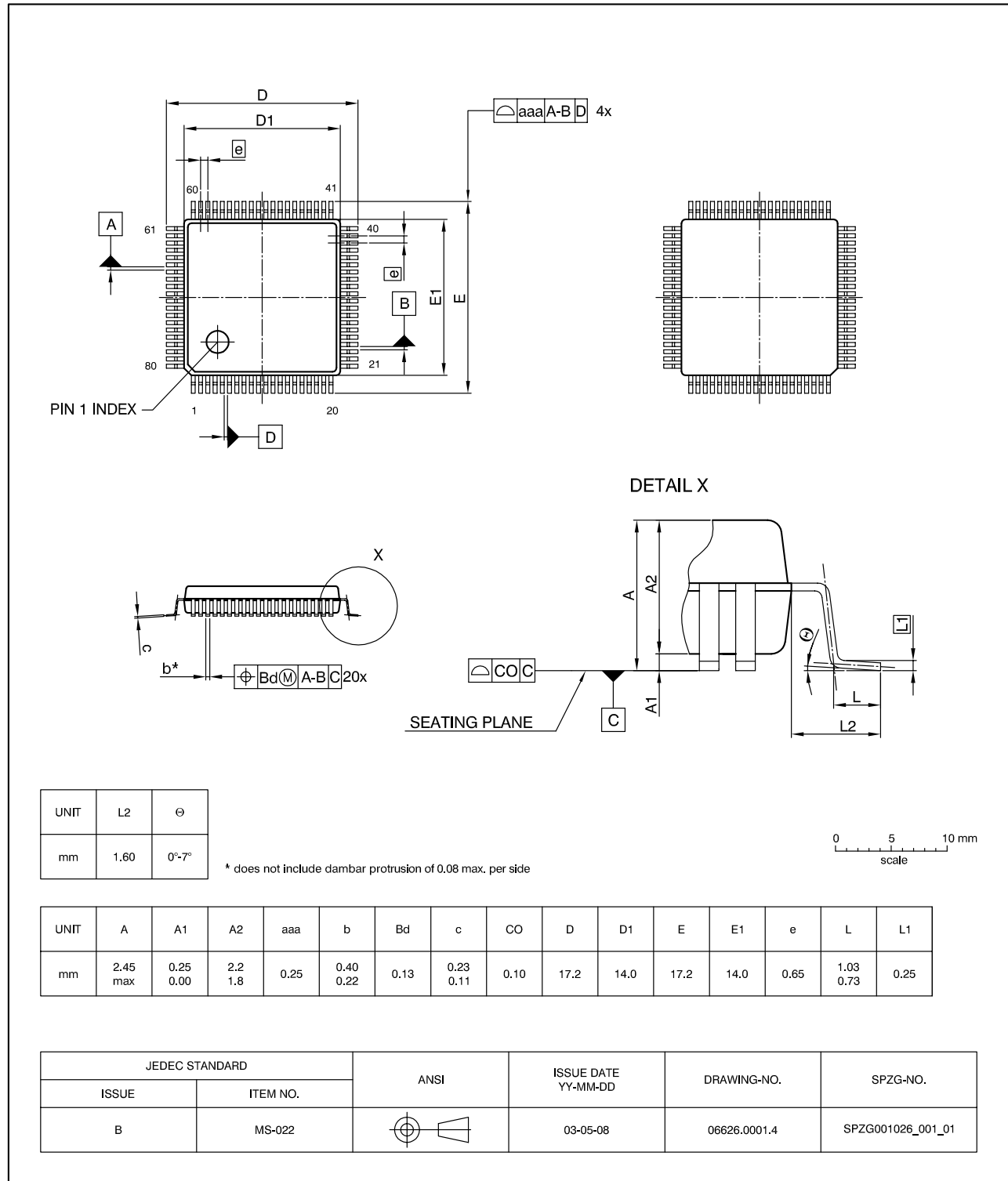
Fig. 4–1:
PMQFP80-1: Plastic **M**etric **Q**uad **F**lat **P**ackage, **80** leads, 14 × 14 × 2 mm^3
Ordering code: VK
Weight approximately 0.96 g

4.2. Pin Connections and Short Descriptions for VSP 9402 and VSP 9412[1]

[1] For VSP 9412, the pin connections differ for pins: 1, 2, 3, 75, 76, 77, 78, 79 ,80 (see Section 4.3. on page 109).

Pin No.	Pin Name	Type	Connection (If not used)	Short Description
1	VDDDACY	S/I		DAC (Y)
2	AYOUT	O/I		Y output
3	VSSDACY	S/I		DAC (Y)
4	VSSD2	S		Supply voltage for digital (0 V digital)
5	VDDD2	S		Supply voltage for digital (1.8 V digital)
6	SDA	I/O		I^{2}C-Bus data
7	TMS	I		Testmode select (Connected to vdd33)
8	656VIN/BLANK[1]	I/O	Connect to Vss and disable blank	Separate V input for 656 / BLANK output
9	656CLK	I/O	Leave open	Digital input / output clock
10	656IO7	I/O	Leave open	Digital input / output (MSB)
11	VSSP2	S		Supply voltage for digital (0 V pad)
12	VDDP2	S		Supply voltage for digital (3.3 V pad)
13	SCL	I		I^{2}C-Bus clk
14	V[2]	I	Connect to Vss	Vertical pulse for RGB input
15	656IO6	I/O	Leave open	Digital input / output
16	656IO5	I/O	Leave open	Digital input / output
17	HOUT	O	Leave open	Horizontal output (Single or double scan, dependent on version)
18	H50[3]	O	Leave open	Hout 50 Hz (with skew)
19	ADR / TDI	I		I^{2}C address / test data in
20	V50[4]	O	Leave open	Vout 50 Hz
21	656IO4	I/O	Leave open	Digital input / output
22	656IO3	I/O	Leave open	Digital input / output
23	VOUT	O	Leave open	Vertical output (Single or double scan, dependent on version)
24	RESET	I		Reset input (Reset when low)
25	VDDP3	S		Supply voltage for digital (0 V pad)
26	VSSP3	S		Supply voltage for digital (3.3 V pad)

Pin No.	Pin Name	Type	Connection (If not used)	Short Description
27	CLKOUT	O	Leave open	Output clock (27 MHz nom.)
28	VDDD3	S		Supply voltage for DRAM (1.8 V digital)
29	VSSD3	S		Supply voltage for digital (0 V digital)
30	656IO2	I/O	Leave open	Digital input / output
31	656IO1	I/O	Leave open	Digital input / output
32	656IO0	I/O	Leave open	Digital input / output (LSB)
33	VSSD4	S		Supply voltage for digital (0 V digital)
34	VDDD4	S		Supply voltage for digital 1.8 V digital
35	VDDAFBL	S		Supply voltage for FBL (1.8 V)
36	VSSAFBL	S		Supply voltage for FBL (0 V)
37	FBL1	I	Connect to Vss	Fast Blank input 1 (H1) (Analog input)
38	FBL2	I	Connect to Vss	Fast Blank input 2 (H2) (Analog input)
39	RIN1	I	Connect to Vss	R or V in1 (Analog input)
40	GIN1	I	Connect to Vss	G or Y in1 (Analog input)
41	BIN1	I	Connect to Vss	B of U in1 (Analog input)
42	VDDARGB	S		Supply voltage for RGB (1.8 V)
43	VSSARGB	S		Supply voltage for RGB (0 V)
44	VDD33RGB	S		Supply voltage RGB (3.3 V)
45	VSS33RGB	S		Supply voltage RGB (0 V)
46	RIN2	I	Connect to Vss	R or V in2 (Analog input)
47	GIN2	I	Connect to Vss	G or Y in2 (Analog input)
48	BIN2	I	Connect to vss	B of U in2 (Analog inpu)
49	VSSD5[5]	S	Connect to Vss	Supply voltage for digital (0 V)
50	VDDAC1	S		Supply voltage CVBS1 (1.8 V)
51	VSSAC1	S		Supply voltage CVBS1 (0 V)
52	CVBS1	I	Connect to Vss	CVBS input (Analog input)

Pin No.	Pin Name	Type	Connection (If not used)	Short Description
53	CVBS2	I	Connect to Vss	CVBS input (Analog input)
54	CVBS3	I	Connect to Vss	CVBS input (Analog input)
55	CVBS4	I	Connect to Vss	CVBS input or Y1 (Analog input)
56	CVBS5	I	Connect to Vss	CVBS input or C1 (Analog input)
57	CVBS6	I	Connect to Vss	CVBS input or Y2 (Analog input)
58	CVBS7	I	Connect to Vss	CVBS input or C2 (Analog input)
59	VDD33C	S		Supply voltage CVBS (3.3 V)
60	VSS33C	S		Supply voltage CVBS (0 V)
61	CVBSO3	O	Leave open	CVBS output 3 (Analog output)
62	CVBSO2	O	Leave open	CVBS output 2 (Analog output)
63	CVBSO1	O	Leave open	CVBS output 1 (Analog output)
64	VDDAC2	S		Supply voltage CVBS2 (1.8 V)
65	VSSAC2	S		Supply voltage CVBS2 (0 V)
66	VDDD1	S		Supply voltage for digital (1.8 V digital)
67	VSSD1	S		Supply voltage for digital (0 V digital)
68	VDDAPLL	S		Supply voltage for PLL (1.8 V)
69	XOUT	O		Crystal connection 2
70	XIN	I		Crystal connection 1
71	TCLK	I		Testclock
72	VDDP1	S		Supply voltage for digital (3.3 V pad)
73	VSSP1	S		Supply voltage for digital (0 V pad)
74	656HIN/CLKF20	I/O	Connect to Vss and disable clock	Separate H input for 656 / 20.25 clock output
75	VDDDACV	S/I	Leave open	DAC (V) (27 MHz nom.)
76	AVOUT	O/I	Leave open	V output
77	VSSDACV	S/I	Leave open	DAC (V)
78	VDDDACU	S/I		DAC (U)
79	AUOUT	O/I		U output

Aug. 16, 2004; 6251-552-1DS   Micronas

Pin No.	Pin Name	Type	Connection (If not used)	Short Description
80	VSSDACU	S/I		DAC (U)

[1] In VSP 9402, A31 (and higher) and in VSP 94xxA/B/C, this pin is shared by 656vin and blank.
[2] In VSP 94xxB and VSP 94xxC, this pin is shared by v and intr (C800 controller output).
[3] In VSP 94xxB and VSP 94xxC, this pin is shared by h50 and irq (Data-slicer-interrupt).
[4] In VSP 94xxB and VSP 94xxC, this pin is shared by v50 and blank.
[5] This pin is not used and not bonded in VSP 9402A. The use of this pin in VSP 94xxB/C will be V_{SS}.
For upgradability, it is recommended to not leave this pin open.

4.3. Differing Pin Connections and Short Descriptions for VSP 9412

Pin No.	Pin Name	Type	Connection (If not used)	Short Description
1	I656I5	S/I	Leave open	656 input
2	I656I6	O/I		656 input
3	I656I7	S/I		656 input (MSB)
75	I656ICLK	S/I		656 input clock
76	I656I0	O/I		656 input (LBS)
77	I656I1	S/I		656 input
78	I656I2	S/I		656 input
79	I656I3	O/I		656 input
80	I656I4	S/I		656 input

4.4. Pin Configurations
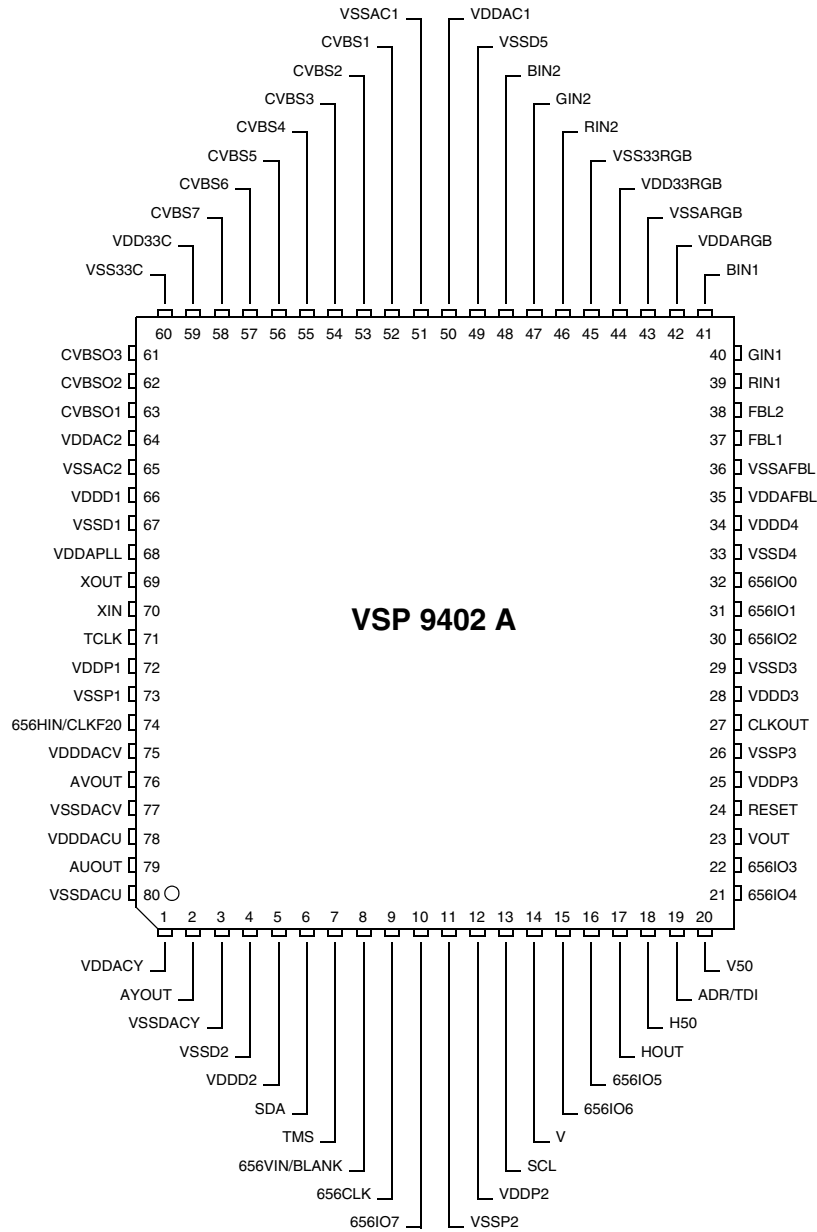
Fig. 4–2: PMQFP80-1 Package (Version VSP 9402A)
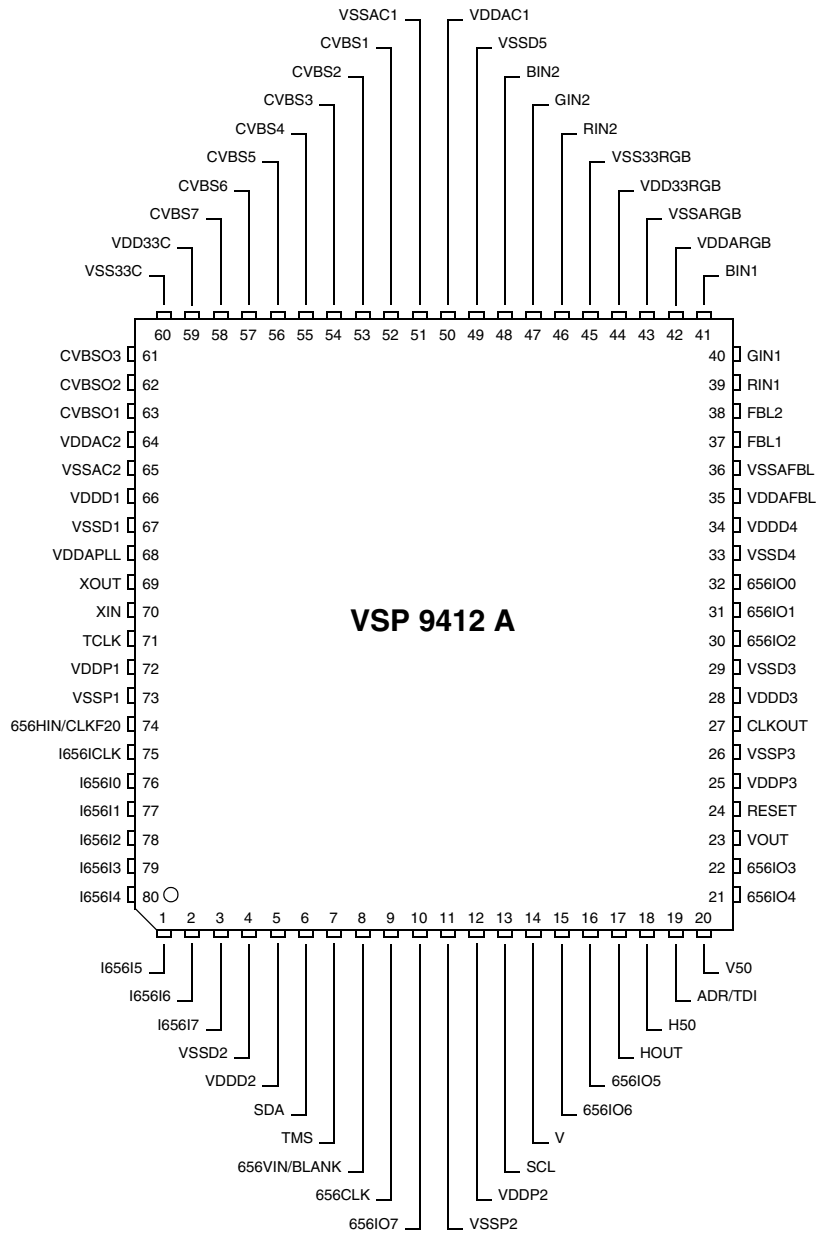
Fig. 4–3: PMQFP80-1 Package (Version VSP 9412A)

4.5. Pin Circuits
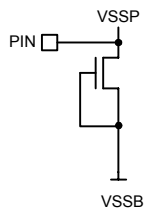
Fig. 4–4: Supply Pins (Ground): **VSSDACY, VSSDACU, VSSDACV, VSS33C, VSS33RGB, VSSP1, VSSP2, VSSP3**
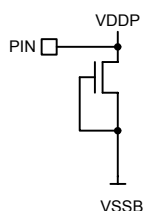
Fig. 4–5: Supply Pins (Power 3.3 V): **VDDDACY, VDDDACU, VDDACV, VDD33C, VDD33RGB, VDDP1, VDDP2, VDDP3**
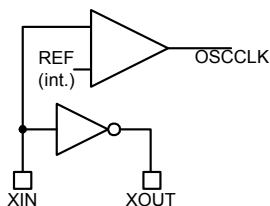
Fig. 4–6: Input/Output Pins (Crystal connection): **XIN, XOUT**
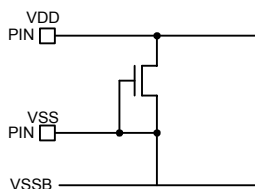
Fig. 4–7: Supply Pins (Power 1.8 V and Ground): **VDDAC1, VSSAC1, VDDAC2, VSSAC2, VDDARGB,VSSARGB, VDDAFBL, VSSAFBL, VDDAPLL, VDDD1, VSSS1, VDDD2, VSSS2, VDDD3, VSSS3, VDDD4, VSSS4**
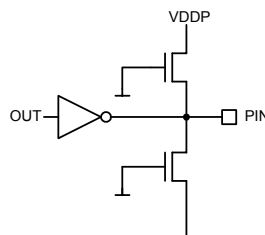
Fig. 4–8: Digital Output Pins: **H50, V50, CLKOUT, HOUT, VOUT**
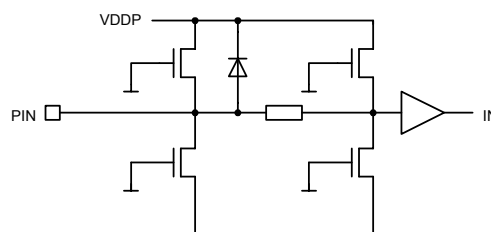
Fig. 4–9: Digital Input Pins: **V, TMS, ADR/TDI, RESET**
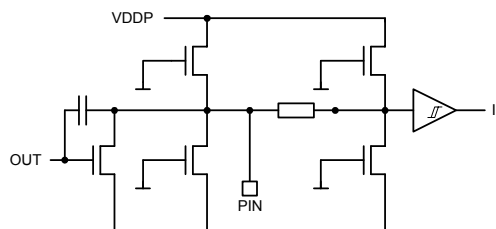
Fig. 4–10: I^{2}C bus Pins: **SDA, SCL**
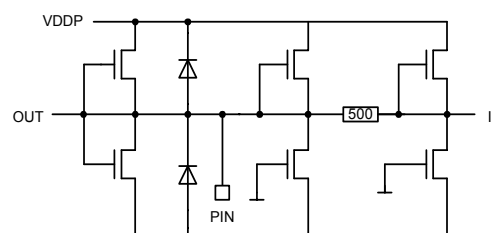
Fig. 4–11: Digital Input/Output Pins: **656IOX,656CLK, 656HIN/CLKF20, 656VIN/BLANK**
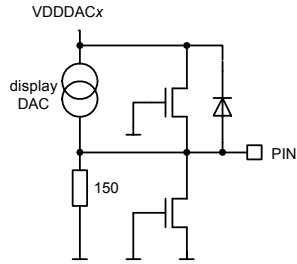
Fig. 4–12: Analog Output Pins: **AYOUT, AUOUT, AVOUT**
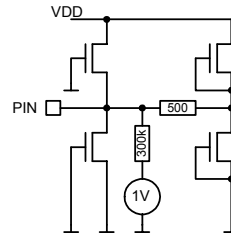
Fig. 4–14: Analog Input Pins: **CVBS1...CVBS7**
(if cvbsx is not connected to any ADC)
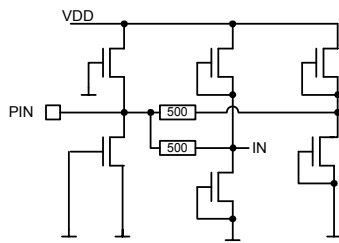
Fig. 4–13: Analog Input Pins: **RIN1, RIN2, GIN1, GIN2, BIN1, BIN2, FBL1, FBL2, CVBS1...CVBS7**
(if cvbsx is connected to any ADC)
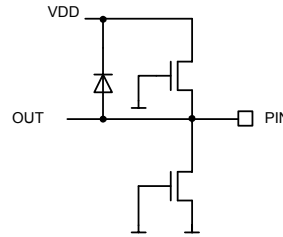
Fig. 4–15: Analog Output Pins: **CVBSO1...CVBSO3**

4.6. Electrical Characteristics

Abbreviations
tbd = to be defined
vacant= not applicable
positive current values means current flowing into the chip

4.6.1. Absolute Maximum Ratings

Stresses beyond those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only. Functional operations of the device at these conditions in not implied Exposure to absolute maximum rating conditions for extended periods will affect device reliability.

This device contains circuitry to protect the inputs and outputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than absolute maximum-rated voltages to this high-impedance circuit.

All voltages listed are referenced to ground except where noted.

All GND pins must be connected to a low-resistive ground plane close to the IC.

Table 4–1: Absolute Maximum Ratings

Symbol	Parameter	Pin Name	Limit Values		Unit
			Min	Max	
T_A [1]	Ambient Temperature PMQFP80-1		−10	70 [2]	°C
T_C	Case Temperature PMQFP80-1		−10	105	°C
T_S	Storage Temperature		−65	125	°C
P_{MAX}	Maximum Power Dissipation [3] PMQFP80-1			1500	mW
V_{DD1}	Supply Voltages1	VDDDx, VDDAFBL VDDARGB VDDAC1 VDDAC2 VDDAPLL	-0.3	$2^{[4][5]}$	V
L_{DD2}	Supply Voltages2	VDDPx, VDD33C, VDD33RGB, VDDACU, VDDACV	-0.3	$3.6^{[4][5]}$	V
ΔV_{SUP}	Internally Conected Power Supplies have to be connected externally with an impedance of less than 0.05 Ω	Groups of internally conected power supply pins: {VSSDx, VSSPx}, {VDDDx}, {VDDPx}, {VDDACU/V}			V

Table 4–1: Absolute Maximum Ratings

Symbol	Parameter	Pin Name	Limit Values		Unit
			Min	**Max**	
ΔV_{SUP}	Voltage Differences between not internally connected supply pins of the same nominal supply voltage	Groups of independant grounds: {VSSDx; VSSPx}, {VSSARGB, VSSAFBL, VSS33RGB}, {VSSAC1, VSSAC2, VSS33C}, {VSSDACx}, Groups of independant 1.8 V supply voltages: {VDDDx}, {VDDAC1, VDDAC2}, {VDDARGB, VDDAFBL}, {VDDAPLL} Groups of independant 3.3 V supply voltages {VDDPx}, {VDDACU/V}, {VDD33C}, {VDD33RGB}	-0.3	0.3	V
V_I	Input Voltage [2]	All input pins with reference to their relevant VDD	-0.3	V_{DD}+0.3	V
I_{I_low}	Input Current at 0.4 V	All digital inputs with pull-up	55	157	μA
I_{I_high}	Input Current at 2.4 V	All digital inputs with pull-down	57	230	μA
V_O	Output Voltage [3]	All output pins with reference to their relevant VDD	-0.3	V_{DD2}+0.3	V
$I_{O\_low\ (I2C)}$	Output Sink Current (at 0.4 V)	I^{2}C pads	10.3	36	mA
$I_{O\_high(I2C)}$	Output Source Current (at 2.4 V)	I^{2}C pads		(open drain)	mA
I_{O_low}	Output Sink Current (at 0.4 V)	Digital outputs	30.1	58.8	mA

Table 4–1: Absolute Maximum Ratings

Symbol	Parameter	Pin Name	Limit Values		Unit
			Min	**Max**	
I_{O_high}	Output Source Current (at 2.4 V)	Digital outputs	31.7	97.1	mA

[1] Measured on Micronas typical 2-layer (1s1p) board based on JESD - 51.2 Standard with maximum power consumption allowed for this package

[2] A power-optimized board layout is recommended. The case temperature mentioned in the "Absolute Maximum Ratings" must not be exceeded at worst case conditions of the application.

[3] Package limit

[4] V_{DD2} (3.3 V nom.) must always be higher than V_{DD1} (1.8 V nom.) -0.3 V (even during power-up)

[5] The deviation among all V_{DD1} or V_{DD2} supplies may never exceed 0.3 V.

4.6.2. Recommended Operating Conditions

Functional operation of the device beyond those indicated in the "Recommended Operating Conditions/Characteristics" is not implied and may result in unpredictable behaivior, reduce reliability and lifetime of the device.

All voltage listed are referenced to ground except where noted.

Do not insert the device into a live socket. Instead, apply power by switching on the external power supply.

Symbol	Parameter	Pin Name	Limit Values			Unit
			Min	Typ	Max	
T_A	Ambient Operating Temperature PMQFP80-1		0	25	70 [1)	°C
T_C	Case Operating Temperature PMQFP80-1			35	85	°C
P_{MAX}	Maximum Power Dissipation PMQFP80-1				700	mW
V_{DDxx}	Supply voltages (3.3 V)	VDDP1, VDDP2, VDDP3, VDDACY, VDDACU, VDDACV, VDD33C, VDD33RGB	3.14	3.3	3.47	V
V_{DDxx}	Supply voltages (1.8 V)	VDDAC1, VDDAC2, VDDARGB, VDDAFBL, VDDAPLL; VDDD1; VDDD2;VDDD3; VDDD4	1.71	1.8	1.89	V
$V_{in,L}$	Input voltage low	TMS, ADR/TDI, V, TCLK, RESET, 656VIN/BLANK, 656HIN/, 656IOX, 656CLK, I656IX, I656ICLK			1.0	V
$V_{in,H}$	Input voltage high		1.7			V
t_{RES}	Active time reset	RESET	1.3			µs
R_L	Load resistance	AYOUT, AUOUT, AVOUT	10			kΩ
C_L	Load capacitance		tbd			pF

Micronas   Aug. 16, 2004; 6251-552-1DS   117

Symbol	Parameter	Pin Name	Limit Values			Unit
			Min	Typ	Max	
$V_{i,CVBS}$	Analog CVBS input voltage	CVBS1, CVBS2, CVBS3, CVBS4, CVBS5, CVBS6, CVBS7, RIN1, RIN2, GIN1, GIN2, BIN1, BIN2, FBL1, FBL2	0.6	1.2	1.8	V
$V_{i,RGB}$	Analog RGB input voltage		0.5	1.2	1.5	V
$V_{i,FBL}$	Analog FBL input voltage		0.5	1.2	1.5	V
	Analog chroma input voltage (burst)			0.3		V
	Input coupling capacitors CVBS			100		nF
	Input coupling capacitors RGB/FBL			47		nF
	Source resistance			0.1		$k\Omega$
Crystal Specification						
f_{xtal}	Frequency (fundamental)[3]	XIN, XOUT	20.248	20.25	20.252	MHz
$\Delta f_{max}/f_{xtal}$	Maximum permissible frequency deviation[3]		−100		100	ppm
$\Delta f/f_{xtal}$	Recommended permissible frequency deviation[4]		−40	0	40	ppm
C_L	Load capacitance			13		pF
R_S	Series resistance			tbd	25	W
C_1	Motional capacitance		20		30	fF
C_0	Parallel capacitance			7		pF
$C_{L,EXT}$	External load capacitance to ground			13		pF

[1] A power-optimized board layout is recommended. The Case Operating Temperature mentioned in the Recommended Operating Conditions must not be exceeded at worst case conditions of the application

[2] P_{MAX} variation: User-determined by application circuit for I/O's

[3] Values outside this range may cause color decoding failures.

[4] After (subcarrier) adjustment // including temperature and aging deviations

4.6.3. Characteristics

For Min./Max. values: at T_A = 0 to 70°C,
f_{CLOCK} =20.25MHz,
$V_{SUP3.3V}$ = 3.14 to 3.47 V,
$V_{SUP1.8V}$ = 1.71 to 1.89V

For typical values: at T_A = 25°C,
f_{CLOCK} = 20.25MHz,
$V_{SUP3.3V}$ = 3.14 to 3.47 V,
$V_{SUP1.8V}$ = 1.71 to 1.89V

4.6.3.1. General Characteristics

Symbol	Parameter	Pin Name	LImit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
$I_{DDtot\ 1.8\ V}$	Average total supply current			220		mA	
$I_{DDtot\ 3.3\ V}$	Average total supply current			65		mA	
I_{DDPD} 1.8 V	Average supply current in power-down-mode			74		mA	STANDBY= '10'
I_{DDPD} 3.3 v	Average supply current in power-down-mode			36		mA	STANDBY= '10'
P_{tot}	Total power dissipation			0.61	0.8	W	
P_{totPD}	Total power dissipation in power-down-mode			0.27		W	STANDBY= '10'
Digital Inputs							
C_I	Input capacitance	TMS, ADR/TDI, V, TCLK, RESET, 656VIN/ BLANK, 656HIN/, 656IOX, 656CLK, I656IX, I656ICLK		7		pF	
	Input leakage current		−10		10	µA	Incl. leakage current of SDA output stage
Digital Outputs							
V_{OH}	Output voltage high	H50, V50, CLKOUT, HOUT, VOUT	2.5		V_{dd2}	V	
V_{OL}	Output voltage low				0.6	V	
I_{OH}	Output current high					mA	
I_{OL}	Output current low					mA	
Clock Outputs							
t	CLKOUT cycle time	CLKOUT		37		ns	
	CLKOUT duty cycle		40		60	%	
t	656CLK cycle time	656CLK		37		ns	
	656CLK duty cycle		40		60	%	

Symbol	Parameter	Pin Name	LImit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Analog CVBS Front-end							
	Input leakage current	CVBS1, CVBS2, CVBS3, CVBS4, CVBS5, CVBS6, CVBS7	−100		100	nA	Clamping inactive
C_I	Input capacitance			7		pF	
	Input clamping error		−1		1	LSB	Settled state
$|\bar{I}_{CLP}|$	Input clamping current					µA	Dependent on clamping error
DNL	Differential nonlinearity		-0.5		0.5	LSB	Nominal conditions
INL	Integral nonlinearity		-1		1	LSB	Nominal conditions
CT	Crosstalk between CVBS inputs		-50			dB	f_{sig}<5 MHz
BW	Bandwidth		7			MHz	-3 dB
V_{in}	Input voltage		0.6	1.2	1.8	V	
A_{cvbso}	CVBS output amplification	CVBSO1, CVBSO2, CVBSO3	0.9		1.1		
Analog RGBF Front-end							
	Input leakage current	RIN1, RIN2, BIN1, BIN2, GIN1, GIN2, FBL1, FBL2	−100		100	nA	Clamping inactive
C_I	CVBS input capacitance			7		pF	
	Input clamping error		−1		1	LSB	Settled state
$|\bar{I}_{CLP}|$	Input clamping current					µA	Dependent on clamping error
DNL	Differential nonlinearity		−0.5		0.5	LSB	Nominal conditions
INL	Integral nonlinearity		−1		1	LSB	Nominal conditions
CT	Crosstalk between RGB inputs		-50			dB	
BW	Bandwidth		10			MHz	−3 dB
V_{in}	Input voltage		0.5	1.2	1.5	V	
Digital To Analog Converters							
DNL	Differential nonlinearity	AUOUT, AUOUT, AVOUT	−1		1	LSB	Nominal conditions
INL	Integral nonlinearity		−2		2	LSB	Nominal conditions
U_{OL}	Full range output voltage			0.4		V	Nominal conditions PKLY/U/V=min
U_{OH}	Full range output voltage			1.9		V	Nominal conditions PKLY/U/V=max
	Output matching		−3		3	%	

Symbol	Parameter	Pin Name	LImit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Color Decoder/Synchronization and Luminance Processing							
Δf_{Hf}	Horizontal PLL pull-in-range			±4.9		%	Based on 15625 kHz
	ACC range			-30	$+6$	dB	
	AGC range			-7.5	$+2$	dB	
Δf_{SC}	Chroma PLL pull-in-range			±500		Hz	Nominal crystal frequency

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics spec-ify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at $T_A = 25\,°C$ and the given supply voltage.

4.6.3.2. I^{2}C Bus Characteristics

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Fast I^{2}C Bus (All Values are Referred to Min(V_{IH}) and Max(V_{IL}))							
C_b	Capacitive load/bus line	SDA/SCL			400	pF	
t_R, t_F	SDA/SCL rise/fall times		20+$		300	ns	$=0.1 C_b/pF
t_{BUF}	Inactive time before start of transmission		1300			ns	
f_{SCL}	I^{2}C clock frequency	SCL	0		400	kHz	
t_{LOW}	SCL low time		1300			ns	
t_{HIGH}	SCL high time		600			ns	
$t_{SU;STA}$	Set-up time start condition	SDA	600			ns	
$t_{HD;STA}$	Hold time start condition		600			ns	
$t_{SU;DAT}$	Set-up time DATA		100			ns	
$t_{HD;DAT}$	Hold time DATA		0		900	ns	
$t_{SU;STO}$	Set-up time stop condition		600			ns	
I^{2}C Bus pins							
V_{IHr}	Threshold rise	SDA, SCL		2.08		V	
V_{IL}	Threshold fall			1.8		V	
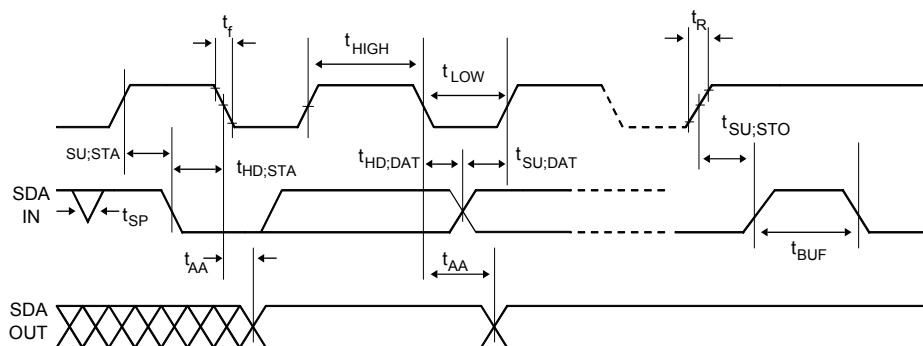
Fig. 4–16: I^{2}C bus timing data
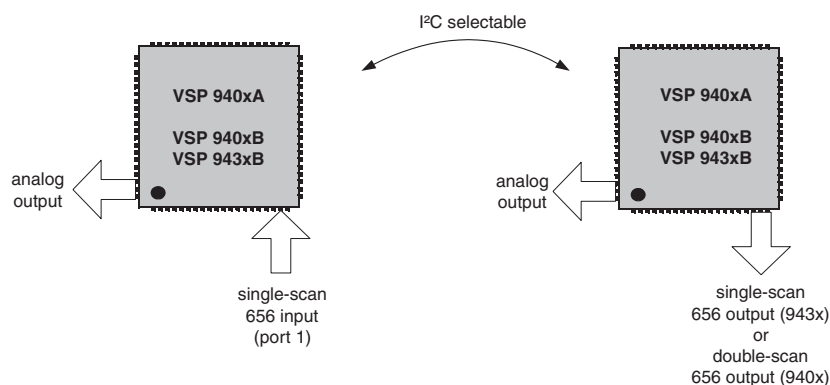
Fig. 4–17: Signal Flow 940x
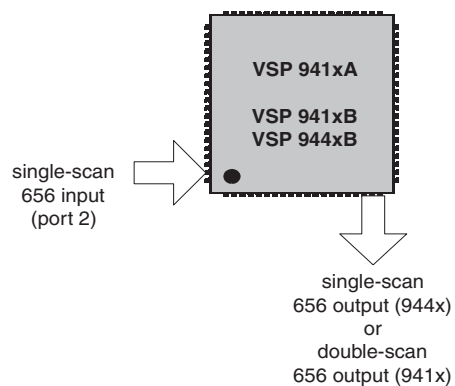
Fig. 4–18: Signal flow 941x, 944x, 942x

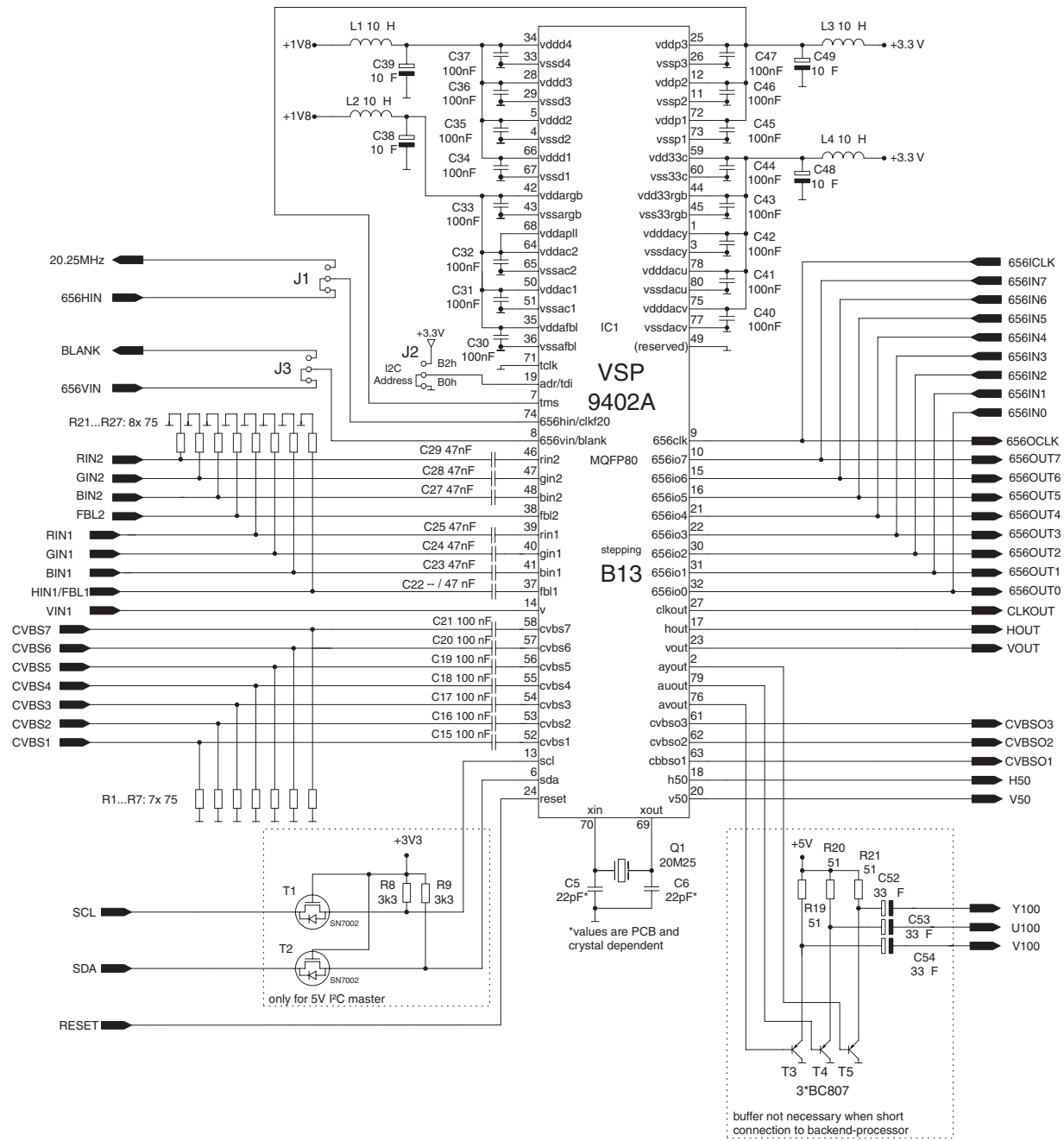## 5. Application Circuit

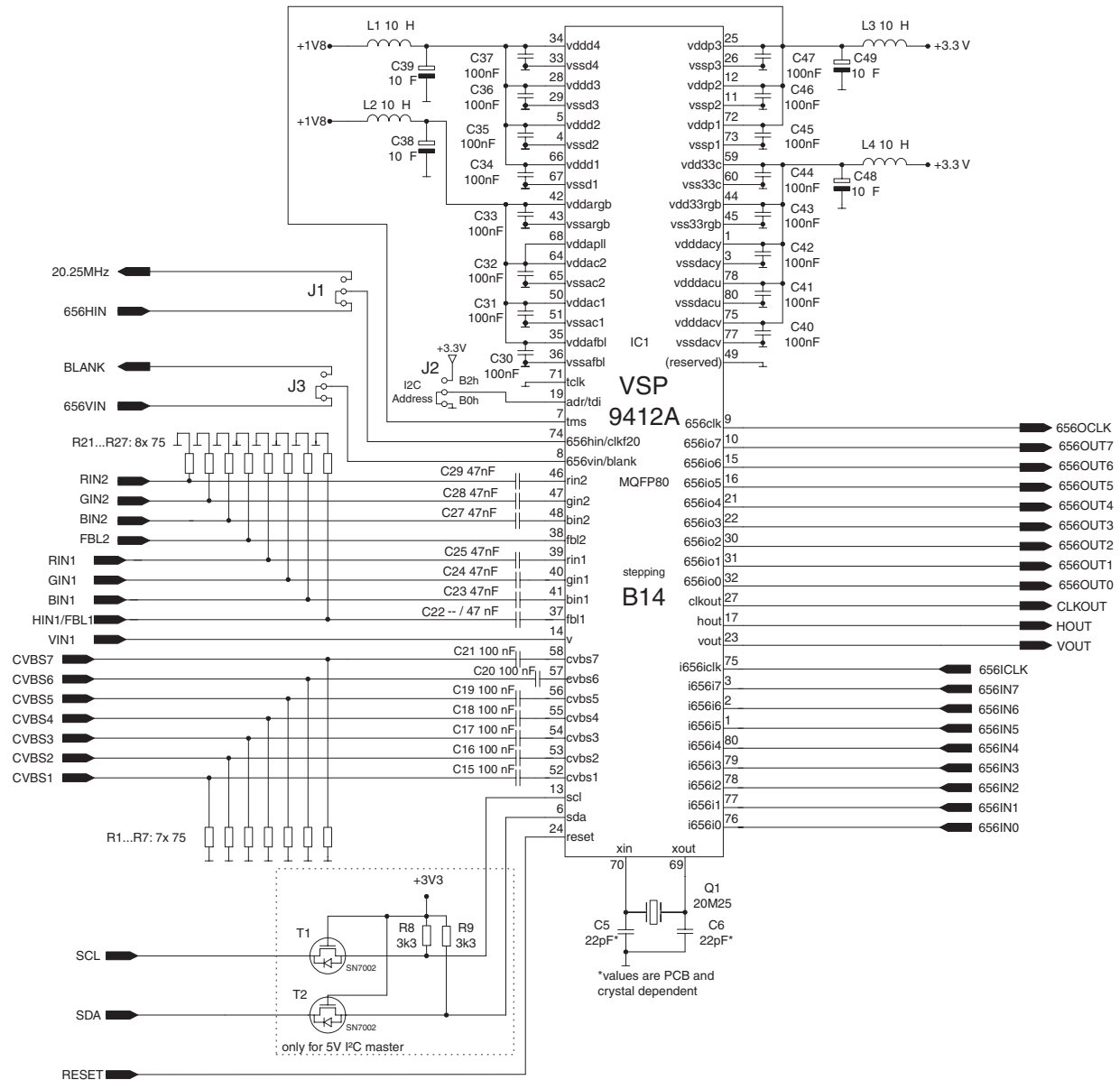**Fig. 5–1:** VSP 9402A

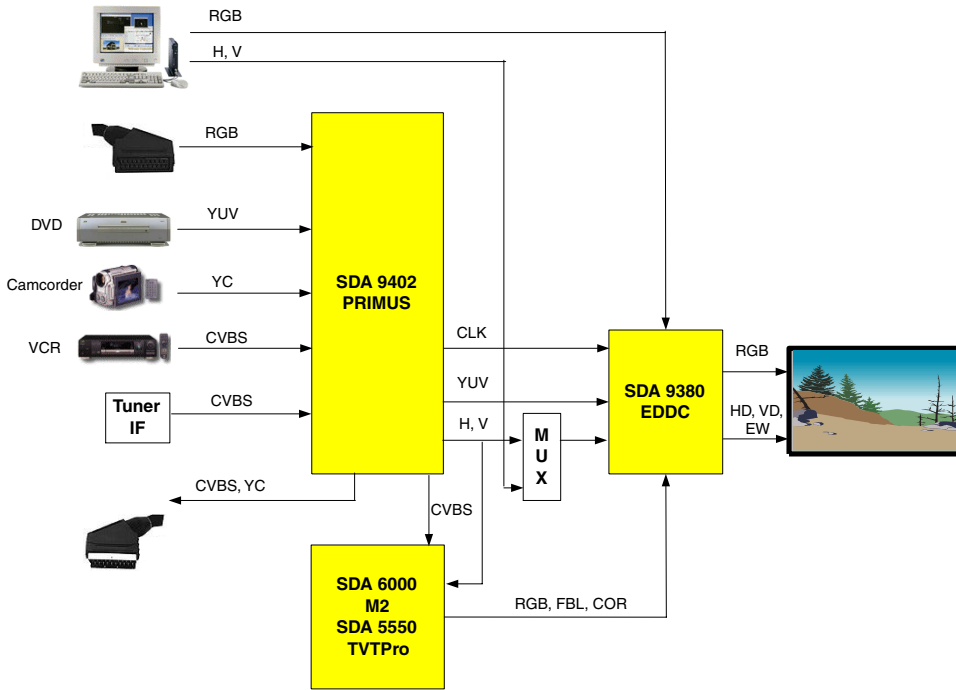**Fig. 5–2:** VSP 9412A

5.1. Application Overview
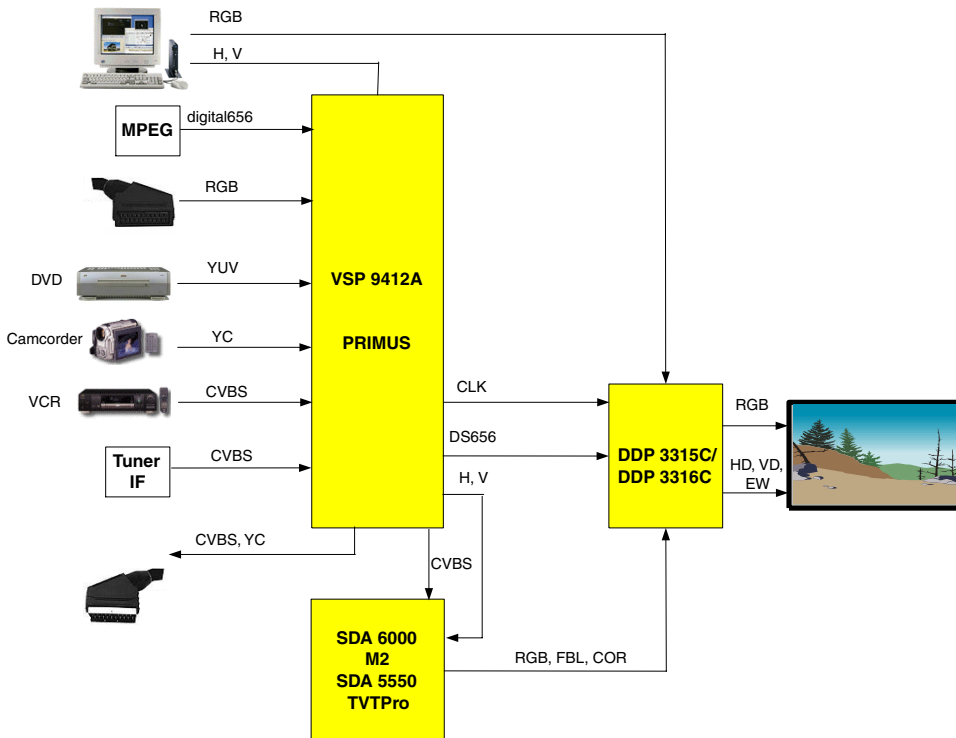

Fig. 5–3: Application Overview with SDA 9380

Fig. 5–4: Application Overview with DDP 3315C/DDP 3316C

6. Data Sheet History

1. Preliminary Data Sheet: "VSP 94x2A-B13/B14
   Powerful Scan-Rate Converter including Multistan-
   dard Color Decoder", July 26, 2002, 6251-552-4PD.
   Fourth release of the preliminary data sheet.
   Mayor changes:

   – New I^2C registers added

2. Data Sheet: "VSP 94x2A-B13/B14
   Powerful Scan-Rate Converter including Multistan-
   dard Color Decoder", Aug. 16, 2004,
   6251-552-1DS. First release of the data sheet.
   Major changes:

   – Version VSP 9432A and VSP 9442A omitted

   – Section 4. Specification updated

   – Application diagrams updated

   – Subadress 7Bh updated