Si5369

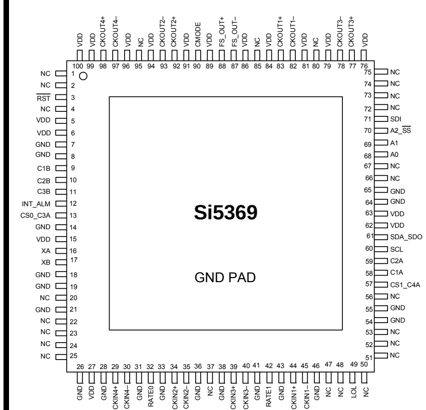
ANY-FREQUENCY PRECISION CLOCK MULTIPLIER/JITTER ATTENUATOR

Features

- Generates any frequency from 2 kHz to 945 MHz and select frequencies to 1.4 GHz from an input frequency of 2 kHz to 710 MHz
- Ultra-low jitter clock outputs with jitter generation as low as 300 fs rms (50 kHz–80 MHz)
- Integrated loop filter with selectable loop bandwidth (60 Hz to 8.4 kHz)
- Meets OC-192 GR-253-CORE jitter specifications
- Four clock inputs with manual or automatically controlled hitless switching and phase build-out
- Supports holdover and freerun modes of operation
- SONET frame sync switching and regeneration
- Five clock outputs with selectable signal format (LVPECL, LVDS, CML, CMOS)
- Support for ITU G.709 and custom FEC ratios (253/226, 239/237, 255/238, 255/237, 255/236)
- LOL, LOS, FOS alarm outputs
- Digitally-controlled output phase adjust
- I^2C or SPI programmable settings
- On-chip voltage regulator for 1.8 V ±5%, 2.5 V ±10%, or 3.3 V ±10% operation
- Small size: 14 x 14 mm 100-pin TQFP
- Pb-free, RoHS compliant

Ordering Information:
See page 77.

Pin Assignments



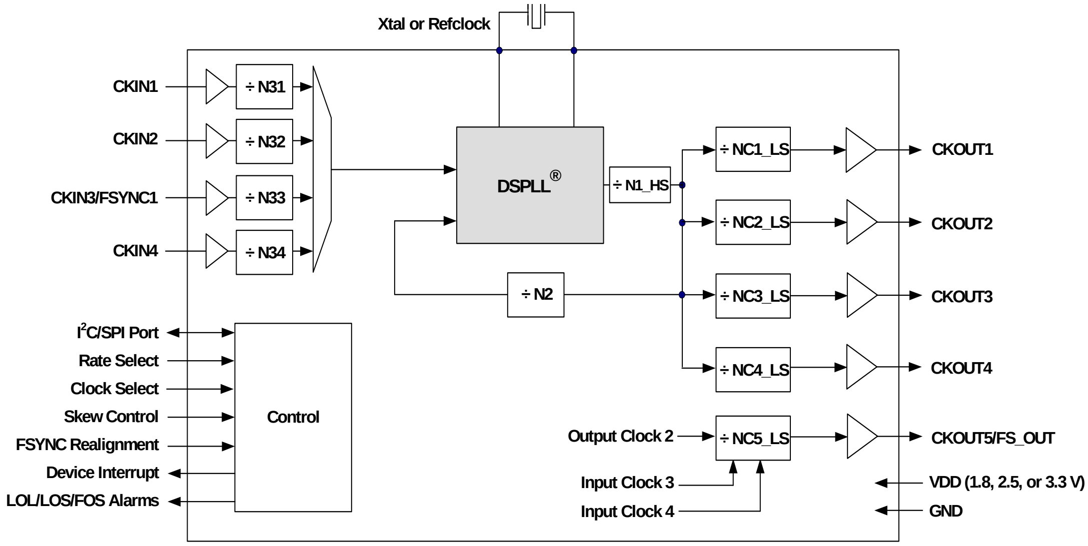
Applications

- SONET/SDH OC-48/STM-16/OC-192/STM-64 line cards
- GbE/10GbE, 1/2/4/8/10G FC line cards
- ITU G.709 and custom FEC line cards
- Wireless repeaters/wireless backhaul
- Data converter clocking
- OTN/WDM Muxponder, MSPP, ROADM line cards
- SONET/SDH + PDH clock synthesis
- Test and measurement
- Synchronous Ethernet
- Broadcast video

Description

The Si5369 is a jitter-attenuating precision clock multiplier for applications requiring sub 1 ps rms jitter performance. The Si5369 accepts four clock inputs ranging from 2 kHz to 710 MHz and generates five clock outputs ranging from 2 kHz to 945 MHz and select frequencies to 1.4 GHz. The device provides virtually any frequency translation combination across this operating range. The outputs are divided down separately from a common source. The Si5369 input clock frequency and clock multiplication ratio are programmable through an I^2C or SPI interface. The Si5369 is based on Silicon Laboratories' third-generation DSPLL® technology, which provides any-frequency synthesis and jitter attenuation in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The DSPLL loop bandwidth is digitally programmable, providing jitter performance optimization at the application level. Operating from a single 1.8, 2.5 ,or 3.3 V supply, the Si5369 is ideal for providing clock multiplication and jitter attenuation in high performance timing applications.

Functional Block Diagram



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1. Electrical Specifications

Table 1. Recommended Operating Conditions[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Temperature	T_A		-40	25	85	C
Supply Voltage during Normal Operation	V_{DD}	3.3 V Nominal[2]	2.97	3.3	3.63	V
		2.5 V Nominal	2.25	2.5	2.75	V
		1.8 V Nominal	1.71	1.8	1.89	V

Notes:

1. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise stated.
2. The LVPECL and CMOS output formats draw more current than either LVDS or CML; however, there are restrictions in the allowed output format pin settings so that the maximum power dissipation for the TQFP devices is limited when they are operated at 3.3 V. When there are four enabled LVPECL or CMOS outputs, the fifth output must be disabled. When there are five enabled outputs, there can be no more than three outputs that are either LVPECL or CMOS.

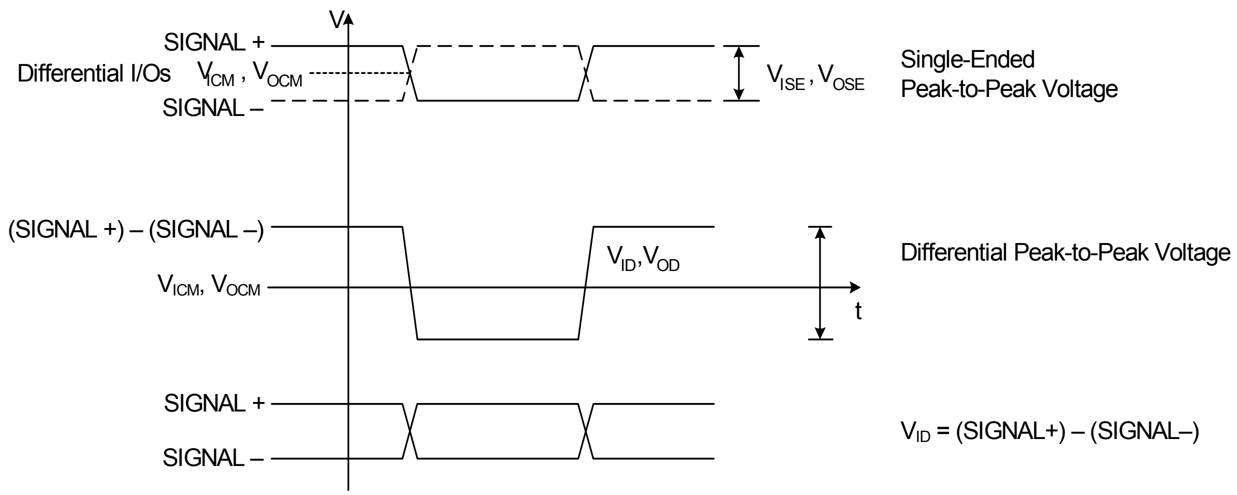


Figure 1. Differential Voltage Characteristics

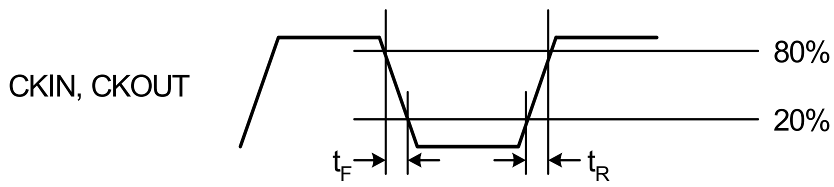


Figure 2. Rise/Fall Time Characteristics

Table 2. Absolute Limits

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC Supply Voltage	V_{DD}		–0.5	—	3.8	V
LVCMOS Input Voltage	V_{DIG}		–0.3		V_{DD}+0.3	V
CKINn Voltage Level Limits	CKN_{VIN}		0	—	V_{DD}	V
XA/XB Voltage Level Limits	XA_{VIN}		0	—	1.2	V
Operating Junction Temperature	T_{JCT}		–55	—	150	ºC
Storage Temperature Range	T_{STG}		–55	—	150	ºC
ESD HBM Tolerance (100 pF, 1.5 kΩ); All pins except CKIN+/CKIN–			2	—	—	kV
ESD MM Tolerance; All pins except CKIN+/CKIN–			150	—	—	V
ESD HBM Tolerance (100 pF, 1.5 kΩ); CKIN+/CKIN–			700	—	—	V
ESD MM Tolerance; CKIN+/CKIN–			100	—	—	V
Latch-up Tolerance			JESD78 Compliant			

Table 3. DC Characteristics

(V_{DD} = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Current[1,6]	I_{DD}	LVPECL Format 622.08 MHz Out All CKOUTs Enabled	—	394	435	mA
		LVPECL Format 622.08 MHz Out 1 CKOUT Enabled	—	253	284	mA
		CMOS Format 19.44 MHz Out All CKOUTs Enabled	—	278	321	mA
		CMOS Format 19.44 MHz Out 1 CKOUT Enabled	—	229	261	mA
		Disable Mode	—	165	—	mA
CKINn Input Pins[2]						
Input Common Mode Voltage (Input Threshold Voltage)	V_{ICM}	1.8 V ± 5%	0.9	—	1.4	V
		2.5 V ± 10%	1	—	1.7	V
		3.3 V ± 10%	1.1	—	1.95	V
Input Resistance	CKN_{RIN}	Single-ended	20	40	60	kΩ
Single-Ended Input Voltage Swing (See Absolute Specs)	V_{ISE}	f_{CKIN} < 212.5 MHz See Figure 1.	0.2	—	—	V_{PP}
		f_{CKIN} > 212.5 MHz See Figure 1.	0.25	—	—	V_{PP}
Differential Input Voltage Swing (See Absolute Specs)	V_{ID}	f_{CKIN} < 212.5 MHz See Figure 1.	0.2	—	—	V_{PP}
		fCKIN > 212.5 MHz See Figure 1.	0.25	—	—	V_{PP}

Notes:
1. Current draw is independent of supply voltage
2. No under- or overshoot is allowed.
3. LVPECL outputs require nominal VDD ≥ 2.5 V.
4. This is the amount of leakage that the 3-Level inputs can tolerate from an external driver. See Si53xx Family Reference Manual for more details.
5. LVPECL, CML, LVDS and low-swing LVDS measured with Fo = 622.08 MHz.
6. The LVPECL and CMOS output formats draw more current than either LVDS or CML; however, there are restrictions in the allowed output format pin settings so that the maximum power dissipation for the TQFP devices is limited when they are operated at 3.3 V. When there are four enabled LVPECL or CMOS outputs, the fifth output must be disabled. When there are five enabled outputs, there can be no more than three outputs that are either LVPECL or CMOS.

Table 3. DC Characteristics (Continued)
(V_{DD} = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Clocks (CKOUTn)[3,5,6]						
Common Mode	CKO_{VCM}	LVPECL 100 Ω load line-to-line	V_{DD} – 1.42	—	V_{DD} –1.25	V
Differential Output Swing	CKO_{VD}	LVPECL 100 Ω load line-to-line	1.1	—	1.9	V_{PP}
Single Ended Output Swing	CKO_{VSE}	LVPECL 100 Ω load line-to-line	0.5	—	0.93	V_{PP}
Differential Output Voltage	CKO_{VD}	CML 100 Ω load line-to-line	350	425	500	mV_{PP}
Common Mode Output Voltage	CKO_{VCM}	CML 100 Ω load line-to-line	—	V_{DD}-0.36	—	V
Differential Output Voltage	CKO_{VD}	LVDS 100 Ω load line-to-line	500	700	900	mV_{PP}
		Low Swing LVDS 100 Ω load line-to-line	350	425	500	mV_{PP}
Common Mode Output Voltage	CKO_{VCM}	LVDS 100 Ω load line-to-line	1.125	1.2	1.275	V
Differential Output Resistance	CKO_{RD}	CML, LVPECL, LVDS	—	200	—	Ω
Output Voltage Low	CKO_{VOLLH}	CMOS	—	—	0.4	V
Output Voltage High	CKO_{VOHLH}	V_{DD} = 1.71 V CMOS	0.8 x V_{DD}	—	—	V

Notes:
1. Current draw is independent of supply voltage
2. No under- or overshoot is allowed.
3. LVPECL outputs require nominal VDD ≥ 2.5 V.
4. This is the amount of leakage that the 3-Level inputs can tolerate from an external driver. See Si53xx Family Reference Manual for more details.
5. LVPECL, CML, LVDS and low-swing LVDS measured with Fo = 622.08 MHz.
6. The LVPECL and CMOS output formats draw more current than either LVDS or CML; however, there are restrictions in the allowed output format pin settings so that the maximum power dissipation for the TQFP devices is limited when they are operated at 3.3 V. When there are four enabled LVPECL or CMOS outputs, the fifth output must be disabled. When there are five enabled outputs, there can be no more than three outputs that are either LVPECL or CMOS.

Table 3. DC Characteristics (Continued)
(V_{DD} = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Drive Current (CMOS driving into CKO_{VOL} for output low or CKO_{VOH} for output high. CKOUT+ and CKOUT– shorted externally)	CKO_{IO}	ICMOS[1:0] =11 V_{DD} = 1.8 V	—	7.5	—	mA
		ICMOS[1:0] =10 V_{DD} = 1.8 V	—	5.5	—	mA
		ICMOS[1:0] =01 V_{DD} = 1.8 V	—	3.5	—	mA
		ICMOS[1:0] =00 V_{DD} = 1.8 V	—	1.75	—	mA
		ICMOS[1:0] =11 V_{DD} = 3.3 V	—	32	—	mA
		ICMOS[1:0] =10 V_{DD} = 3.3 V	—	24	—	mA
		ICMOS[1:0] =01 V_{DD} = 3.3 V	—	16	—	mA
		ICMOS[1:0] =00 V_{DD} = 3.3 V	—	8	—	mA
2-Level LVCMOS Input Pins						
Input Voltage Low	V_{IL}	V_{DD} = 1.71 V	—	—	0.5	V
		V_{DD} = 2.25 V	—	—	0.7	V
		V_{DD} = 2.97 V	—	—	0.8	V
Input Voltage High	V_{IH}	V_{DD} = 1.89 V	1.4	—	—	V
		V_{DD} = 2.25 V	1.8	—	—	V
		V_{DD} = 3.63 V	2.5	—	—	V

Notes:
1. Current draw is independent of supply voltage
2. No under- or overshoot is allowed.
3. LVPECL outputs require nominal VDD ≥ 2.5 V.
4. This is the amount of leakage that the 3-Level inputs can tolerate from an external driver. See Si53xx Family Reference Manual for more details.
5. LVPECL, CML, LVDS and low-swing LVDS measured with Fo = 622.08 MHz.
6. The LVPECL and CMOS output formats draw more current than either LVDS or CML; however, there are restrictions in the allowed output format pin settings so that the maximum power dissipation for the TQFP devices is limited when they are operated at 3.3 V. When there are four enabled LVPECL or CMOS outputs, the fifth output must be disabled. When there are five enabled outputs, there can be no more than three outputs that are either LVPECL or CMOS.

Table 3. DC Characteristics (Continued)

(V_{DD} = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
3-Level Input Pins[4]						
Input Voltage Low	V_{ILL}		—	—	0.15 x V_{DD}	V
Input Voltage Mid	V_{IMM}		0.45 x V_{DD}	—	0.55 x V_{DD}	V
Input Voltage High	V_{IHH}		0.85 x V_{DD}	—	—	V
Input Low Current	I_{ILL}	See Note 4	–20	—	—	µA
Input Mid Current	I_{IMM}	See Note 4	–2	—	+2	µA
Input High Current	I_{IHH}	See Note 4	—	—	20	µA
LVCMOS Output Pins						
Output Voltage Low	V_{OL}	IO = 2 mA V_{DD} = 1.71 V	—	—	0.4	V
Output Voltage Low		IO = 2 mA V_{DD} = 2.97 V	—	—	0.4	V
Output Voltage High	V_{OH}	IO = –2 mA V_{DD} = 1.71 V	V_{DD} – 0.4	—	—	V
Output Voltage High		IO = –2 mA V_{DD} = 2.97 V	V_{DD} – 0.4	—	—	V
Disabled Leakage Current	I_{OZ}	RSTb = 0	–100	—	100	µA

Notes:

1. Current draw is independent of supply voltage
2. No under- or overshoot is allowed.
3. LVPECL outputs require nominal VDD ≥ 2.5 V.
4. This is the amount of leakage that the 3-Level inputs can tolerate from an external driver. See Si53xx Family Reference Manual for more details.
5. LVPECL, CML, LVDS and low-swing LVDS measured with Fo = 622.08 MHz.
6. The LVPECL and CMOS output formats draw more current than either LVDS or CML; however, there are restrictions in the allowed output format pin settings so that the maximum power dissipation for the TQFP devices is limited when they are operated at 3.3 V. When there are four enabled LVPECL or CMOS outputs, the fifth output must be disabled. When there are five enabled outputs, there can be no more than three outputs that are either LVPECL or CMOS.

Table 4. AC Specifications

(V_{DD} = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Single-Ended Reference Clock Input Pin XA (XB with cap to GND)						
Input Resistance	XA_{RIN}	RATE[1:0] = LM, MH, ac coupled	—	12	—	kΩ
Input Voltage Swing	XA_{VPP}	RATE[1:0] = LM, MH, ac coupled	0.5	—	1.2	V_{PP}
Differential Reference Clock Input Pins (XA/XB)						
Input Voltage Swing	XA/XB_{VPP}	RATE[1:0] = LM, MH	0.5	—	2.4	V_{PP}
CKINn Input Pins						
Input Frequency	CKN_F		0.002	—	710	MHz
Input Duty Cycle (Minimum Pulse Width)	CKN_{DC}	Whichever is smaller (i.e., the 40% / 60% limitation applies only to high frequency clocks)	40	—	60	%
			2	—	—	ns
Input Capacitance	CKN_{CIN}		—	—	3	pF
Input Rise/Fall Time	CKN_{TRF}	20–80% See Figure 2	—	—	11	ns
CKOUTn Output Pins (See ordering section for speed grade vs frequency limits)						
Output Frequency (Output not configured for CMOS or Disabled)	CKO_F	N1 ≥ 6	0.002	—	945	MHz
		N1 = 5	970	—	1134	MHz
		N1 = 4	1.213	—	1.4	GHz
Maximum Output Frequency in CMOS Format	CKO_F		—	—	212.5	MHz
Output Rise/Fall (20–80 %) @ 622.08 MHz output	CKO_{TRF}	Output not configured for CMOS or Disabled See Figure 2	—	230	350	ps
Output Rise/Fall (20–80%) @ 212.5 MHz output	CKO_{TRF}	CMOS Output V_{DD} = 1.71 C_{LOAD} = 5 pF	—	—	8	ns

***Note:** Input to output phase skew after an ICAL is not controlled and can assume any value.

Table 4. AC Specifications (Continued)
(V_{DD} = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Rise/Fall (20–80%) @ 212.5 MHz output	CKO_{TRF}	CMOS Output V_{DD} = 2.97 C_{LOAD} = 5 pF	—	—	2	ns
Output Duty Cycle Uncertainty @ 622.08 MHz	CKO_{DC}	100 Ω Load Line-to-Line Measured at 50% Point (Not for CMOS)	—	—	±40	ps
LVCMOS Input Pins						
Minimum Reset Pulse Width	t_{RSTMN}		1			µs
Reset to Microprocessor Access Ready	t_{READY}				10	ms
Input Capacitance	C_{in}		—	—	3	pF
LVCMOS Output Pins						
Rise/Fall Times	t_{RF}	C_{LOAD} = 20pf See Figure 2	—	25	—	ns
LOSn Trigger Window	LOS_{TRIG}	From last CKINn ↑ to ↓ Internal detection of LOSn N3 ≠ 1	—	—	4.5 x N3	T_{CKIN}
Time to Clear LOL after LOS Cleared	t_{CLRLOL}	↓LOS to ↓LOL Fold = Fnew Stable Xa/XB reference	—	10	—	ms
Device Skew						
Output Clock Skew	t_{SKEW}	↑ of CKOUTn to ↑ of CKOUT_m, CKOUTn and CKOUT_m at same frequency and signal format PHASEOFFSET = 0 CKOUT_ALWAYS_ON = 1 SQ_ICAL = 1	—	—	100	ps
Phase Change due to Temperature Variation*	t_{TEMP}	Max phase changes from –40 to +85 °C	—	300	500	ps

***Note:** Input to output phase skew after an ICAL is not controlled and can assume any value.

Table 4. AC Specifications (Continued)
(V_{DD} = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
PLL Performance (fin = fout = 622.08 MHz; BW = 120 Hz; LVPECL)						
Lock Time	t_{LOCKMP}	Start of ICAL to ↓ of LOL	—	1	—	s
Settle Time	t_{SETTLE}	End of ICAL to F_{OUT} within 1 ppm of final value	—	5	—	s
Output Clock Phase Change	t_{P_STEP}	After clock switch f3 ≥ 128 kHz	—	200	—	ps
Closed Loop Jitter Peaking	J_{PK}		—	0.05	0.1	dB
Jitter Tolerance	J_{TOL}	Jitter Frequency ≥ Loop Bandwidth	5000/BW	—	—	ns pk-pk
Phase Noise fout = 622.08 MHz	CKO_{PN}	100 Hz Offset	—	–95	—	dBc/Hz
		1 kHz Offset	—	–110	—	dBc/Hz
		10 kHz Offset	—	–117	—	dBc/Hz
		100 kHz Offset	—	–118	—	dBc/Hz
		1 MHz Offset	—	–131	—	dBc/Hz
Spurious Noise	SP_{SPUR}	Max spur @ n x F3 (n ≥ 1, n x F3 < 100 MHz)	—	–67	—	dBc
***Note:** Input to output phase skew after an ICAL is not controlled and can assume any value.						

Table 5. Microprocessor Control
(V_{DD} = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
I^2C Bus Lines (SDA, SCL)						
Input Voltage Low	VIL_{I2C}		—	—	0.25 x V_{DD}	V
Input Voltage High	VIH_{I2C}		0.7 x V_{DD}	—	V_{DD}	V
Input Current	II_{I2C}	VIN = 0.1 x V_{DD} to 0.9 x V_{DD}	–10	—	10	µA
Hysteresis of Schmitt trigger inputs	$VHYS_{I2C}$	V_{DD} = 1.8V	0.1 x V_{DD}	—	—	V
		V_{DD} = 2.5 or 3.3 V	0.05 x V_{DD}	—	—	V
Output Voltage Low	VOL_{I2C}	V_{DD} = 1.8 V IO = 3 mA	—	—	0.2 x V_{DD}	V
		V_{DD} = 2.5 or 3.3 V IO = 3 mA	—	—	0.4	V

Table 5. Microprocessor Control (Continued)

(V_{DD} = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SPI Specifications						
Duty Cycle, SCLK	t_{DC}	SCLK = 10 MHz	40	—	60	%
Cycle Time, SCLK	t_c		100	—	—	ns
Rise Time, SCLK	t_r	20–80%	—	—	25	ns
Fall Time, SCLK	t_f	20–80%	—	—	25	ns
Low Time, SCLK	t_{lsc}	20–20%	30	—	—	ns
High Time, SCLK	t_{hsc}	80–80%	30	—	—	ns
Delay Time, SCLK Fall to SDO Active	t_{d1}		—	—	25	ns
Delay Time, SCLK Fall to SDO Transition	t_{d2}		—	—	25	ns
Delay Time, SS Rise to SDO Tri-state	t_{d3}		—	—	25	ns
Setup Time, SS to SCLK Fall	t_{su1}		25	—	—	ns
Hold Time, SS to SCLK Rise	t_{h1}		20	—	—	ns
Setup Time, SDI to SCLK Rise	t_{su2}		25	—	—	ns
Hold Time, SDI to SCLK Rise	t_{h2}		20	—	—	ns
Delay Time between Slave Selects	t_{cs}		25	—	—	ns

Table 6. Jitter Generation

Parameter	Symbol	Test Condition*		Min	Typ	Max	GR-253-Specification	Unit
		Measurement Filter	DSPLL BW[2]					
Jitter Gen OC-192	JGEN	0.02–80 MHz	120 Hz	—	4.2	—	30	ps_{PP}
				—	.27	—	N/A	ps_{rms}
		4–80 MHz	120 Hz	—	3.7	—	10	ps_{PP}
				—	.14	—	N/A	ps_{rms}
		0.05–80 MHz	120 Hz	—	4.4	—	10	ps_{PP}
				—	.26	—	1.0	ps_{rms}
Jitter Gen OC-48	JGEN	0.12–20 MHz	120 Hz	—	3.5	—	40.2	ps_{PP}
				—	.27	—	4.02	ps_{rms}

***Note:** Test conditions:
1. fIN = fOUT = 622.08 MHz
2. Clock input: LVPECL
3. Clock output: LVPECL
4. PLL bandwidth: 120 Hz
5. 114.285 MHz 3rd OT crystal used as XA/XB input
6. V_{DD} = 2.5 V
7. T_A = 85 °C

Table 7. Thermal Characteristics

(V_{DD} = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Value	Unit
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	40	C°/W

2. Typical Phase Noise Performance

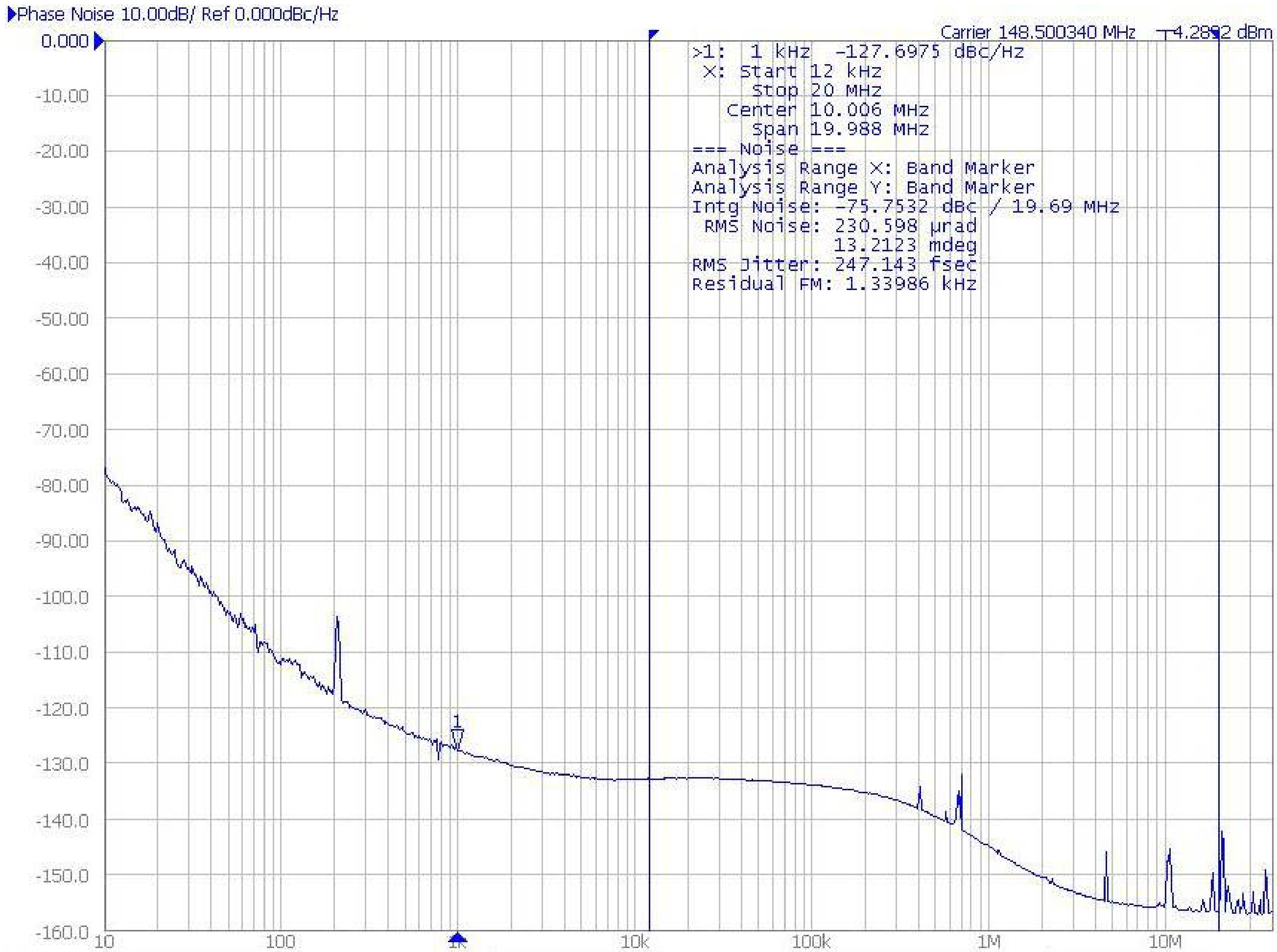


Figure 3. Broadcast Video

Jitter Bandwidth	Jitter (peak-peak)	Jitter (RMS)
10 Hz to 20 MHz	5.24 ps	484
Note: Number of samples: 8.91E9		

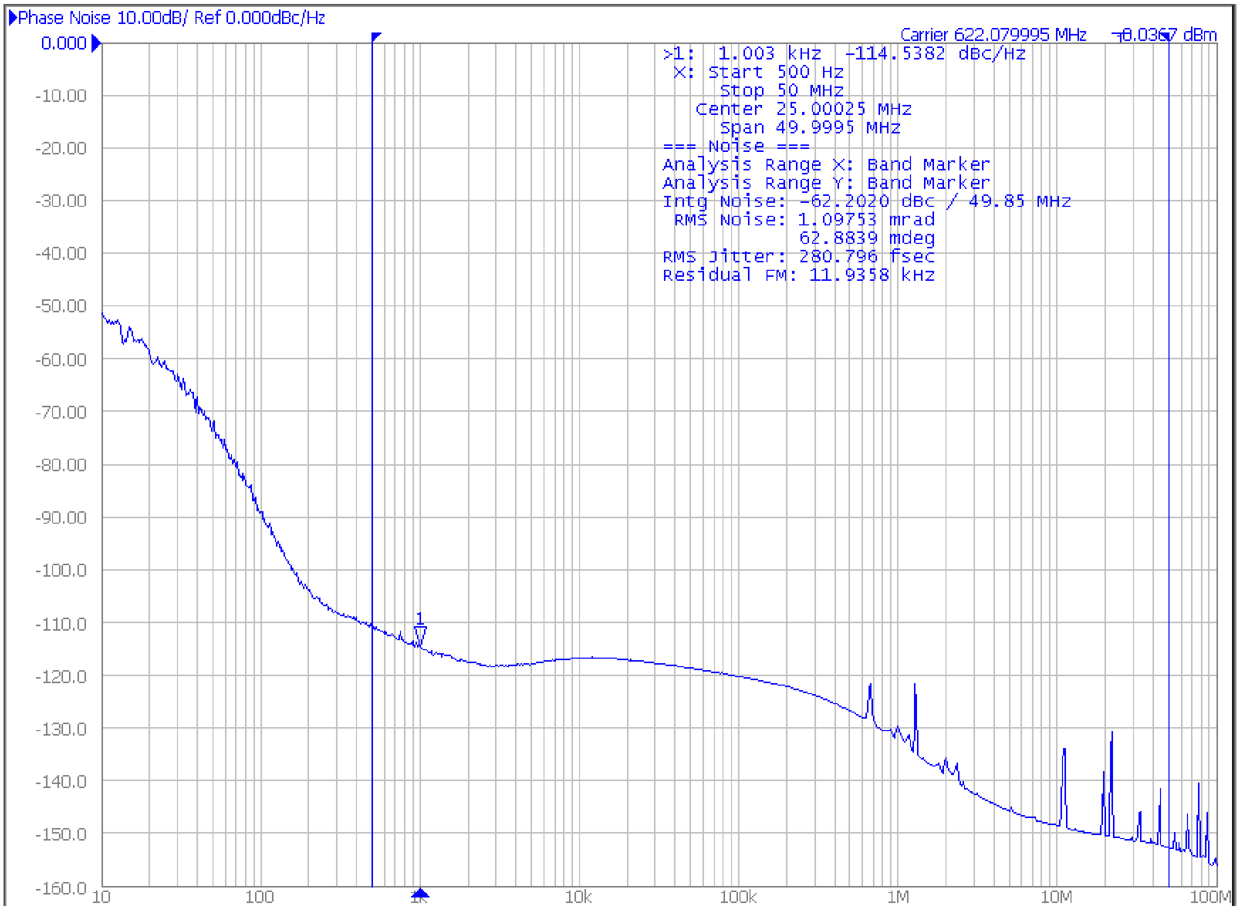


Figure 4. OTN/SONET/SDH Phase Noise

Note: Phase noise plot uses brick wall integration.

Jitter Bandwidth	Jitter, RMS
SONET_OC48, 12 kHz to 20 MHz	266 fs
SONET_OC192_A, 20 kHz to 80 MHz	283 fs
SONET_OC192_B, 4 MHz to 80 MHz	155 fs
SONET_OC192_C, 50 kHz to 80 MHz	275 fs
Brick Wall_800 Hz to 80 MHz	287 fs
Note: Jitter integration bands include low-pass (–20 dB/Dec) and hi-pass (–60 dB/Dec) roll-offs per Telecordia GR-253-CORE.	

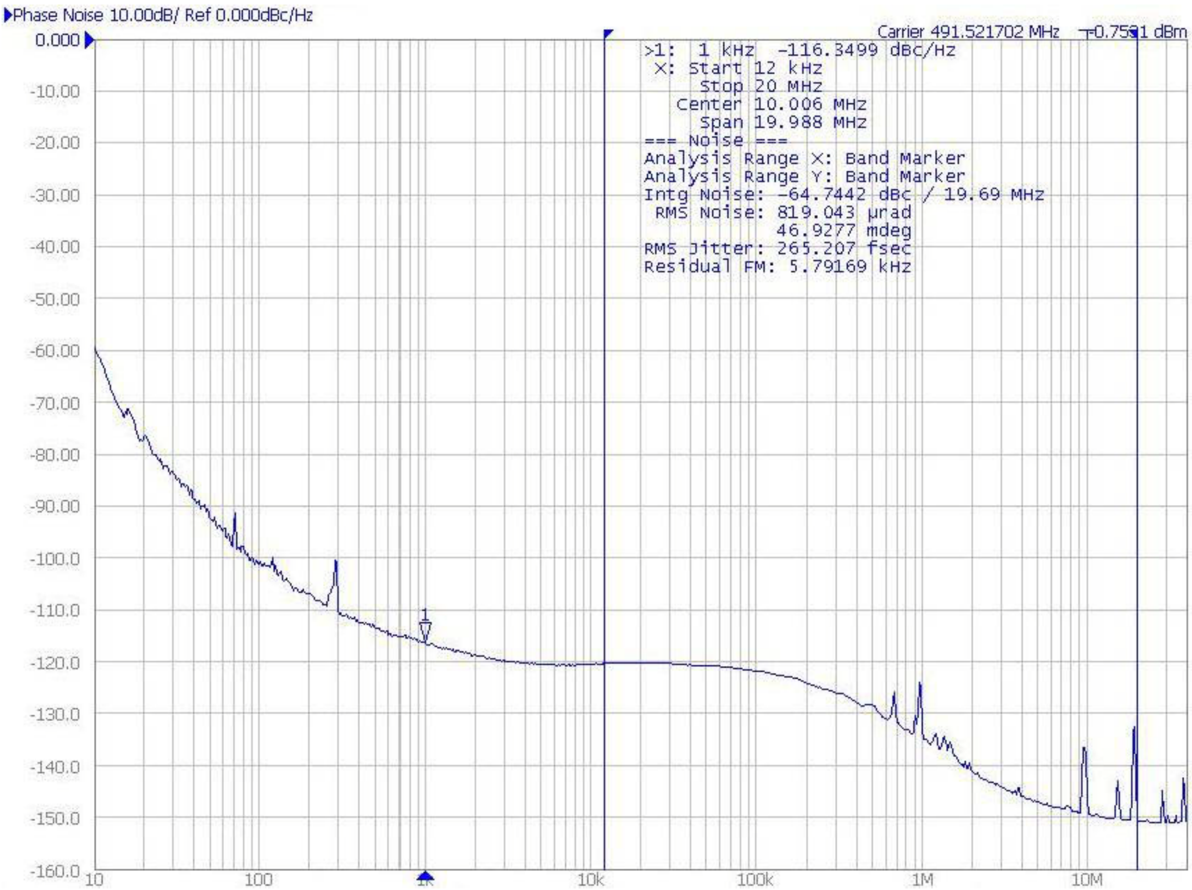
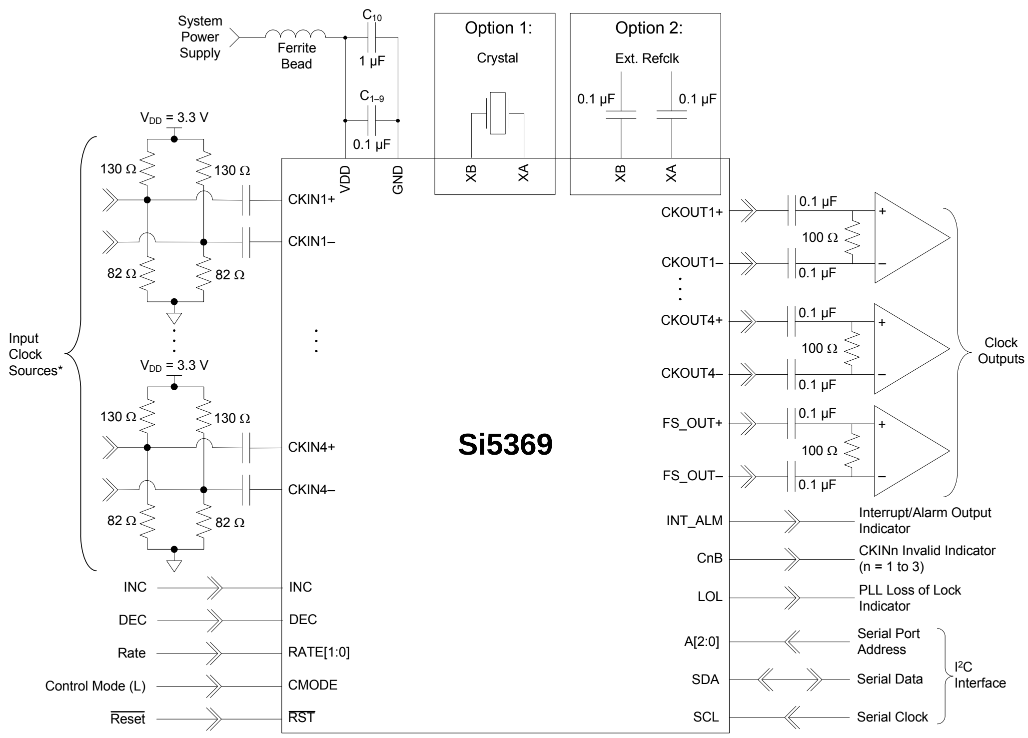


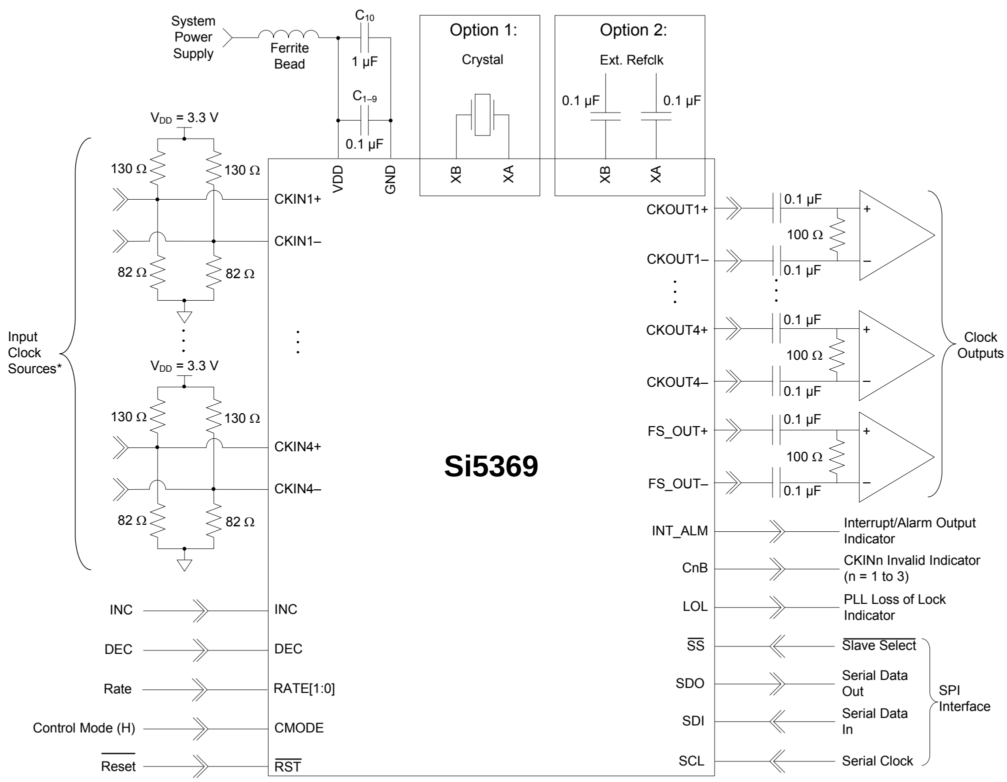
Figure 5. Wireless Base Station Phase Noise

Jitter Bandwidth	Jitter (peak-peak)	Jitter (RMS)
10 Hz to 20 MHz	7.28 ps	581
Note: Number of samples: 8.91E9		



***Note:** Assumes differential LVPECL termination (3.3 V) on clock inputs.

Figure 6. Si5369 Typical Application Circuit (I^2C Control Mode)



***Note:** Assumes differential LVPECL termination (3.3 V) on clock inputs.

Figure 7. Si5369 Typical Application Circuit (SPI Control Mode)

3. Functional Description

The Si5369 is a jitter-attenuating precision clock multiplier for applications requiring sub 1 ps rms jitter performance. The Si5369 accepts four clock inputs ranging from 2 kHz to 710 MHz and generates five clock outputs ranging from 2 kHz to 945 MHz and select frequencies to 1.4 GHz. The device provides virtually any frequency translation combination across this operating range. Independent dividers are available for every input clock and output clock, so the Si5369 can accept input clocks at different frequencies and it can generate output clocks at different frequencies. The Si5369 input clock frequency and clock multiplication ratio are programmable through an I^2C or SPI interface. Optionally, the fifth clock output can be configured as a 2 to 512 kHz SONET/SDH frame synchronization output that is phase aligned with one of the high-speed output clocks. Silicon Laboratories offers a PC-based software utility, DSPLL*sim*, that can be used to determine the optimum PLL divider settings for a given input frequency/clock multiplication ratio combination that minimizes phase noise and power consumption. This utility can be downloaded from http://www.silabs.com/timing (click on Documentation).

The Si5369 is based on Silicon Laboratories' 3rd-generation DSPLL® technology, which provides any-frequency synthesis and jitter attenuation in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The Si5369 PLL loop bandwidth is digitally programmable and supports a range from 4 to 525 Hz. The DSPLL*sim* software utility can be used to calculate valid loop bandwidth settings for a given input clock frequency/clock multiplication ratio.

The Si5369 supports hitless switching between input clocks in compliance with GR-253-CORE and GR-1244-CORE that greatly minimizes the propagation of phase transients to the clock outputs during an input clock transition (<200 ps typ). Manual, automatic revertive and non-revertive input clock switching options are available. The Si5369 monitors the four input clocks for loss-of-signal and provides a LOS alarm when it detects missing pulses on any of the four input clocks. The device monitors the lock status of the PLL. The lock detect algorithm works by continuously monitoring the phase of the input clock in relation to the phase of the feedback clock. The Si5369 monitors the frequency of CKIN1, CKIN2, CKIN3, and CKIN4 with respect to a selected reference frequency and generates a frequency offset alarm (FOS) if the threshold is exceeded. This FOS feature is available for SONET applications in which both the monitored frequency on CKIN1, CKIN3, and CKIN4 and the reference frequency are integer multiples of 19.44 MHz. Both Stratum 3/3E and SONET Minimum Clock (SMC) FOS thresholds are supported.

The Si5369 provides a digital hold capability that allows the device to continue generation of a stable output clock when the selected input reference is lost. During digital hold, the DSPLL generates an output frequency based on a historical average that existed a fixed amount of time before the error event occurred, eliminating the effects of phase and frequency transients that may occur immediately preceding digital hold.

The Si5369 has five differential clock outputs. The electrical format of the clock outputs is programmable to support LVPECL, LVDS, CML, or CMOS loads. If not required, unused clock outputs can be powered down to minimize power consumption. The phase difference between the selected input clock and the output clocks is adjustable in 200 ps increments for system skew control. In addition, the phase of one output clock may be adjusted in relation to the phase of the other output clock. The resolution varies from 800 ps to 2.2 ns depending on the PLL divider settings. Consult the DSPLL*sim* configuration software to determine the phase offset resolution for a given input clock/clock multiplication ratio combination. For system-level debugging, a bypass mode is available which drives the output clock directly from the input clock, bypassing the internal DSPLL. The device is powered by a single 1.8, 2.5, or 3.3 V supply.

3.1. External Reference

An external clock or a low-cost 114.285 MHz 3rd overtone crystal is typically used as part of a fixed-frequency oscillator within the DSPLL. This external reference is required for the device to operate. Silicon Laboratories recommends using a high-quality crystal. Specific recommendations may be found in the Family Reference Manual. An external clock from a high-quality OCXO or TCXO can also be used as a reference for the device.

In digital hold, the DSPLL remains locked to this external reference. Any changes in the frequency of this reference when the DSPLL is in digital hold, will be tracked by the output of the device. Note that crystals can have temperature sensitivities.

3.2. Further Documentation

Consult the Silicon Laboratories Any-Frequency Precision Clock Family Reference Manual (FRM) for detailed information about the Si5369. Additional design support is available from Silicon Laboratories through your distributor.

Silicon Laboratories has developed a PC-based software utility called DSPLL*sim* to simplify device configuration, including frequency planning and loop bandwidth selection. The FRM and this utility can be downloaded from http://www.silabs.com/timing; click on Documentation.

4. Register Map

All register bits that are not defined in this map should always be written with the specified Reset Values. The writing to these bits of values other than the specified Reset Values may result in undefined device behavior. Registers not listed, such as Register 64, should never be written to.

<table>
<tr><th>Register</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>0</td><td></td><td>FREE_RUN</td><td>CKOUT_ ALWAYS_ ON</td><td></td><td></td><td></td><td>BYPASS_ REG</td><td></td></tr>
<tr><td>1</td><td colspan="2">CK_PRIOR4 [1:0]</td><td colspan="2">CK_PRIOR3 [1:0]</td><td colspan="2">CK_PRIOR2 [1:0]</td><td colspan="2">CK_PRIOR1 [1:0]</td></tr>
<tr><td>2</td><td colspan="4">BWSEL_REG [3:0]</td><td></td><td></td><td></td><td></td></tr>
<tr><td>3</td><td colspan="2">CKSEL_REG [1:0]</td><td>DHOLD</td><td>SQ_ICAL</td><td></td><td></td><td></td><td></td></tr>
<tr><td>4</td><td colspan="2">AUTOSEL_REG [1:0]</td><td></td><td colspan="5">HIST_DEL [4:0]</td></tr>
<tr><td>5</td><td colspan="2">ICMOS [1:0]</td><td colspan="3">SFOUT2_REG [2:0]</td><td colspan="3">SFOUT1_REG [2:0]</td></tr>
<tr><td>6</td><td></td><td></td><td colspan="3">SFOUT4_REG [2:0]</td><td colspan="3">SFOUT3_REG [2:0]</td></tr>
<tr><td>7</td><td></td><td></td><td colspan="3">SFOUT5_REG [2:0]</td><td colspan="3">FOSREFSEL [2:0]</td></tr>
<tr><td>8</td><td colspan="2">HLOG_4 [1:0]</td><td colspan="2">HLOG_3 [1:0]</td><td colspan="2">HLOG_2 [1:0]</td><td colspan="2">HLOG_1 [1:0]</td></tr>
<tr><td>9</td><td colspan="5">HIST_AVG [4:0]</td><td></td><td colspan="2">HLOG_5 [1:0]</td></tr>
<tr><td>10</td><td></td><td></td><td>DSBL5_ REG</td><td></td><td>DSBL4_ REG</td><td>DSBL3_ REG</td><td>DSBL2_ REG</td><td>DSBL1_ REG</td></tr>
<tr><td>11</td><td colspan="3"></td><td></td><td>PD_CK4</td><td>PD_CK3</td><td>PD_CK2</td><td>PD_CK1</td></tr>
<tr><td>19</td><td>FOS_EN</td><td colspan="2">FOS_THR [1:0]</td><td colspan="2">VALTIME [1:0]</td><td colspan="3">LOCKT [2:0]</td></tr>
<tr><td>20</td><td></td><td></td><td>ALRMOUT_ PIN</td><td>CK3_BAD_ PIN</td><td>CK2_BAD_ PIN</td><td>CK1_BAD_ PIN</td><td>LOL_PIN</td><td>INT_PIN</td></tr>
<tr><td>21</td><td></td><td></td><td></td><td>CK4_ACTV_ PIN</td><td>CK3_ACTV_ PIN</td><td>CK2_ACTV_ PIN</td><td>CK1_ACTV_ PIN</td><td>CKSEL_PIN</td></tr>
<tr><td>22</td><td></td><td></td><td></td><td></td><td>CK_ACTV_ POL</td><td>CK_BAD_ POL</td><td>LOL_POL</td><td>INT_POL</td></tr>
<tr><td>23</td><td></td><td></td><td></td><td>LOS4_MSK</td><td>LOS3_MSK</td><td>LOS2_MSK</td><td>LOS1_MSK</td><td>LOSX_MSK</td></tr>
<tr><td>24</td><td></td><td></td><td></td><td>FOS4_MSK</td><td>FOS3_MSK</td><td>FOS2_MSK</td><td>FOS1_MSK</td><td>LOL_MSK</td></tr>
<tr><td>25</td><td colspan="3">N1_HS [2:0]</td><td></td><td colspan="4">NC1_LS [19:16]</td></tr>
<tr><td>26</td><td colspan="8">NC1_LS [15:8]</td></tr>
<tr><td>27</td><td colspan="8">NC1_LS [7:0]</td></tr>
<tr><td>28</td><td></td><td></td><td></td><td></td><td colspan="4">NC2_LS [19:16]</td></tr>
<tr><td>29</td><td colspan="8">NC2_LS [15:8]</td></tr>
<tr><td>30</td><td colspan="8">NC2_LS [7:0]</td></tr>
<tr><td>31</td><td></td><td></td><td></td><td></td><td colspan="4">NC3_LS [19:16]</td></tr>
</table>

Register	D7	D6	D5	D4	D3	D2	D1	D0
32	NC3_LS [15:8]							
33	NC3_LS [7:0]							
34					NC4_LS [19:16]			
35	NC4_LS [15:8]							
36	NC4_LS [7:0]							
37					NC5_LS [19:16]			
38	NC5_LS [15:8]							
39	NC5_LS [7:0]							
40	N2_HS [2:0]				N2_LS [19:16]			
41	N2_LS [15:8]							
42	N2_LS [7:0]							
43						N31_ [18:16]		
44	N31_[15:8]							
45	N31_ [7:0]							
46						N32_ [18:16]		
47	N31_ [15:8]							
48	N32_[7:0]							
49						N33_[18:16]		
50	N33_[15:8]							
51	N33_[7:0]							
52						N34_[18:16]		
53	N34_[15:8]							
54	N34_[7:0]							
55			CLKIN2RATE_[2:0]			CLKIN1RATE[2:0]		
56			CLKIN4RATE_[2:0]			CLKIN3RATE[2:0]		
128					CK4_ACTV_ REG	CK3_ACTV_ REG	CK2_ACTV_ REG	CK1_ACTV_ REG
129				LOS4_INT	LOS3_INT	LOS2_INT	LOS1_INT	LOSX_INT
130		DIGHOLD-VALID		FOS4_INT	FOS3_INT	FOS2_INT	FOS1_INT	LOL_INT
131				LOS4_FLG	LOS3_FLG	LOS2_FLG	LOS1_FLG	LOSX_FLG

Register	D7	D6	D5	D4	D3	D2	D1	D0
132			FOS4_FLG	FOS3_FLG	FOS2_FLG	FOS1_FLG	LOL_FLG	
134	PARTNUM_RO [11:4]							
135	PARTNUM_RO [3:0]				REVID_RO [3:0]			
136	RST_REG	ICAL						
137								FASTLOCK
138					LOS4_EN [1:1]	LOS3_EN [1:1]	LOS2_EN [1:1]	LOS1_EN [1:1]
139	LOS4_EN [0:0]	LOS3_EN [0:0]	LOS2_EN [0:0]	LOS1_EN [0:0]	FOS4_EN	FOS3_EN	FOS2_EN	FOS1_EN
140	INDEPENDENTSKEW1 [7:0]							
141	INDEPENDENTSKEW2 [7:0]							
142	INDEPENDENTSKEW3 [7:0]							
143	INDEPENDENTSKEW4 [7:0]							
144	INDEPENDENTSKEW5 [7:0]							

5. Register Descriptions

Register 0.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		FREE_RUN	CKOUT_ALWAYS_ON				BYPASS_REG	
Type	R	R/W	R/W	R	R	R	R/W	R

Reset value = 0001 0100

Bit	Name	Function
7	Reserved	
6	FREE_RUN	**Free Run.** Internal to the device, route XA/XB to CKIN2. This allows the device to lock to its external reference. 0: Disable Free Run 1: Enable
5	CKOUT_ALWAYS_ON	**CKOUT Always On.** This will bypass the SQ_ICAL function. Output will be available even if SQ_ICAL is on and ICAL is not complete or successful. See Table 8. 0: Squelch output until part is calibrated (ICAL). 1: Provide an output. Note: The frequency may be significantly off until the part is calibrated.
4:2	Reserved	
1	BYPASS_REG	**Bypass Register.** This bit enables or disables the PLL bypass mode. Use is only valid when the part is in digital hold or before the first ICAL. 0: Normal operation 1: Bypass mode. Selected input clock is connected to CKOUT buffers, bypass-ing PLL.
0	Reserved	

Register 1.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CK_PRIOR4 [1:0]		CK_PRIOR3 [1:0]		CK_PRIOR2 [1:0]		CK_PRIOR1 [1:0]	
Type	R/W		R/W		R/W		R/W	

Reset value = 1110 0100

Bit	Name	Function
7:6	CK_PRIOR4 [1:0]	**CK_PRIOR 4.** Selects which of the input clocks will be 4th priority in the autoselection state machine. 00: CKIN0 is 4th priority. 01: CKIN1 is 4th priority. 10: CKIN2 is 4th priority. 11: CKIN3 is 4th priority.
5:4	CK_PRIOR3 [1:0]	**CK_PRIOR 3.** Selects which of the input clocks will be 3rd priority in the autoselection state machine. 00: CKIN0 is 3rd priority. 01: CKIN1 is 3rd priority. 10: CKIN2 is 3rd priority. 11: CKIN3 is 3rd priority.
3:2	CK_PRIOR2 [1:0]	**CK_PRIOR 2.** Selects which of the input clocks will be 2nd priority in the autoselection state machine. 00: CKIN1 is 2nd priority. 01: CKIN2 is 2nd priority. 10: CKIN3 is 2nd priority. 11: CKIN4 is 2nd priority.
1:0	CK_PRIOR1 [1:0]	**CK_PRIOR 1.** Selects which of the input clocks will be 1st priority in the autoselection state machine. 00: CKIN0 is 1st priority. 01: CKIN1 is 1st priority. 10: CKIN2 is 1st priority. 11: CKIN3 is 1st priority.

Register 2.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	BWSEL_REG [3:0]				Reserved			
Type	R/W				R			

Reset value = 0100 0010

Bit	Name	Function
7:4	BWSEL_REG [3:0]	**BWSEL_REG.** Selects nominal f3dB bandwidth for PLL. See the DSPLLsim for settings. After BWSEL_REG is written with a new value, an ICAL is required for the change to take effect.
3:0	Reserved	

Register 3.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CKSEL_REG [1:0]		DHOLD	SQ_ICAL	Reserved			
Type	R/W		R/W	R/W	R			

Reset value = 0000 0101

Bit	Name	Function
7:6	CKSEL_REG [1:0]	**CKSEL_REG.** If the device is operating in manual register-based clock selection mode (AUTOSEL_REG = 00), and CKSEL_PIN = 0, then these bits select which input clock will be the active input clock. If CKSEL_PIN = 1, the CKSEL[1:0] input pins continue to control clock selection and CKSEL_REG is of no consequence. 00: CKIN_1 selected. 01: CKIN_2 selected. 10: CKIN_3 selected. 11: CKIN_4 selected.
5	DHOLD	**DHOLD.** Forces the part into digital hold. This bit overrides all other manual and automatic clock selection controls. 0: Normal operation. 1: Force digital hold mode. Overrides all other settings and ignores the quality of all of the input clocks.
4	SQ_ICAL	**SQ_ICAL.** This bit determines if the output clocks will remain enabled or be squelched (disabled) during an internal calibration. See Table 8. 0: Output clocks enabled during ICAL. 1: Output clocks disabled during ICAL.
3:0	Reserved	

Register 4.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	AUTOSEL_REG [1:0]		Reserved	HIST_DEL [4:0]				
Type	R/W		R	R/W				

Reset value = 0001 0010

Bit	Name	Function
7:6	AUTOSEL_REG [1:0]	**AUTOSEL_REG [1:0].** Selects method of input clock selection to be used. 00: Manual (either register or pin controlled. See CKSEL_PIN). 01: Automatic Non-Revertive 10: Automatic Revertive 11: Reserved
5	Reserved	
4:0	HIST_DEL [4:0]	**HIST_DEL [4:0].** Selects amount of delay to be used in generating the history information MHIST, the value of M used during Digital Hold.

Register 5.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ICMOS [1:0]		SFOUT2_REG [2:0]			SFOUT1_REG [2:0]		
Type	R/W		R/W			R/W		

Reset value = 1110 1101

Bit	Name	Function
7:6	ICMOS [1:0]	**ICMOS [1:0].** When the output buffer is set to CMOS mode, these bits determine the output buffer drive strength. The first number below refers to 3.3 V operation; the second to 1.8 V operation. These values assume CKOUT+ is tied to CKOUT-. 00: 8 mA/2 mA 01: 16 mA/4 mA 10: 24 mA/6 mA 11: 32 mA (3.3 V operation)/8mA (1.8 V operation)
5:3	SFOUT2_REG [2:0]	**SFOUT2_REG [2:0]** Controls output signal format and disable for CKOUT2 output buffer. The LVPECL and CMOS output formats draw more current than either LVDS or CML; however, there are restrictions in the allowed output format pin settings so that the maximum power dissipation for the TQFP devices is limited when they are operated at 3.3 V. When there are four enabled LVPECL or CMOS outputs, the fifth output must be disabled. When there are five enabled outputs, there can be no more than three outputs that are either LVPECL or CMOS. 000: Reserved 001: Disable 010: CMOS 011: Low swing LVDS 100: Reserved 101: LVPECL 110: CML 111: LVDS
2:0	SFOUT1_REG [2:0]	**SFOUT1_REG [2:0]** Controls output signal format and disable for CKOUT1 output buffer. The LVPECL and CMOS output formats draw more current than either LVDS or CML; however, there are restrictions in the allowed output format pin settings so that the maximum power dissipation for the TQFP devices is limited when they are operated at 3.3 V. When there are four enabled LVPECL or CMOS outputs, the fifth output must be disabled. When there are five enabled outputs, there can be no more than three outputs that are either LVPECL or CMOS. 000: Reserved 001: Disable 010: CMOS 011: Low swing LVDS 100: Reserved 101: LVPECL 110: CML 111: LVDS

Register 6.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			SFOUT4_REG [2:0]			SFOUT3_REG [2:0]		
Type	R	R	R/W			R/W		

Reset value = 0010 1100

Bit	Name	Function
7:6	Reserved	
5:3	SFOUT4_REG [2:0]	**SFOUT4_REG [2:0].** Controls output signal format and disable for CKOUT4 output buffer. The LVPECL and CMOS output formats draw more current than either LVDS or CML; however, there are restrictions in the allowed output format pin settings so that the maximum power dissipation for the TQFP devices is limited when they are operated at 3.3 V. When there are four enabled LVPECL or CMOS outputs, the fifth output must be disabled. When there are five enabled outputs, there can be no more than three outputs that are either LVPECL or CMOS. 000: Reserved 001: Disable 010: CMOS 011: Low swing LVDS 100: Reserved 101: LVPECL 110: CML 111: LVDS
2:0	SFOUT3_REG [2:0]	**SFOUT3_REG [2:0].** Controls output signal format and disable for CKOUT3 output buffer. The LVPECL and CMOS output formats draw more current than either LVDS or CML; however, there are restrictions in the allowed output format pin settings so that the maximum power dissipation for the TQFP devices is limited when they are operated at 3.3 V. When there are four enabled LVPECL or CMOS outputs, the fifth output must be disabled. When there are five enabled outputs, there can be no more than three outputs that are either LVPECL or CMOS. 000: Reserved 001: Disable 010: CMOS 011: Low swing LVDS 100: Reserved 101: LVPECL 110: CML 111: LVDS

Register 7.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved		SFOUT5_REG [2:0]			FOSREFSEL [2:0]		
Type	R		R/W			R/W		

Reset value = 0010 1010

Bit	Name	Function
7:6	Reserved.	
5:3	SFOUT5_REG [2:0]	**SFOUT5_REG [2:0]** Controls output signal format and disable for CKOUT5 output buffer. The LVPECL and CMOS output formats draw more current than either LVDS or CML; however, there are restrictions in the allowed output format pin settings so that the maximum power dissipation for the TQFP devices is limited when they are operated at 3.3 V. When there are four enabled LVPECL or CMOS outputs, the fifth output must be disabled. When there are five enabled outputs, there can be no more than three outputs that are either LVPECL or CMOS. 000: Reserved 001: Disable 010: CMOS 011: Low swing LVDS 100: Reserved 101: LVPECL 110: CML 111: LVDS
2:0	FOSREFSEL [2:0]	**FOSREFSEL [2:0].** Selects which input clock is used as the reference frequency for Frequency Off-Set (FOS) alarms. 000: XA/XB (External reference) 001: CKIN1 010: CKIN2 011: CKIN3 100: CKIN4 101: Reserved 110: Reserved 111: Reserved

Register 8.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	HLOG_4[1:0]		HLOG_3[1:0]		HLOG_2[1:0]		HLOG_1[1:0]	
Type	R/W		R/W		R/W		R/W	

Reset value = 0000 0000

Bit	Name	Function
7:6	HLOG_4 [1:0]	**HLOG_4 [1:0].** 00: Normal operation 01: Holds CKOUT4 output at static logic 0. Entrance and exit from this state will occur without glitches or runt pulses. 10: Holds CKOUT4 output at static logic 1. Entrance and exit from this state will occur without glitches or runt pulses. 11: Reserved
5:4	HLOG_3 [1:0]	**HLOG_3 [1:0].** 00: Normal operation 01: Holds CKOUT3 output at static logic 0. Entrance and exit from this state will occur without glitches or runt pulses. 10: Holds CKOUT3 output at static logic 1. Entrance and exit from this state will occur without glitches or runt pulses. 11: Reserved.
3:2	HLOG_2 [1:0]	**HLOG_2 [1:0].** 00: Normal operation 01: Holds CKOUT2 output at static logic 0. Entrance and exit from this state will occur without glitches or runt pulses. 10: Holds CKOUT2 output at static logic 1. Entrance and exit from this state will occur without glitches or runt pulses. 11: Reserved.
1:0	HLOG_1 [1:0]	**HLOG_1 [1:0].** 00: Normal operation 01: Holds CKOUT1 output at static logic 0. Entrance and exit from this state will occur without glitches or runt pulses. 10: Holds CKOUT1 output at static logic 1. Entrance and exit from this state will occur without glitches or runt pulses. 11: Reserved

Register 9.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	HIST_AVG [4:0]						HLOG_5 [1:0]	
Type	R/W					R	R/W	

Reset value = 1100 0000

Bit	Name	Function
7:3	HIST_AVG [4:0]	**HIST_AVG [4:0].** Selects amount of averaging time to be used in generating MHIST, the value of M used during digital hold. See Family Reference Manual for settings.
2	Reserved	
1:0	HLOG_5 [1:0]	**HLOG_5 [1:0].** 00: Normal Operation 01: Holds CKOUT5 output at static logic 0. Entrance and exit from this state will occur without glitches or runt pulses. 10: Holds CKOUT5 output at static logic 1. Entrance and exit from this state will occur without glitches or runt pulses. 11: Reserved

Register 10.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			DSBL5_REG	Reserved	DSBL4_REG	DSBL3_REG	DSBL2_REG	DSBL1_REG
Type	R	R	R/W	R	R/W	R/W	R	R

Reset value = 0000 0000

Bit	Name	Function
7:6	Reserved	
5	DSBL5_REG	**DSBL5_REG.** This bit controls the powerdown and disable of the CKOUT5 output buffer. If disable mode is selected, the NC5_LS output divider is also powered down. 0: CKOUT5 enabled. 1: CKOUT5 disabled.
4	Reserved	
3	DSBL4_REG	**DSBL4_REG.** This bit controls the powerdown and disable of the CKOUT4 output buffer. If disable mode is selected, the NC4 output divider is also powered down. 0'b=CKOUT4 enabled 1'b=CKOUT4 disabled
2	DSBL3_REG	**DSBL3_REG.** This bit controls the powerdown and disable of the CKOUT3 output buffer. If disable mode is selected, the NC3 output divider is also powered down. 0: CKOUT3 enabled 1: CKOUT3 disabled
1	DSBL2_REG	**DSBL2_REG.** This bit controls the powerdown and disable of the CKOUT2 output buffer. If disable mode is selected, the NC2 output divider is also powered down. 0: CKOUT2 enabled 1: CKOUT2 disabled
0	DSBL1_REG	**DSBL1_REG.** This bit controls the powerdown and disable of the CKOUT1 output buffer. If disable mode is selected, the NC1 output divider is also powered down. 0: CKOUT1 enabled 1: CKOUT1 disabled

Register 11.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					PD_CK4	PD_CK3	PD_CK2	PD_CK1
Type	R	R	R	R	R/W	R/W	R/W	R/W

Reset value = 0100 0000

Bit	Name	Function
7:4	Reserved	
3	PD_CK4	**PD_CK4.** This bit controls the powerdown of the CKIN4 input buffer. 0: CKIN4 enabled 1: CKIN4 disabled
2	PD_CK3	**PD_CK3.** This bit controls the powerdown of the CKIN3 input buffer. 0: CKIN3 enabled 1: CKIN3 disabled
1	PD_CK2	**PD_CK2.** This bit controls the powerdown of the CKIN2 input buffer. 0: CKIN2 enabled 1: CKIN2 disabled
0	PD_CK1	**PD_CK1.** This bit controls the powerdown of the CKIN1 input buffer. 0: CKIN1 enabled 1: CKIN1 disabled

Register 19.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	FOS_EN	FOS_THR [1:0]		VALTIME [1:0]		LOCKT [2:0]		
Type	R/W	R/W		R/W		R/W		

Reset value = 0010 1100

Bit	Name	Function
7	FOS_EN	**FOS_EN.** Frequency offset enable globally disables FOS. See the individual FOS enables (FOSx_EN, register 139). 00: FOS disable 01: FOS enabled by FOSx_EN
6:5	FOS_THR [1:0]	**FOS_THR [1:0].** Frequency Offset at which FOS is declared: 00: ± 11 to 12 ppm Stratum 3/3E compliant, with a Stratum 3/3E used for REFCLK. 01: ± 48 to 49 ppm (SMC). 10: ± 30 ppm SONET Minimum Clock (SMC), with a Stratum 3/3E used for REFCLK. 11: ± 200 ppm
4:3	VALTIME [1:0]	**VALTIME [1:0].** Sets amount of time for input clock to be valid before the associated alarm is removed. 00: 2 ms 01: 100 ms 10: 200 ms 11: 13 s
2:0	LOCKT [2:0]	**LOCKT [2:0].** Sets retrigger interval for one shot monitoring phase detector output. One shot is triggered by phase slip in DSPLL. Refer to the Family Reference Manual for more details. 000: 106 ms 001: 53 ms 010: 26.5 ms 011: 13.3 ms 100: 6.6 ms 101: 3.3 ms 110: 1.66 ms 111: 833 µs

Register 20.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			ALRMOUT_PIN	CK3_BAD_PIN	CK2_BAD_PIN	CK1_BAD_PIN	LOL_PIN	INT_PIN
Type	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Reset value = 0011 1100

Bit	Name	Function
7:6	Reserved	
5	ALRMOUT_PIN	**ALRMOUT_PIN.** The ALRMOUT status can be reflected on the ALRMOUT output pin. The request to reflect the interrupt status on this pin (INT_PIN=1) overrides the ALRMOUT_PIN request. 0: ALRMOUT not reflected on output pin. Output pin disabled if INT_PIN=0. 1: ALRMOUT reflected to output pin if INT_PIN=0. If INT_PIN=1, interrupt status appears on the output pin and ALRMOUT is not available on an output pin.
4	CK3_BAD_PIN	**CK3_BAD_PIN.** The CK3_BAD status can be reflected on the C3B output pin. 0: C3B output pin tristated 1: C3B status reflected to output pin
3	CK2_BAD_PIN	**CK2_BAD_PIN.** The CK2_BAD status can be reflected on the C2B output pin. 0: C2B output pin tristated 1: C2B status reflected to output pin
2	CK1_BAD_PIN	**CK1_BAD_PIN.** The CK1_BAD status can be reflected on the C1B output pin. 0: C1B output pin tristated 1: C1B status reflected to output pin
1	LOL_PIN	**LOL_PIN.** The LOL_INT status bit can be reflected on the LOL output pin. 0: LOL output pin tristated 1: LOL_INT status reflected to output pin
0	INT_PIN	**INT_PIN.** Reflects the interrupt status on the INT output pin. 0: Interrupt status not displayed on INT output pin. If ALRMOUT_PIN = 0, output pin is tristated. 1: Interrupt status reflected to output pin. ALRMOUT_PIN ignored.

Register 21.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				CK4_ACTV_PIN	CK3_ACTV_PIN	CK2_ACTV_PIN	CK1_ACTV_PIN	CKSEL_ PIN
Type	R	R	R	R/W	R/W	R/W	R/W	R/W

Reset value = 1111 1111

Bit	Name	Function
7:5	Reserved	
4	CK4_ACTV_PIN	**CK4_ACTV_PIN.** If the CKSEL[1]/CK4_ACTV pin is functioning as the CK4_ACTV output (see CKSEL[1]/CK4_ACTV pin description on CK4_ACTV), the CK4_ACTV_REG status bit can be reflected to the CK4_ACTV output pin using the CK4_ACTV_PIN enable function. 0: CK4_ACTV output pin tristated 1: CK4_ACTV status reflected to output pin.
3	CK3_ACTV_PIN	**CK3_ACTV_PIN.** If the CKSEL[0]/CK3_ACTV pin is functioning as the CK3_ACTV output (see CKSEL[0]/CK3_ACTV pin description on CK3_ACTV), the CK3_ACTV_REG status bit can be reflected to the CK3_ACTV output pin using the CK3_ACTV_PIN enable function. 0: CK3_ACTV output pin tristated. 1: CK3_ACTV status reflected to output pin.
2	CK2_ACTV_PIN	**CK2_ACTV_PIN.** The CK2_ACTV_REG status bit can be reflected to the CK2_ACTV output pin using the CK2_ACTV_PIN enable function. 0: CK2_ACTV output pin tristated. 1: CK2_ACTV status reflected to output pin.
1	CK1_ACTV_PIN	**CK1_ACTV_PIN.** The CK1_ACTV_REG status bit can be reflected to the CK1_ACTV output pin using the CK1_ACTV_PIN enable function. 0: CK1_ACTV output pin tristated. 1: CK1_ACTV status reflected to output pin.
0	CKSEL_PIN	**CKSEL_PIN.** If manual clock selection is being used, clock selection can be controlled via the CKSEL_REG[1:0] register bits or the CKSEL[1:0] input pins. 0: CKSEL pins ignored. CKSEL_REG[1:0] register bits control clock selection. 1: CKSEL[1:0] input pins controls clock selection.

Register 22.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					CK_ACTV_POL	CK_BAD_ POL	LOL_POL	INT_POL
Type	R	R	R	R	R/W	R/W	R/W	R/W

Reset value = 1101 1111

Bit	Name	Function
7:4	Reserved	
3	CK_ACTV_ POL	**CK_ACTV_POL.** Sets the active polarity for the CK1_ACTV, CK2_ACTV, CK3_ACTV, and CK4_ACTV signals when reflected on an output pin. 0: Active low 1: Active high
2	CK_BAD_ POL	**CK_BAD_POL.** Sets the active polarity for the C1B, C2B, C3B, and ALRMOUT signals when reflected on output pins. 0: Active low 1: Active high
1	LOL_POL	**LOL_POL.** Sets the active polarity for the LOL status when reflected on an output pin. 0: Active low 1: Active high
0	INT_POL	**INT_POL.** Sets the active polarity for the interrupt status when reflected on the INT_ALM output pin. 0: Active low 1: Active high

Register 23.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				LOS4_MSK	LOS3_MSK	LOS2_ MSK	LOS1_ MSK	LOSX_ MSK
Type	R	R	R	R/W	R/W	R/W	R/W	R/W

Reset value = 0001 1111

Bit	Name	Function
7:5	Reserved	
4	LOS4_MSK	**LOS4_MSK.** Determines if a LOS on CKIN4 (LOS4_FLG) is used in the generation of an interrupt. Writes to this register do not change the value held in the LOS4_FLG register. 0: LOS4 alarm triggers active interrupt on INT output (if INT_PIN=1). 1: LOS4_FLG ignored in generating interrupt output.
3	LOS3_MSK	**LOS3_MSK.** Determines if a LOS on CKIN3 (LOS3_FLG) is used in the generation of an interrupt. Writes to this register do not change the value held in the LOS3_FLG register. 0: LOS3 alarm triggers active interrupt on INT output (if INT_PIN=1). 1: LOS3_FLG ignored in generating interrupt output.
2	LOS2_MSK	**LOS2_MSK.** Determines if a LOS on CKIN2 (LOS2_FLG) is used in the generation of an interrupt. Writes to this register do not change the value held in the LOS2_FLG register. 0: LOS2 alarm triggers active interrupt on INT output (if INT_PIN=1). 1: LOS2_FLG ignored in generating interrupt output.
1	LOS1_MSK	**LOS1_MSK.** Determines if a LOS on CKIN1 (LOS1_FLG) is used in the generation of an interrupt. Writes to this register do not change the value held in the LOS1_FLG register. 0: LOS1 alarm triggers active interrupt on INT output (if INT_PIN=1). 1: LOS1_FLG ignored in generating interrupt output.
0	LOSX_MSK	**LOSX_MSK.** Determines if a LOS on XA/XB(LOSX_FLG) is used in the generation of an interrupt. Writes to this register do not change the value held in the LOSX_FLG register. 0: LOSX alarm triggers active interrupt on INT output (if INT_PIN=1). 1: LOSX_FLG ignored in generating interrupt output.

Register 24.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				FOS4_MSK	FOS3_MSK	FOS2_MSK	FOS1_MSK	LOL_MSK
Type	R	R	R	R/W	R/W	R/W	R/W	R/W

Reset value = 0011 1111

Bit	Name	Function
7:5	Reserved	
4	FOS4_MSK	**FOS4_MSK.** Determines if the FOS4_FLG is used to in the generation of an interrupt. Writes to this register do not change the value held in the FOS4_FLG register. 0: FOS4 alarm triggers active interrupt on INToutput (if INT_PIN = 1). 1: FOS4_FLG ignored in generating interrupt output.
3	FOS3_MSK	**FOS3_MSK.** Determines if the FOS3_FLG is used in the generation of an interrupt. Writes to this register do not change the value held in the FOS3_FLG register. 0: FOS3 alarm triggers active interrupt on INT output (if INT_PIN = 1). 1: FOS3_FLG ignored in generating interrupt output.
2	FOS2_MSK	**FOS2_MSK.** Determines if the FOS2_FLG is used in the generation of an interrupt. Writes to this register do not change the value held in the FOS2_FLG register. 0: FOS2 alarm triggers active interrupt on INT output (if INT_PIN = 1). 1: FOS2_FLG ignored in generating interrupt output.
1	FOS1_MSK	**FOS1_MSK.** Determines if the FOS1_FLG is used in the generation of an interrupt. Writes to this register do not change the value held in the FOS1_FLG register. 0: FOS1 alarm triggers active interrupt on INT output (if INT_PIN = 1). 1: FOS1_FLG ignored in generating interrupt output.
0	LOL_MSK	**LOL_MSK.** Determines if the LOL_FLG is used in the generation of an interrupt. Writes to this register do not change the value held in the LOL_FLG register. 0: LOL alarm triggers active interrupt on INT output (if INT_PIN = 1). 1: LOL_FLG ignored in generating interrupt output.

Register 25.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N1_HS [2:0]				NC1_LS [19:16]			
Type	R/W			R	R/W			

Reset value = 0010 0000

Bit	Name	Function
7:5	N1_HS [2:0]	**N1_HS [2:0].** Sets value for N1 high speed divider which drives NCn_LS (n = 1 to 4) low-speed divider. 000: N1 = 4 Note: Changing the coarse skew via the INC pin is disabled for this value. 001: N1 = 5 010: N1 = 6 011: N1 = 7 100: N1 = 8 101: N1 = 9 110: N1 = 10 111: N1 = 11
4	Reserved	
3:0	NC1_LS [19:16]	**NC1_LS [19:0].** Sets value for NC1 low-speed divider, which drives CKOUT1 output. Must be 0 or odd. 00000000000000000000 = 1 00000000000000000001 = 2 00000000000000000011 = 4 00000000000000000101 = 6 ... 11111111111111111111 = 2^{20} Valid divider values=[1, 2, 4, 6, ..., 2^{20}].

Register 26.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	NC1_LS [15:8]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	NC1_LS [15:8]	**NC1_LS [15:8].** See Register 25.

Register 27.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	NC1_LS [7:0]							
Type	R/W							

Reset value = 0011 0001

Bit	Name	Function
7:0	NC1_LS [7:0]	**NC1_LS [7:0].** See Register 25.

Register 28.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					NC2_LS [19:16]			
Type	R	R	R	R	R/W			

Reset value = 0000 0000

Bit	Name	Function
7:4	Reserved	
3:0	NC1_LS [19:0]	**NC2_LS [19:16].** Sets value for NC2 low-speed divider, which drives CKOUT2 output. Must be 0 or odd. 00000000000000000000 = 1 00000000000000000001 = 2 00000000000000000011 = 4 00000000000000000101 = 6 ... 11111111111111111111 = 2^{20} Valid divider values = [1, 2, 4, 6, ..., 2^{20}]

Register 29.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	NC2_LS [15:8]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	NC2_LS [15:8]	**NC2_LS [15:8].** See Register 28.

Register 30.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	NC2_LS [7:0]							
Type	R/W							

Reset value = 0011 0001

Bit	Name	Function
7:0	NC2_LS [7:0]	**NC2_LS [7:0].** See Register 28.

Register 31.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					NC3_LS [19:16]			
Type	R	R	R	R	R/W			

Reset value = 0000 0000

Bit	Name	Function
7:4	Reserved	
3:0	NC3_LS [19:0]	**NC3_LS [19:0.** Sets value for NC3 low-speed divider, which drives CKOUT3 output. Must be 0 or odd. 00000000000000000000 = 1 00000000000000000001 = 2 00000000000000000011 = 4 00000000000000000101 = 6 ... 11111111111111111111 = 2^{20} Valid divider values = [1, 2, 4, 6, ..., 2^{20}].

Register 32.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	NC3_LS [15:8]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	NC3_LS [15:8]	**NC3_LS [15:8].** See Register 31.

Register 33.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	NC3_LS [7:0]							
Type	R/W							

Reset value = 0011 0001

Bit	Name	Function
7:0	NC3_LS [7:0]	**NC3_LS [7:0].** See Register 31.

Register 34.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					NC4_LS [19:16]			
Type	R	R	R	R	R/W			

Reset value = 0000 0000

Bit	Name	Function
7:4	Reserved	
3:0	NC4_LS [19:0]	**NC4_LS [19:0].** Sets value for NC4 low-speed divider, which drives CKOUT4 output. Must be 0 or odd. 00000000000000000000 = 1 00000000000000000001 = 2 000000000000000000011 = 4 000000000000000000101 = 6 ... 111111111111111111 = 2^{20} Valid divider values = [1, 2, 4, 6, ..., 2^{20}].

Register 35.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	NC4_LS [15:8]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	NC4_LS [15:8]	**NC4_LS [15:8].** See Register 34.

Register 36.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	NC4_LS [7:0]							
Type	R/W							

Reset value = 0011 0001

Bit	Name	Function
7:0	NC4_LS [7:0]	**NC4_LS [7:0].** See Register 34.

Register 37.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					NC5_LS [19:16]			
Type	R	R	R	R	R/W			

Reset value = 0000 0000

Bit	Name	Function
7:4	Reserved	
3:0	NC5_LS [19:0]	**NC5_LS [19:0].** Sets value for NC5 low-speed divider, which drives CKOUT5 output. Must be 0 or odd. When CK_CONFIG=0: 00000000000000000000 = 1 00000000000000000001 = 2 000000000000000000011 = 4 000000000000000000101 = 6 ... 11111111111111111111 = 2^{20} Valid divider values = [1, 2, 4, 6, ..., 2^{20}]. When CK_CONFIG = 1, maximum value limited to 2^{19}.: 00000000000000000000 = 1 00000000000000000001 = 2 000000000000000000011 = 4 000000000000000000101 = 6 ... 01111111111111111111 = 2^{19} Valid divider values = [1, 2, 4, 6, ..., 2^{19}].

Register 38.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	NC5_LS [15:8]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	NC5_LS [15:8]	**NC5_LS [15:8].** See Register 37.

Register 39.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	NC5_LS [7:0]							
Type	R/W							

Reset value = 0011 0001

Bit	Name	Function
7:0	NC5_LS [7:0]	**NC5_LS [7:0].** See Register 37.

Register 40.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N2_HS [2:0]				N2_LS [19:16]			
Type	R/W			R	R/W			

Reset value = 1100 0000

Bit	Name	Function
7:5	N2_HS [2:0]	**N2_HS [2:0].** Sets value for N2 high speed divider which drives NCn_LS (n = 1 to 4) low-speed divider. 000:4 001:5 010:6 011:7 100:8 101:9 110:10 111:11.
4	Reserved	
3:0	N2_LS [19:16]	**NC2_LS [19:0].** Sets value for N2 low-speed divider, which drives phase detector. 00000000000000000001 = 2 00000000000000000011 = 4 00000000000000000101 = 6 ... 11111111111111111111 = 2^{20} Valid divider values = [2, 4, 6, ..., 2^{20}].

Register 41.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N2_LS [15:8]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	N2_LS [15:8]	**N2_LS [15:8].** See Register 40.

Register 42.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N2_LS [7:0]							
Type	R/W							

Reset value = 1111 1001

Bit	Name	Function
7:0	N2_LS [7:0]	**N2_LS [7:0].** See Register 40.

Register 43.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						N31 [18:16]		
Type	R	R	R	R	R	R/W		

Reset value = 0000 0000

Bit	Name	Function
7:3	Reserved	
2:0	N31 [18:0]	**N31 [18:0].** Sets value for input divider for CKIN1. 0000000000000000000 = 1 0000000000000000001 = 2 0000000000000000010 = 3 ... 1111111111111111111 = 2^{19} Valid divider values=[1, 2, 3, ..., 2^{19}].

Register 44.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N31 [15:8]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	N31 [15:8]	**N31 [15:8].** See Register 43.

Register 45.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N31 [7:0]							
Type	R/W							

Reset value = 0000 1001

Bit	Name	Function
7:0	N31 [7:0]	**N31 [7:0].** See Register 43.

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Register 46.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						N32_[18:16]		
Type	R	R	R	R	R	R/W		

Reset value = 0000 0000

Bit	Name	Function
7:3	Reserved	
2:0	N32_[18:0]	**N32_[18:0].** Sets value for input divider for CKIN2. 0000000000000000000 = 1 0000000000000000001 = 2 0000000000000000010 = 3 ... 1111111111111111111 = 2^{19} Valid divider values=[1, 2, 3, ..., 2^{19}].

Register 47.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N32_[15:8]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	N32_[15:8]	**N32_[15:8].** See Register 46.

Register 48.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N32_[7:0]							
Type	R/W							

Reset value = 0000 1001

Bit	Name	Function
7:0	N32_[7:0]	**N32_[7:0].** See Register 46.

Register 49.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						N33_[18:0]		
Type	R	R	R	R	R	R/W		

Reset value = 0000 0000

Bit	Name	Function
18:0	N33_[18:0]	**N33_[18:0].** Sets value for input divider for CKIN3. 0000000000000000000 = 1 0000000000000000001 = 2 0000000000000000010 = 3 ... 1111111111111111111 = 2^{19} Valid divider values=[1, 2, 3, ..., 2^{19}].

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Register 50.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N33_[15:8]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	N33_[15:8]	**N33_[15:8].** See Register 49.

Register 51.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N33_[7:0]							
Type	R/W							

Reset value = 0000 1001

Bit	Name	Function
7:0	N33_[7:0]	**N33_[7:0].** See Register 49.

Register 52.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							N34_[18:16]	
Type	R	R	R	R	R		R/W	

Reset value = 0000 0000

Bit	Name	Function
7:3	Reserved	
2:0	N34_[18:0]	**N34_[18:0].** Sets value for input divider for CKIN4. 0000000000000000000 = 1 0000000000000000001 = 2 0000000000000000010 = 3 ... 1111111111111111111 = 2^{19} Valid divider values=[1, 2, 3, ..., 2^{19}].

Register 53.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				N34_[15:8]				
Type				R/W				

Reset value = 0000 0000

Bit	Name	Function
7:0	N34_[15:8]	**N34_[15:8].** See Register 52.

Register 54.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N34_[7:0]							
Type	R/W							

Reset value = 0000 1001

Bit	Name	Function
7:0	N34_[15:8]	**N34_[7:0].** See Register 52.

Register 55.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			CLKIN2RATE_[2:0]			CLKIN1RATE[2:0]		
Type	R	R	R/W			R/W		

Reset value = 0000 0000

Bit	Name	Function
7:6	Reserved	
5:3	CLKIN2RATE[2:0]	**CLKIN2RATE[2:0].** CKINn frequency selection for FOS alarm monitoring. 000: 10–27 MHz 001: 25–54 MHz 002: 50–105 MHz 003: 95–215 MHz 004: 190–435 MHz 005: 375–710 MHz 006: Reserved 007: Reserved
2:0	CLKIN1RATE [2:0]	**CLKIN1RATE[2:0].** CKINn frequency selection for FOS alarm monitoring. 000: 10–27 MHz 001: 25–54 MHz 002: 50–105 MHz 003: 95–215 MHz 004: 190–435 MHz 005: 375–710 MHz 006: Reserved 007: Reserved

Register 56.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			CLKIN4RATE_[2:0]			CLKIN3RATE[2:0]		
Type	R	R	R/W			R/W		

Reset value = 0000 0000

Bit	Name	Function
7:6	Reserved	
5:3	CLKIN4RATE[2:0]	**CLKIN4RATE[2:0].** CKINn frequency selection for FOS alarm monitoring. 000: 10–27 MHz 001: 25–54 MHz 002: 50–105 MHz 003: 95–215 MHz 004: 190–435 MHz 005: 375–710 MHz 006: Reserved 007: Reserved
2:0	CLKIN3RATE [2:0]	**CLKIN3RATE[2:0].** CKINn frequency selection for FOS alarm monitoring. 000: 10–27 MHz 001: 25–54 MHz 002: 50–105 MHz 003: 95–215 MHz 004: 190–435 MHz 005: 375–710 MHz 006: Reserved 007: Reserved

Register 128.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					CK4_ACTV_REG	CK3_ACTV_REG	CK2_ACTV_REG	CK1_ACTV_REG
Type	R	R	R	R	R	R	R	R

Reset value = 0010 0000

Bit	Name	Function
7:4	Reserved	
3	CK4_ACTV_REG	**CK4_ACTV_REG.** Indicates if CKIN4 is currently the active clock for the PLL input. 0: CKIN4 is not the active input clock. Either it is not selected or LOS4_INT is 1. 1: CKIN_4 is the active input clock.
2	CK3_ACTV_REG	**CK3_ACTV_REG.** Indicates if CKIN3 is currently the active clock for the PLL input. 0: CKIN3 is not the active input clock - either it is not selected or LOS3_INT is 1. 1: CKIN3 is the active input clock.
1	CK2_ACTV_REG	**CK2_ACTV_REG.** Indicates if CKIN2 is currently the active clock for the PLL input. 0: CKIN2 is not the active input clock. Either it is not selected or LOS2_INT is 1. 1: CKIN2 is the active input clock.
0	CK1_ACTV_REG	**CK1_ACTV_REG.** Indicates if CKIN1 is currently the active clock for the PLL input. 0: CKIN1 is not the active input clock. Either it is not selected or LOS1_INT is 1. 1: CKIN1 is the active input clock.

Register 129.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				LOS4_INT	LOS3_INT	LOS2_INT	LOS1_INT	LOSX_INT
Type	R	R	R	R	R	R	R	R

Reset value = 0001 1110

Bit	Name	Function
7:5	Reserved	
4	LOS4_INT	**LOS4_INT.** Indicates the LOS status on CKIN4. 0: Normal operation. 1: Internal loss-of-signal alarm on CKIN4 input.
3	LOS3_INT	**LOS3_INT.** Indicates the LOS status on CKIN3. 0: Normal operation. 1: Internal loss-of-signal alarm on CKIN3 input.
2	LOS2_INT	**LOS2_INT.** Indicates the LOS status on CKIN2. 0: Normal operation. 1: Internal loss-of-signal alarm on CKIN2 input.
1	LOS1_INT	**LOS1_INT.** Indicates the LOS status on CKIN1. 0: Normal operation. 1: Internal loss-of-signal alarm on CKIN1 input.
0	LOSX_INT	**LOSX_INT.** Indicates the LOS status of the external reference on the XA/XB pins. 0: Normal operation. 1: Internal loss-of-signal alarm on XA/XB reference clock input.

Register 130.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		DIGHOLDVALID		FOS4_INT	FOS3_INT	FOS2_INT	FOS1_INT	LOL_INT
Type	R	R	R	R	R	R	R	R

Reset value = 0000 0001

Bit	Name	Function
7	Reserved	
6	DIGHOLDVALID	**Digital Hold Valid.** Indicates if the digital hold circuit has enough samples of a valid clock to meet digital hold specifications. 0: Indicates digital filter has not been filled. The digital hold output frequency (from the filter) is not valid. 1: Indicates digital hold filter has been filled. The digital hold output frequency is valid.
5	Reserved	
4	FOS4_INT	**FOS4_INT.** CKIN4 Frequency Offset Status. 0: Normal operation. 1: Internal frequency offset alarm on CKIN4 input.
3	FOS3_INT	**FOS3_INT.** CKIN3 Frequency Offset Status. 0: Normal operation. 1: Internal frequency offset alarm on CKIN3 input.
2	FOS2_INT	**FOS2_INT.** CKIN2 Frequency Offset Status. 0: Normal operation. 1: Internal frequency offset alarm on CKIN2 input.
1	FOS1_INT	**FOS1_INT.** **CKIN1 Frequency Offset Status.** 0: Normal operation. 1: Internal frequency offset alarm on CKIN1 input.
0	LOL_INT	**LOL_INT.** PLL Loss of Lock Status. 0: PLL locked. 1: PLL unlocked.

Register 131.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				LOS4_FLG	LOS3_FLG	LOS2_FLG	LOS1_FLG	LOSX_FLG
Type	R	R	R	R/W	R/W	R/W	R/W	R/W

Reset value = 0001 1111

Bit	Name	Function
7:5	Reserved	
4	LOS4_FLG	**LOS4_FLG.** CKIN4 Loss-of-Signal Flag. 0: Normal operation. 1: Held version of LOS4_INT. Generates active output interrupt if output interrupt pin is enabled (INT_PIN=1) and if not masked by LOS4_MSK bit. Flag cleared by writing location to 0.
3	LOS3_FLG	**LOS3_FLG.** CKIN3 Loss-of-Signal Flag. 0: Normal operation. 1: Held version of LOS3_INT. Generates active output interrupt if output interrupt pin is enabled (INT_PIN=1) and if not masked by LOS3_MSK bit. Flag cleared by writing location to 0.
2	LOS2_FLG	**LOS2_FLG.** CKIN2 Loss-of-Signal Flag. 0: Normal operation. 1: Held version of LOS2_INT. Generates active output interrupt if output interrupt pin is enabled (INT_PIN=1) and if not masked by LOS2_MSK bit. Flag cleared by writing location to 0.
1	LOS1_FLG	**LOS1_FLG.** CKIN1 Loss-of-Signal Flag. 0: Normal operation. 1: Held version of LOS1_INT. Generates active output interrupt if output interrupt pin is enabled (INT_PIN=1) and if not masked by LOS1_MSK bit. Flag cleared by writing location to 0.
0	LOSX_FLG	**LOSX_FLG.** External reference (signal on pins XA/XB) Loss-of-Signal Flag. 0: Normal operation. 1: Held version of LOSX_INT. Generates active output interrupt if output interrupt pin is enabled (INT_PIN=1) and if not masked by LOSX_MSK bit. Flag cleared by writing location to 0.

Register 132.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			FOS4_FLG	FOS3_FLG	FOS2_FLG	FOS1_FLG	LOL_FLG	
Type	R	R	R/W	R/W	R/W	R/W	R/W	R

Reset value = 0000 0010

Bit	Name	Function
7:6	Reserved	
5	FOS4_FLG	**FOS4_FLG.** CLKIN_4 Frequency Offset Flag. 0: Normal operation. 1: Held version of FOS4_INT. Generates active output interrupt if output interrupt pin is enabled (INT_PIN=1) and if not masked by FOS4_MSK bit. Flag cleared by writing location to 0.
4	FOS3_FLG	**FOS3_FLG.** CLKIN_3 Frequency Offset Flag. 0: Normal operation. 1: Held version of FOS3_INT. Generates active output interrupt if output interrupt pin is enabled (INT_PIN=1) and if not masked by FOS3_MSK bit. Flag cleared by writing location to 0.
3	FOS2_FLG	**FOS2_FLG.** CLKIN_2 Frequency Offset Flag. 0: Normal operation. 1: Held version of FOS2_INT. Generates active output interrupt if output interrupt pin is enabled (INT_PIN = 1) and if not masked by FOS2_MSK bit. Flag cleared by writing location to 0.
2	FOS1_FLG	**FOS1_FLG.** CLKIN_1 Frequency Offset Flag. 0: Normal operation. 1: Held version of FOS1_INT. Generates active output interrupt if output interrupt pin is enabled (INT_PIN = 1) and if not masked by FOS1_MSK bit. Flag cleared by writing location to 0.
1	LOL_FLG	**LOL_FLG.** PLL Loss of Lock Flag. 0: PLL locked 1: Held version of LOL_INT. Generates active output interrupt if output interrupt pin is enabled (INT_PIN = 1) and if not masked by LOL_MSK bit. Flag cleared by writing location to 0.
0	Reserved	

Register 134.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PARTNUM_RO [11:4]							
Type	R							

Reset value = 0000 0100

Bit	Name	Function
7:0	PARTNUM_RO [11:0]	**PARTNUM_RO [11:0].** Device ID: 0000 0100 0100'b=Si5369

Register 135.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PARTNUM_RO [3:0]				REVID_RO [3:0]			
Type	R				R			

Reset value = 0100 0010

Bit	Name	Function
7:4	PARTNUM_RO [3:0]	**PARTNUM_RO [3:0].** See Register 134.
3:0	REVID_RO [3:0]	**REVID_RO [3:0].** Indicates revision number of device. 0000: Revision A 0001: Revision B 0010: Revision C Other codes: Reserved

Register 136.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RST_REG	ICAL						
Type	R/W	R/W	R	R	R	R	R	R

Reset value = 0000 0000

Bit	Name	Function
7	RST_REG	**RST_REG.** Internal Reset. 0: Normal operation. 1: Reset of all internal logic. Outputs tristated or disabled during reset.
6	ICAL	**ICAL.** Start an Internal Calibration Sequence. For proper operation, the device must go through an internal calibration sequence. ICAL is a self-clearing bit. Writing a one to this location initiates an ICAL. The calibration is complete once the LOL alarm goes low. A valid stable clock (within 100 ppm) must be present to begin ICAL. **Note:** Any divider, CLKINn_RATE or BWSEL_REG changes require an ICAL to take effect. Changes in SFOUTn_REG, PD_CKn, or DSBLn_REG will cause a random change in skew until an ICAL is completed. 0: Normal operation. 1: Writing a "1" initiates internal self-calibration. Upon completion of internal self-calibration, ICAL is internally reset to zero.
5:0	Reserved	

Register 137.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved							FASTLOCK
Type	R							R/W

Reset value = 0000 0000

Bit	Name	Function
7:1	Reserved	Do not modify.
0	FASTLOCK	This bit must be set to 1 to enable FASTLOCK. This improves initial lock time by dynamically changing the loop bandwidth.

Register 138.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved				LOS4_EN[1:1]	LOS3_EN[1:1]	LOS2_EN[1:1]	LOS1_EN [1:1]
Type	R				R/W	R/W	R/W	R/W

Reset value = 0000 1111

Bit	Name	Function
7:4	Reserved	
3	LOS4_EN [1:0]	**LOS4_EN [1:0].** **Note:** LOS1_EN is split between two registers. 00: Disable LOS monitoring. 01: Reserved. 10: Enable LOSA monitoring. 11: Enable LOS monitoring. LOSA is a slower and less sensitive version of LOS. See the Family Reference Manual for details.
2	LOS3_EN [1:0]	**LOS3_EN [1:0].** **Note:** LOS1_EN is split between two registers. 00: Disable LOS monitoring. 01: Reserved. 10: Enable LOSA monitoring. 11: Enable LOS monitoring. LOSA is a slower and less sensitive version of LOS. See the Family Reference Manual for details.

1	LOS2_EN [1:0]	**LOS2_EN [1:0].** **Note:** LOS1_EN is split between two registers. 00: Disable LOS monitoring. 01: Reserved. 10: Enable LOSA monitoring. 11: Enable LOS monitoring. LOSA is a slower and less sensitive version of LOS. See the Family Reference Manual for details.
0	LOS1_EN [1:0]	**LOS1_EN [1:0].** **Note:** LOS1_EN is split between two registers. 00: Disable LOS monitoring. 01: Reserved. 10: Enable LOSA monitoring. 11: Enable LOS monitoring. LOSA is a slower and less sensitive version of LOS. See the Family Reference Manual for details.

Register 139.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	LOS4_EN [0:0]	LOS3_EN [0:0]	LOS2_EN [0:0]	LOS1_EN [0:0]	FOS4_EN	FOS3_EN	FOS2_EN	FOS1_EN
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset value = 1111 1111

Bit	Name	Function
7	LOS4_EN [0:0]	**LOS4_EN [0:0].** **Enable CKIN1 LOS Monitoring on the Specified Input (1 of 2).** **Note:** LOS1_EN is split between two registers. 00: Disable LOS monitoring. 01: Reserved. 10: Enable LOSA monitoring. 11: Enable LOS monitoring. LOSA is a slower and less sensitive version of LOS. See the family reference manual for details.
6	LOS3_EN [0:0]	**LOS3_EN [0:0].** **Enable CKIN1 LOS Monitoring on the Specified Input (1 of 2).** **Note:** LOS1_EN is split between two registers. 00: Disable LOS monitoring. 01: Reserved. 10: Enable LOSA monitoring. 11: Enable LOS monitoring. LOSA is a slower and less sensitive version of LOS. See the family reference manual for details.
5	LOS2_EN [0:0]	**LOS2_EN.** **Enable CKIN1 LOS Monitoring on the Specified Input (1 of 2).** **Note:** LOS1_EN is split between two registers. 00: Disable LOS monitoring. 01: Reserved. 10: Enable LOSA monitoring. 11: Enable LOS monitoring. LOSA is a slower and less sensitive version of LOS. See the family reference manual for details.
4	LOS1_EN [0:0]	**LOS1_EN [0:0].** **Enable CKIN1 LOS Monitoring on the Specified Input (1 of 2).** **Note:** LOS1_EN is split between two registers. 00: Disable LOS monitoring. 01: Reserved. 10: Enable LOSA monitoring. 11: Enable LOS monitoring. LOSA is a slower and less sensitive version of LOS. See the family reference manual for details.

Bit	Name	Function
3	FOS4_EN	**FOS4_EN.** **Enables FOS on a Per Channel Basis.** 0: Disable FOS monitoring. 1: Enable FOS monitoring.
2	FOS3_EN	**FOS3_EN.** **Enables FOS on a Per Channel Basis.** 0: Disable FOS monitoring. 1: Enable FOS monitoring.
1	FOS2_EN	**FOS2_EN.** **Enables FOS on a Per Channel Basis.** 0: Disable FOS monitoring. 1: Enable FOS monitoring.
0	FOS1_EN	**FOS1_EN.** **Enables FOS on a Per Channel Basis.** 0: Disable FOS monitoring. 1: Enable FOS monitoring.

Register 140.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	INDEPENDENTSKEW1[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	INDEPENDENTSKEW1[7:0]	**INDEPENDENTSKEW1 [7:0].** 8 bit field that represents a twos complement of the phase offset in terms of clocks from the high speed output divider.

Register 141.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	INDEPENDENTSKEW2[7:0]							
Type	R/W							

Reset value = 0000 0001

Bit	Name	Function
7:0	INDEPENDENTSKEW2[7:0]	**INDEPENDENTSKEW2.** 8 bit field that represents a twos complement of the phase offset in terms of clocks from the high speed output divider.

Register 142.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	INDEPENDENTSKEW3 [7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	INDEPENDENTSKEW3[7:0]	**INDEPENDENTSKEW3 .** 8 bit field that represents a twos complement of the phase offset in terms of clocks from the high speed output divider.

Register 143.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	INDEPENDENTSKEW4[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	INDEPEND-ENTSKEW4[7:0]	**INDEPENDENTSKEW4.** 8 bit field that represents a twos complement of the phase offset in terms of clocks from the high speed output divider.

Register 144.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	INDEPENDENTSKEW5[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	INDEPENDENTSKEW5[7:0]	**INDEPENDENTSKEW5.** 8 bit field that represents a twos complement of the phase offset in terms of clocks from the high speed output divider when CK_CONFIG = 0.

Table 8. CKOUT_ALWAYS_ON and SQICAL Truth Table

CKOUT_ALWAYS_ON	SQICAL	Results	Output to Output Skew Preserved?
0	0	CKOUT OFF until after the first ICAL	N
0	1	CKOUT OFF until after the first successful ICAL (i.e., when LOL is low)	Y
1	0	CKOUT always ON, including during an ICAL	N
1	1	CKOUT always ON, including during an ICAL	Y

Table 9 lists all of the register locations that should be followed by an ICAL after their contents are changed.

Table 9. Register Locations Requiring ICAL

Addr	Register
0	BYPASS_REG
0	CKOUT_ALWAYS_ON
1	CK_PRIOR4
1	CK_PRIOR3
1	CK_PRIOR2
1	CK_PRIOR1
2	BWSEL_REG
4	HIST_DEL
5	ICMOS
7	FOSREFSEL
9	HIST_AVG
10	DSBL5_REG
10	DSBL4_REG
10	DSBL3_REG
10	DSBL2_REG
10	DSBL1_REG
11	PD_CK2
11	PD_CK1
19	FOS_EN
19	FOS_THR
19	VALTIME
19	LOCKT
25	N1_HS
26	NC1_LS
28	NC2_LS
31	NC3_LS
34	NC4_LS
37	NC5_LS

Table 9. Register Locations Requiring ICAL

Addr	Register
40	N2_HS
40	N2_LS
43	N31
46	N32
49	N33
51	N34
55	CLKIN2RATE
55	CLKIN1RATE
56	CLKIN4RATE
56	CLKIN3RATE

6. Pin Descriptions: Si5369

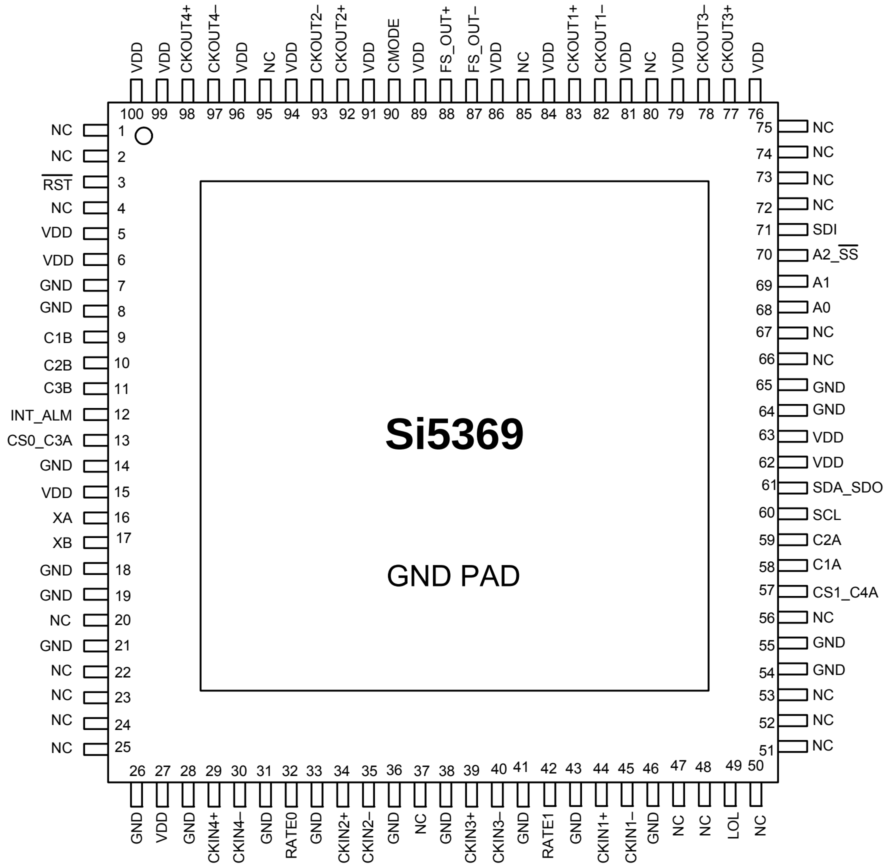

Table 10. Si5369 Pin Descriptions

Pin #	Pin Name	I/O	Signal Level	Description
1, 2, 4, 20, 22, 23, 24, 25, 37, 47, 48, 50, 51, 52, 53, 56, 66, 67, 72, 73, 74, 75, 80, 85, 95	NC			**No Connect.** These pins must be left unconnected for normal operation.
3	$\overline{\text{RST}}$	I	LVCMOS	**External Reset.** Active low input that performs external hardware reset of device. Resets all internal logic to a known state and forces the device registers to their default value. Clock outputs are disabled during reset. The part must be programmed after a reset or power-on to get a clock output. See Family Reference Manual for details. This pin has a weak pull-up.
Note: Internal register names are indicated by underlined italics, e.g., *INT_PIN*. See Si5369 Register Map.				

Table 10. Si5369 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
5, 6, 15, 27, 62, 63, 76, 79, 81, 84, 86, 89, 91, 94, 96, 99, 100	V_{DD}	Vdd	Supply	**V_{DD}.** The device operates from a 1.8, 2.5, or 3.3 V supply. Bypass capacitors should be associated with the following V_{DD} pins: Pins — Bypass Cap 5, 6 — 0.1 µF 15 — 0.1 µF 27 — 0.1 µF 62, 63 — 0.1 µF 76, 79 — 1.0 µF 81, 84 — 0.1 µF 86, 89 — 0.1 µF 91, 94 — 0.1 µF 96, 99, 100 — 0.1 µF
7, 8, 14, 18, 19, 21, 26, 28, 31, 33, 36, 38, 41, 43, 46, 54, 55, 64, 65	GND	GND	Supply	**Ground.** This pin must be connected to system ground. Minimize the ground path impedance for optimal performance.
9	C1B	O	LVCMOS	**CKIN1 Invalid Indicator.** This pin performs the *CK1_BAD* function if *CK1_BAD_PIN* = 1 and is tristated if *CK1_BAD_PIN* = 0. Active polarity is controlled by *CK_BAD_POL*. 0 = No alarm on CKIN1. 1 = Alarm on CKIN1.
10	C2B	O	LVCMOS	**CKIN2 Invalid Indicator.** This pin performs the *CK2_BAD* function if *CK2_BAD_PIN* = 1 and is tristated if *CK2_BAD_PIN* = 0. Active polarity is controlled by *CK_BAD_POL*. 0 = No alarm on CKIN2. 1 = Alarm on CKIN2.
11	C3B	O	LVCMOS	**CKIN3 Invalid Indicator.** This pin performs the *CK3_BAD* function if *CK3_BAD_PIN* = 1 and is tristated if *CK3_BAD_PIN* = 0. Active polarity is controlled by *CK_BAD_POL*. 0 = No alarm on CKIN3. 1 = Alarm on CKIN3.
12	INT_ALM	O	LVCMOS	**Interrupt/Alarm Output Indicator.** This pin functions as a maskable interrupt output with active polarity controlled by the *INT_POL* register bit. The INT output function can be turned off by setting *INT_PIN* = 0. If the ALRMOUT function is desired instead on this pin, set *ALRMOUT_PIN* = 1 and *INT_PIN* = 0. 0 = *ALRMOUT* not active. 1 = *ALRMOUT* active. The active polarity is controlled by *CK_BAD_POL*. If no function is selected, the pin tristates.

Note: Internal register names are indicated by underlined italics, e.g., *INT_PIN*. See Si5369 Register Map.

Table 10. Si5369 Pin Descriptions (Continued)

<table>
<tr><th>Pin #</th><th>Pin Name</th><th>I/O</th><th>Signal Level</th><th>Description</th></tr>
<tr><td>13
57</td><td>CS0_C3A
CS1_C4A</td><td>I/O</td><td>LVCMOS</td><td>Input Clock Select/CKIN3 or CKIN4 Active Clock Indicator.
Input: If manual clock selection is chosen, and if CKSEL_PIN = 1, the CKSEL pins control clock selection and the CKSEL_REG bits are ignored.
<table>
<tr><th>CS[1:0]</th><th>Active Input Clock</th></tr>
<tr><td>00</td><td>CKIN1</td></tr>
<tr><td>01</td><td>CKIN2</td></tr>
<tr><td>10</td><td>CKIN3</td></tr>
<tr><td>11</td><td>CKIN4</td></tr>
</table>
If CKSEL_PIN = 0, the CKSEL_REG register bits control this function and these inputs tristate. If configured as inputs, these pins must not float.
Output: If auto clock selection is enabled, then they serve as the CKIN_n active clock indicator.
0 = CKIN3 (CKIN4) is not the active input clock
1 = CKIN3 (CKIN4) is currently the active input to the PLL
The CKn_ACTV_REG bit always reflects the active clock status for CKIN_n. If CKn_ACTV_PIN = 1, this status will also be reflected on the CnA pin with active polarity controlled by the CK_ACTV_POL bit. If CKn_ACTV_PIN = 0, this output tristates.</td></tr>
<tr><td>16
17</td><td>XA
XB</td><td>I</td><td>ANALOG</td><td>External Crystal or Reference Clock.
External crystal should be connected to these pins to use internal oscillator based reference. Refer to Family Reference Manual for interfacing to an external reference. External reference must be from a high-quality clock source (TCXO, OCXO). Frequency of crystal or external clock is set by the RATE pins.</td></tr>
<tr><td>29
30</td><td>CKIN4+
CKIN4–</td><td>I</td><td>MULTI</td><td>Clock Input 4.
Differential clock input. This input can also be driven with a single-ended signal. CKIN4 serves as the frame sync input associated with the CKIN2 clock when CK_CONFIG_REG = 1.</td></tr>
<tr><td>32
42</td><td>RATE0
RATE1</td><td>I</td><td>3-Level</td><td>External Crystal or Reference Clock Rate.
Three level inputs that select the type and rate of external crystal or reference clock to be applied to the XA/XB port. Refer to the Family Reference Manual for settings. These pins have both a weak pull-up and a weak pull-down; they default to M.</td></tr>
<tr><td>34
35</td><td>CKIN2+
CKIN2–</td><td>I</td><td>MULTI</td><td>Clock Input 2.
Differential input clock. This input can also be driven with a single-ended signal.</td></tr>
<tr><td>39
40</td><td>CKIN3+
CKIN3–</td><td>I</td><td>MULTI</td><td>Clock Input 3.
Differential clock input. This input can also be driven with a single-ended signal. CKIN3 serves as the frame sync input associated with the CKIN1 clock when CK_CONFIG_REG = 1.</td></tr>
<tr><td>44
45</td><td>CKIN1+
CKIN1–</td><td>I</td><td>MULTI</td><td>Clock Input 1.
Differential clock input. This input can also be driven with a single-ended signal.</td></tr>
<tr><td colspan="5">Note: Internal register names are indicated by underlined italics, e.g., INT_PIN. See Si5369 Register Map.</td></tr>
</table>

Table 10. Si5369 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
49	LOL	O	LVCMOS	**PLL Loss of Lock Indicator.** This pin functions as the active high PLL loss of lock indicator if the *LOL_PIN* register bit is set to one. 0 = PLL locked. 1 = PLL unlocked. If LOL_PIN = 0, this pin will tristate. Active polarity is controlled by the *LOL_POL* bit. The PLL lock status will always be reflected in the *LOL_INT* read only register bit.
58	C1A	O	LVCMOS	**CKIN1 Active Clock Indicator.** This pin serves as the CKIN1 active clock indicator. The *CK1_ACTV_REG* bit always reflects the active clock status for CKIN1. If *CK1_ACTV_PIN* = 1, this status will also be reflected on the C1A pin with active polarity controlled by the *CK_ACTV_POL* bit. If *CK1_ACTV_PIN* = 0, this output tristates.
59	C2A	O	LVCMOS	**CKIN2 Active Clock Indicator.** This pin serves as the CKIN2 active clock indicator. The *CK2_ACTV_REG* bit always reflects the active clock status for CKIN_2. If *CK2_ACTV_PIN* = 1, this status will also be reflected on the C2A pin with active polarity controlled by the *CK_ACTV_POL* bit. If *CK2_ACTV_PIN* = 0, this output tristates.
60	SCL	I	LVCMOS	**Serial Clock.** This pin functions as the serial port clock input for both SPI and I^{2}C modes. This pin has a weak pull-down.
61	SDA_SDO	I/O	LVCMOS	**Serial Data.** In I^{2}C microprocessor control mode (CMODE = 0), this pin functions as the bidirectional serial data port. In SPI microprocessor control mode (CMODE = 1), this pin functions as the serial data output.
68 69	A0 A1	I	LVCMOS	**Serial Port Address.** In I^{2}C microprocessor control mode (CMODE = 0), these pins function as hardware controlled address bits. The I^{2}C address is 1101 [A2] [A1] [A0]. In SPI microprocessor control mode (CMODE = 1), these pins are ignored. This pin has a weak pull-down.
70	A2_$\overline{SS}$	I	LVCMOS	**Serial Port Address/Slave Select.** In I^{2}C microprocessor control mode (CMODE = 0), this pin functions as a hardware controlled address bit [A2]. In SPI microprocessor control mode (CMODE = 1), this pin functions as the slave select input. This pin has a weak pull-down.
71	SDI	I	LVCMOS	**Serial Data In.** In SPI microprocessor control mode (CMODE = 1), this pin functions as the serial data input. In I^{2}C microprocessor control mode (CMODE = 0), this pin is ignored. This pin has a weak pull-down.

Note: Internal register names are indicated by underlined italics, e.g., *INT_PIN*. See Si5369 Register Map.

Table 10. Si5369 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
77 78	CKOUT3+ CKOUT3–	O	MULTI	**Clock Output 3.** Differential clock output. Output signal format is selected by *SFOUT3_REG* register bits. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.
82 83	CKOUT1– CKOUT1+	O	MULTI	**Clock Output 1.** Differential clock output. Output signal format is selected by *SFOUT1_REG* register bits. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.
87 88	FS_OUT– FS_OUT+	O	MULTI	**Frame Sync Output.** Differential frame sync output or fifth high-speed clock output. Output signal format is selected by *SFOUT_FSYNC_REG* register bits. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs. Duty cycle and active polarity are controlled by *FSYNC_PW* and *FSYNC_POL* bits, respectively. Detailed operations and timing characteristics for these pins may be found in the Any-Frequency Precision Clock Family Reference Manual.
90	CMODE	I	LVCMOS	**Control Mode.** Selects I^2C or SPI control mode for the device. 0 = I^2C Control Mode. 1 = SPI Control Mode. This pin must be tied high or low.
92 93	CKOUT2+ CKOUT2–	O	MULTI	**Clock Output 2.** Differential clock output. Output signal format is selected by *SFOUT2_REG* register bits. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.
97 98	CKOUT4– CKOUT4+	O	MULTI	**Clock Output 4.** Differential clock output. Output signal format is selected by *SFOUT4_REG* register bits. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.
GND PAD	GND PAD	GND	Supply	**Ground Pad.** The ground pad must provide a low thermal and electrical impedance to a ground plane.

Note: Internal register names are indicated by underlined italics, e.g., *INT_PIN*. See Si5369 Register Map.

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7. Ordering Guide

Ordering Part Number	Output Clock Frequency Range	Package	ROHS6, Pb-Free	Temperature Range
Si5369A-C-GQ	2 kHz–945 MHz 970–1134 MHz 1.213–1.417 GHz	100-Pin 14 x 14 mm TQFP	Yes	–40 to 85 °C
Si5369B-C-GQ	2 kHz–808 MHz	100-Pin 14 x 14 mm TQFP	Yes	–40 to 85 °C
Si5369C-C-GQ	2 kHz–346 MHz	100-Pin 14 x 14 mm TQFP	Yes	–40 to 85 °C
Si5369D-C-GQ	2 kHz–243 MHz	100-Pin 14 x 14 mm TQFP	Yes	–40 to 85 °C
Note: Add an R at the end of the device to denote tape and reel options (for example, Si5369-C-GMR).				

8. Package Outline: 100-Pin TQFP

Figure 8 illustrates the package details for the Si5369. Table 11 lists the values for the dimensions shown in the illustration.

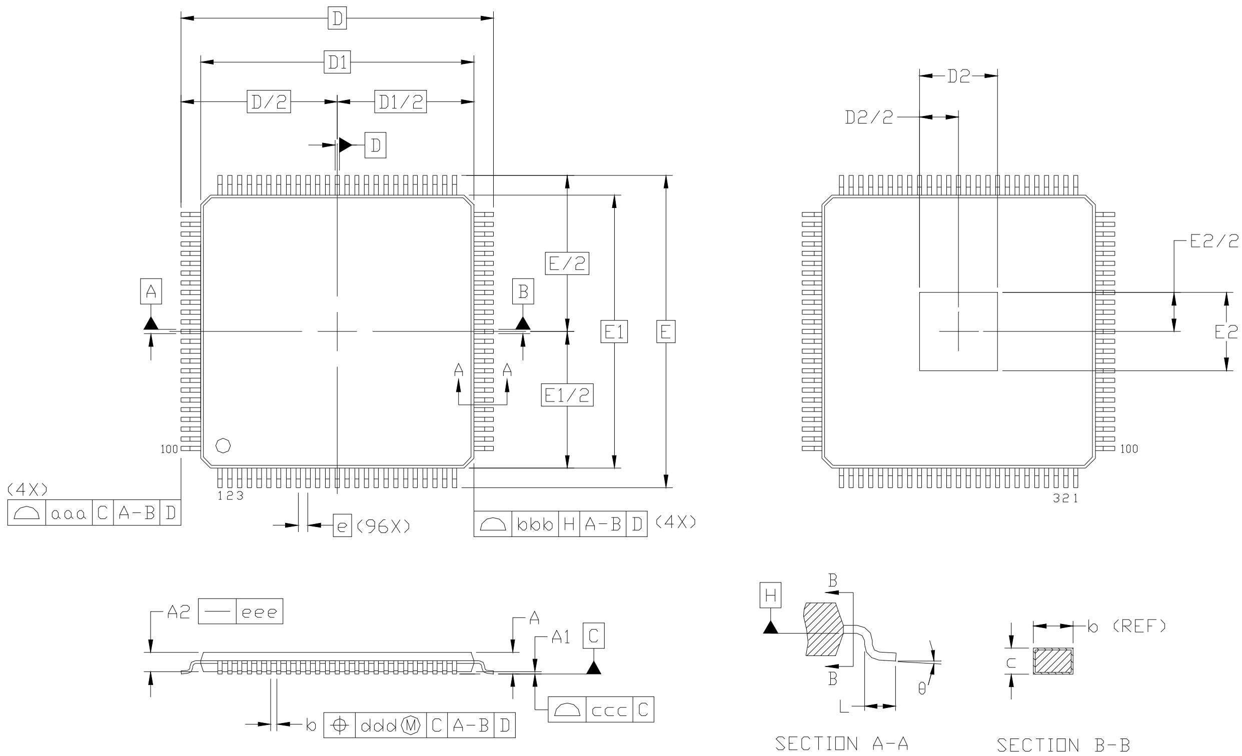

Figure 8. 100-Pin Thin Quad Flat Package (TQFP)

Table 11. 100-Pin Package Diagram Dimensions

Dimension	Min	Nom	Max	Dimension	Min	Nom	Max
A	—	—	1.20	E	16.00 BSC.		
A1	0.05	—	0.15	E1	14.00 BSC.		
A2	0.95	1.00	1.05	E2	3.85	4.00	4.15
b	0.17	0.22	0.27	L	0.45	0.60	0.75
c	0.09	—	0.20	aaa	—	—	0.20
D	16.00 BSC.			bbb	—	—	0.20
D1	14.00 BSC.			ccc	—	—	0.08
D2	3.85	4.00	4.15	ddd	—	—	0.08
e	0.50 BSC.			θ	0º	3.5º	7º

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This package outline conforms to JEDEC MS-026, variant AED-HD.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9. Recommended PCB Layout

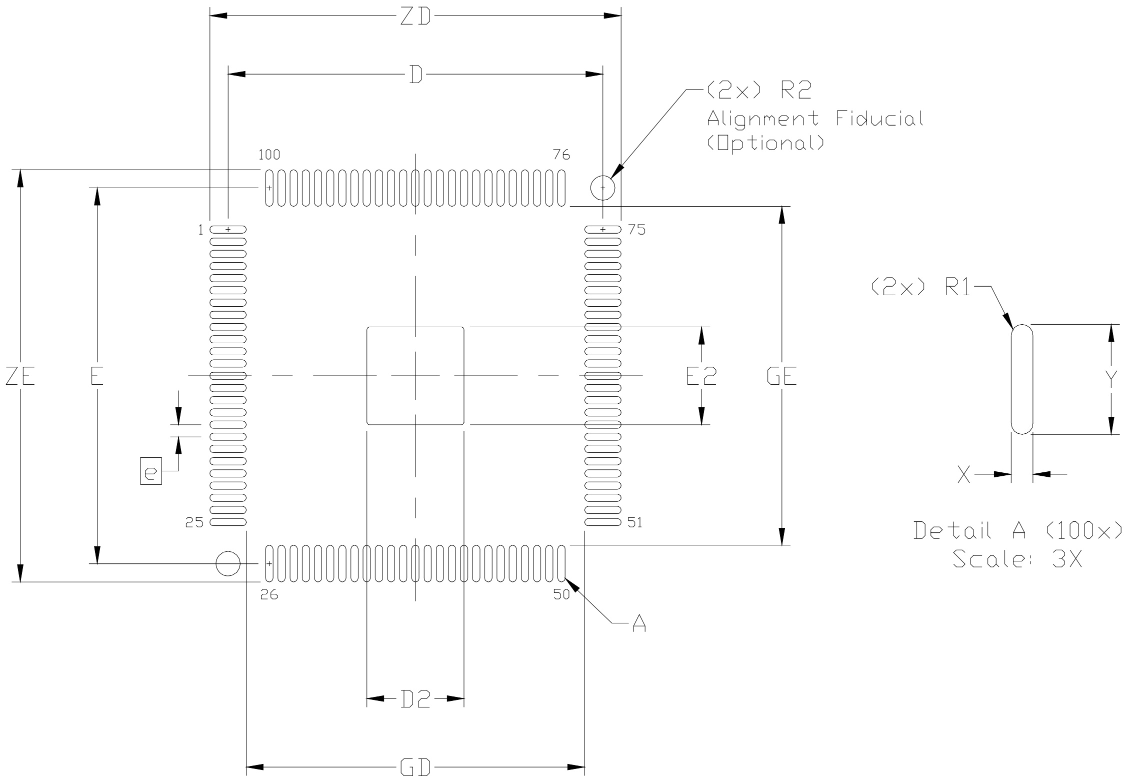

Figure 9. PCB Land Pattern Diagram

Table 12. PCB Land Pattern Dimensions

Dimension	MIN	MAX
e	0.50 BSC.	
E	15.40 REF.	
D	15.40 REF.	
E2	3.90	4.10
D2	3.90	4.10
GE	13.90	—
GD	13.90	—
X	—	0.30
Y	1.50 REF.	
ZE	—	16.90
ZD	—	16.90
R1	0.15 REF	
R2	—	1.00

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

5. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
7. The stencil thickness should be 0.125 mm (5 mils).
8. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
9. A 4 x 4 array of 0.80 mm square openings on 1.05 mm pitch should be used for the center ground pad.

Card Assembly

10. A No-Clean, Type-3 solder paste is recommended.
11. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

10. Top Marking

Mark Method:	Laser	
Logo Size:	9.2 x 3.1 mm Center-Justified	
Font Size:	3.0 Point (1.07 mm) Right-Justified	
Line 1 Marking:	Device Part Number	X = Speed Grade See "7. Ordering Guide" on page 77.
Line 2 Marking:	YY = Year WW = Workweek	Assigned by the Assembly Supplier. Corresponds to the year and work-week of the mold date.
	TTTTTT = Mfg Code	Manufacturing Code
Line 3 Marking:	Circle = 1.8 mm Diameter Center-Justified	“e3” Pb-Free Symbol
	Country of Origin ISO Code Abbreviation	

DOCUMENT CHANGE LIST

Revision 0.1 to Revision 0.4

- Updated Table 4, “AC Specifications,” on page 10.
  - Added table note.

NOTES:

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