CY7C148
CY7C149

1Kx4 Static RAM

Features

- **Automatic power-down when deselected (7C148)**
- **CMOS for optimum speed/power**
- **25-ns access time**
- **Low active power**
  - **—440 mW (commercial)**
  - **—605 mW (military)**
- **Low standby power (7C148)**
  - **—82.5 mW (25-ns version)**
  - **—55 mW (all others)**
- **5-volt power supply ± 10% tolerance, both commercial and military**
- **TTL-compatible inputs and outputs**

Functional Description

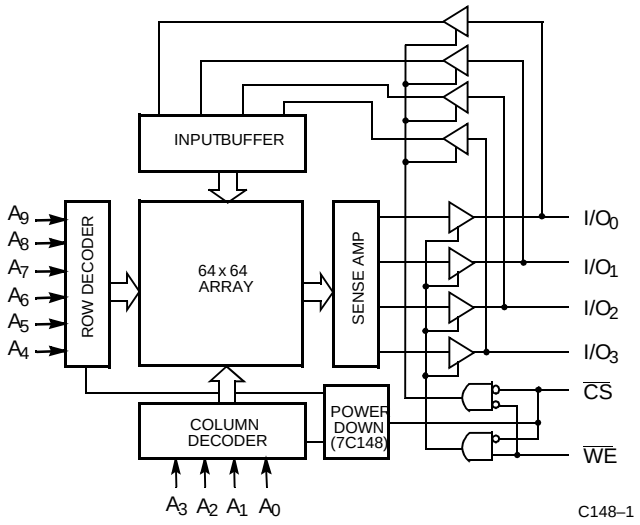
The CY7C148 and CY7C149 are high-performance CMOS static RAMs organized as 1024 by 4 bits. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and three-state outputs. The CY7C148 remains in a low-power mode as long as the device remains unselected; i.e., ($\overline{CS}$) is HIGH, thus reducing the average power requirements of the device. The chip select ($\overline{CS}$) of the CY7C149 does not affect the power dissipation of the device.

Writing to the device is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the I/O pins (I/O_0 through I/O_3) is written into the memory locations specified on the address pins (A_0 through A_9).

Reading the device is accomplished by taking chip select ($\overline{CS}$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the location specified on the address pins will appear on the four data I/O pins.

The I/O pins remain in a high-impedance state when chip select ($\overline{CS}$) is HIGH or write enable ($\overline{WE}$) is LOW.

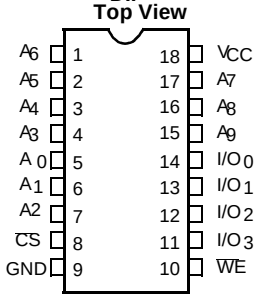
Logic Block Diagram



C148–1

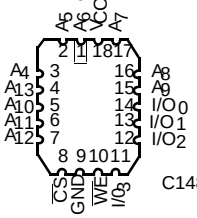
Pin Configurations

DIP
Top View



C148–2

LCC
Top View



C148–3

Selection Guide

		7C148–25	7C148–35	7C148–45	7C149–25	7C149–35	7C149–45
Maximum Access Time (ns)		25	35	45	25	35	45
Maximum Operating Current (mA)	Commercial	90	80	80	90	80	80
	Military		110	110		110	110
Maximum Standby Current (mA)	Commercial	15	10	10			
	Military		10	10			

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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage to Ground Potential (Pin 18 to Pin 9).....–0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State.....–0.5V to +7.0V

DC Input Voltage .....–3.0V to +7.0V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage .....>2001V (per MIL-STD-883, Method 3015)

Latch-Up Current.....>200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[1]	–55°C to +125°C	5V ± 10%

Note:
1. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range[2]

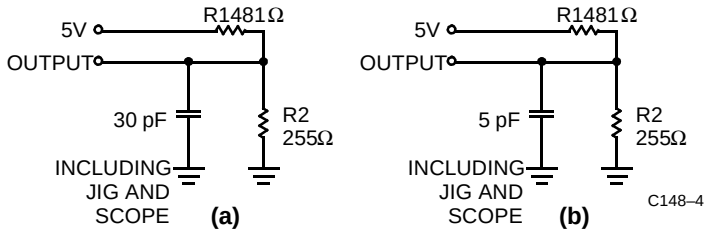
Parameter	Description	Test Conditions			7C148–25 7C149–25 Min.	7C148–25 7C149–25 Max.	7C148–35, 45 7C149–35, 45 Min.	7C148–35, 45 7C149–35, 45 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA			2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA				0.4		0.4	V
V_{IH}	Input HIGH Voltage				2.0	6.0	2.0	6.0	V
V_{IL}	Input LOW Voltage				–3.0	0.8	–3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			–10	10	–10	10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC} Output Disabled			–50	50	–50	50	µA
I_{CC}	V_{CC} Operating Supply Current	Max. V_{CC}, $\overline{CS}$ ≤ V_{IL}, Output Open		Com'l		90		80	mA
				Mil				110	
I_{SB}	Automatic $\overline{CS}$ Power-Down Current	Max. V_{CC}, $\overline{CS}$ ≥ V_{IH}	7C148 Only	Com'l		15		10	mA
				Mil				10	
I_{PO}	Peak Power-On Current[3]	Max. V_{CC}, $\overline{CS}$ ≥ V_{IH}	7C148 Only	Com'l		15		10	mA
				Mil				10	
I_{OS}	Output Short Circuit Current[4]	GND ≤ V_O ≤ V_{CC}		Com'l		±275		±275	mA
				Mil				±350	

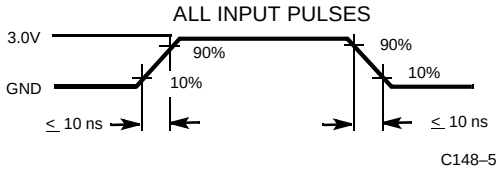
Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	8	pF
C_{OUT}	Output Capacitance		8	pF

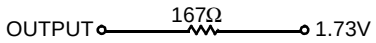
Notes:
2. See the last page of this specification for Group A subgroup testing information.
3. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up. Otherwise current will exceed values given (CY7C148 only).
4. For test purposes, not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[2]

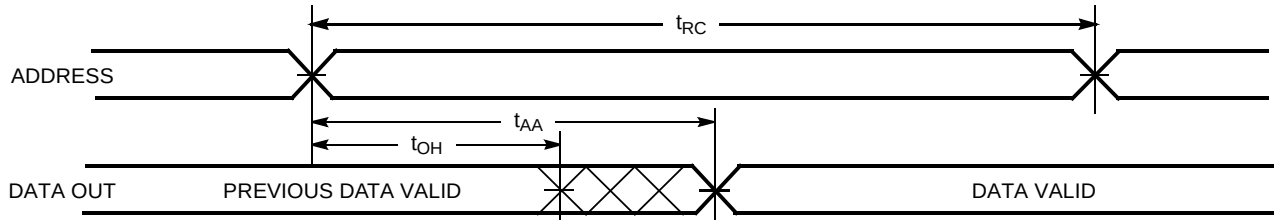
Parameter	Description		7C148–25 7C149–25 Min.	7C148–25 7C149–25 Max.	7C148–35 7C149–35 Min.	7C148–35 7C149–35 Max.	7C148–45 7C149–45 Min.	7C148–45 7C149–45 Max.	Unit
READ CYCLE									
t_{RC}	Address Valid to Address Do Not Care Time (Read Cycle Time)		25		35		45		ns
t_{AA}	Address Valid to Data Out Valid Delay (Address Access Time)			25		35		45	ns
t_{ACS1}	Chip Select LOW to Data Out Valid (7C148 only)			25[6]		35		45	ns
t_{ACS2}				30[7]		35		45	ns
t_{ACS}	Chip Select LOW to Data Out Valid (7C149 only)			15		15		20	ns
t_{LZ}[8]	Chip Select LOW to Data Out On	7C148	8		10		10		ns
		7C149	5		5		5		
t_{HZ}[8]	Chip Select HIGH to Data Out Off		0	15	0	20	0	20	ns
t_{OH}	Address Unknown to Data Out Unknown Time		0		0		5		ns
t_{PD}	Chip Select HIGH to Power-Down Delay	7C148		20		30		30	ns
t_{PU}	Chip Select LOW to Power-Up Delay	7C148	0		0		0		ns
WRITE CYCLE									
t_{WC}	Address Valid to Address Do Not Care (Write Cycle Time)		25		35		45		ns
t_{WP}[9]	Write Enable LOW to Write Enable HIGH		20		30		35		ns
t_{WR}	Address Hold from Write End		5		5		5		ns
t_{WZ}[8]	Write Enable to Output in High Z		0	8	0	8	0	8	ns
t_{DW}	Data in Valid to Write Enable HIGH		12		20		20		ns
t_{DH}	Data Hold Time		0		0		0		ns
t_{AS}	Address Valid to Write Enable LOW		0		0		0		ns
t_{CW}[9]	Chip Select LOW to Write Enable HIGH		20		30		40		ns
t_{OW}[8]	Write Enable HIGH to Output in Low Z		0		0		0		ns
t_{AW}	Address Valid to End of Write		20		30		35		ns

Notes:

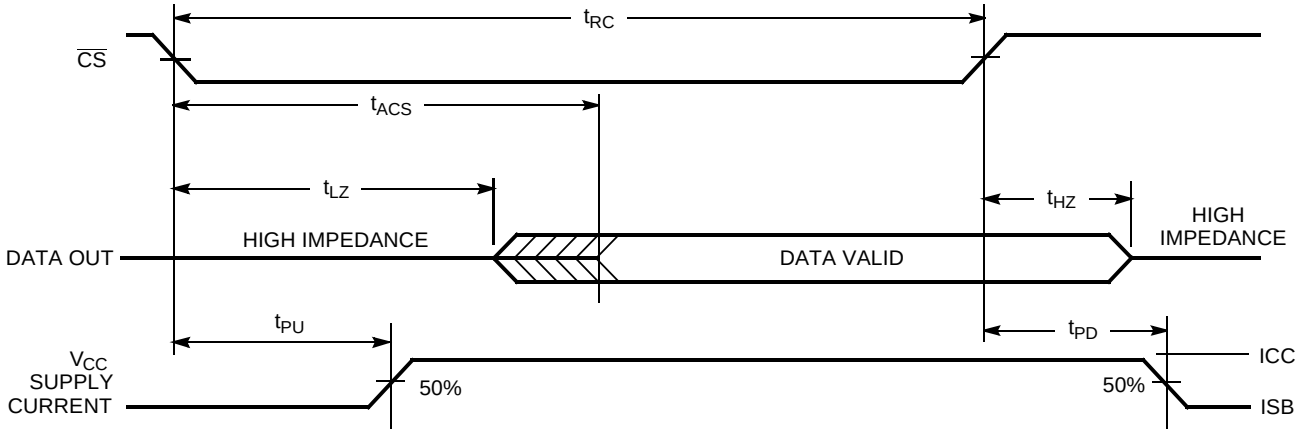
6. Chip deselected greater than 25 ns prior to selection.
7. Chip deselected less than 25 ns prior to selection.
8. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for all devices. Transition is measured ±500 mV from steady-state voltage with specified loading in part (b) of AC Test Loads.
9. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going high. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

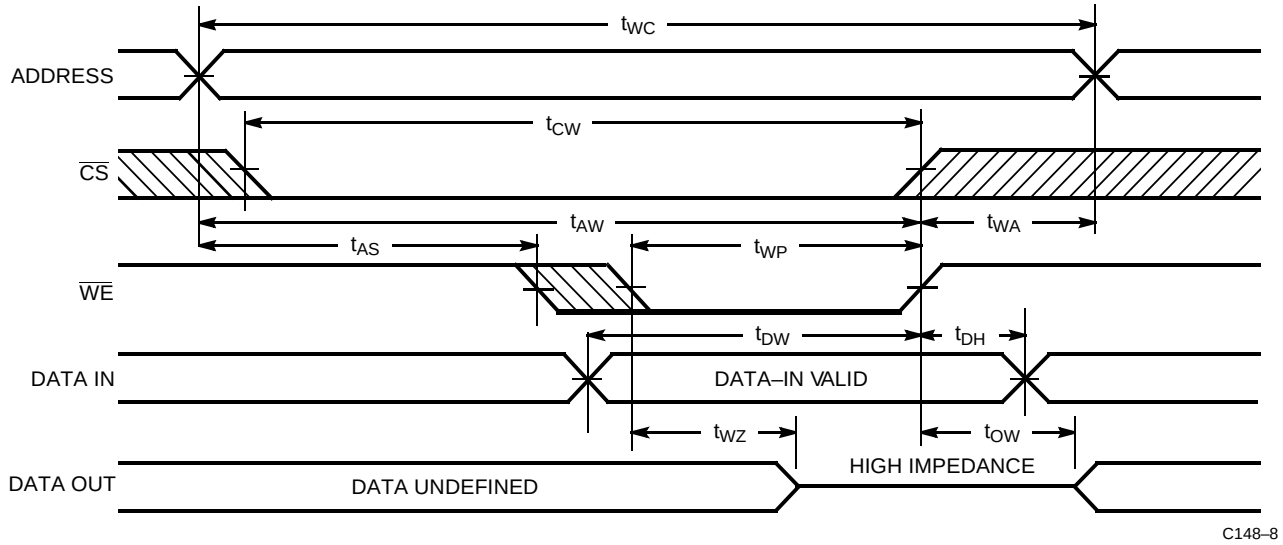
Read Cycle No. 1 [10,11]



Read Cycle No. 2 [10,12]



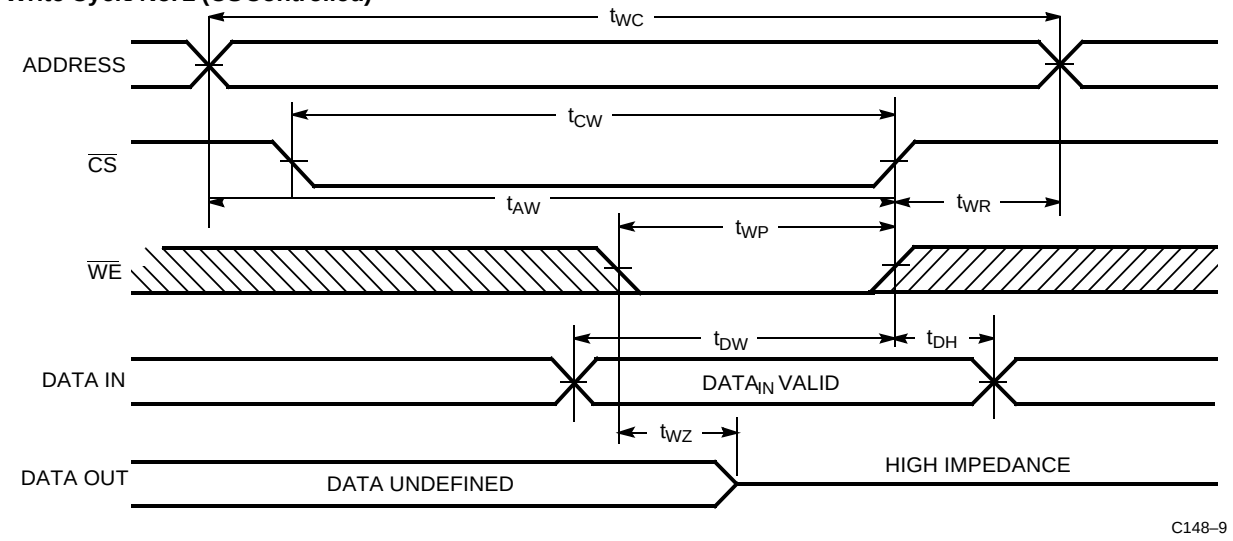
Write Cycle No. 1 (WE Controlled)



Notes:
10. $\overline{WE}$ is HIGH for read cycle.
11. Device is continuously selected, $\overline{CS} = V_{IL}$.
12. Address valid prior to or coincident with $\overline{CS}$ transition LOW.

Switching Waveforms (continued)

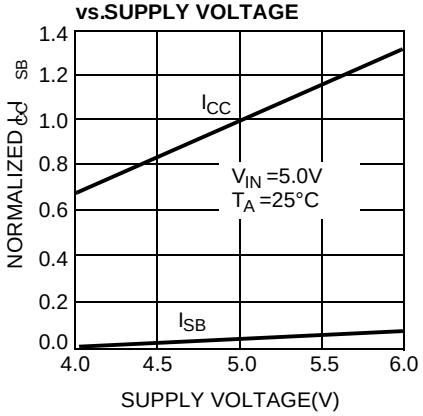
Write Cycle No. 2 ($\overline{CS}$ Controlled)[13]



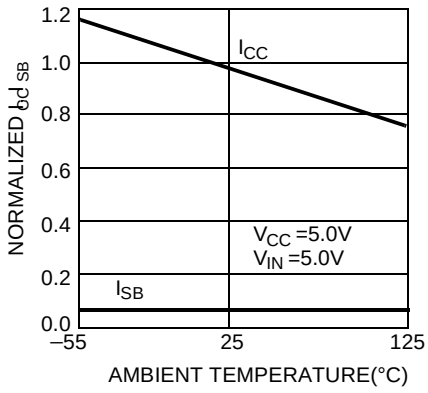
Notes:
13. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Typical DC and AC Characteristics

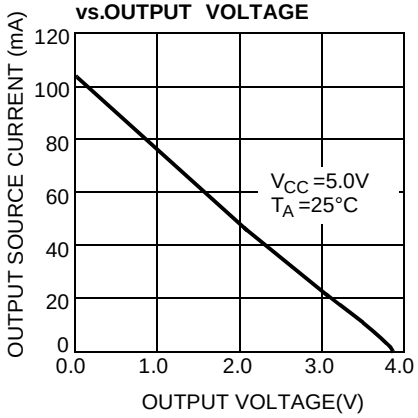
NORMALIZED SUPPLY CURRENT vs.SUPPLY VOLTAGE



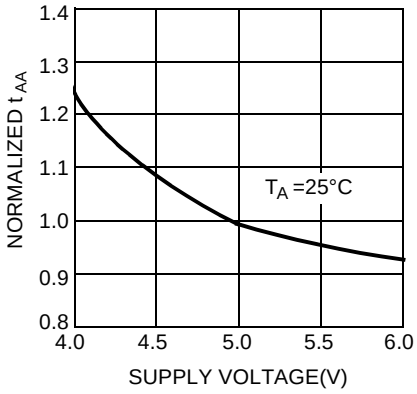
NORMALIZED SUPPLY CURRENT vs.AMBIENT TEMPERATURE



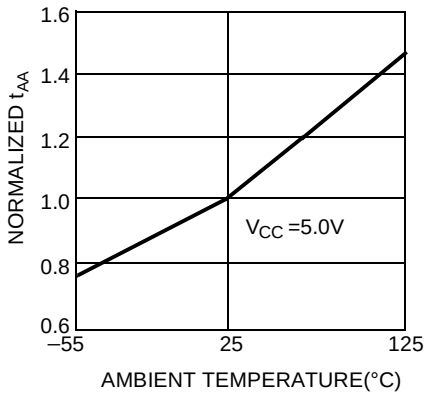
OUTPUT SOURCE CURRENT vs.OUTPUT VOLTAGE



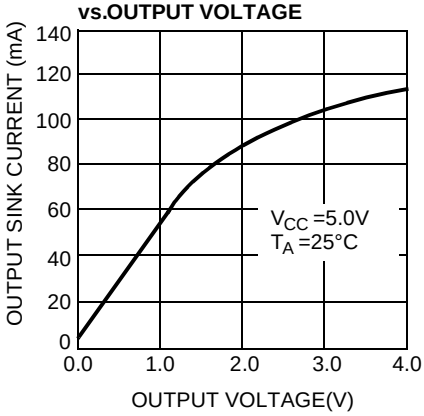
NORMALIZED ACCESS TIME vs.SUPPLY VOLTAGE



NORMALIZED ACCESS TIME vs.AMBIENT TEMPERATURE

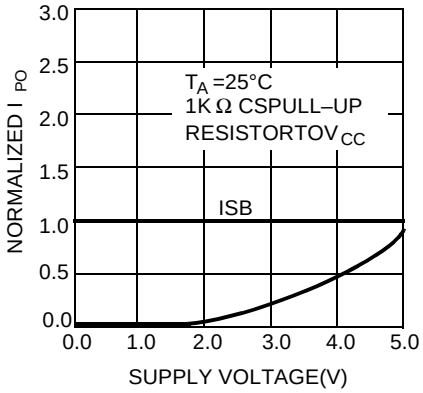


OUTPUT SINK CURRENT vs.OUTPUT VOLTAGE

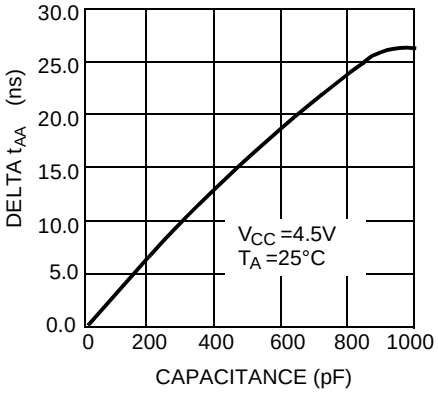


Typical DC and AC Characteristics

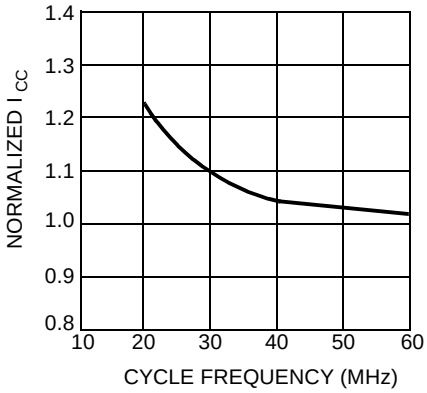
TYPICAL POWER–ON CURRENT vs.SUPPLY VOLTAGE(7C148)



TYPICAL ACCESS TIME CHANGE vs.OUTPUT LOADING



NORMALIZED I CC vs.ACCESS TIME



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C148–25PC	P3	18-Lead (300-Mil) Molded DIP	Commercial
35	CY7C148–35PC	P3	18-Lead (300-Mil) Molded DIP	Commercial
	CY7C148–35DMB	D4	18-Lead (300-Mil) CerDIP	Military
45	CY7C148–45PC	P3	18-Lead (300-Mil) Molded DIP	Commercial
	CY7C148–45DMB	D4	18-Lead (300-Mil) CerDIP	Military

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C149–25PC	P3	18-Lead (300-Mil) Molded DIP	Commercial
35	CY7C149–35PC	P3	18-Lead (300-Mil) Molded DIP	Commercial
	CY7C149–35DMB	D4	18-Lead (300-Mil) CerDIP	Military
	CY7C149–35LMB	L50	18-Pin Rectangular Leadless Chip Carrier	
45	CY7C149–45PC	P3	18-Lead (300-Mil) Molded DIP	Commercial
	CY7C149–45DMB	D4	18-Lead (300-Mil) CerDIP	Military
	CY7C149–45LMB	L50	18-Pin Rectangular Leadless Chip Carrier	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
I_{OH}	1, 2, 3
I_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}[14]	1, 2, 3

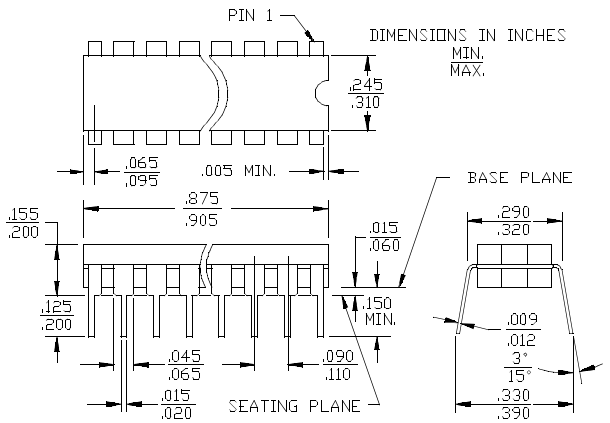
Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{ACS1}[14]	7, 8, 9, 10, 11
t_{ACS2}[14]	7, 8, 9, 10, 11
t_{ACS}[15]	7, 8, 9, 10, 11
t_{OH}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{WP}	7, 8, 9, 10, 11
t_{WR}	7, 8, 9, 10, 11
t_{DW}	7, 8, 9, 10, 11
t_{DH}	7, 8, 9, 10, 11
t_{AS}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11

Notes:
14. 7C148 only.
15. 7C149 only.

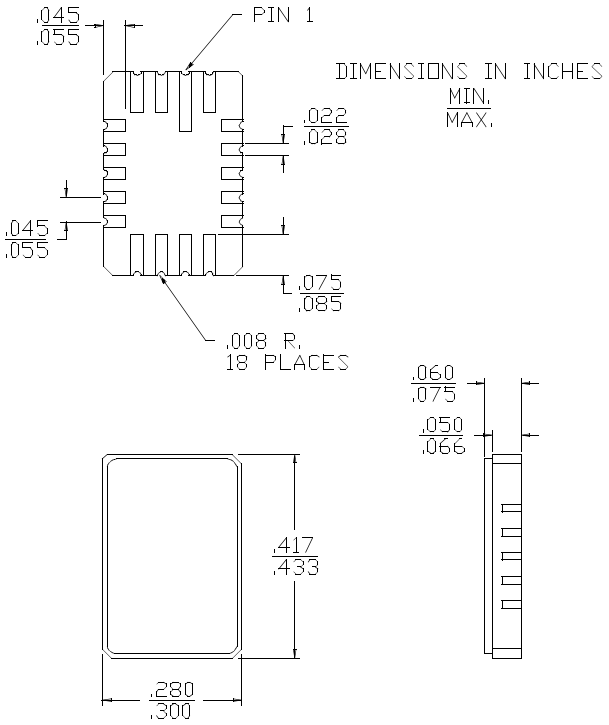
18–Lead(300–Mil) CerDIP D4

MIL–STD–1835 D– 8Config.A

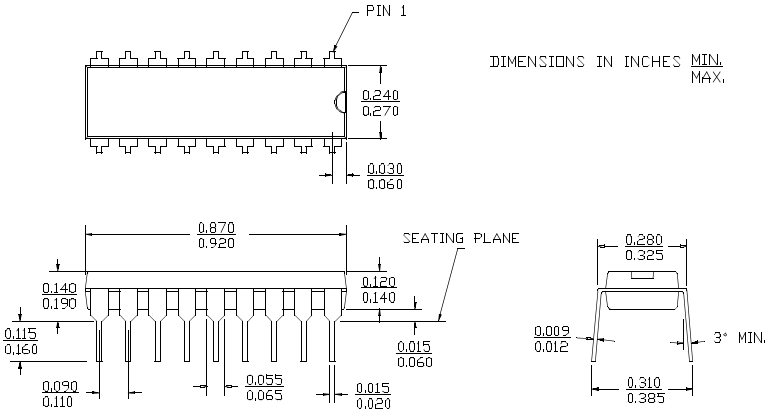


18–Pin Rectangular Leadless Chip Carrier L50

MIL–STD–1835 C–10A



18–Lead(300–Mil) Molded DIP P3



Document Title: CY7C148 / CY7C149 1K x 4 Static RAM Document Number: 38-05059				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	110170	09/29/01	SZV	Change from Spec number: 38-00031 to 38-05059