

## PCI-EXPRESS GEN 1, GEN 2, & GEN 3 FANOUT BUFFER

### Features

- PCI-Express Gen 1, Gen 2, and Gen 3 compliant
- Low power push-pull type differential output buffers
- Integrated resistors on differential clocks
- Dedicated output enable pin for each buffered clocks
- Six PCI-Express Gen 1, Gen 2 & Gen 3 buffered clocks
- 100 to 210 MHz clock input range
- I<sup>2</sup>C support with readback capabilities
- Spread aware for maximum electromagnetic interference (EMI) reduction
- Industrial temperature: -40 to 85 °C
- 3.3 V power supply
- 32-pin QFN package



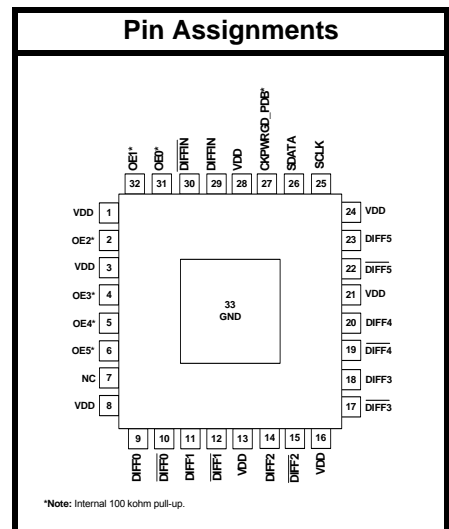
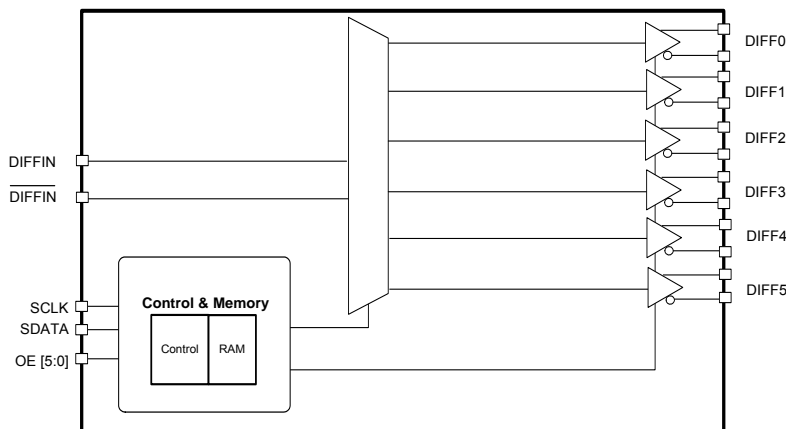
### Applications

- Network attached storage
- Multi-function printers
- Wireless access point
- Routers

### Description

The Si53156 is a spread aware PCIe clock buffer that can source six PCIe clocks simultaneously. The device has six hardware output enable control inputs for enabling the respective differential outputs on the fly while powered on along with output enable control through I<sup>2</sup>C communication. In addition to the hardware control pins, I<sup>2</sup>C programmability is also available to promptly achieve optimum clock signal integrity through skew and edge rate control on true, compliment, or both differential outputs as well as amplitude control.

### Functional Block Diagram



Patents pending



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## 1. Electrical Specifications

**Table 1. DC Electrical Specifications**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
3.3 V Operating Voltage	VDD core	3.3 ± 5%	3.135	—	3.465	V
3.3 V Input High Voltage	V <sub>IH</sub>	Control input pins	2.0	—	V <sub>DD</sub> + 0.3	V
3.3 V Input Low Voltage	V <sub>IL</sub>	Control input pins	V <sub>SS</sub> - 0.3	—	0.8	V
Input High Voltage	V <sub>IHI2C</sub>	SDATA, SCLK	2.2	—	—	V
Input Low Voltage	V <sub>ILI2C</sub>	SDATA, SCLK	—	—	1.0	V
Input High Leakage Current	I <sub>IH</sub>	Except internal pull-down resistors, 0 < V <sub>IN</sub> < V <sub>DD</sub>	—	—	5	μA
Input Low Leakage Current	I <sub>IL</sub>	Except internal pull-up resistors, 0 < V <sub>IN</sub> < V <sub>DD</sub>	-5	—	—	μA
High-impedance Output Current	I <sub>OZ</sub>		-10	—	10	μA
Input Pin Capacitance	C <sub>IN</sub>		1.5	—	5	pF
Output Pin Capacitance	C <sub>OUT</sub>		—	—	6	pF
Pin Inductance	L <sub>IN</sub>		—	—	7	nH
Power Down Current	I <sub>DD_PD</sub>		—	—	1	mA
Dynamic Supply Current in Fanout Mode	I <sub>DD_3.3V</sub>	Differential clocks with 5" traces and 2 pF load, frequency at 100 MHz	—	—	45	mA

Table 2. AC Electrical Specifications

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>DIFFIN at 0.7 V</b>						
Average Period	$T_{PERIOD}$	Measured at crossing point $V_{OX}$	9.997 0	—	10.0533	ns
Absolute minimum clock periods	$T_{ABSMIN-IN}$	Measured at crossing point $V_{OX}$	9.872 0	—	—	ns
DIFFIN and $\overline{DIFFIN}$ Rise and Fall Times	$T_R/T_F$	Single ended measurement: $V_{OL} = 0.175$ to $V_{OH} = 0.525$ V (Averaged)	0.6	—	4	V/ns
Differential Input High Voltage	$V_{IH}$		150	—	—	mV
Differential Input Low Voltage	$V_{IL}$		—	—	-150	mV
Crossing Point Voltage at 0.7 V Swing	$V_{OX}$	Single-ended measurement	250	—	550	mV
Vcross Variation over all edges	$\Delta V_{OX}$	Single-ended measurement	—	—	140	mV
Differential Ringback Voltage	$V_{RB}$		-100	—	100	mV
Time before ringback allowed	$T_{STABLE}$		500	—	—	ps
Absolute maximum input voltage	$V_{MAX}$		—	—	1.15	V
Absolute minimum input voltage	$V_{MIN}$		-0.3	—	—	V
DIFFIN and $\overline{DIFFIN}$ Duty Cycle	$T_{DC}$	Measured at crossing point $V_{OX}$	45	—	55	%
Rise/Fall Matching	$T_{RFM}$	Determined as a fraction of $2 \times (T_R - T_F)/(T_R + T_F)$	—	—	20	%
<b>DIFF at 0.7 V</b>						
DIFF Duty Cycle	$T_{DC}$	Measured at 0 V differential	45	—	55	%
DIFF Clock Skew	$T_{SKEW}$	Measured at 0 V differential	—	—	50	ps
Output PCIe Gen1 Additive REF-CLK Phase Jitter	$RMS_{GEN1}$	Includes PLL BW 8–16 MHz, $\zeta = 0.54$ , $T_d=10$ ns, $F_{trk}=1.5$ MHz with BER=1E-12	0	—	10	ps
Output PCIe Gen2 Additive REF-CLK Phase Jitter	$RMS_{GEN2}$	Includes PLL BW 8–16 MHz, Jitter Peaking = 3 dB, $\zeta = 0.54$ , $T_d=12$ ns, Low Band, $F < 1.5$ MHz	0	—	0.5	ps
Output PCIe Gen2 Additive REF-CLK Phase Jitter	$RMS_{GEN2}$	Includes PLL BW 8–16 MHz, Jitter Peaking = 3 dB, $\zeta = 0.54$ , $T_d=12$ ns, High Band, 1.5 MHz $< F < Nyquist$	0	—	0.5	ps
Output PCIe Gen3 Additive REF-CLK Phase Jitter	$RMS_{GEN3}$	Includes PLL BW 2–4 MHz, CDR = 10 MHz)	0	—	0.10	ps

**Table 2. AC Electrical Specifications** (Continued)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Additive Cycle to Cycle Jitter	$T_{CCJ}$	In buffer mode. Measured at 0 V differential	—	—	50	ps
Long-term Accuracy	$L_{ACC}$	Measured at 0 V differential	—	—	100	ppm
Rising/Falling Slew rate	$T_R / T_F$	Measured differentially from $\pm 150$ mV	2.5	—	8	V/ns
Crossing Point Voltage at 0.7 V Swing	$V_{OX}$		300	—	550	mV
<b>Enable/Disable and Setup</b>						
Clock Stabilization from Power-Up	$T_{STABLE}$		—	—	1.8	ms
Stopclock Set-up Time	$T_{SS}$		10.0	—	—	ns

**Table 3. Absolute Maximum Conditions**

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Main Supply Voltage	$V_{DD\_3.3V}$	Functional	—	—	4.6	V
Input Voltage	$V_{IN}$	Relative to $V_{SS}$	-0.5	—	4.6	$V_{DC}$
Temperature, Storage	$T_S$	Non-functional	-65	—	150	$^{\circ}C$
Industrial Temperature, Operating Ambient	$T_A$	Functional	-40	—	85	$^{\circ}C$
Commercial Temperature, Operating Ambient	$T_A$	Functional	0	—	85	$^{\circ}C$
Temperature, Junction	$T_J$	Functional	—	—	150	$^{\circ}C$
Dissipation, Junction to Case	$\theta_{JC}$	JEDEC (JESD 51)	—	—	17	$^{\circ}C/W$
Dissipation, Junction to Ambient	$\theta_{JA}$	JEDEC (JESD 51)	—	—	35	$^{\circ}C/W$
ESD Protection (Human Body Model)	$ESD_{HBM}$	JEDEC (JESD 22 - A114)	2000	—	—	V
Flammability Rating	UL-94	UL (Class)	V-0			
Moisture Sensitivity Level	MSL	JEDEC (J-STD-020)	1			
<b>Note: Multiple Supplies:</b> The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is not required.						

## 2. Functional Description

### 2.1. OE Clarification

The OE pins are active high inputs used to enable and disable the output clocks. To enable the output clock, the OE pin needs to be logic high and the I<sup>2</sup>C output enable bit needs to be logic high. There are two methods to disable the output clocks: the OE is pulled to a logic low, or the I<sup>2</sup>C enable bit is set to a logic low. The OE pins is required to be driven at all time and even though it has an internally 100 k $\Omega$  resistor.

### 2.2. OE Assertion

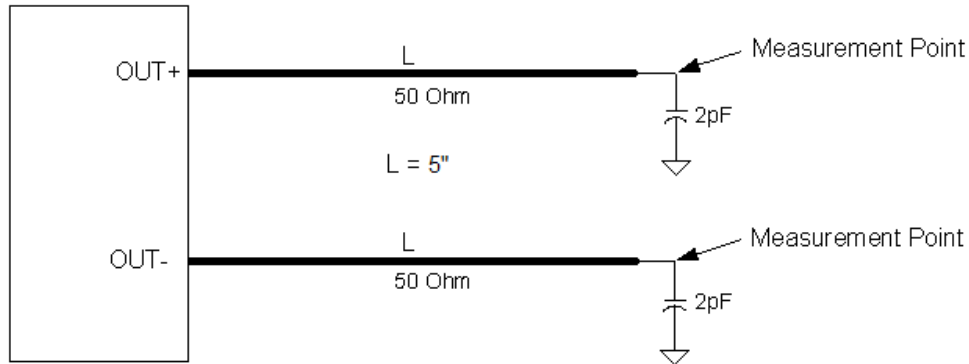
The OE signals are active high input used for synchronous stopping and starting the DIFF output clocks respectively while the rest of the clock generator continues to function. The assertion of the OE signal by making it logic high causes stopped respective DIFF output to resume normal operation. No short or stretched clock pulses are produced when the clock resumes. The maximum latency from the assertion to active outputs is no more than two to six output clock cycles.

### 2.3. OE Deassertion

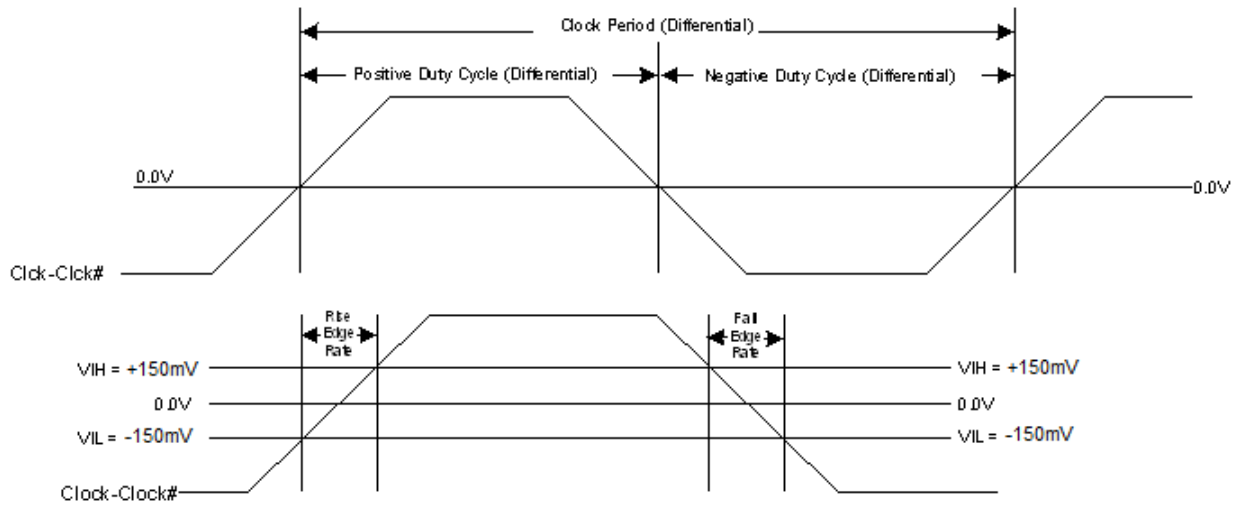
When the OE pin is deasserted by making its logic low, the corresponding DIFF output is stopped cleanly, and the final output state is driven low.

## 3. Test and Measurement Setup

This diagram shows the test load configuration for the differential clock signals.

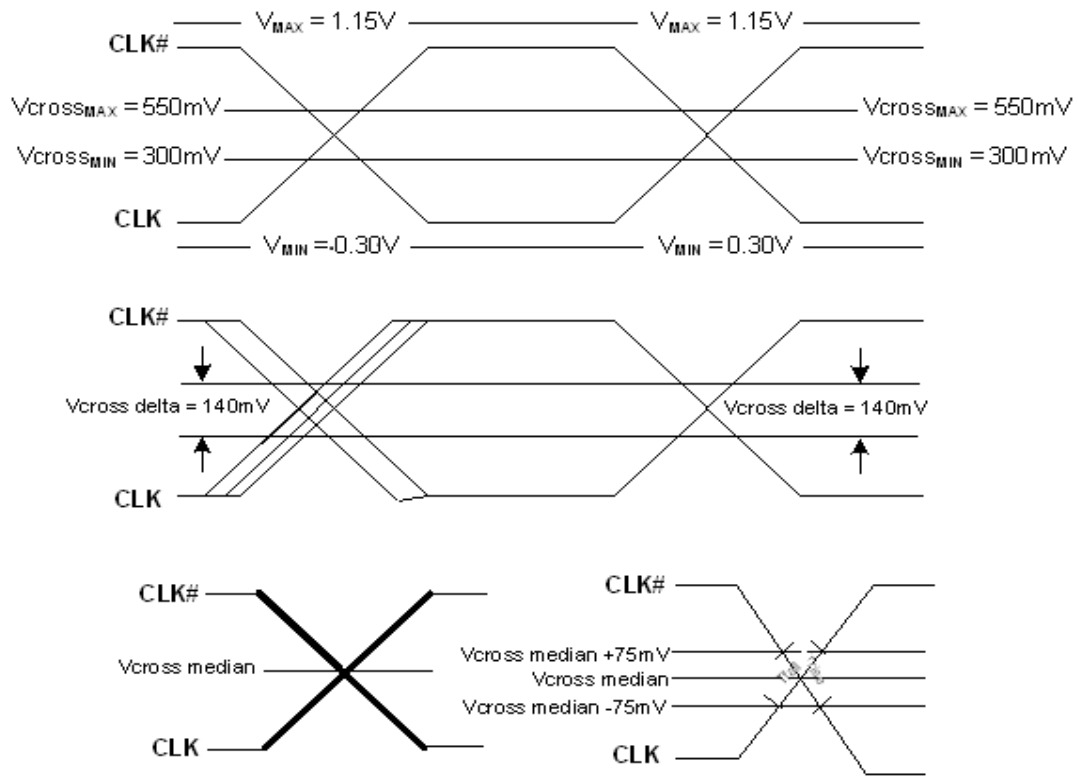


**Figure 1. 0.7 V Differential Load Configuration**



**Figure 2. Differential Measurement for Differential Output Signals (for AC Parameters Measurement)**





**Figure 3. Single-Ended Measurement for Differential Output Signals  
(for AC Parameters Measurement)**

## 4. Control Registers

### 4.1. Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers are individually enabled or disabled. The registers associated with the Serial Data Interface initialize to their default setting at power-up. The use of this interface is optional. Clock device register changes are normally made at system initialization, if any are required. The interface cannot be used during system operation for power management functions.

### 4.2. Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, access the bytes in sequential order from lowest to highest (most significant bit first) with the ability to stop after any complete byte is transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code described in Table 1 on page 4.

The block write and block read protocol is outlined in Table 4 on page 10 while Table 5 on page 11 outlines byte write and byte read protocol. The slave receiver address is 11010110 (D6h).

**Table 4. Block Read and Block Write Protocol**

Block Write Protocol		Block Read Protocol	
Bit	Description	Bit	Description
1	Start	1	Start
8:2	Slave address—7 bits	8:2	Slave address—7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code—8 bits	18:11	Command Code—8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Byte Count—8 bits	20	Repeat start
28	Acknowledge from slave	27:21	Slave address—7 bits
36:29	Data byte 1—8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
45:38	Data byte 2—8 bits	37:30	Byte Count from slave—8 bits
46	Acknowledge from slave	38	Acknowledge
....	Data Byte/Slave Acknowledges	46:39	Data byte 1 from slave—8 bits
....	Data Byte N—8 bits	47	Acknowledge
....	Acknowledge from slave	55:48	Data byte 2 from slave—8 bits
....	Stop	56	Acknowledge
		....	Data bytes from slave/Acknowledge
		....	Data Byte N from slave—8 bits
		....	NOT Acknowledge
		....	Stop

Table 5. Byte Read and Byte Write Protocol

Byte Write Protocol		Byte Read Protocol	
Bit	Description	Bit	Description
1	Start	1	Start
8:2	Slave address–7 bits	8:2	Slave address–7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code–8 bits	18:11	Command Code–8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Data byte–8 bits	20	Repeated start
28	Acknowledge from slave	27:21	Slave address–7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		37:30	Data from slave–8 bits
		38	NOT Acknowledge
		39	Stop

## Control Register 0. Byte 0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 00000000

Bit	Name	Function
7:0	Reserved	

## Control Register 1. Byte 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				DIFF0_OE		DIFF1_OE		DIFF2_OE
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 00010101

Bit	Name	Function
7:5	Reserved	
4	DIFF0_OE	<b>Output Enable for DIFF0.</b> 0: Output disabled. 1: Output Enabled.
3	Reserved	
2	DIFF1_OE	<b>Output Enable for DIFF1.</b> 0: Output disabled. 1: Output enabled.
1	Reserved	
0	DIFF2_OE	<b>Output Enable for DIFF2.</b> 0: Output disabled. 1: Output enabled.

**Control Register 2. Byte 2**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	DIFF3_OE	DIFF4_OE	DIFF5_OE					
<b>Type</b>	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 11100000

Bit	Name	Function
7	DIFF3_OE	<b>Output Enable for DIFF3.</b> 0: Output disabled. 1: Output enabled.
6	DIFF4_OE	<b>Output Enable for DIFF4.</b> 0: Output disabled. 1: Output enabled.
5	DIFF5_OE	<b>Output Enable for DIFF5.</b> 0: Output disabled. 1: Output enabled.
4:0	Reserved	

**Control Register 3. Byte 3**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	Rev Code[3:0]				Vendor ID[3:0]			
<b>Type</b>	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 00001000

Bit	Name	Function
7:4	Rev Code[3:0]	<b>Program Revision Code.</b>
3:0	Vendor ID[3:0]	<b>Vendor Identification Code.</b>

## Control Register 4. Byte 4

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	BC[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 00000110

Bit	Name	Function
7:0	BC[7:0]	Byte Count Register.

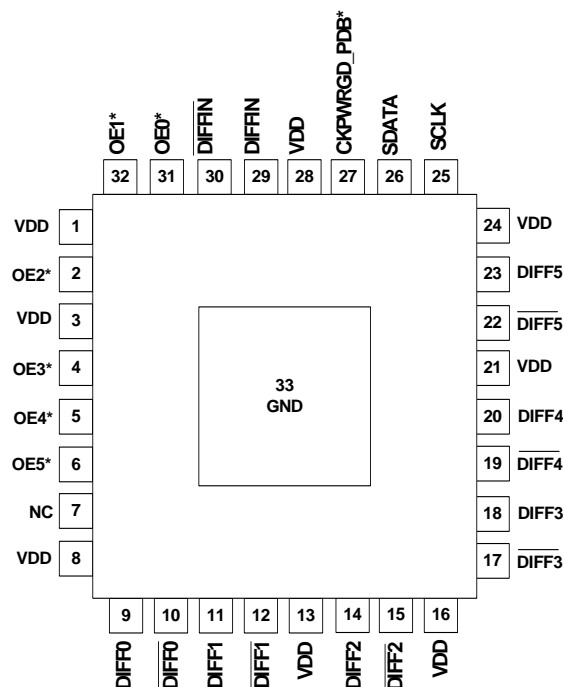
## Control Register 5. Byte 5

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DIFF_Amp_Sel	DIFF_Amp_Cntl[2]	DIFF_Amp_Cntl[1]	DIFF_Amp_Cntl[0]				
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 11011000

Bit	Name	Function
7	DIFF_Amp_Sel	<b>Amplitude Control for DIFF Differential Outputs.</b> 0: Differential outputs with Default amplitude. 1: Differential outputs amplitude is set by Byte 5[6:4].
6	DIFF_Amp_Cntl[2]	<b>DIFF Differential Outputs Amplitude Adjustment.</b> 000: 300 mV 001: 400 mV 010: 500 mV 011: 600 mV 100: 700 mV 101: 800 mV 110: 900 mV 111: 1000 mV
5	DIFF_Amp_Cntl[1]	
4	DIFF_Amp_Cntl[0]	
3:0	Reserved	

## 5. Pin Descriptions: 32-Pin QFN



\*Note: Internal 100 kohm pull-up.

Table 6. Si53156 32-Pin QFN Descriptions

Pin #	Name	Type	Description
1	VDD	PWR	3.3 V Power Supply
2	OE2	I,PU	3.3 V input to disable DIFF2 (internal 100 kΩ pull-up). Refer to Table 1 on page 4 for OE specifications.
3	VDD	PWR	3.3 V Power Supply
4	OE3	I,PU	3.3 V input to disable DIFF3 (internal 100 kΩ pull-up). Refer to Table 1 on page 4 for OE specifications.
5	OE4	I,PU	3.3 V input to disable DIFF4 (internal 100 kΩ pull-up). Refer to Table 1 on page 4 for OE specifications.
6	OE5	I,PU	3.3 V input to disable DIFF5 (internal 100 kΩ pull-up). Refer to Table 1 on page 4 for OE specifications.
7	NC	NC	No Connect
8	VDD	PWR	3.3 V Power Supply
9	DIFF0	O, DIF	0.7 V, 100 MHz differential clock
10	$\overline{\text{DIFF0}}$	O, DIF	0.7 V, 100 MHz differential clock
11	DIFF1	O, DIF	0.7 V, 100 MHz differential clock
12	$\overline{\text{DIFF1}}$	O, DIF	0.7 V, 100 MHz differential clock

**Table 6. Si53156 32-Pin QFN Descriptions**

Pin #	Name	Type	Description
13	VDD	PWR	3.3 V Power Supply
14	DIFF2	O, DIF	0.7 V, 100 MHz differential clock
15	$\overline{\text{DIFF2}}$	O, DIF	0.7 V, 100 MHz differential clock
16	VDD	PWR	3.3 V Power Supply
17	$\overline{\text{DIFF3}}$	O, DIF	0.7 V, 100 MHz differential clock
18	DIFF3	O, DIF	0.7 V, 100 MHz differential clock
19	$\overline{\text{DIFF4}}$	O, DIF	0.7 V, 100 MHz differential clock
20	DIFF4	O, DIF	0.7 V, 100 MHz differential clock
21	VDD	PWR	3.3 V Power Supply
22	$\overline{\text{DIFF5}}$	O, DIF	0.7 V, 100 MHz differential clock
23	DIFF5	O, DIF	0.7 V, 100 MHz differential clock
24	VDD	PWR	3.3 V Power Supply
25	SCLK	I	SMBus compatible SCLOCK
26	SDATA	I/O	SMBus compatible SDATA
27	CKPWRGD_PDB	I, PU	3.3 V LVTTTL input. This pin is a level sensitive strobe used to determine when latch inputs are valid and are ready to be sampled. A real-time active low input for asserting power down (PDB) and disabling all outputs (internal 100 k $\Omega$ pull-up).
28	VDD	PWR	3.3 V Power Supply
29	DIFFIN	I	0.7 V Differential True Input, typically 100 MHz. Input frequency range 100 to 210 MHz.
30	$\overline{\text{DIFFIN}}$	O	0.7 V Differential Complement Input, typically 100 MHz. Input frequency range 100 to 210 MHz.
31	OE0	I,PU	3.3 V input to disable DIFF0 (internal 100 k $\Omega$ pull-up). Refer to Table 1 on page 4 for OE specifications.
32	OE1	I,PU	3.3 V input to disable DIFF1 (internal 100 k $\Omega$ pull-up). Refer to Table 1 on page 4 for OE specifications.
33	GND	GND	Ground for bottom pad of the IC.

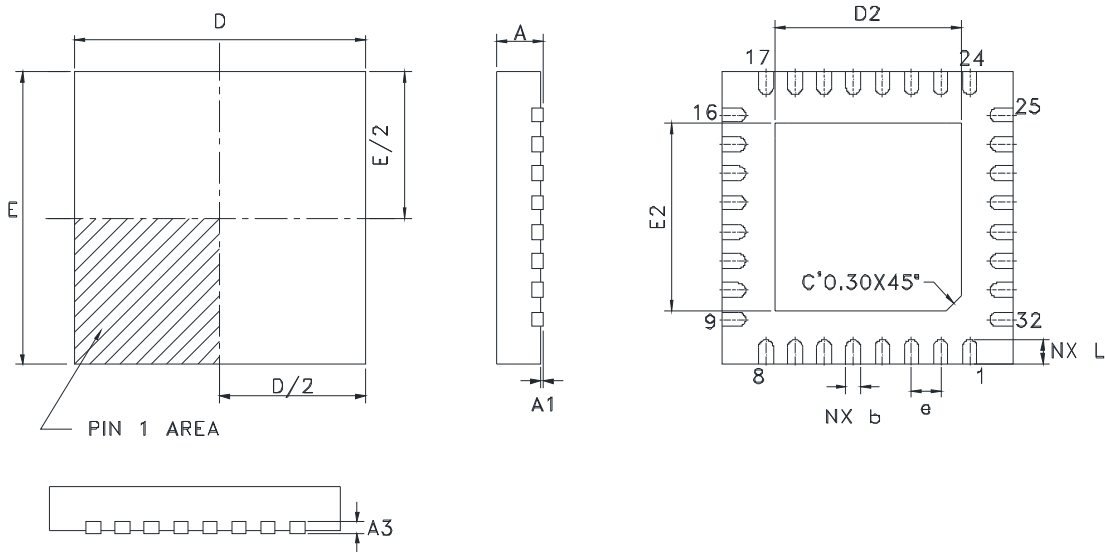


**6. Ordering Guide**

<b>Part Number</b>	<b>Package Type</b>	<b>Temperature</b>
<b>Lead-free</b>		
Si53156-A01AGM	32-pin QFN	Industrial, –40 to 85 °C
Si53156-A01AGMR	32-pin QFN—Tape and Reel	Industrial, –40 to 85 °C

## 7. Package Outline

Figure 4 illustrates the package details for the Si53156. Table 7 lists the values for the dimensions shown in the illustration.



**Figure 4. 32-Pin Quad Flat No Lead (QFN) Package**

**Table 7. Package Diagram Dimensions**

Symbol	Millimeters		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.175	0.20	0.225
b	0.20	0.25	0.30
D	4.90	5.00	5.10
D2	3.15	3.20	3.25
e	0.50 BSC		
E	4.90	5.00	5.10
E2	3.15	3.20	3.25
L	0.30	0.40	0.50

**Notes:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.
4. Coplanarity less than 0.08 mm.
5. Terminal #1 identifier and terminal numbering convention conform to JESD 95-1 SPP-012.

**NOTES:**

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