REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with N.O.R. 5962-R016-93.	92-11-09	M. A. FRYE
B	Redrawn with changes. Add device type 04. Add vendor CAGE 33256.	94-09-01	M. A. FRYE
C	Changes in accordance with N.O.R. 5962-R017-95.	95-01-17	M. A. FRYE
D	Changes in accordance with N.O.R. 5962-R060-95.	95-01-25	M. A. FRYE
E	Add device type 05 with a temperature range of –55°C to +90°C. Make limit changes to the +PSS1 test as specified under table I. - ro	02-10-31	R. MONNIN

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV																				
SHEET																				
REV	E	E	E	E	E	E														
SHEET	15	16	17	18	19	20														

REV STATUS	REV	E	E	E	E	E	E	E	E	E	E	E	E	E	E
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
CHARLES E. BESORE

APPROVED BY
MICHAEL A. FRYE

DRAWING APPROVAL DATE
92-05-14

MICROCIRCUIT, LINEAR, 12-BIT A/D CONVERTER WITH MICROPROCESSOR INTERFACE, MONOLITHIC SILICON

REVISION LEVEL	SIZE	CAGE CODE	
E	A	**67268**	**5962-91690**

SHEET 1 OF 20

DSCC FORM 2233
APR 97

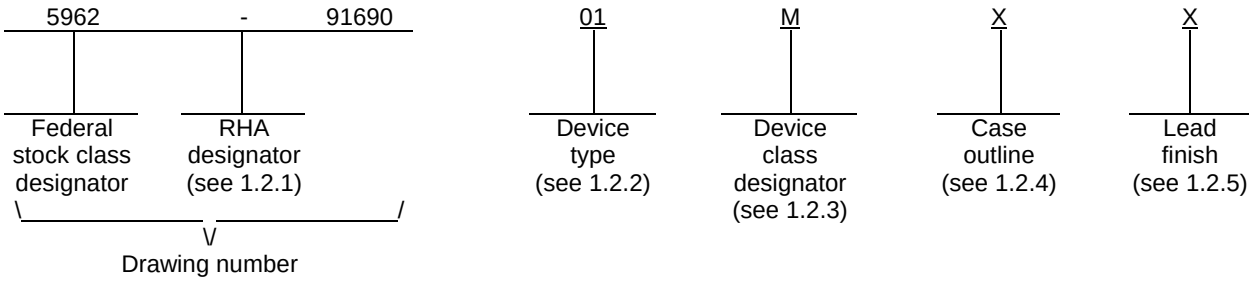
5962-E014-03

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	674ZA	High performance, 12-bit A/D converter with microprocessor interface and S/H
02	674ZB	Medium performance, 12-bit A/D converter with microprocessor interface and S/H
03	674BT	12-bit A/D converter with microprocessor interface
04	674AT	12-bit A/D converter with microprocessor interface
05	674BT	12-bit A/D converter with microprocessor interface

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP1-T28 or CDIP2-T28	28	Dual-in-line
3	CQCC1-N28	28	Square leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

V_{CC} to digital common ..... 0 V dc to +16.5 V dc
V_{EE} to digital common ..... 0 V dc to -16.5 V dc 2/
V_{LOGIC} to digital common ..... 0 V dc to +7 V dc
Analog common to digital common:
  Device types 01, 02, and 04 ..... -0.5 V dc to +1 V dc
  Device types 03 and 05 ..... ±1 V dc
Control inputs (CE, $\overline{CS}$, A_0, 12/8, R / $\overline{C}$) to
  digital common ..... -0.5 V dc to V_{LOGIC} + 0.5 V dc
Analog inputs (REF IN, BIP OFF, 10 V_{IN}) to
  analog common ..... ±16.5 V dc
20 V_{IN} analog input voltage to analog common ..... ±24 V dc
$V_{REF\ OUT}$ ..... Indefinite short to common
  momentary short to V_{CC}
Power dissipation (P_D):
  Device types 01 02, and 04 (T_A = +25°C) ..... 1000 mW
  Device types 03 and 05 (T_A = +25°C) ..... 470 mW
Lead temperature (soldering, 10 seconds) ..... +300°C
Storage temperature range ..... -65°C to +150°C
Junction temperature (T_J) ..... +175°C
Thermal resistance, junction-to-case (θ_{JC}) ..... See MIL-STD-1835
Thermal resistance, junction-to-ambient (θ_{JA}):
  Device types 01 and 02 case X ..... 48°C/W
  Device types 03 and 05 case X ..... 60°C/W
  Device type 04 case X ..... 50°C/W
  Case 3 ..... 48°C/W

1.4 Recommended operating conditions.

Logic supply voltage (V_{LOGIC}) ..... +4.5 V dc to +5.5 V dc
Positive supply voltage (V_{CC}) ..... +11.4 V dc to +16.5 V dc
Negative supply voltage (V_{EE}) ..... -11.4 V dc to -16.5 V dc 2/
Ambient operating temperature range (T_A) :
  Device types 01 – 04 ..... -55°C to +125°C
  Device type 05 ..... -55°C to +90°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ V_{EE} is not required for operation of devices 01, 02, and 04.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Block diagrams. The block diagrams shall be as specified on figure 3.

3.3 Electrical performance characteristics and post irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post irradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ V_{CC} = +15 V, V_{EE} = -15 V, V_{LOGIC} = +5 V, unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Power supply current 2/ from V_{LOGIC}	I_{LOGIC}	Three-state outputs	1,2,3	01,02, 04		+1.0	mA
				03,05		+7.0	
Power supply current 2/ from V_{CC}	I_{CC}	Three-state outputs	1,2,3	01,02, 04		+9.0	mA
				03,05		+7.0	
Power supply current 2/ from V_{EE}	I_{EE}	Three-state outputs	1,2,3	03,05	-14		mA
Resolution			1,2,3	All	12		Bits
Integral linearity error	ILE	Unipolar 10 V span, Bipolar 20 V span	1	All	-0.5	+0.5	LSB
			2,3		-1.0	+1.0	
Differential linearity error (minimum resolution for which no missing codes are guaranteed)	DLE		1,2,3	All	12		Bits
Unipolar offset voltage error	V_{IO}	10 V span	1	All	-2.0	+2.0	LSB
Unipolar offset voltage drift	$\Delta V_{IO} / \Delta T$	10 V span, using internal reference	2,3	All	-1.0	+1.0	LSB
Bipolar zero offset error	B_Z	20 V span	1	01,02, 04	-4.0	+4.0	LSB
				03,05	-3.0	+3.0	
Bipolar zero offset drift	$\Delta B_Z / \Delta T$	20 V span, using internal reference	2,3	02,03, 04,05	-2.0	+2.0	LSB
				01	-1.0	+1.0	
Gain error	AE	Bipolar 20 V span 50 Ω resistor from REF OUT to REF IN	1	01,02, 04		0.3	%FSR
				03,05		0.125	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ V_{CC} = +15 V, V_{EE} = -15 V, V_{LOGIC} = +5 V, unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Gain error drift	$\Delta A_E / \Delta T$	Bipolar 20 V span, using internal reference	2,3	01		12.5	ppm/°C
				02,04		25.0	
				03,05		17.5	
Power supply sensitivity to V_{CC} 3/ 4/	+PSS1		1,2,3	01-04	-1.5	+1.5	LSB
				05	-1.0	+1.0	
Power supply sensitivity to V_{LOGIC} 3/ 5/	+PSS2		1,2,3	All	-0.5	+0.5	LSB
Power supply sensitivity to V_{EE} 3/ 6/	-PSS3		1,2,3	All	-1.0	+1.0	LSB
Input impedance 2/	Z_{IN}	10 V span	1,2,3	01,02, 04	3.75	6.25	kΩ
				03,05	3.0	7.0	
		20 V span		01,02, 04	15	25	
				03,05	6	14	
Internal reference voltage 7/	V_{REF}	I_{REFOUT} = 2 mA	1,2,3	01,02	9.97	10.03	V
				03,04, 05	9.9	10.1	
Logic input high voltage (CE, $\overline{CS}$, 12/$\overline{8}$, R/$\overline{C}$, A_O) 2/ 8/	V_{IH}	Logic "1"	1,2,3	All	+2.0	+5.5	V
Logic input low voltage (CE, $\overline{CS}$, 12/$\overline{8}$, R/$\overline{C}$, A_O) 2/ 8/	V_{IL}	Logic "0"	1,2,3	All	-0.5	+0.8	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$, V_{CC} = +15 V, V_{EE} = -15 V, V_{LOGIC} = +5 V, unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Logic input current 2/	$I_{IN(LOG)}$	0 to +5.5 V input	1,2,3	01,02		+1.0	µA
				04	-20	+20	
		0 to +5.0 V input		03,05	-10	+10	
Logic low output voltage (DB11-DB0, STS) 2/	V_{OL}	Logic "0', I_{SINK} = 1.6 mA	1,2,3	All		+0.4	V
Logic high output voltage (DB11-DB0) 2/	V_{OH}	Logic "1", I_{SOURCE} = 500 µA	1,2,3	All	+2.4		V
Three-state output leakage current	I_Z	High-Z state, (DB11- DB0 only), $V_{applied}$ = 5.0 V	1,2,3	01,02	-5.0	+5.0	µA
				03,05	-10	+10	
				04	-20	+20	
Functional tests 2/		See section 4.4.1b	7,8	All			
Low R/$\overline{C}$ pulse width 9/	t_{HRL}	See figure 4	9,10,11	All	50		ns
STS delay from R/$\overline{C}$ 10/	t_{DS}	See figure 4	9,10,11	01,02, 04		200	ns
				03,05		225	
Data valid after R/$\overline{C}$ low 11/	t_{HDR}	See figure 4	9,10,11	All	25		ns
STS delay after data valid	t_{HS}	See figure 4	9,10,11	01,02, 04	300	1000	ns
				03,05	30	600	
High R/$\overline{C}$ pulse width 9/	t_{HRH}	See figure 4	9,10,11	All	150		ns
Data access time 12/	t_{DDR}	See figure 4	9,10,11	All		150	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ V_{CC} = +15 V, V_{EE} = -15 V, V_{LOGIC} = +5 V, unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
STS delay from CE 10/	t_{DSC}	See figure 5	1,2,3	01,02		200	ns
				03,05		225	
CE pulse width 9/	t_{HEC}	See figure 5	1,2,3	All	50		ns
$\overline{CS}$ to CE setup	t_{SSC}	See figure 5	1,2,3	All	50		ns
Conversion time 13/	t_C	8-bit cycle, see figure 5	9,10,11	All	6	10	µs
		12-bit cycle, see figure 5			9	15	
$\overline{CS}$ low during CE high	t_{HSC}	See figure 5	9,10,11	All	50		ns
R/$\overline{C}$ to CE setup	t_{SRC}	See figure 5	9,10,11	All	50		ns
R/$\overline{C}$ low during CE high	t_{HRC}	See figure 5	9,10,11	All	50		ns
A_O to CE setup	t_{SAC}	See figure 5	9,10,11	All	0		ns
A_O valid during CE high	t_{HAC}	See figure 5	9,10,11	All	50		ns
Access time (from CE) 12/	t_{DD}	See figure 6	9,10,11	All		150	ns
Data valid after CE low 11/	t_{HD}		9,10,11	01,02, 04	25		ns
			9,10,	03,05	25		
			11		15		
Output float delay 11/	t_{HL}		9,10,11	All		150	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ V_{CC} = +15 V, V_{EE} = -15 V, V_{LOGIC} = +5 V, unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$\overline{CS}$ to CE setup	t_{SSR}	See figure 6	9,10,11	All	50		ns
R/$\overline{C}$ to CE setup	t_{SRR}	See figure 6	9,10,11	All	0		ns
Sample and hold acquisition time 14/	t_{acq}	T_A = +25°C	9	01,02, 04	1.2	2.0	µs
A_O to CE setup	t_{SAR}	See figure 6	9,10,11	All	50		ns
$\overline{CS}$ valid after CE low	t_{HSR}	See figure 6	9,10,11	All	0		ns
R/$\overline{C}$ high after CE low	t_{HRR}	See figure 6	9,10,11	All	0		ns
A_O valid after CE low	t_{HAR}	See figure 6	9,10,11	All	50		ns

1/ For device types 01, 02, 03, 04, T_A = -55°C to +125°C. For device type 05, T_A = -55°C to +90°C 12/$\overline{8}$ connected to V_{LOGIC}, A_O and $\overline{CS}$ at logic "0", CE at logic "1". 10 V unipolar: 50 Ω resistor pin 8 to pin 10, 50 Ω resistor pin 12 to ground. Analog input connected to pin 13. 20 V bipolar: 50 Ω resistor pin 8 to pin 12, 50 Ω resistor pin 8 to pin 10. Analog input connected to pin 14. Unless otherwise noted, these conditions apply.

2/ Device types are tested to the conditions stated in table I, but are guaranteed to the specified limits for the following variations in the supply voltage ranges. V_{LOGIC} = +5 V to ±5%, V_{CC} = +12 V ±5% and +15 V to ±10%, V_{EE} = -12 V ±5% and -15 V ±10%. (V_{EE} not required for operation of devices 01, 02, and 04). For device types 03 and 05, V_{LOGIC} = +5 V to ±10%.

3/ Maximum change in full scale calibration due to supply voltage shifts. Full scale calibration to be measured at minimum and maximum voltage settings for each individual supply.

4/ +13.5 V ≤ V_{CC} ≤ +16.5 V, V_{LOGIC} = 5 V, V_{EE} = -15 V and +11.4 V ≤ V_{CC} ≤ +12.6 V, V_{LOGIC} = 5 V, V_{EE} = -12 V. (V_{EE} not required for operation of devices 01, 02 and 04).

5/ 4.5 V ≤ V_{LOGIC} ≤ 5.5 V, V_{CC} = 15 V, V_{EE} = -15 V. (V_{EE} not required for operation of devices 01, 02, and 04).

6/ -16.5 V ≤ V_{EE} ≤ -13.5 V, V_{LOGIC} = 5 V, V_{CC} = +15 V and -12.6 V ≤ V_{EE} ≤ -11.4 V, V_{LOGIC} = 5 V, V_{CC} = +12 V.

7/ Reference should be buffered for operation on ±12 V supplies. External load should not change during conversion.

TABLE I. Electrical performance characteristics – Continued.

8/ For devices types 01, 02, and 04, 12/ $\overline{8}$ is not TTL compatible, must be hard-wired to V_{LOGIC} or digital common.

9/ Pulse width is measured at the Schottky TTL input logic threshold voltage (1.3 V).

10/ t_{DS} and t_{DSC} are measured from the point when the input signal crosses the Schottky TTL logic threshold voltage (1.3 V) to when the STS output reaches 2.4 V. No external loading is applied to STS.

11/ t_{HDR}, t_{HD}, and t_{HL} are measured from the point when the input signal crosses the Schottky TTL logic threshold voltage (1.3 V), to when the output voltage has moved 0.5 V in the direction of its final high impedance output voltage. Each individual data bit (DBO - DB11) is measured for both logic one to "high Z" and logic zero to "high Z" transitions. External loading is as shown on figure 7.

12/ t_{DDR} and t_{DD} are measured from the point when the input signal crosses the Schottky TTL logic threshold voltage (1.3 V), to when the output crosses either 2.4 V for a logic one, or 0.4 V for a logic zero. Each individual data bit (DBO - DB11) is measured for both "high Z" to logic zero transitions. External loading is as shown on figure 8.

13/ t_C is measured as the time from when the STS line crosses the 1.0 V level, going positive, to when it crosses the 1.0 V level going negative. No external loading is applied to STS.

14/ Guaranteed by design.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-PRF-38535, appendix A.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

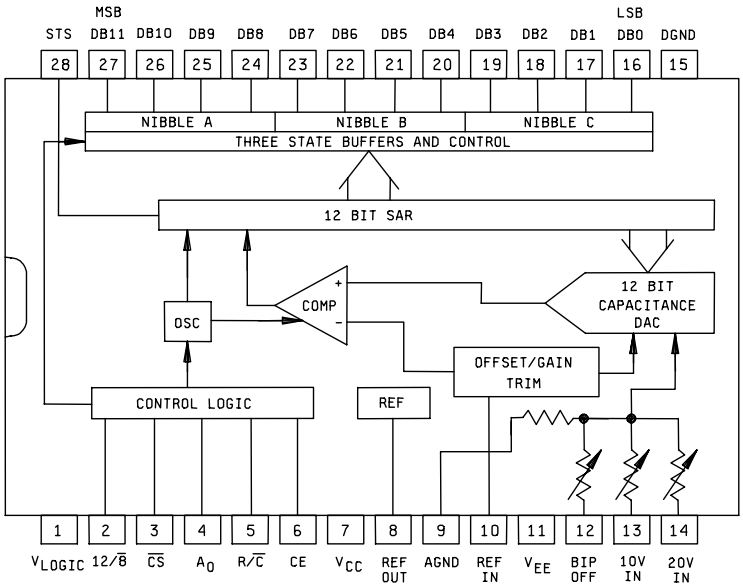
3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 93 (see MIL-PRF-38535, appendix A).

Device types	01, 02, 04	03, 05	05
Case outlines	X and 3	X and 3	3
Terminal number	Terminal symbol		
1	+5 V supply (V_{LOGIC})	+5 V supply (V_{LOGIC})	+5 V supply (V_{LOGIC})
2	Data mode select (12/$\overline{8}$)	Data mode select (12/$\overline{8}$)	Data mode select (12/$\overline{8}$)
3	Chip select ($\overline{CS}$)	Chip select ($\overline{CS}$)	Chip select ($\overline{CS}$)
4	Byte address / short cycle (A_O)	Byte address / short cycle (A_O)	Byte address / short cycle (A_O)
5	Read / convert (R / $\overline{C}$)	Read / convert (R / $\overline{C}$)	Read / convert (R / $\overline{C}$)
6	Chip enable (CE)	Chip enable (CE)	Chip enable (CE)
7	+12 V / +15 V supply (V_{CC})	+12 V / +15 V supply (V_{CC})	+12 V / +15 V supply (V_{CC})
8	+10 V reference (REF OUT)	+10 V reference (REF OUT)	+10 V reference (REF OUT)
9	Analog common (AGND)	Analog common (AGND)	Analog common (AGND)
10	Reference input (REF IN)	Reference input (REF IN)	Reference input (REF IN)
11	-12 / -15 V supply (V_{EE})	-12 / -15 V supply (V_{EE})	-12 / -15 V supply (V_{EE})
12	Bipolar offset (BIP OFF)	Bipolar offset (BIP OFF)	Bipolar offset (BIP OFF)
13	10 V span input (10 V_{IN})	10 V span input (10 V_{IN})	10 V span input (10 V_{IN})
14	20 V span input (20 V_{IN})	20 V span input (20 V_{IN})	20 V span input (20 V_{IN})
15	Digital common (DGND)	Digital common (DGND)	Digital common (DGND)
16	DB0 (LSB)	DB0 (LSB)	DB0 (LSB)
17	DB1	DB1	DB1
18	DB2	DB2	DB2
19	DB3	DB3	DB3
20	DB4	DB4	DB4
21	DB5	DB5	DB5
22	DB6	DB6	DB6
23	DB7	DB7	DB7
24	DB8	DB8	DB8
25	DB9	DB9	DB9
26	DB10	DB10	DB10
27	DB11 (MSB)	DB11 (MSB)	DB11 (MSB)
28	Status (STS)	Status (STS)	Status (STS)

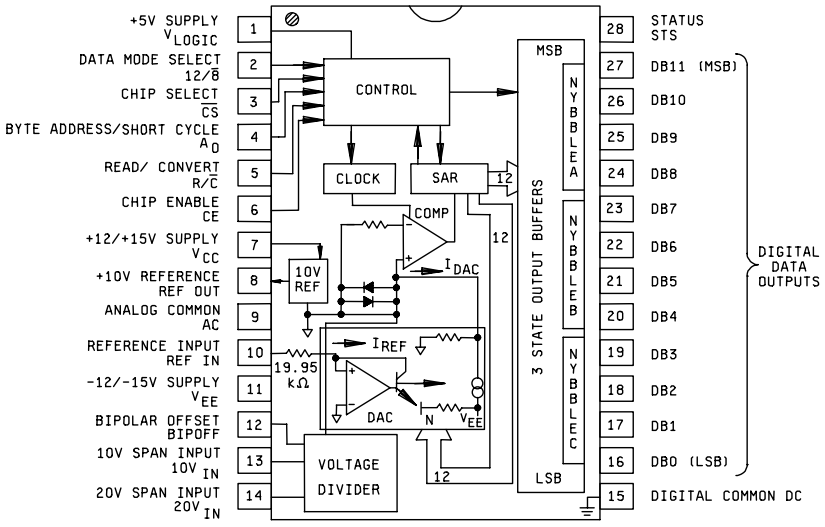
FIGURE 1. Terminal connections.

CE	$\overline{CS}$	R / $\overline{C}$	12/$\overline{8}$	A_O	Operation
0	X	X	X	X	None
X	1	X	X	X	None
1	0	0	X	0	Initiate 12-bit conversion
1	0	0	X	1	Initiate 8-bit conversion
1	0	1	1	X	Enable 12-bit parallel output
1	0	1	0	0	Enable 8 most significant bits
1	0	1	0	1	Enable 4 LSBs + 4 trailing zeros

FIGURE 2. Truth table.

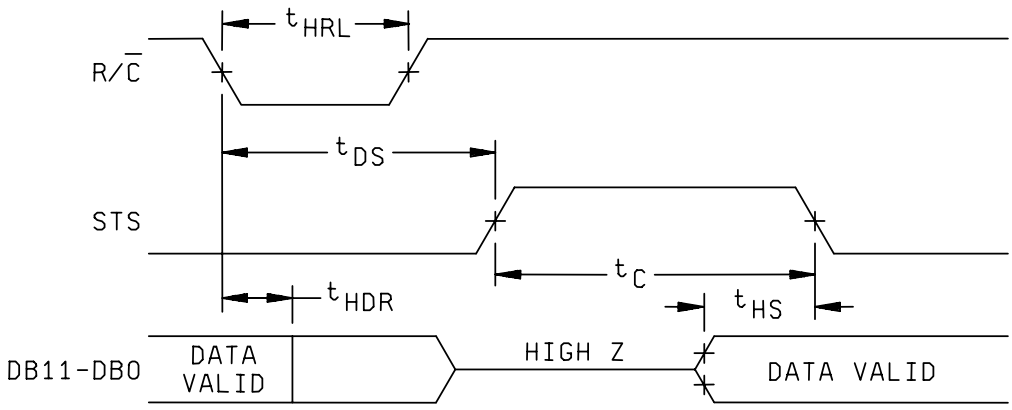


DEVICE TYPES 01,02, AND 04

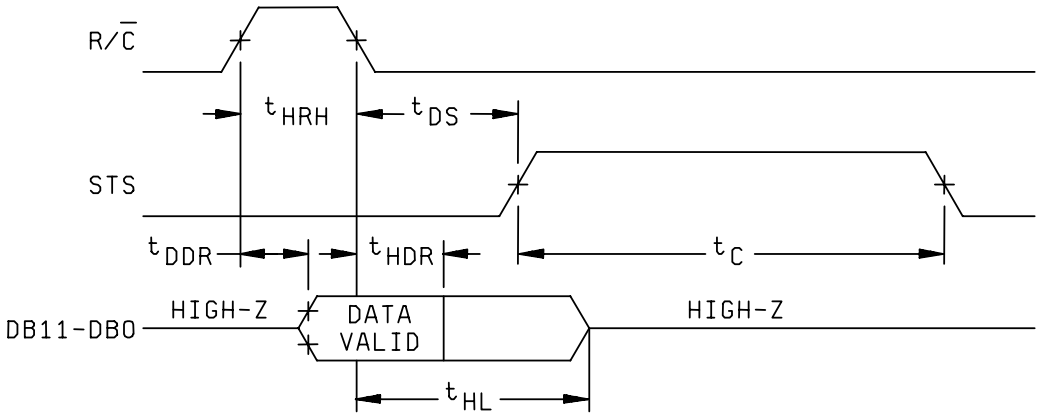


DEVICE TYPES 03 AND 05

FIGURE 3. Block diagram.



LOW PULSE FOR R / $\overline{C}$ - OUTPUTS ENABLED AFTER CONVERSION



HIGH PULSE FOR R / $\overline{C}$ - OUTPUTS ENABLED WHILE R / $\overline{C}$ HIGH, OTHERWISE HIGH - Z

FIGURE 4. High / low pulse for R / $\overline{C}$.

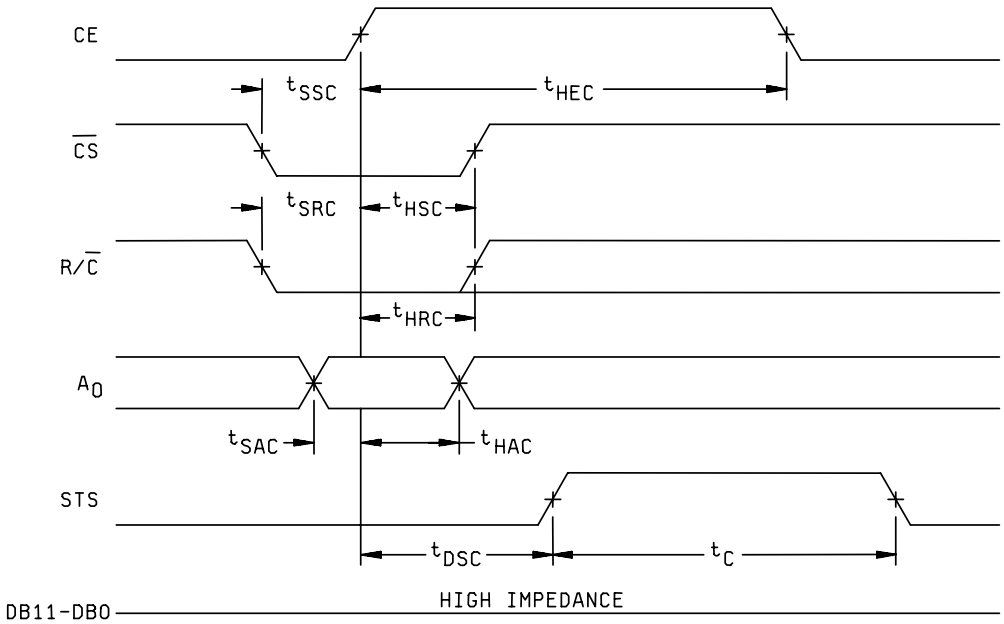


FIGURE 5. Convert start diagram.

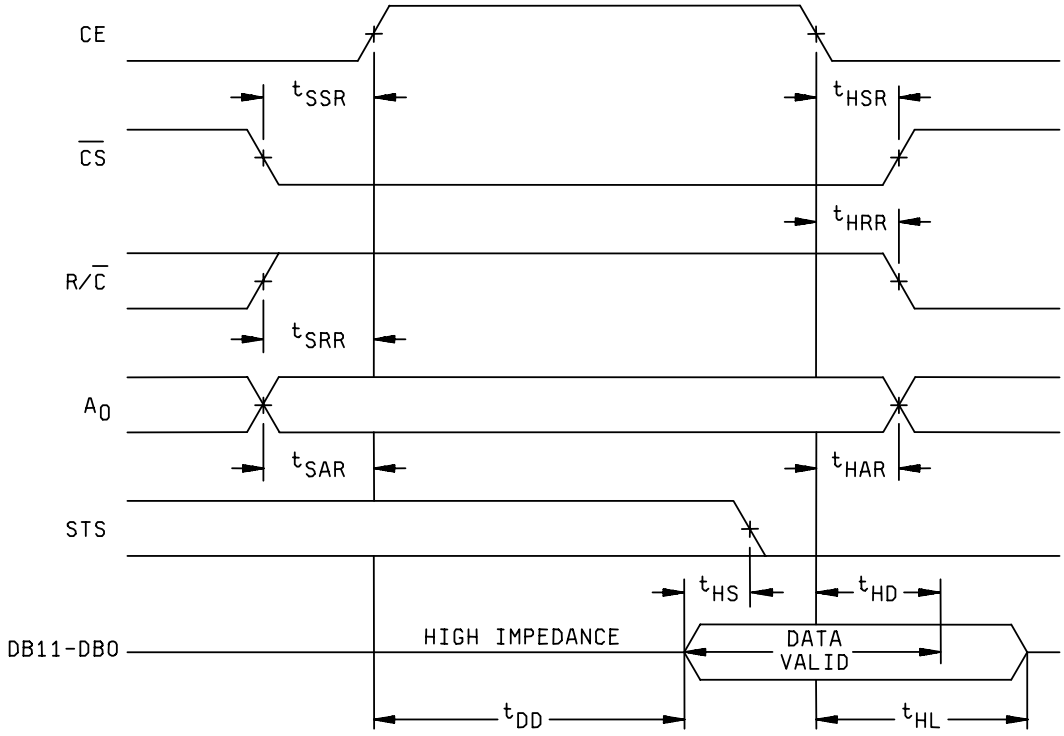


FIGURE 6. Read cycle timing.

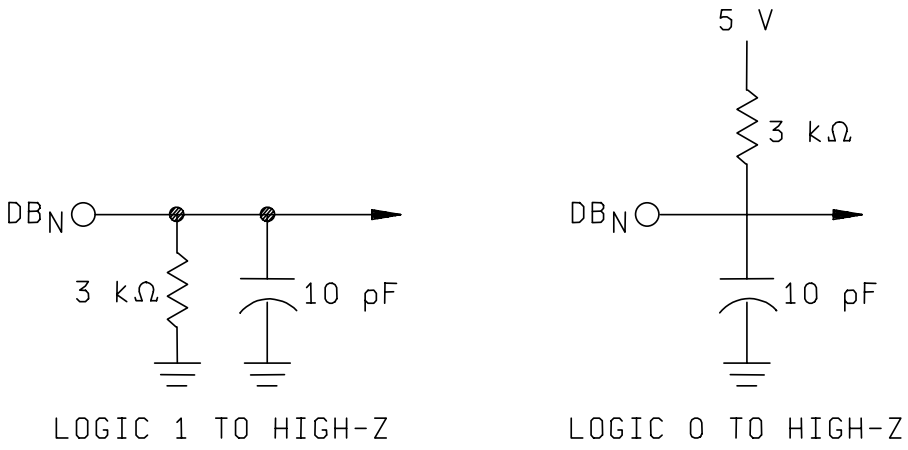


FIGURE 7. Load circuit for output float delay test.

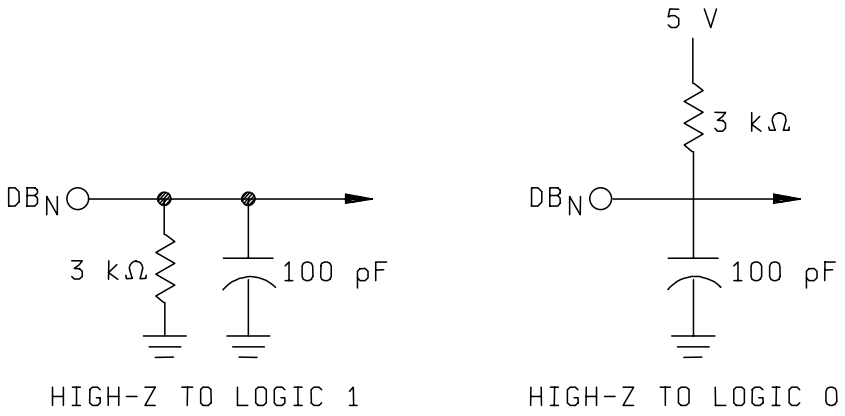


FIGURE 8. Load circuit for access time test.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1	1
Final electrical parameters (see 4.2)	1,2,3 1/	1,2,3 1/	1,2,3 1/
Group A test requirements (see 4.4)	1,2,3,7,8,9,10,11 2/	1,2,3,7,8, 2/ 9,10,11	1,2,3,7,8, 2/ 9,10,11
Group C end-point electrical parameters (see 4.4)	1	1	1
Group D end-point electrical parameters (see 4.4)	1	1	1
Group E end-point electrical parameters (see 4.4)	---	---	---

1/ PDA applies to subgroup 1.
2/ Subgroups 10 and 11, if not tested, shall be guaranteed to the limits specified in table I.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the post irradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 02-10-31

Approved sources of supply for SMD 5962-91690 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/	Reference military specification PIN
5962-9169001MXC	3/	HADC674ZAMD/883	M38510/14005BXA
5962-9169001M3A	3/	HADC674ZAMC/883	
5962-9169002MXC	3/	HADC674ZBMD/883	M38510/14006BXA
5962-9169002M3A	3/	HADC674ZBMC/883	
5962-9169003MXA	24355	AD674BTD/883B	M38510/14006BXA
5962-9169003M3A	24355	AD674BTE/883B	
5962-9169004MXC	3/	SP674AT/B	M38510/14006BXA
5962-9169004M3C	3/	SP674AT/B	
5962-9169005M3A	24355	AD674BTE/883B	

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: 804 Woburn Street Wilmington, MA 01887-3462

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.