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Tools and Solutions for the 16-bit Designer

A comprehensive overview of libraries, boards and software development tools for Microchip's 16-bit embedded control product families.

www.microchip.com/16bit

Microchip's Whole Product Solution

It has always been Microchip's goal to provide great silicon solutions to our customers. However, silicon is only part of the story. Support tools, such as programmers, compilers, reference designs, libraries, application notes, evaluation boards and the like are required to make your evaluation and product development process as efficient as possible. Microchip considers a product released when the silicon and its appropriate support tools are ready for production. This document describes Microchip's rapidly evolving solutions to support the ongoing enhancements to the 16-bit PIC24 Microcontrollers (MCUs) and dsPIC® Digital Signal Controllers (DSCs), including:

Development Tools:

- MPLAB® IDE Integrated Development Environment
- MPASM™ Assembler, MPLINK™ Linker, MPLIB™ Librarian and MPLAB® SIM Simulator
- MPLAB® C30 C Compiler
- MPLAB® Visual Device Initializer
- MPLAB® ICD 2 In-Circuit Debugger/Programmer
- MPLAB® REAL ICE™ In-Circuit Emulation System
- Software libraries and more

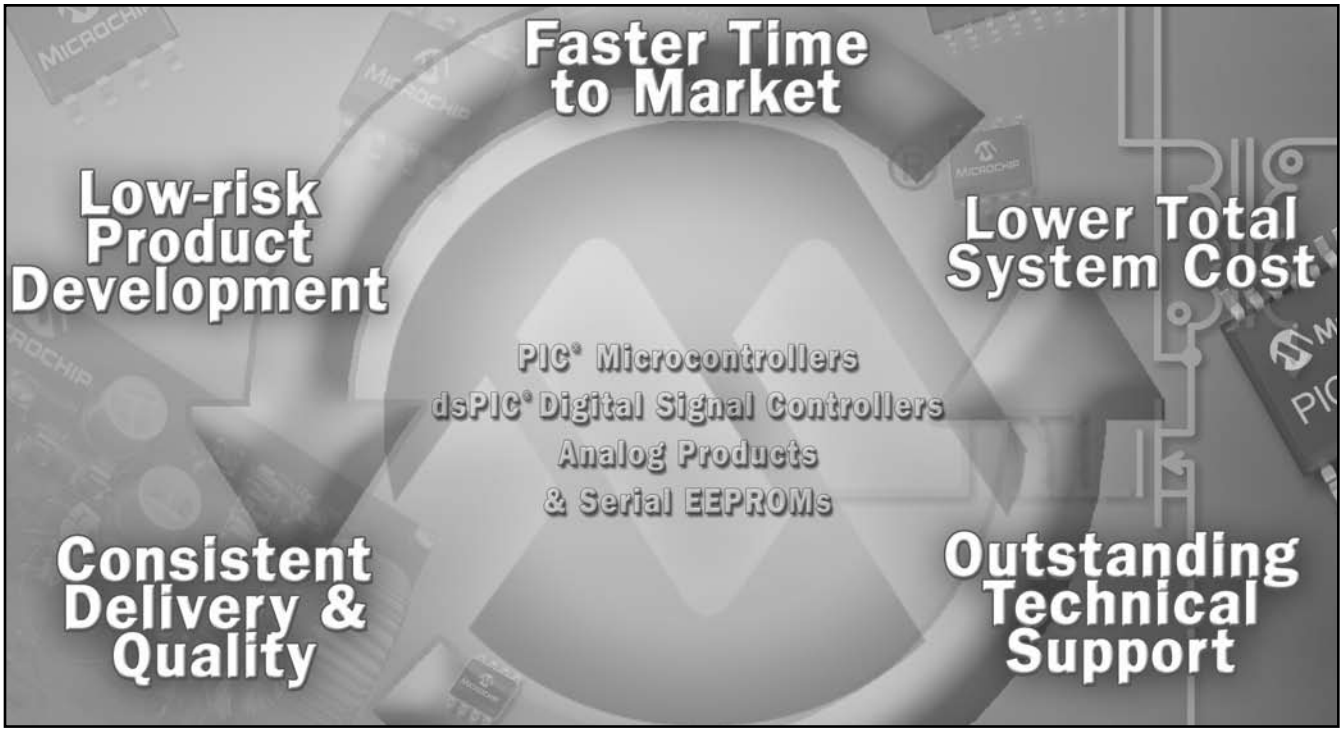
Reference Designs and Development Boards:

- Development boards
- Reference designs supported by application notes and web-based materials
- Application development designs

Design Materials and Training:

- Data sheets and reference manuals are available in print, online or on CD
- Training support including regional seminars, MASTERs, web seminars, Getting Started Guides and more

For more the most current information on the whole product solution available today for the PIC24 MCUs and dsPIC DSCs, please refer to the Microchip web site at **www.microchip.com/16bit.**



Tools and Solutions for the 16-bit Designer

Development Board Overview

Overview

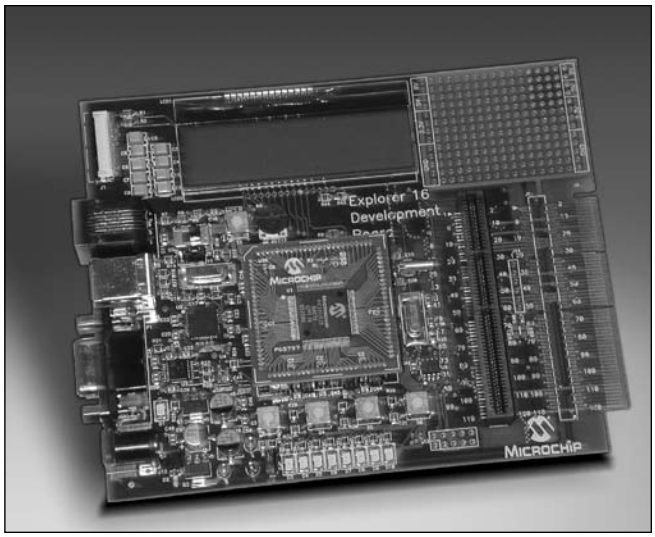
A full suite of cost-effective hardware development boards is available to support Microchip's 16-bit PIC24 Microcontroller (MCU) and dsPIC® Digital Signal Controller (DSC) product families. The table below presents a summary reference of the boards offered and the 16-bit devices supported. Additional information on specific boards are provided within this section.

Development Board	16-bit Device Support				Description/Comments
	dsPIC30F	dsPIC33F	PIC24H	PIC24F	
Explorer 16 Development Board	—	Yes	Yes	Yes	General Purpose Development Board Supports PICtail™ Plus plug-in boards via Expansion header
PICtail™ Plus Daughter Boards	—	Yes	Yes	Yes	
dsPICDEM™ 80-pin Starter Development Board	Yes	Yes	Yes	—	General Purpose Development Board Basic Starter Board
16-bit, 28-pin Starter Development Board	Yes	Yes	Yes	Yes	Basic Starter Board
dsPICDEM™ 1.1 Plus General Purpose Development Board	Yes	Yes	Yes	—	General Purpose Board and Voiceband Codec
dsPICDEM™ 2 General Purpose Development Board	Yes	—	—	—	General Purpose Development Board Supports dsPIC30F 18-, 28- and 40-pin DIP devices
dsPICDEM.net™ Connectivity Development Boards	Yes	—	—	—	V.32bis Soft-Modem / 10-BaseT Ethernet External 16-bit SRAM access example code
dsPICDEM™ MC1 Motor Control Development Board	Yes	—	—	—	Motor Control Development Board Interfaces to dsPICDEM MC1H and MC1L Power Modules
dsPICDEM™ MC1H High-voltage Power Module	Yes	Yes	—	—	3-Phase High-voltage Power Module
dsPICDEM™ MC1L Low-voltage Power Module	Yes	Yes	—	—	3-Phase Low-voltage Power Module
dsPICDEM™ SMPS Buck Development Board	Yes	—	—	—	Switch Mode Power Supply Development Board Basic Starter Board

Explorer 16 Development Board

Summary

This development board offers an economical way to evaluate both the PIC24F and PIC24H microcontrollers, as well as the dsPIC33F General Purpose and Motor Control families. This board is an ideal prototyping tool to help you quickly develop and validate key design requirements.



Features

Key features of the Explorer 16 Development Board include:

- A 100-pin dsPIC33F General Purpose (MA330011) and 100-pin PIC24F (MA240011) plug-in modules
- Supports 100-pin PIC24H (MA240012) plug-in module
- Supports the dsPIC33FJ256GP710 and the PIC24FJ128GA010
- Modular design for plug-in demonstration boards, expansion header
- RS-232 serial channel
- MPLAB® ICD 2 support ready
- 2x16 LCD
- LEDs, switches and potentiometer

Package Contents

- Explorer 16 Development Board (DM240001) preprogrammed with a 100-pin dsPIC33F General Purpose plug-in module (MA330011) and a 100-pin PIC24F (MA240011) plug-in module
- Documentation on CD

Minimum Requirements:

- MPLAB IDE v7.40 or later
- MPLAB ICD 2
- MPLAB C30 v2.02 or later

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PICtail™ Plus Daughter Boards

PICtail™ Plus Daughter Boards: Card Edge Modular Expansion Connectors

The Explorer 16 board has been designed with the PICtail Plus modular expansion interface, allowing the board to provide basic generic functionality and still be easily extendable to new technologies as they become available.

PICtail Plus is based on a 120-pin connection divided into three sections of 30 pins, 30 pins and 56 pins. The two 30-pin connections have parallel functionality. For example, pins 1, 3, 5 and 7 have SPI functionality on the top 30-pin segment, with similar SPI functionality on the corresponding pins in the middle 30-pin segment.

Each 30-pin section provides connections to all of the serial communication peripherals, as well as many I/O ports, external interrupts and A/D channels. This provides enough signals to develop many different expansion interfaces, such as Ethernet, ZigBee™ Technology, IrDA® Protocol and so on. The 30-pin PICtail Plus daughter boards can be used in either the top or middle 30-pin sections.

The Explorer 16 board provides footprints for two edge connectors for daughter boards, one populated (J5, Samtec # MEC1-160-02-S-D-A) and one unpopulated (J6). The board also has a matching male edge connection (J9), allowing it to be used as an expansion card itself.

SD/MMC PICtail™ Plus Daughter Board (AC164122)

The SD/MMC PICtail Plus Daughter Board is a universal board that interfaces the Secure Digital (SD) and Multi-Media Card (MMC) to the Serial Peripheral Interface (SPI) bus of the microcontroller. This PICtail board is designed to operate with a multitude of demonstration boards, including all those having PICtail signals, those with PICtail Plus signals (utilizing the card-edge connectors like the Explorer 16), and those with non-standard PICtail signals. This card plugs into one of the 30-pin sections on the PICtail Plus expansion header. This card is compatible with all 16-bit products.

Ethernet PICtail™ Plus Daughter Board (AC164123)

The Ethernet PICtail Plus Daughter Board provides a cost-effective method of evaluating and developing Ethernet control applications. The development board is populated with the 28-pin ENC28J60 Ethernet controller, which interfaces to the SPI bus of the microcontroller. Also included is the RJ-45 connector to make the Ethernet connection to the network. This card is compatible with all 16-bit products operating at 3V.

IrDA® Protocol PICtail Plus Daughter Board (AC164124)

The IrDA® Protocol PICtail Plus Daughter Board expands the functionality of the Explorer 16 demo board to include IrDA communications. This card features a TFDU100 infrared optical sensor module from Vishay Semiconductor. The PIC24 and dsPIC33F UART module implement the 3/16 encoder and decoder necessary to interface directly to the TFDU100. This card is compatible with all PIC24 and dsPIC33F products.

CompactFlash PICtail™ Plus Daughter Board (Future)

The CompactFlash PICtail Plus Daughter Board provides an interface between 16-bit products and a CompactFlash memory card. The interface is based on general-purpose I/O pins or the PMP module found on some of the higher pin count 16-bit devices. This card is compatible with all 16-bit products.

Wireless Communications PICtail™ Plus Daughter Board (AC163027)

The Wireless PICtail Plus Daughter Board interfaces to an IEEE 802.15.4™ to the 16-bit devices through the SPI module. The board includes provisions to select the PCB trace antenna or a user-supplied SMA connector. This card can be used with the ZigBee protocol or Microchip's MiWi™ wireless networking protocol. This card is compatible with all 16-bit products operating at 3V.

Speech playback PICtail™ Plus Daughter Board (AC164125)

The Speech playback PICtail Plus Daughter Board implements a fourth-order Low Pass Filter (LPF), speaker amplifier, speaker and 1 Mbit SPI serial EEPROM for playback only applications. Speech playback is accomplished by using the integrated PWM module on the 16-bit products and filtered into a voice waveform using the LPF. This board is designed to operate on both PICtail and PICtail Plus connectors. This card is compatible with all 16-bit products operating at 3V.

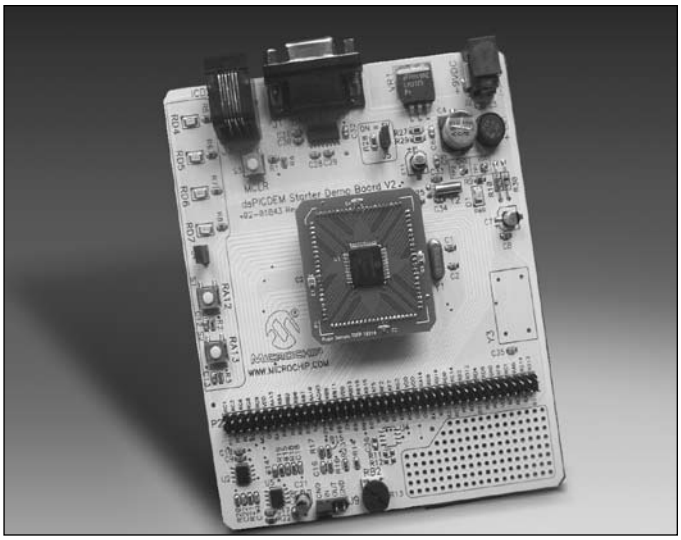
Prototype PICtail™ Plus Daughter Board (AC164126)

The Prototype PICtail Plus Daughter Board is an expansion breadboard card for the Explorer 16 Development Board using a PIC24 MCU or dsPIC33 DSC. This board is an 8x8 cm board with a card-edge connector to plug directly into the PICtail Plus expansion socket. The breadboard area provides access to all of the processor pins and a general purpose prototyping area. This kit contains three blank Prototype PICtail Plus Daughter Boards.

dsPICDEM™
80-pin Starter Development Board

Summary

This development board offers an economical way to evaluate both the PIC24 and dsPIC® Digital Signal Controller (DSC) General Purpose and Motor Control families. This board is an ideal prototyping tool to help you quickly develop and validate key design requirements.



Features

Key features of the dsPICDEM 80-pin Starter Development Board include:

- An 80-pin dsPIC30F6014A plug-in module (MA300014)
- A 100- to 80-pin adapter dsPIC33F plug-in module (MA330012) (uses 3.3V V_{DD} solution)
- Power input from 9V supply
- Selectable voltage regulator outputs of 5V and 3.3V
- LEDs, switches, potentiometer, UART interface
- A/D input filter circuit for speech band signal input
- On-board DAC and filter for speech band signal output
- Circuit prototyping area
- Assembly language demonstration program and tutorial
- Can accommodate 80-pin dsPIC30F6010A plug-in module (MA300015) — sold separately
- Can accommodate 100 to 80-pin adapter PIC24H plug-in module (MA33001X) — sold separately (uses 3.3V V_{DD} solution)

Package Contents

- dsPICDEM 80-pin Starter Development Board
- dsPIC30F6014A plug-in module
- dsPIC33FJ256GP710 plug-in-module
- Documentation on CD

Minimum Requirements:

- MPLAB® IDE v7.40 or later
- MPLAB ICD 2
- MPLAB C30 v2.02 or later
- dsPICDEM 80-pin Development Board (DM300019)

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16-bit, 28-pin Starter Development Board

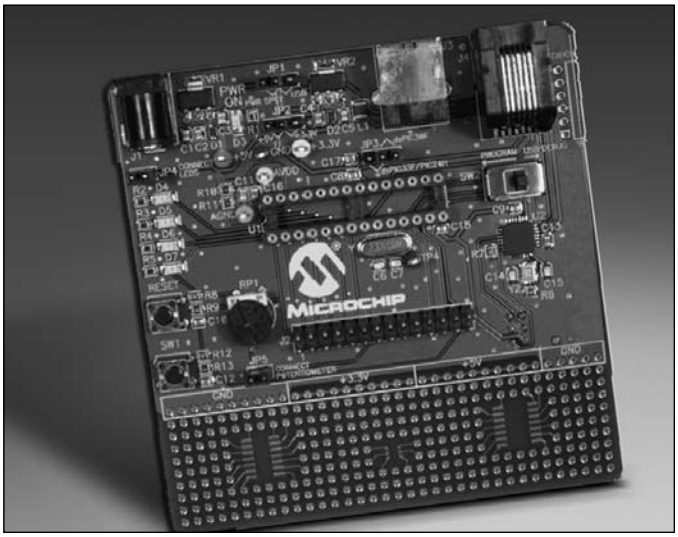
Summary

The low-cost, 16-bit, 28-pin Starter Development Board allows the user to easily evaluate 28-pin, PIC24 microcontroller or dsPIC Digital Signal Controller (DSC) devices. This board is ideal prototyping tool to help you validate key design requirements

Features

Key features of the 16-bit, 28-pin Starter Development Board include:

- Prototyping tool for all 28-pin, SDIP PIC24, dsPIC30F and dsPIC33F devices
- Includes a 28-pin PIC24FJ64GA002 and dsPIC33FJ12GP202
- On-board regulators for 3.3V or 5V operation
- Power input from 9V power supply or USB power source
- Single UART communication channel via USB bridge
- Connectors for MPLAB® ICD 2 In-circuit Debugger/ Programmer and PICkit™ 2
- Header for access to all device I/O pins
- Circuit prototyping area including pads for SOIC and SOT-23 devices



Package Contents

- 16-bit, 28-pin Starter Board
- 28-pin, PIC24FJ64GA002 and dsPIC33FJ12GP202 devices
- Example software and documentation on CD

Minimum Requirements:

- MPLAB IDE v7.60 or later
- MPLAB C30 C Compiler v2.05 or later
- MPLAB ICD 2 (DM300017)

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dsPICDEM™ 1.1 Plus General Purpose Development Board

Summary

The dsPICDEM 1.1 Plus General Purpose Development Board provides the application designer with a low cost development tool to become familiar with the dsPIC30F, dsPIC33F and PIC24H 16-bit architecture, high-performance peripherals and powerful instruction set.

The board features an active demonstration program loaded on the installed dsPIC30F6014A device. Several program functions are selectable via a menu system displayed on the LCD. These include: temperature and voltage measurements, frequency domain characteristics of a sine wave signal generated on-board from a digital potentiometer, FIR and IIR digital filter selections and DTMF tone generation using the codec interface peripheral (external speaker required).

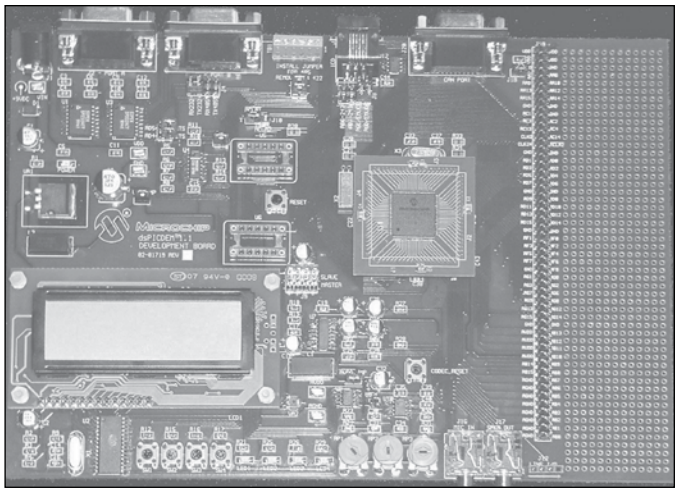
Also included is a simple tutorial written in assembly language. Users can create a project, assemble and link the code, program and/or debug the code using Microchip's MPLAB® IDE Integrated Development Environment – included free, and an MPLAB ICD 2 In-Circuit Debugger – available separately.

The development board serves as an ideal prototyping tool to quickly develop and validate design requirements.

Features

Key features of the dsPICDEM 1.1 Plus General Purpose Development Board include:

- dsPIC30F6014A plug-in sample (MA300014)
- Serial communication channels interface (two UARTs, SPI, CAN, RS-485)
- Si3000 voiceband codec with MIC In/speaker jacks
- General purpose prototyping area with expansion header
- 122 x 32 dot-addressable LCD
- MPLAB® ICD 2 and MPLAB ICE 4000 emulator support
- LEDs, switches and potentiometers
- Temperature sensor
- Separate digital and analog voltage regulators
- Digital potentiometer for DAC capability



Package Contents

- dsPICDEM 1.1 General Purpose Development Board with pre-programmed dsPIC30F6014A device
- RS-232 cable
- Power supply
- Example software and documentation on CD

Minimum Requirements:

- MPLAB IDE v7.40 or later
- MPLAB ICD 2
- MPLAB C30 v2.02 or later
- dsPICDEM 1.1 Development Board (DM300014)

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dsPICDEM™ 2 Development Board

Summary

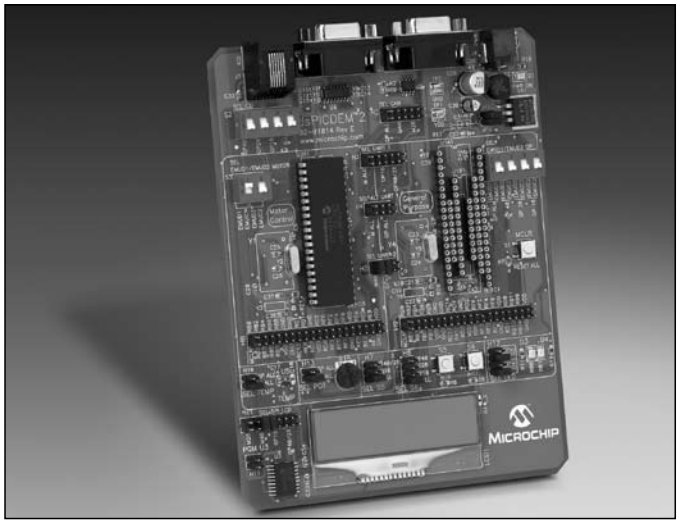
The dsPICDEM 2 Development Board is a development and evaluation tool that helps create embedded applications using dsPIC® Digital Signal Controllers (DSCs). Sockets are provided for 28- and 40-pin devices in the dsPIC30F Motor Control Family and 18-, 28- and 40-pin devices in the dsPIC30F General Purpose and Sensor Family. The supported devices are shown in the table below.

The board includes a sample dsPIC30F4011 in the 40-pin motor control socket, a power supply regulator, crystal oscillators for each set of sockets, an ICD connector for the MPLAB® ICD 2 In-Circuit Debugger and both RS-232 and CAN ports for external communication. In addition, the board is populated with prototyping hardware, including LED indicators, push button switches, a potentiometer, a temperature sensor and a 2x16 LCD screen. All pins on all the device sockets are accessible through headers.

dsPIC30F Device	Supported Packages
Motor Control Family	
dsPIC30F2010	28-pin SPDIP
dsPIC30F3010	28-pin SPDIP
dsPIC30F4012	28-pin PDIP
dsPIC30F3011	40-pin PDIP
dsPIC30F4011	40-pin PDIP
Sensor Family	
dsPIC30F2011	18-pin PDIP
dsPIC30F3012	18-pin PDIP
dsPIC30F2012	28-pin SPDIP
dsPIC30F3013	28-pin SPDIP
General Purpose Family	
dsPIC30F3014	40-pin PDIP
dsPIC30F4013	40-pin PDIP

Minimum Requirements:

- MPLAB IDE v7.40 or later
- MPLAB ICD 2
- MPLAB C30 v2.02 or later
- dsPICDEM 2 Development Board (DM300018)



Features

Key features of the dsPICDEM 2 Development Board include:

- Multiple sockets for 18-, 28- and 40-pin PDIP and SPDIP devices
- Sample application programs complete with MPLAB IDE workspace and project files provided for supported dsPIC30F devices
- A dsPIC30F4011 40-pin PDIP sample device installed on board
- 5V regulator provides VDD and AVDD from a 9V DC power supply
- MPLAB ICD 2 in-circuit debugger ready
  - Options for selecting alternate debugging channels
- RS-232 interface
- Controller Area Network (CAN) interface
- Temperature sensor and analog potentiometer to simulate A/D inputs
- 2 push button switches and 2 LED indicators to simulate digital input and output
- 2x16 ASCII character LCD with SPI interface
- Access to all pins on the dsPIC30F device sockets via 2x40-pin headers
- CD with documentation and ample application programs
- A sample pack containing dsPIC30F3012 and dsPIC30F4013 devices

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dsPICDEM.net™ 1 and dsPICDEM.net™ 2 Connectivity Development Boards

Summary

The dsPICDEM.net 1 and dsPICDEM.net 2 Connectivity Development Boards provide the application developer a basic platform for developing and evaluating both connectivity and non-connectivity based requirements.

The dsPICDEM.net board provides the hardware circuitry for supporting both the Public Switched Telephone Network (PSTN) and 10-Base T MAC/PHY interfaces.

- The PSTN interface hardware on the dsPICDEM.net 1 board is suited for FCC/JATE compliancy
- The PSTN interface hardware on the dsPICDEM.net 2 board is suited for CTR-21 compliancy

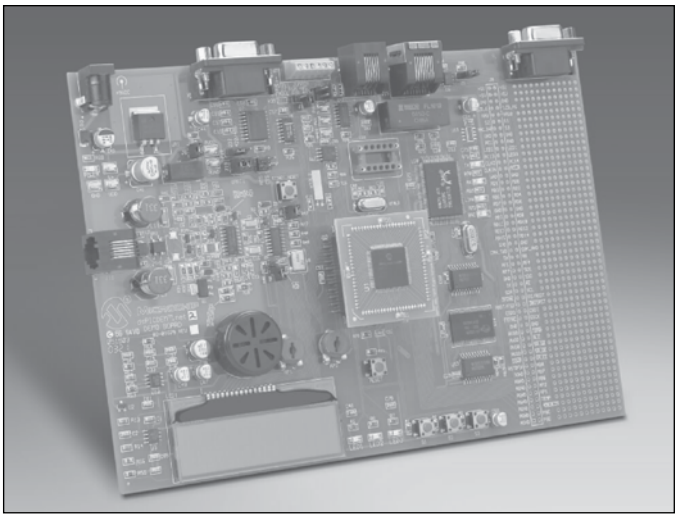
The board comes with an ITU-T compliant V.22bis/V.22 modem development module pre-programmed on the installed dsPIC30F6014 device. This demo provides full source code to connect and transfer data between the dsPIC® Digital Signal Controller (DSC) Soft Modem (dsPIC DSC SM) and an ITU-T compliant reference modem. The modem can be configured for either the Originate or Answer mode of operation. Configuration and control of the dsPIC30F Soft Modem demo is supported with an optimized AT command set, which is entered into a suitable communication program running on the PC, such as HyperTerminal™, and communicated to the dsPIC DSC over a RS-232 serial channel.

Also included are the CMX-MicroNet™ web and FTP Server programs, which demonstrate two TCP/IP protocol-based applications over the 10-Base T Ethernet datalink layer.

Features

Key features of the dsPICDEM.net 1 and dsPICDEM.net 2 Connectivity Development Boards include:

- dsPIC30F6014 plug-in module (MA300011)
- 10-Base T Ethernet MAC and PHY interface
- PSTN interface with DAA/AFE chipset
- Serial communication channels interface (UART and CAN)
- External I²C™ EEPROM memory for storing constants
- External 64K x 16 RAM memory
- General purpose prototyping area with expansion header
- Dual channel digital potentiometer
- 2 x 16 LCD display



Features (Continued)

- LEDs, switches and potentiometers
- Temperature sensor
- Full suite of development code
  - Getting Started tutorial
  - Full featured dsPICDEM.net board configuration and control demo
  - V.22bis Soft-Modem (full source code provided)
  - CMX-MicroNet Web Server
  - CMX-MicroNet FTP Server
- Comprehensive User's Guide describing development code

Package Contents

- dsPICDEM.net Connectivity Board with pre-programmed dsPIC30F6014
- RS-232 cable
- CAT 5 crossover cable
- Power supply
- Example software and documentation on CD

Minimum Requirements:

- MPLAB IDE v7.40 or later
- MPLAB ICD 2
- MPLAB C30 v2.02 or later
- dsPICDEM.net Development Board (DM300004-1 or DM300004-2)

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dsPICDEM™ MC1
Motor Control Development System

Summary

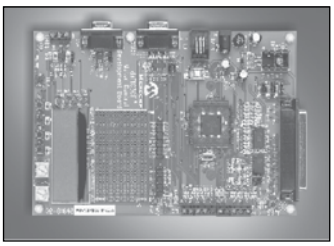
The dsPICDEM MC1 Motor Control Development System provides the application developer with three main components for quick prototyping and validation of BLDC, PMAC and ACIM applications. The three main components include the dsPICDEM MC1 Motor Control Development Board, the dsPICDEM MC1L, 3-phase low-voltage power module and the dsPICDEM MC1H, 3-phase high-voltage power module.

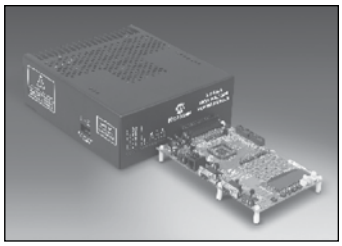
The dsPICDEM MC1 Motor Control Development System contains the dsPIC30F6010, but supports all dsPIC® Digital Signal Controller (DSC) motor control variants, various peripheral interfaces and a custom interface header system, which allows different motor power modules to be connected to the PCB. The control board also has connectors for mechanical position sensors, such as incremental rotary encoders and hall effect sensors, and a breadboard area for custom circuits. The main control board receives its power from a standard plug-in transformer.

The dsPICDEM MC1L 3-phase low-voltage power module is optimized for 3-phase motor applications that require a DC bus voltage less than 50 volts and can deliver up to 400 W power output. The 3-phase low-voltage power module is intended to power BLDC and PMAC motors.

The dsPICDEM MC1H 3-phase high-voltage power module is optimized for 3-phase motor applications that require DC bus voltages up to 400 volts and can deliver up to 1 kW power output. The high-voltage module has an active power factor correction circuit that is controlled by the dsPIC DSC. This power module is intended for AC induction motor and power inverter applications that operate directly from the AC line voltage.

Two compatible motors are available for the dsPICDEM MC1 Motor Control Development System.





Features

The dsPICDEM MC1 Motor Control Development System features:

- A dsPIC30F6010 Motor Control microcontroller-based board

The optional power modules provide:

- Heatsink for ambient cooling of power sections
- Full automatic protection of power circuits
- Electrical isolation from power circuits
- Many options for motor feedback signals

Package Contents

Motor Control Development Board

- dsPICDEM MC1 Motor Control Development Board with pre-programmed dsPIC30F6010 plug-in module (MA300013)
- RS-232 cable
- Power supply
- Example software and documentation on CD

Power Modules

- High-voltage or low-voltage power module
- Example software and documentation on CD

Minimum Requirements:

- MPLAB® IDE v7.40 or later
- MPLAB ICD 2
- MPLAB C30 v2.02 or later
- dsPICDEM MC1 Motor Control Development System (DM300020)

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PICDEM™ MC LV Development Board

Summary

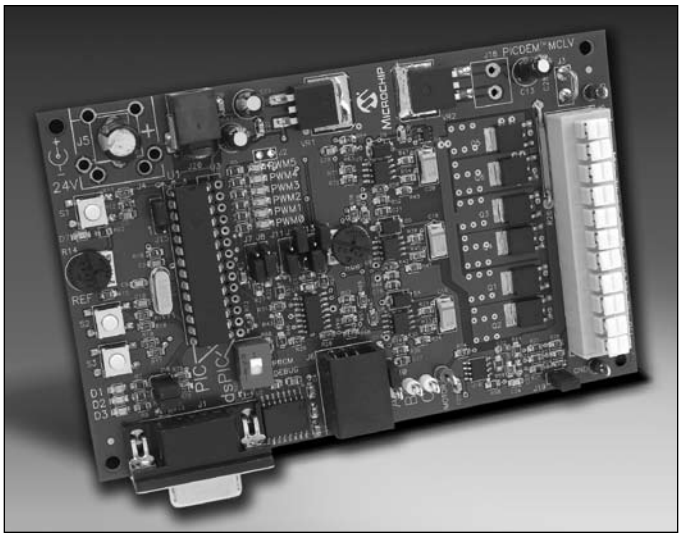
The PICDEM MC LV Development Board is an easy, ready-to-use BLDC motor control hardware platform built around the dsPIC30F2010, dsPIC30F3010 and dsPIC30F4012 (along with the PIC18F2431/2331). The PICDEM MC LV board has a control section around the onboard dsPIC® Digital Signal Controller (DSC) or the PIC® microcontroller, 3-phase voltage source inverter, fault-monitoring circuit, temperature sensor, monitoring LEDs, serial interface for PC connection, and In-Circuit Serial Program™ (ICSP™) connector for programming and debugging. In addition, the board has hardware interfaces that make it easy to implement sensor and sensorless control of a BLDC motor using the dsPIC30F2010, the dsPIC30F3010 or the dsPIC30F4012.

The PICDEM MC LV Development Board has all of the necessary hardware to support a direct drive to a 10 to 48 VDC BLDC (up to 2.2A max.) motor using a sensored or sensorless algorithm.

Features

The PICDEM MC LV Development Board features:

- A 3-phase voltage source inverter bridge
- Motion sensor inputs
- Over-current protection, level programmable using potentiometer
- Temperature sensor with I²C™ interface
- Test points for motor current and back EMF sensing
- Speed control potentiometer
- Example software and documentation available on CD
- 24V external power supply (optional)
- A 3-phase, 24V BLDC low-voltage motor (optional)



Package Contents

- PICDEM MC LV Development Board pre-programmed with a PIC18F2431 and a dsPIC30F3010 (shipped separately)
- Free Motor Control Graphical User Interface (MC-GUI) available in MPLAB® 7.20 and later revisions

Minimum Requirements:

- MPLAB IDE v7.40 or later
- MPLAB ICD 2
- MPLAB C30 v2.02 or later
- PICDEM MC LV Development Board (DM183021)

dsPICDEM™ SMPS Buck Development Board

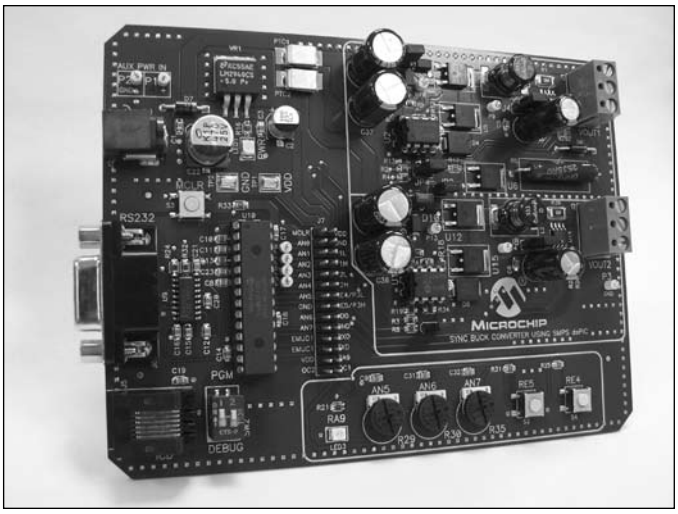
Summary

This development board serves as a simple DC-DC Switch Mode Power Supply (SMPS) reference design and a good starting point for designers new to SMPS design. This board is an ideal prototyping tool to help you quickly develop and validate key design requirements.

Features

Key features of the dsPICDEM SMPS Buck Development Board include:

- Dual independent Buck converters demonstrate the SMPS dsPIC® Digital Signal Controllers' (DSC) capabilities to control multiple SMPS circuits
- Buck converters can operate in Synchronous or Asynchronous modes
- Input voltage range 7V to 15V (nominal 9V)
- User can enable a dynamic output load to investigate transient response
- User potentiometers to simulate application features such as voltage trim, remote voltage sense, voltage tracking, current sharing, etc.
- MPLAB® ICD 2 support ready
- RS-232 serial channel
- Contact Microchip for more information



Package Contents

- dsPICDEM SMPS Buck Development Board
- Documentation on CD

Minimum Requirements:

- MPLAB IDE v7.40 or later
- MPLAB ICD 2
- MPLAB C30 v2.02 or later
- dsPICDEM.SMPS Buck Development Board

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Software Application Library Overview

Overview

A suite of advanced solution libraries have been developed and are available for your application requirements. The table below presents a summary reference of the libraries offered and the PIC24 Microcontroller (MCU) and dsPIC® Digital Signal Controller (DSC) devices supported. Additional information on the specific library is provided within this section.

- Comprehensive library suite for 16-bit product family
- One-stop library shopping
- Reduce development time by using ready-made libraries
- No royalties for libraries and only a one-time license fee per project lifetime for some libraries

Application Library	16-bit Device Support				Free	Comments
	dsPIC30F	dsPIC33F	PIC24H	PIC24F		
dsPIC® DSC Soft Modem Library	Now	Planned	—	—	√	V.22bis and DTMF
dsPIC® DSC Speech Recognition Library	Now	Now	—	—		
dsPIC® DSC Noise Suppression Library	Now	Now	—	—		
dsPIC® DSC Acoustic Echo Cancellation Library	Now	Now	—	—		
dsPIC® DSC Line Echo Cancellation Library	Now	Now	—	—		
dsPIC® DSC Symmetric Key Embedded Encryption Library	Now	Now	—	—		
Triple DES/AES Encryption Libraries	Now	Now	Now	Now	√	
dsPIC® DSC Asymmetric Key Embedded Encryption Library	Now	Now	—	—		
dsPIC® DSC Speex Speech Encoding/Decoding Library	Now	Now	—	—		
PIC24/dsPIC® DSC G.711 Speech Encoding/Decoding Library	Now	Now	Now	Now		
dsPIC® DSC G.726A Speech Encoding/Decoding Library	Now	Now	—	—		
FAT 16 File System	Contact Microchip	Contact Microchip	Contact Microchip	Contact Microchip	√	
dsPIC® DSC DSP Library	Now	Now	—	—	√	
PIC24/dsPIC® DSC Math Library	Now	Now	Now	Now	√	
PIC24/dsPIC® DSC Peripheral Library	Now	Now	Now	Now	√	
Microchip TCP/IP Stack + ENC28J60	Now	Now	Now	Now	√	
dsPICworks™ Data Analysis and DSP Software	Now	Now	Now	Now	√	
Digital Filter Design Tool	Now	Now	—	—		
Digital Filter Design Lite	Now	Now	—	—		
RTOS/CMX-RTX™ for PIC24/dsPIC® DSC	Now	Now	Now	Now		
RTOS/CMX-Tiny+™ for PIC24/dsPIC® DSC	Now	Now	Now	Now		
RTOS/CMX-Scheduler ™ for PIC24/dsPIC® DSC	Now	Now	Now	Now	√	
TCP/IP–CMX-MicroNet™ for PIC24/dsPIC® DSC	Now	Now	Now	Now		
CANbedded (Vector)	Now	Contact Microchip	Contact Microchip	—		
OsCAN (Vector)	Now	Contact Microchip	Contact Microchip	—		

dsPIC® DSC Soft Modem Library

Summary

The dsPIC Digital Signal Controller (DSC) Soft Modem Library is composed of ITU-T compliant algorithms for V.21, V.22, V.22bis, V.23, V.32 and V.32bis modem recommendations. Bell standard 103 is also included in this library.

V.21, V.23 and Bell 103 are Frequency Shift Keying (FSK) modems. V.32, V.32bis and V.22bis are Quadrature Amplitude Modulated (QAM) modems. V.22 is a Quadrature Phase Shift Keyed (QPSK) modem. V.21, V.22, V.22bis, V.32 and V.32bis are all 2-wire, full-duplex modems. V.23 is full-duplex when it operates with a 75 bps backwards channel.

V.22bis includes fallback to V.22, V.23 and V.21 standards. V.32bis optionally falls back to V.22bis, V.22, V.23 and V.21 standards.

Typical Applications

The dsPIC DSC Soft Modem Library is well suited for small transaction orientated-based applications such as, but not limited to:

- POS terminals
- Set top boxes
- Drop boxes
- Fire panels
- Internet-enabled home security systems
- Internet-connected power, gas and water meters
- Internet-connected vending machines
- Smart appliances
- Industrial monitoring

Contents

The dsPIC DSC Soft Modem Library is provided in two basic software packages:

- V.22bis/V.22 offered free with full source code, includes:
  - V.22bis/V.22, V.23, V.21/Bell 103, V.42, DP and V.42 API, AT command set
- V.32bis/V.32 offered in object code, includes:
  - V.32bis/V.32, V.22bis/V.22, V.23, V.21/Bell 103, V.42, DP and V.42 API, AT command set

The library currently supports single-channel data-pump implementations.

Both libraries are supported with fallback data pump modulations down to V.21. Each data modem library is provided with a respective library archive containing all the data pump object code modules required to link to an application. UART and Data Converter Interface (DCI) for DAA/AFE I/O hardware component drivers are provided in assembly source code for linking with an application.

ITU-T Recommendation V.42 is provided with each library. V.42 contains a High Level Data Link Control (HDLC) protocol referred to as Link Access Procedure for Modems (LAPM) and defines error-correcting protocols for modems.

All data pump modulations are developed in ASM30 assembly code yielding optimal code size and execution time. The AT, V.42 and data pump APIs are based on the MPLAB® C30 C Compiler language.

Electronic documentation accompanies this library to help implement its functions. A comprehensive *Soft Modem User's Guide* describes the required APIs for the AT, V.42 and data pump layers. **Example demo programs are provided which implement the required library APIs.**

Features and Performance of Data Modems

Algorithm[1] (Kbps)	Performance: Data Rate Duplex	Performance: Half/Full Mod.	Program Data (Kbytes)	Data Memory[2, 3] (Kbytes)	Memory[2, 3]	MIPS
V.21/Bell 103[4]	0.3	Full	FSK	13	1.0	4.5
V.22/V.22bis	1.2	Full	PSK/QAM	22	1.7	7
2.4						
V.23[4]	1.2	Half	FSK	15	1.0	4.5
0.6						
V.32	9.6	Full	QAM/TCM	31	3.2	12
4.8						
V.32bis	14.4	Full	QAM/TCM	36	3.6	15
12						
9.6						
7.2						
4.8						
V.42		—		14	2.0	1.5
DP + V.42 API		—		7	1.2	—
AT Command Set		—		8	0.15	—

Notes:

1. Data pump modules, V.21, V.22, V.22bis, V.23, V.32, V.32bis and Bell 103 are implemented in Assembly language; V.42, data pump; AT command APIs are implemented in C language.
2. The program/data memory usage for the V-series data pumps is NOT cumulative, due to the sharing of components internally.
3. Memory size does not account for applications combining data pump, V.42 and AT commands (if required).
4. V.21/Bell 103 and V.23 data pumps do not require V.42.

Technical Notes

V.21 operates at 300 symbols per second, at mean frequencies of 1080 ±100 Hz and 1750 ±100 Hz. V.23 operates at mean frequencies of 1500 ±200 Hz for the 600 bps forward channel and 1700 ±400 Hz for the 1200 bps forward channel. The V.23 75 bps backwards channel has a mean frequency of 420 ±30 Hz.

V.32 and V.32bis data modems operate at 2400 symbols per second on a carrier frequency of 1800 Hz, in both directions. Both V.32 and V.32bis implement Trellis Coding Modulation (TCM) for all data rates, except 4800 bps. V.32 includes uncoded 9600 bps.

dsPIC® DSC
Speech Recognition Library

Summary

The dsPIC Digital Signal Controller (DSC) Speech Recognition Library provides voice control of embedded applications with isolated, speaker-independent word recognition of US English. It allows control of an application through a set of fixed voice commands. The library has already been pre-trained by a demographic cross-section of male and female US English speakers. Conveniently, no training is required for end-users of the product.

This library is an ideal front-end for hands-free products such as modern appliances, security panels and cell phones. The Speech Recognition Library has very modest memory and processing requirements and is targeted for the dsPIC30F5011, dsPIC30F5013, dsPIC30F6012 and dsPIC30F6014 processors.

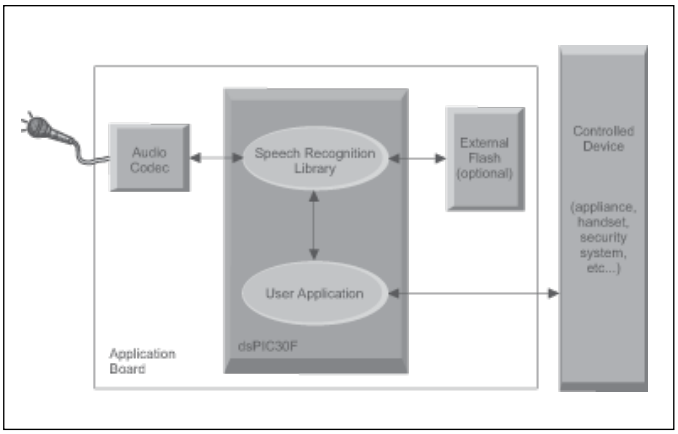
The library samples speech data from a voice codec connected to the dsPIC30F's data converter interface. The data is processed a frame at a time, and when a word ending is detected, the received word is identified using Hidden Markov Model (HMM) processing. After the library identifies the word, the application can respond accordingly.

The speech recognition algorithm is written in assembly language to optimize performance and minimize RAM usage. A well defined API makes it easy to integrate the Speech Recognition Library with your application. Library functions allow the application to easily disable and enable speech recognition. The library lets other system processing operations take place without disrupting speech recognition.

A PC-based word library builder program creates a custom library from a master library of 100 common words to allow users to control their application vocally. A noise profile is selected to suit the operating environment. The noise profile consists of a noise type and a Signal-to-Noise Ratio (SNR). The noise type can be any combination of 3 different noise sources (automobile, office and white noise), and the SNR may be as low as 15 dB. The word library builder program generates source files that can be used to build an application. These files contain data tables that the library uses to perform.

Devices Supported

- dsPIC30F5011
- dsPIC30F5013
- dsPIC30F6012
- dsPIC30F6012A
- dsPIC30F6014
- dsPIC30F6014A
- dsPIC33FXXXX



Features

Key features of the dsPIC30F Speech Recognition Library include:

- US English language support
- Speaker-independent recognition of isolated words
- No speaker training is required
- Hidden-Markov Model-based recognition system
- Recognition time < 500 msec
- Master Library of 100 common words (available in the *dsPIC® DSC Speech Recognition Library User's Guide*)
- Windows® operating system-based utility creates a custom library from the master library
- Additional words can be added to the master library (fee based)
- Data tables can be stored in external memory
- Optional keyword activation and silence detection
- Optional system self-test using a predefined keyword
- Flexible API
- Full compliance with MPLAB® C30 Language Tools
- *dsPIC® DSC Speech Recognition Library User's Guide* is provided with the library
- Designed to run on dsPICDEM™ 1.1 General Purpose Development Board (DM300014)

Resource Requirements

- Sampling interface: SI-3000 audio codec operating at 12.0 kHz
- System operating frequency: 12.288, 18.432 or 24.576 MHz
- Computational power: 8 MIPS
- Program Flash memory: 18 KB + 1.5 KB for each library word
- RAM: <3.0 KB

dsPIC® DSC
Noise Suppression Library

Summary

The dsPIC Digital Signal Controller (DSC) Noise Suppression (NS) Library provides a function to suppress the effect of noise interfering with a speech signal. This function is useful for microphone-based applications, which have a potential for incoming speech getting corrupted by ambient noise captured by the microphone. It is especially suitable for systems in which an acoustically isolated noise reference is not available, such as:

- Hands-free cell phone kits
- Speakerphones
- Intercoms
- Teleconferencing systems
- Headsets
- A front-end to a speech recognition system
- Any microphone-based application that needs to eliminate undesired noise

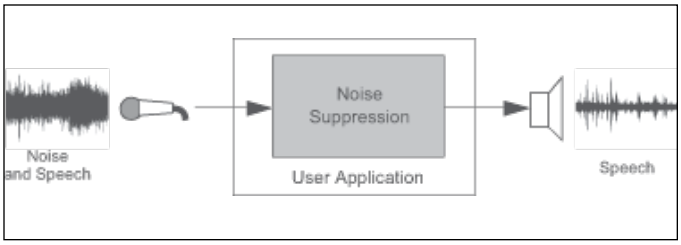
The Noise Suppression Library is written entirely in assembly language and is highly optimized to make extensive use of the dsPIC DSC DSP instruction set and advanced addressing modes. The algorithm avoids data overflow. The Noise Suppression Library provides a "NoiseSuppressionInit" function for initializing the various data structures required by the algorithm and a "NoiseSuppression" function to remove noise from a 10 ms block of sampled 16-bit speech data. Both functions are executed through a well-documented Application Programmer's Interface (API).

The "NoiseSuppression" function is primarily a frequency domain algorithm. A Fast Fourier Transform (FFT) is performed on each 10 ms block of data to analyze the frequency components of the signal. Thereafter, a Voice Activity Detection (VAD) algorithm is used to determine if the signal segment is speech or noise. The NS algorithm maintains a profile of the noise and updates it every time a noise segment is detected by the VAD. Every frequency band of the input signal is then scaled according to the proportion of noise contained in that frequency band, thereby causing a significant degree of noise suppression in the resultant signal. The algorithm, adapts to changes in the nature and level of noise, and does not require a separate noise reference input.

The dsPIC DSC Noise Suppression Library uses an 8 kHz sampling rate. However, the library includes a sample rate conversion function that ensures interoperability with libraries designed for higher sampling rates (9.6 kHz, 11.025 kHz or 12 kHz). The conversion function allows incoming signals at higher sampling rates to be converted to a representative 8 kHz sample. Similarly, the conversion function allows the output signal to be converted upward from 8 kHz to match the user application.

Devices Supported

dsPIC30F6014
dsPIC30F6014A
dsPIC30F6012
dsPIC30F6012A
dsPIC30F5013
dsPIC30F5011
dsPIC30F4013
dsPIC33FXXXGPXXX



Features

Key features of the Noise Suppression Library include:

- All functions can be called from either a C or assembly application program
- Five user functions:
  - NoiseSuppressionInit
  - NoiseSuppression
  - InitRateConverter
  - SRC_upConvert
  - SRC_downConvert
- Full compliance with the Microchip's MPLAB® C30 C compiler, assembler and linker
- Simple user interface – one library file and one header file
- Highly optimized assembly code, utilizing DSP instructions and advanced addressing modes
- Audio bandwidth: 0 to 4 kHz at 8 kHz sampling rate
- 10-20 dB noise reduction, depending on type of noise
  - Several speech recordings corrupted by babble, car cabin, white and narrowband noise included for library evaluation
- *dsPIC® DSC Noise Suppression Library User's Guide* is provided
- Demo application source code is provided
- Accessory kit available for purchase includes: an audio cable, headset, oscillators, microphone, speaker, DB9 M/F RS-232 cable, DB9M-DB9M null modem adapter and can be used for library evaluation

Resource Requirements

Noise Suppression

Computational requirements:	3.3 MIPS
Program Flash memory:	7 KB
RAM:	1 KB

Sample Rate Conversion

Computational requirements:	1 MIPS
Program Flash memory:	2.6 KB
RAM:	0.5 KB

Note: The user application might require an additional 1 KB to 1.5 KB of RAM for data buffering (application-dependent).

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dsPIC® DSC
Acoustic Echo Cancellation Library

Summary

The dsPIC Digital Signal Controller (DSC) Acoustic Echo Cancellation (AEC) Library provides a function to eliminate echo generated in the acoustic path between a speaker and a microphone. This function is useful for speech and telephony applications in which a speaker and a microphone are located in close proximity to each other and are susceptible to signals propagating from the speaker to the microphone resulting in a perceptible and distracting echo effect at the far end. It is especially suitable for these applications:

- Hands-free cell phone kits
- Speakerphones
- Intercoms
- Teleconferencing systems

For hands-free phones intended to be used in compact environments, such as a car cabin, this library is fully compliant with the G.167 standard for acoustic echo cancellation.

The AEC Library is written entirely in assembly language and is highly optimized to make extensive use of the dsPIC DSC DSP instruction set and advanced addressing modes. The algorithm avoids data overflow. The AEC Library provides an "`AcousticEchoCancellerInit`" function for initializing the various data structures required by the algorithm and an "`AcousticEchoCanceller`" function to remove the echo component from a 10 ms block of sampled 16-bit speech data. The user can easily call both functions through a well-documented Application Programmer's Interface (API).

The "`AcousticEchoCanceller`" function is primarily a Time Domain algorithm. The received far-end speech samples (typically received across a communication channel such as a telephone line) are filtered using an adaptive Finite Impulse Response (FIR) filter. The coefficients of this filter are adapted using the Normalized Least Mean Square (NLMS) algorithm, such that the filter closely models the acoustic path between the near-end speaker and the near-end microphone (i.e., the path traversed by the echo). Voice Activity Detection (VAD) and Double Talk Detection (DTD) algorithms are used to avoid updating the filter coefficients when there is no far-end speech and also when there is simultaneous speech from both ends of the communication link (double talk). As a consequence, the algorithm functions correctly even in the presence of full-duplex communication. A Non-Linear Processor (NLP) algorithm is used to eliminate residual echo.

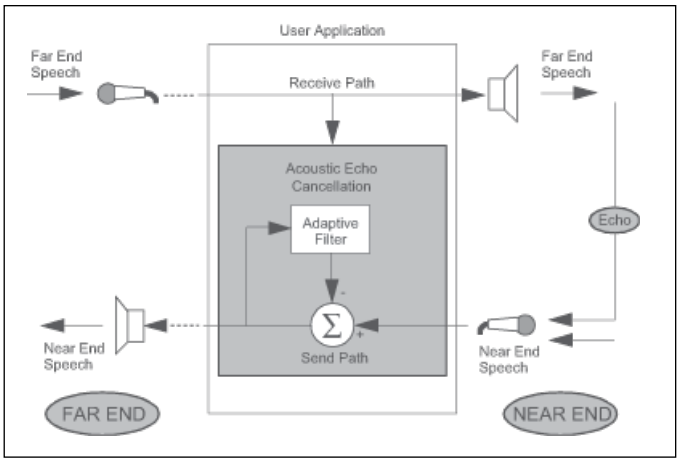
This library uses an 8 kHz sampling rate. However, the library includes a sample rate conversion function that ensures interoperability with libraries designed for higher sampling rates (9.6 kHz, 11.025 kHz or 12 kHz). The conversion function allows incoming signals at higher sampling rates to be converted to a representative 8 kHz sample. Similarly, the conversion function allows the output signal to be converted upward from 8 kHz to match the user application.

Echo Tail Length (ms)	MIPS	Program Flash Memory (KB)	RAM (KB)
64	16.5	12	5.7
32	10.5	12	3.4
16	7.5	12	2.6

Sample Rate Conversion

Computational requirements:	1 MIPS
Program Flash memory:	2.6 KB
RAM:	0.5 KB

Note: The user application might require an additional 2 to 2.5 KB of RAM for data buffering (application-dependent).



Features

Key features of the Acoustic Echo Cancellation Library include:

- All functions can be called from either a C or Assembly application program
- Five user functions:
  - `AcousticEchoCancellerInit`
  - `AcousticEchoCanceller`
  - `InitRateConverter`
  - `SRC_upConvert`
  - `SRC_downConvert`
- Full compliance with the Microchip MPLAB® C30 C compiler, assembler and linker
- Simple user interface – one library file and one header file
- Highly optimized assembly code, utilizing DSP instructions and advanced addressing modes
- Echo cancellation for 16, 32 or 64 ms echo delays or 'tail lengths' (configurable)
- Fully tested for compliance with G.167 specifications for in-car applications
- Audio bandwidth: 0 to 4 kHz at 8 kHz sampling rate
- Convergence rate: Up to 43 dB/sec., typically > 30 dB/sec.
- Echo cancellation: Up to 50 dB; typically > 40 dB
- Can be used together with the Noise Suppression (NS) Library, since the same processing block size (10 ms) is used
- *dsPIC® DSC Acoustic Echo Cancellation Library User's Guide* included
- Demo application source code is provided with the library
- Accessory kit available for purchase includes an audio cable, headset, oscillators, microphone, speaker, DB9 M/F RS-232 cable, DB9M-DB9M null modem adapter and can be used for library

Devices Supported

dsPIC30F6014
dsPIC30F6014A
dsPIC30F6012
dsPIC30F6012A
dsPIC30F5013 (for a max. of 32 ms echo delay)
dsPIC30F5011 (for a max. of 32 ms echo delay)
dsPIC33FXXXGPXXX

dsPIC® DSC
Line Echo Cancellation Library

Summary

Line echo cancellation eliminates echoes generated in the electrical path between the transmitter and receiver in a communication device. Typically, echoes are the result of signal reflection caused by impedance mismatch in telephone hybrids and other network components. This “far-end” line echo results in a perceptible and distracting echo effect at the near end.

Line echo cancellation is useful for telephony applications that involve transmitting and receiving signals through a telephone hybrid. It is also useful for digital network applications, such as cellular telephony and voice-over internet protocol. Though the dsPIC Digital Signal Controller (DSC) Line Echo Cancellation Library is targeted to eliminate far-end echo (as demonstrated by the demo application), the library functions are equally applicable to eliminating near-end echo.

The dsPIC DSC Line Echo Cancellation Library is written predominantly in Assembly language and is highly optimized to make extensive use of the dsPIC DSC instruction set and advanced addressing modes. The algorithm avoids data overflow. The library provides a `LineEchoCancellerInit` function for initializing the various data structures required by the algorithm and a `LineEchoCanceller` function to remove the echo component from a 10 ms block of sampled 16-bit speech data. You can easily call both functions through a well-documented Application Programmer’s Interface (API). Both the processing frame size and echo tail length (the maximum echo path for which the algorithm can eliminate the echo) are user-configurable through constants defined in a header file.

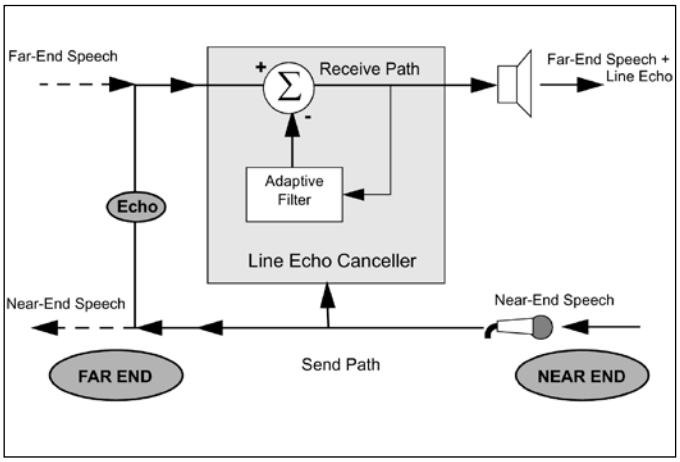
The `LineEchoCanceller` function is primarily a time domain algorithm. The received near-end speech samples (typically sampled from a microphone) are filtered using an adaptive Finite Impulse Response (FIR) filter. The coefficients of this filter are adapted using the Normalized Least Mean Square (NLMS) algorithm, such that the filter closely models the electrical path between the transmitter and receiver (e.g., the path through a telephone hybrid), which is essentially the path traversed by the echo. An optional Double Talk Detection (DTD) feature can be used to avoid updating the filter coefficients when there is simultaneous speech from both ends of the communication link (double talk). As a consequence, the algorithm functions correctly even in the presence of full-duplex communication. An optional Nonlinear Processor (NLP) feature can be used to eliminate residual echo.

Echo Tail Length (ms)	MIPS	Program Flash Memory (KB)	RAM (KB)
64	16	9	5.5
32	10	9	3.5
16	7	9	2.5

Sample Rate Conversion

Computational requirements:	1 MIPS
Program Flash memory:	2.6 KB
RAM:	0.5 KB

Note: The user application might require an additional 1 KB of RAM for data buffering.



Features

Key features of the Line Echo Cancellation Library include:

- Simple user interface – only one library file and one header file
- All functions can be called from a C application program
- Two user functions:
  - `LineEchoCancellerInit`
  - `LineEchoCanceller`
- Full compliance with the Microchip MPLAB® C30 C compiler, assembler and linker
- Functions predominantly written in highly optimized assembly code that uses DSP instructions and advanced addressing modes
- Echo cancellation for 16, 32 or 64 ms echo delays or tail lengths (configurable)
- Speech processing interval of 5, 10 or 20 ms (configurable)
- Fully tested for compliance with ITU-T G.168 specifications for digital network echo cancellers
- Audio Bandwidth: 0 to 4 kHz at 8 kHz sampling rate
- Convergence Rate: Up to 60 dB/sec., typically greater than 30 dB/sec.
- Echo Cancellation: Up to 70 dB; typically > 40 dB
- Can be used together with the dsPIC DSC Noise Suppression Library, since the same processing block size (10 ms) can be used
- Comprehensive User’s Guide is provided to help the user understand and implement the library
- Demonstration application source code is provided with the library

Devices Supported

dsPIC30F6014
dsPIC30F6014A
dsPIC30F6012
dsPIC30F6012A
dsPIC30F5013 (for a max. of 32 ms echo delay)
dsPIC30F5011 (for a max. of 32 ms echo delay)
dsPIC33FXXXGPXXX

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dsPIC® DSC Symmetric Key Embedded Encryption Library

Summary

Microchip offers a reliable security solution for embedded applications built on the dsPIC Digital Signal Controller (DSC) platform. This solution is provided by means of two libraries – Symmetric Key and Asymmetric Key Embedded Encryption Libraries. The Symmetric Key Library features:

- Hash functions
  - SHA-1 secure hash standard
  - MD5 message digest
- Symmetric key encryption/decryption functions
  - Advanced Encryption Standard (AES)
  - Triple Data Encryption Algorithm (Triple-DES)
- Random number generator functions
  - Deterministic Random Bit Generator ANSI X9.82

Typical Applications

The algorithms supported by this library have emerged as the de facto standard for many large scale, secured applications like web access, E-mail, secure XML transactions and Virtual Private Networks (VPN). These algorithms are also recommended by most Internet Engineering Task Force (IETF), Federal Information Processing Standards (FIPS) and IPSec standards. Some typical applications for this library include:

- Mobile and wireless devices, PDAs
- Secure banking
- Secure web transactions
  - Secure Socket Layer (SSL)
  - Transport Layer Security (TLS)
  - Secure Multi-purpose Internet Mail Extensions (S/MIME)
- ZigBee™ technology and other monitoring and control applications
- Smart card readers/trusted card readers
- Friend/foe identification

Typical Applications (Continued)

- Secure devices and peripherals interoperating with TCG and NGSCB PC's

The Trusted Computing Group (TCG) and related Microsoft® Next- generation Secure Computing Base (NGSCB) both specify RSA and Triple-DES. RSA and other asymmetric solutions are featured in the dsPIC DSC Asymmetric Key Embedded Encryption Library (SW300055).

Features

- C-callable library functions developed in MPLAB® ASM30 Assembly language
- Optimized for speed, code size and RAM usage:
  - RAM usage below 60 bytes
- Library functions extensively tested for adherence to applicable standards
- Symmetric key encryption/decryption functions support multiple modes of operation:
  - Electronic Code Book (ECB) mode
  - Cipher Block Chaining with Message Authentication (CBC-MAC) mode
  - Counter (CTR) mode
  - Combined CBC-MAC and Counter (CCM) mode
- A comprehensive *dsPIC® DSC Embedded Encryption Libraries User's Guide* describes the required APIs for library functions
- Several examples of use are provided for each library function

Getting Started

- Review the dsPIC DSC Symmetric Key Embedded Encryption Library web page at www.microchip.com
- Download the dsPIC DSC Embedded Encryption Libraries User's Guide from the Microchip web site
- Purchase part number SW300050
- If Asymmetric Key Embedded Encryption Library support is required (part number SW300055), visit www.microchip.com and review the applicable information

Cryptographic Functions

Cryptographic Algorithm	Applicable Specification	Cryptographic Function[2]	Code Size (bytes)	Data Rate[4] (Kbytes/sec)
RNG	ANSI X9.82, FIPS 180-2	Deterministic Random Bit Generator	1353	—
SHA-1	FIPS 180-2	Secure Hash Algorithm – 160 bit	909	423
MD5	RFC 1321	Message Digest – 128 bit	1428	656
T-DES	FIPS 46-3	Basic Encryption and Decryption	8892	49(3)
	FIPS 46-3	ECBWrapper(1)	123	
	NISTSP 800-38A	CBCWrapper(1)	903	
	NISTSP 800-38A	CTRWrapper(1)	348	
AES (128-bit)	FIPS 197	Basic Encryption	2505	232(3)
	FIPS 197	Basic Decryption	2895	
	FIPS 197	ECBWrapper(1)	234	
	FIPS 113	CBC-MAC Encryption Wrapper(1)	663	
	NISTSP 800-38A	CBCDecryption Wrapper(1)	357	
	NISTSP 800-38A	CTRWrapper(1)	348	
	IEEE 802.11i	CCMWrapper(1)	930	

Notes:
1. Wrapper functions are used in combination with the underlying basic encryption and/or decryption functions for the respective algorithm (AES,T-DES).
2. All library functions use the stack and require input and output message buffers to be set up by the calling application, stack usage is below 60 bytes of RAM.
3. AES and T-DES data rate represents the average of the data rates for performing basic encryption and decryption functions for a single block of data.
4. All data rate statistics shown here assume device operation of 30 MIPS.

Triple DES/AES Encryption Libraries

Summary

Microchip offers a reliable security solution for embedded applications built on the 16-bit microcontroller platform. This solution is provided by means of a single library. This library features the symmetric key encryption/decryption functions Advanced Encryption Standard (AES) and Triple-Data Encryption Algorithm (Triple-DES). This solution is provided by means of two libraries – Symmetric Key and Asymmetric Key Embedded Encryption Libraries. The Symmetric Key Library features:

- Hash functions
  - SHA-1 secure hash standard
  - MD5 message digest
- Symmetric key encryption/decryption functions
  - Advanced Encryption Standard (AES)
  - Triple-Data Encryption Algorithm (Triple-DES)
- Random number generator functions
  - Deterministic Random Bit Generator ANSI X9.82

Typical Applications

The algorithms supported by this library have emerged as the de facto standard for many large scale, secured applications like web access, E-mail, secure XML transactions and Virtual Private Networks (VPN). These algorithms are also recommended by most Internet Engineering Task Force (IETF), Federal Information Processing Standards (FIPS) and IPSec standards. Some typical applications for this library include:

- Mobile and wireless devices, PDAs
- Secure banking
- Secure web transactions
- ZigBee™ technology and other monitoring and control applications
- Smart card readers/trusted card readers
- Friend/foe identification

Typical Applications (Continued)

- Secure devices and peripherals inter-operating with TCG and NGSCB PC's

The Trusted Computing Group (TCG) and related Microsoft® Next- generation Secure Computing Base (NGSCB) both specify RSA and Triple-DES. RSA and other asymmetric solutions are featured in the dsPIC DSC Asymmetric Key Embedded Encryption Library (SW300055).

Features

- Optimized for speed, code size and RAM usage
- Library functions tested for adherence to applicable standards
- Application note describing APIs
- Several examples of use are provided for each library function

Getting Started

- Review the dsPIC DSC Symmetric Key Embedded Encryption Library web page at www.microchip.com
- Download the dsPIC DSC Embedded Encryption Libraries User's Guide from the Microchip web site
- Purchase part number SW300050
- If Asymmetric Key Embedded Encryption Library support is required (part number SW300055), visit www.microchip.com and review the applicable information

Cryptographic Functions

Cryptographic Algorithm	Applicable Specification	Cryptographic Function (1)	Code Size (in bytes)	Data Rate (2) (Kbytes/sec)
T-DES	FIPS 46-3	Basic Encryption and Decryption	7500	19.8 (16 MIPs) 37.2 (30 MIPs)
AES (128-bit)	FIPS 197	Basic Encryption	3018	74.1 (16 MIPs) 138.9 (30 MIPs)

Notes:
1. **Wrapper functions are used in combination with the underlying basic encryption and/or decryption functions for the respective algorithm (AES,T-DES).**
2. **AES and T-DES data rate represents the average of the data rates for performing basic encryption and decryption functions for a single block of data.**

dsPIC® DSC Asymmetric Key Embedded Encryption Library

Summary

Microchip offers a reliable security solution for embedded applications built on the dsPIC Digital Signal Controller (DSC) platform. This solution is provided by means of two libraries – Symmetric Key and Asymmetric Key Embedded Encryption Libraries. The Asymmetric Key Library implements the following:

- Public key encryption/decryption functions
  - RSA (1024 and 2048 bit)
- Key agreement protocol
  - Diffie-Hellman (1024 and 2048 bit)
- Signing and verification
  - DSA (1024 bit)
  - RSA (1024 and 2048 bit)
- Hash and message digest functions
  - SHA-1, MD5
- Random Number Generator (RNG)
  - ANSI X9.82

Typical Applications

The algorithms supported by this library have emerged as the de facto standard for many large-scale, secured applications like web access, E-mail, secure XML transactions, and virtual private networks (VPN). These algorithms are also recommended by most Internet Engineering Task Force (IETF), Federal Information Processing Standards (FIPS) and IPSec standards. Some typical applications for this library include:

- Mobile and wireless devices, PDAs
- Secure banking
- Secure web transactions
  - Secure Socket Layer (SSL)
  - Transport Layer Security (TLS)
  - Secure Multi-purpose Internet Mail Extensions (S/MIME)
- ZigBee™ technology and other monitoring and control applications
- Smart card readers
- Friend/foe identification
- Peripherals interoperating with TCG and NGSCB personal computers

The Trusted Computing Group (TCG) and related Microsoft® Next Generation Secure Computing Base (NGSCB), both specify RSA and Triple-DES. AES, Triple DES and other symmetric solutions are featured in the dsPIC DSC Symmetric Key Embedded Encryption Library (SW300050).

Execution Time

For a 1024-bit modulus, when the dsPIC DSC operates up to 40 MIPS, average execution times are provided below (in milliseconds):

- RSA Encryption and Verification functions execute in 5.25 ms for a 17-bit exponent
- RSA Decryption and Signing functions execute in 114 ms for a 17-bit exponent
- DSA Signing function executes in 60 ms
- DSA Verification function executes in 114 ms
- Diffie-Hellman key agreement executes in:
  - 59 ms for 160-bit key
  - 366 ms for 1024-bit key

Features

- C-callable library functions developed in MPLAB® ASM30 Assembly language
- Optimized for speed, code size and RAM usage
  - RAM usage below 100 bytes
- Library functions extensively tested for adherence to applicable standards
- A comprehensive *dsPIC® DSC Embedded Encryption Libraries User's Guide* describing the required APIs for the library functions
- Several examples of use provided for each library function

Getting Started

- Review the dsPIC DSC Asymmetric Key Embedded Encryption Library web page at www.microchip.com
- Download the *dsPIC® DSC Embedded Encryption Libraries User's Guide* from the Microchip web site
- Purchase part number SW300055
- If Symmetric Key Embedded Encryption Library support is required (part number SW300050), please visit www.microchip.com and

Cryptographic Functions

Cryptographic Algorithm	Applicable Specification	Cryptographic Function (1)	Security Strength (in bits)	Code Size((in bytes) (2)
Primary Functions				
RSA	PKSC#1 v1.5	Encryption/Decryption	1024, 2048	2574
RSA	PKSC#1 v1.5	Signing/Verification	1024, 2048	2658
Diffie-Hellman	PKCS#3	Key Agreement Protocol	1024, 2048	2067
DSA	FIPS 186-2	Signing/Verification	1024	4341
Auxillary Functions				
Big Integer (3)	–	Modulus Arithmetic Functions Inverse Modulus Arithmetic Montgomery Arithmetic	– – –	927 495 552
Deterministic	ANSI X9.82	Random Number Generator	–	1353
SHA-1	FIPS 180-2	Secure Hash Algorithm	160	912
MD5	RFC 1321	Message Digest MD5	128	1428

Notes:

1. All library functions use the stack and require input and output message buffers to be set up by the calling application. Stack usage is below 100 bytes of RAM.
2. If more than one primary function is used in an application, code size required by the library will be less than the sum of code sizes for individual primary functions. For example, if RSA Signing/Verification and Diffie-Hellman Key Agreement are both used by an application, the library code size linked into the application is 3246 bytes, which is significantly lesser than (2658 + 2067) bytes.
3. The dsPIC30F6010/6011/6012/6013/6014 devices may not be used with the big integer arithmetic package (and as a consequence library). However, the dsPIC30F601XA devices and all other dsPIC DSC devices do support the library.

dsPIC® DSC
Speex Speech Encoding/Decoding Library

Summary

The dsPIC Digital Signal Controller (DSC) Speex Speech Encoding/Decoding Library performs toll-quality voice compression and voice decompression. The library is a modified version of the Speex speech coder made specifically for the dsPIC DSC families and features a 16:1 compression ratio. Encoding uses Code Excited Linear Prediction (CELP), which is a popular coding technique. CELP provides a reasonable trade-off between performance and computational complexity.

The library is appropriate for both half-duplex and full-duplex systems. With its small footprint and low output data rate, it is also ideal for playback-only applications that require storage of encoded speech including:

- Answering machines
- Building and home safety systems
- Intercoms
- Smart appliances
- Voice recorders
- Walkie-talkies
- Any application using message playback

Predominantly written in assembly language, the Speex Speech Encoding/Decoding Library optimizes computational performance and minimizes RAM usage. A well-defined API makes it easy to integrate with the application.

A flexible analog interface gives your design several options to consider. The speech encoder samples speech at 8 kHz using either an external codec or the on-chip 12-bit analog-to-digital converter. The speech decoder plays decoded speech through an external codec or the on-chip Pulse Width Modulator (PWM). Storing compressed speech for playback requires approximately 1 Kbyte of memory for each second of speech.

A PC-based Speech Encoder Utility program (pictured above) creates encoded speech files for playback. Encoded speech files are made from either a PC microphone or existing WAV file. Once the encoded speech files are created, they are added to an MPLAB® IDE project, just like a regular source file, and built into the application.

The Speech Encoder Utility allows four target memory areas to store a speech file: program memory, data EEPROM, RAM and external Flash memory. External Flash memory stores many minutes of speech (1 minute of speech requires 60 KB) and it is supported through a dsPIC DSC general purpose I/O port.

Resource Requirements

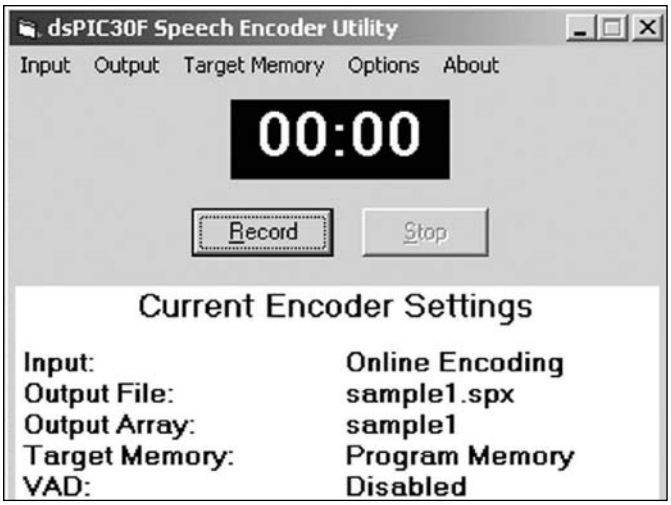
Encoder:

- Sampling Interface: Si-3000 audio codec or 12-bit ADC
- Computational Power: 19 MIPS (worst case)
- Program Flash Memory: 33 KB
- RAM*: 5.4 KB (1.2 KB is scratch)

Decoder

- Playback Interface: Si-3000 audio codec or PWM
- Computational Power: 3 MIPS
- Program Flash Memory: 15 KB
- RAM*: 3.2 KB

* Full-duplex support is now possible and requires 6.8 KB of RAM.



Features

Key features of the Speech Encoding/Decoding Library include:

- Fixed 8 kHz sample rate
- Fixed 8 kbps output rate
- PESQ-based Mean Opinion Score: 3.7 – 4.2 (out of 5.0)
- Code Excited Linear Prediction (CELP)-based coding
- Two analog input interfaces – codec or on-chip 12-bit ADC
- Two analog output interfaces – codec or on-chip PWM
- Optional voice activity detection
- Playback-only applications benefit from the Speech Encoder utility; encoded speech files can be created from the desktop using a PC microphone or WAV file
- Storing compressed speech requires 1 KB of memory per second of speech
- Off-chip support for playback of long speech samples
- Royalty free (only one-time license fee)
- Full compliance with Microchip MPLAB® C30 Language Tools
- *dsPIC® DSC Speech Encoding/Decoding Library User's Guide* assists in using the library (DS70154)
- Designed to run on dsPICDEM™ 1.1 General Purpose Development Board (DM300014)

Devices Supported

Encoder:

- dsPIC30F6014
- dsPIC30F6014A
- dsPIC30F6013
- dsPIC30F6013A
- dsPIC30F6012
- dsPIC30F6012A
- dsPIC30F6011
- dsPIC30F6011A
- dsPIC33FJXXXGPXXX

Decoder:

- dsPIC30F6014
- dsPIC30F6014A
- dsPIC30F6013
- dsPIC30F6013A
- dsPIC30F6012
- dsPIC30F6012A
- dsPIC30F6011
- dsPIC30F6011A
- dsPIC30F5013
- dsPIC30F5011
- dsPIC33FJXXXGPXXX

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PIC24/dsPIC® DSC
G.711 Speech Encoding/Decoding Library

Summary

The PIC24/dsPIC® Digital Signal Controller (DSC) G.711 Speech Encoding/Decoding Library performs toll-quality voice compression and voice decompression. The library is an implementation of the ITU-T G.711 standard on the dsPIC DSC. The encoding algorithm used is either A-law or µ-law companding (user-selectable), and features a 2:1 compression ratio. G.711 uses minimal computational resources, and a well-defined API makes it easy to integrate with the application.

The G.711 library can be used for both half-duplex and full-duplex systems. However, due to its high output data rate, it is most suitable for full-duplex communications applications that do not need to store the encoded speech for subsequent playback. Some target applications include:

- Intercoms
- Emergency phones
- Walkie-talkies
- Mobile hands-free kits
- Digital radios
- Voice-over-IP telephony

A flexible analog interface gives your design several options to consider. The speech encoder samples speech at 8 kHz using either an external codec or the on-chip 12-bit Analog-to-Digital Converter (ADC). The speech decoder plays decoded speech through an external codec or the on-chip Pulse Width Modulator (PWM). Storing compressed speech for playback requires 8 KB of memory for each second of speech.

A PC-based Speech Encoder Utility program creates encoded speech files for playback. Encoded speech files are made from either a PC microphone or existing WAV file. Once the encoded speech files are created, they are added to an MPLAB® IDE project, just like a regular source file, and built into the application.

Resource Requirements

Full-duplex operation

Computational Power:	1 MIPS
Program Flash Memory:	3 KB

Features

Key features of the G.711 Speech Encoding/Decoding Library:

- Fixed 8 kHz input sample rate
- Fixed 64 kbps output data rate
- PESQ-based Mean Opinion Score (MOS): 4.3 to 4.5 (out of 5.0)
- A-law or µ-law based coding
- Two analog input interfaces – codec or on-chip ADC
- Two analog output interfaces – codec or on-chip PWM
- Playback-only applications benefit from the Speech Encoder Utility. Encoded files can be created from the desktop using a PC microphone or WAV file.
- Storing compressed speech requires 8 KB of memory per second of speech
- FREE library
- Full compliance with Microchip's MPLAB® C30 C compiler language tools
- PIC24/dsPIC DSC G.711 Speech Encoding/Decoding Library User's Guide assists in using the library
- Designed to run on dsPICDEM™ 1.1 General Purpose Development Board

Devices Supported

PIC24HJXXXGPXXX
PIC24FJXXXAXXX
dsPIC30F6014
dsPIC30F6014A
dsPIC30F6013
dsPIC30F6013A
dsPIC30F6012
dsPIC30F6012A
dsPIC30F6011
dsPIC30F6011A
dsPIC30F5013
dsPIC30F5011
dsPIC33FXXXGPXXX

dsPIC® DSC
G.726A Speech Encoding/Decoding Library

Summary

The dsPIC Digital Signal Controller (DSC) G.726A Speech Encoding/Decoding Library performs toll-quality voice compression and voice decompression. The library is an implementation of the ITU-T G.726 (Annex A) standard, on the dsPIC DSC. The encoding algorithm used is Adaptive Differential Pulse Code Modulation (ADPCM). The compression can be configured by the user to be either 3.2:1, 4:1, 5.33:1 and 8:1, corresponding to output data rates of 40, 32, 24 and 16 kbps respectively. A well-defined API makes the library easy to integrate with the application.

The G.711 library is suitable for both half-duplex and full-duplex systems. Some key applications include:

- Intercoms
- Emergency phones
- Walkie-talkies
- Mobile hands-free kits
- Digital radios
- Voice-over-IP telephony
- Building and home safety systems
- Smart appliances
- Voice recorders
- Answering machines

A flexible analog interface gives your design several options to consider. The speech encoder samples speech at 8 kHz using either an external codec or the on-chip 12-bit Analog-to-Digital Converter (ADC). The speech decoder plays decoded speech through an external codec or the on-chip Pulse Width Modulator (PWM). Storing compressed speech for playback requires 8 KB of memory for each second of speech.

A PC-based Speech Encoder Utility program creates encoded speech files for playback. Encoded speech files are made from either a PC microphone or existing WAV file. Once the encoded speech files are created, they are added to an MPLAB® IDE project, just like a regular source file, and built into the application.

Resource Requirements

Computational power:	15 MIPS
Program Flash memory:	6 KB
Data RAM:	4 KB (typical)

Features

Key features of the G.726A Speech Encoding/Decoding Library:

- Fixed 8 kHz input sample rate
- User-selectable output data rate of 40, 32, 24 or 16 kbps
- PESQ-based Mean Opinion Score (MOS): 4.3 to 4.5 (out of 5.0)
- Adaptive Differential Pulse Code Modulation (ADPCM)-based coding
- Two analog input interfaces: codec or on-chip ADC
- Two analog output interfaces: codec or on-chip PWM
- Playback-only applications benefit from the Speech Encoder Utility. Encoded files can be created from the desktop using a PC microphone or WAV file.
- Storing compressed speech requires 5, 4, 3 or 2 KB of memory per second of speech
- Royalty-free, one time only, license fee
- Full compliance with Microchip's MPLAB® C30 C compiler language tools
- dsPIC® DSC G.726A Speech Encoding/Decoding Library User's Guide assists in using the library
- Designed to run on dsPICDEM™ 1.1 General Purpose Development Board

Devices Supported

dsPIC30F6014	dsPIC30F6012A
dsPIC30F6014A	dsPIC30F6011
dsPIC30F6013	dsPIC30F6011A
dsPIC30F6013A	dsPIC30F5013
dsPIC30F6012	dsPIC30F5011
	dsPIC33FXXXGPXXX

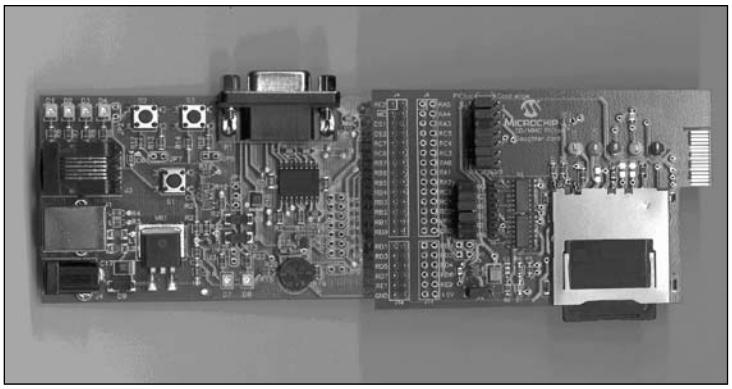
FAT 16
File System Library

Summary

The use of removable Flash-based media cards in embedded systems is becoming more prevalent. The price per megabyte is dropping rapidly and the size is increasing allowing cost effective large memory storage options for designers. Applications that require data logging or retrieval of large blocks of data such as fonts or bitmaps can take advantage of Flash memory cards.

The FAT 16 File System Library allows the designer to easily integrate a removable Flash-based media card up to 2 gigabytes into their application. The FAT16 File System Library is modular and provided in “C” source to easily integrate into any application. This library requires 16 Kbytes of program memory to implement all the standard FAT16 functions: fopen, fread, fwrite, fseek, etc. The library also requires 1.5 Kbytes of RAM for the heap, read/write buffer, disc structures, etc.

While the source code is free, you should contact Microsoft® to obtain a license to use the FAT16 File System.



Features

Key features of the FAT16 File System Library include:

- Available free for use on Microchip microcontrollers
- Portable across all PIC18, PIC24 and dsPIC® DSC products
- Support for MPLAB C18 C Compiler and MPLAB C30 C Compiler
- Supports SD/MMC and CompactFlash memory cards
- Supports up to 2 GB
- Supported by SD/MMC PICtail™ Plus Daughter Board AC164122) and future CompactFlash PICtail Plus Daughter Board
- 16 Kbytes of program memory, 1.5 Kbytes of RAM

dsPIC® DSC DSP Library

Summary

The dsPIC Digital Signal Controller (DSC) DSP Library provides a set of speed optimized functions for the most common digital signal processing applications. The dsPIC DSC DSP Library provides significant performance savings over equivalent functions coded in C and allows developers to dramatically shorten their development time. The dsPIC DSC DSP library may be used with any dsPIC DSC variant.

The dsPIC DSC DSP Library is written predominantly in Assembly language and makes extensive use of the dsPIC DSC DSP instruction set and hardware resources, including X and Y memory addressing, modulo addressing, bit-reversed addressing, 9.31 saturation and REPEAT and DO loops.

The dsPIC DSC DSP Library provides functions for the following:

- Vector operations
- Matrix operations
- Filtering operations
- Transform operations
- Window® operations

Function Execution Times

Function	Cycle Count Equation	Conditions*	Number of Cycles	Execution Time @40 MIPS
Complex FFT**	—	N=64	3739	93.5 µs
Complex FFT**	—	N=128	8485	212.1 µs
Complex FFT**	—	N=256	19055	476.4 µs
Single Tap FIR	—	—	1	25 ns
Block FIR	53+N(4+M)	N=32, M=32	1205	30.2 µs
Block FIR Lattice	41+N(4+7M)	N=32, M=32	7337	183.5 µs
Block IIR Canonic	36+N(8+7S)	N=32, S=4	1188	29.7 µs
Block IIR Lattice	46+N(16+7M)	N=32, M=8	2350	58.7 µs
Matrix Add	20+3(C*R)	C=8, R=8	212	5.3 µs
Matrix Transpose	16+C(6+3(R-1))	C=8, R=8	232	5.8 µs
Vector Dot Product	17+3N	N=32	113	2.9 µs
Vector Max	19+7(N-2)	N=32	229	5.7 µs
Vector Multiply	17+4N	N=32	145	3.6 µs
Vector Power	16+2N	N=32	80	2.0 µs
*C= #columns, N=# samples, M=#taps, S=#sections, R=#rows **Complex FFT routine inherently prevents overflow.				
1 cycle = 25 nanoseconds @ 40 MIPS				

Features

Key features of the dsPIC DSC DSP Library include:

- 49 total functions
- Full compliance with the Microchip MPLAB® C30 C compiler, assembler and linker
- Simple user interface – only one library file and one header file
- Functions are both C and assembly callable
- FIR filtering functions include support for lattice, decimating, interpolating and LMS filters
- IIR filtering functions include support for canonic, transposed canonic and lattice filters
- FIR and IIR functions may be used with the filter files generated by the dsPIC® DSC Digital Filter Design Tool
- Transform functions include support for in-place and out-of-place DCT, FFT and IFFT transforms
- Window functions include support for Bartlett, Blackman, Hamming, Hanning and Kaiser windows
- Support for program space visibility
- Complete function profile information including register usage, cycle count and function size information

Devices Supported

- All processors in the dsPIC DSC families

PIC24/dsPIC® DSC Math Library

Summary

The PIC24/dsPIC Digital Signal Controller (DSC) Math Library is the compiled version of the math library that is distributed with the highly optimized, ANSI-compliant MPLAB® C30 C Compiler (SW006012). It contains advanced single and double-precision floating-point arithmetic and trigonometric functions from the standard C header file `<math.h>`. The library delivers small program code size and data size, reduced cycles and high accuracy.

Function Group	Function	Performance (Cycles)[1, 3, 4]
Basic Floating Point	Addition	122
	Subtraction	124
	Multiplication	109
	Division	361
	Remainder	385
Trigonometric and Hyperbolic	acos	478
	asin	363
	atan	696
	atan2	3206
	cos	3249
	sin	2238
	tan	2460
	cosh	1049
	sinh	525
	tanh	338
Logarithmic and Exponential	exp	530
	frexp	39
	ldexp	44
	log	2889
	log10	3007
Power Functions	pow	2134
	sqrt	493
Rounding Functions	ceil	94
	floor	51
Absolute Value Function	fabs	6
Modular Arithmetic Functions	modf	151
	fmod	129

Features

- The PIC24/dsPIC DSC Math Library is callable from either MPLAB C30 or PIC24/dsPIC DSC Assembly language
- The functions are IEEE-754 compliant, with signed zero, signed infinity, NaN (Not a Number) and denormal support and operated in the “round to nearest” mode
- Compatible with MPLAB ASM30 and MPLAB LINK30, which are available at no charge from www.microchip.com
- Total library memory usage[1, 2]:
  - Code size: 5250 bytes
  - Data size: 4 bytes

Devices Supported

- All processors in the PIC24/dsPIC DSC families

Notes

1. Results are based on using the MPLAB C30 compiler (SW006012) version 1.20.
2. Maximum memory usage when all functions in the library are loaded; most applications will use less.
3. All performance statistics represented here are for 32-bit IEEE 754 floating-point input and output data types.
4. Performance listed represent an average number of instruction cycles required to perform the floating-point operation.

PIC24H/dsPIC® DSC Peripheral Library

Summary

The PIC24H/dsPIC Digital Signal Controller (DSC) Peripheral Library provides a set of functions for setting up and controlling the operation of all the peripheral modules available in the PIC24H microcontrollers and dsPIC DSCs, as well as functions for interfacing with an external LCD. The dsPIC30F Peripheral Library serves as a convenient layer of abstraction over the specific details of the peripherals and their associated control and status registers.

The PIC24H/dsPIC DSC Peripheral Library supports the following hardware peripheral modules:

- Timers
- Input capture
- Output compare
- Quadrature Encoder Interface (QEI)
- Motor control PWM
- Real Time Clock Calendar (RTCC)
- Cyclic Redundancy Check (CRC)
- I/O ports and external interrupts
- Reset
- UART
- SPI
- I²C™
- Data Converter Interface (DCI)
- 10-bit A/D converter
- 12-bit A/D converter
- CAN
- Functions for controlling an external LCD through configurable I/O port pins are also provided

Features

Key features of the PIC24H/dsPIC DSC Peripheral Library include:

- A library file for each device from the PIC24/dsPIC DSC families, including functions corresponding to peripherals present in that particular device.
- C include files that enable pre-defined constants for passing parameters to various library functions, as well as a file for each peripheral module.
- Functions in pre-compiled libraries that may be called from an application program written in either MPLAB® C30 C Compiler or PIC24H/dsPIC DSC assembly languages.
- C source code is included to customize functions to specific application requirements.
- Pre-defined constants in the C include files eliminate the need to refer to the details and structure of every special function register, while initializing peripherals or checking status bits.

Resource Requirements

- Program memory: The PIC24H/dsPIC DSC Peripheral Library functions are optimized for efficient program memory usage.
  - Since the functions are in the form of libraries, the actual program memory requirements depend on the functions being called by the application, as well as on the specific PIC24H or dsPIC DSC being used.
- Data memory: The vast majority of the functions do not use RAM at all.
  - Each of the remaining functions use less than 10 bytes of RAM.

Devices Supported

- All processors in the PIC24H/dsPIC DSC families

Microchip
TCP/IP Stack Software (ENC28J60 Driver)

Summary

Communication over the Internet is accomplished by implementing the TCP/IP protocol. Microchip offers a Free TCP/IP software stack optimized for the PIC18 microcontroller family and all 16-bit devices. The stack is a suite of programs that provide services to all TCP/IP-based applications. Users do not need to know all the intricacies of the TCP/IP specifications in order to use the stack. Based on the TCP/IP reference model, the stack is divided into multiple layers, where each layer accesses services from one or more layers directly below it. Per specifications, many of the TCP/IP layers are "live," in the sense that they not only act when a service is requested, but also when events like time-out or new packet arrival occurs. The stack is modular in design and is written in the 'C' programming language. Effective implementations can be accomplished in roughly 20 Kbytes of code leaving plenty of code space available for the user's application.

The advantages of Ethernet connectivity for data distribution, remote monitoring and remote control of embedded applications are widely acknowledged. Ethernet's infrastructure, performance, interoperability, scalability and ease of development are unrivalled amongst communication standards. Microchip is unveiling embedded Ethernet solutions that meet market demands and requirements.

Microchip's ENC28J60 is a 28-pin, IEEE 802.3-compliant stand-alone Ethernet controller with on board MAC & PHY, 8 Kbytes of buffer RAM and SPI interface. These features, combined with Microchip's Free TCP/IP software stack, provide the smallest whole-product Ethernet solution for embedded applications. With a small package size including a 6x6 mm QFN, the ENC28J60 provides a low-pin count, cost-effective, easy-to-use solution for remote communication with embedded applications.

Features

Key features of the Microchip TCP/IP Stack (ENC28J60 Driver) include:

- Available free for use on Microchip microcontrollers
- Socket support for TCP and UDP
- Portable across all PIC18, PIC24, dsPIC30F and dsPIC33F products
- Support for MPLAB® C18, MPLAB® C30 and Hi-TECH PIC-18 C compilers
- RTOS independent
- Full TCP state machine
- Modular design
- Supported by Ethernet PICtail™ Plus Daighter Board (AC164123)
- Supports the ENC28J60 Ethernet controller

Supported Protocols and Approximate Resource Requirements

- ARP: 800 bytes
- IP: 400 bytes
- ICMP: 300 bytes
- UDP: 800 bytes
- TCP: 3.8 Kbytes
- DHCP: 1.3 Kbytes
- SNMP: 2.8 Kbytes
- HTTP: 1.4 Kbytes

dsPICworks™
Data Analysis and DSP Software

Summary

dsPICworks Data Analysis and DSP Software is an easy-to-use data analysis and signal processing package for designs using dsPIC® Digital Signal Controllers (DSCs). It provides an extensive number of functions encompassing:

- Signal generation
- Arithmetic operations and digital signal processing
- One, two and three-dimensional display and measurement capabilities
- Data import/export compatible with MPLAB® IDE and MPLAB ASM30 assembler

Signal Generation

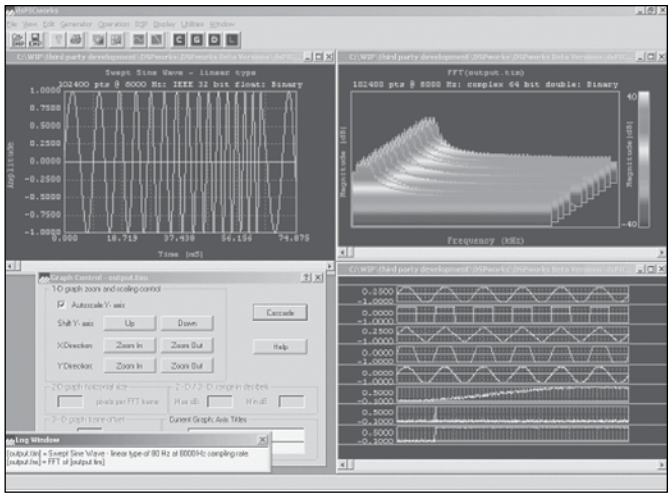
This software supports an extensive set of signal generators including basic sine, square and triangle wave generators as well as advanced generators for window functions, unit step, unit sample, sinc, exponential and noise functions. Noise, with specified distribution, can be added to any signal. Signals can be generated as 32-bit floating point or as 16-bit fractional fixed point values for any desired sampling rate. The length of the generated signal is limited only by available disk space. Signals can be imported or exported from or to MPLAB file register windows. Multi-channel data can be created by a set of multiplexing functions.

Arithmetic and Digital Signal Processing (DSP) Operations

dsPICworks Data Analysis and DSP Software has a wide range of DSP and arithmetic functions that can be applied to signals. Standard DSP functions include transform operations FFT and DCT, convolution and correlation, signal decimation, signal interpolation sample rate conversion and digital filtering. Digital filtering is an important part of this software. It uses filters designed by the sister-application, Digital Filter Design, and applies them to synthesized or imported signals. dsPICworks Data Analysis and DSP Software also features special operations such as signal clipping, scaling and quantization, which are vital in practical analysis of DSP algorithms.

Display and Measurement

This software has a wide variety of display and measurement options. Frequency domain data may be plotted in the form of two-dimensional spectrogram and three-dimensional waterfall options. The signals can be measured accurately by a simple mouse-click. The log window shows current cursor coordinates and derived values, such as difference from last position and signal frequency. Signal strength may be measured over a particular range of frequencies. Special support exists for displaying multi-channel/multiplexed data. Graphs allow zoom options and a set of color scheme options is available to customize display settings.



File Import/Export – MPLAB® and MPLAB ASM30 Support

dsPICworks Data Analysis and DSP Software allows data to be imported from the external world in the form of ASCII text or binary files. Conversely, it allows data to be exported in the form of files. The software supports all file formats supported by the MPLAB import/export table feature, bringing real-world data from MPLAB into dsPICworks for analysis. The software can also create MPLAB ASM30 assembler files that can be included into the MPLAB IDE workspace.

Features

Key features of the dsPICworks Data Analysis and DSP Software include:

- Wide variety of signal generators – sine, square, triangular, window functions, noise
- Extensive DSP functions – FFT, DCT, filtering, convolution, interpolation
- Extensive arithmetic functions – algebraic expressions, data-scaling, clipping, etc.
- One, two and three-dimensional displays
- Multiple data quantization and saturation options
- Multi-channel data support
- Automatic script file-based execution options available for any user-defined sequence of dsPICworks data analysis and DSP software functions
- File import/export interoperable with MPLAB IDE
- Digital filtering options support filters generated by dsPIC® DSC Digital Filter Design
- MPLAB ASM30 assembler file option to export data tables into dsPIC30F and dsPIC33F RAM

Digital Filter Design/ Digital Filter Design Lite

Summary

The Digital Filter Design tool for the 16-bit dsPIC® Digital Signal Controller (DSC) makes designing, analyzing and implementing Finite Impulse Response (FIR) and Infinite Impulse Response (IIR) digital filters easy through a menu-driven and intuitive user interface. The filter design tool performs complex mathematical computations for filter design, provides superior graphical displays and generates comprehensive design reports. Desired filter frequency specifications are entered and the tool generates the filter code and coefficient files ready to use in the MPLAB® IDE Integrated Development Environment. System analysis of the filter transfer function is supported with multiple generated graphs, such as magnitude, phase, group delay, log magnitude, impulse response and pole/zero locations.

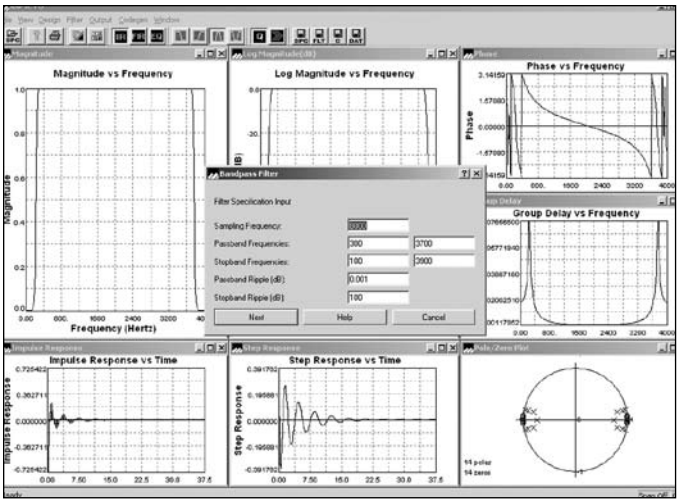
Finite Impulse Response Filter Design

- Design method selection
  - FIR window design
  - FIR equiripple design (Parks-McClellan)
- Low-pass, high-pass, band-pass and band-stop filters
- FIR filters can have up to 513 taps
- Following window functions are supported:

Rectangular	4 term cosine
Hanning (Hann)	4 term cosine with continuous 5th derivative
Hamming	Minimum 4 term cosine
Triangular	Good 4 term Blackman Harris
Blackman	Harris flat top
Exact Blackman	Kaiser
3 term cosine	Dolph-Tschebyscheff
3 term cosine with continuous 3rd derivative	Taylor
Minimum 3 term cosine	Gaussian

- Reports provide design details such as window coefficients and impulse response prior to multiplying by the window function

	Filter Design	Filter Design Lite
List Price	$249	$29
Low-pass	√	√
High-pass	√	√
Band-pass	√	√
Band-stop	√	√
FIR Taps	Up to 513	Up to 64
IIR Taps for LP, HP	Up to 10	Up to 4
IIR Taps for BP, BS	Up to 20	Up to 8
Generate ASM Code	√	√
Export to MPLAB® IDE	√	√
Export to MPLAB® C30 C Compiler	√	√
MATLAB® Support	√	—



Infinite Impulse Response Filter Design

- Low-pass, high-pass, band-pass and band-stop filters
- Filter orders up to 10 for low-pass and high-pass filters
- Filter orders up to 20 for band-pass and band-stop filters
- Five analog prototype filters are available:
  - Butterworth
  - Tschebyscheff
  - Inverse Tschebyscheff
  - Elliptic
  - Bessel
- Digital transformations are performed by bilinear transformation method
- Reports show design details such as all transformations from normalized low-pass filter to desired filter

Code Generation Features

- Generated files are compliant with Microchip's MPLAB C30 C compiler, assembler and linker
- Choice of placement of coefficients in program space or data space
- C wrapper/header code generation

Graphs

- Magnitude response vs. frequency
- Log magnitude vs. frequency
- Phase response vs. frequency
- Group delay vs. frequency
- Impulse response vs. time (per sample)
- Step response vs. time (per sample)
- Pole and zero locations (IIR only)

RTOS/CMX-RTX™ for PIC24/dsPIC® DSC

Summary

In some cases, well-structured linear programming is sufficient for a product. In most cases, however, programmers appreciate not having to worry about structuring their code to perform all necessary tasks in a timely manner. This is where RTOS/CMX-RTX can help. RTOS/CMX-RTX allows tasks (pieces of code that do specific duties) to run quasi-concurrently, doing many specific jobs simultaneously.

RTOS/CMX-RTX takes the worry and headaches out of real time programming. The software lets embedded programmers concentrate on the overall application while taking care of the little details. Finish projects faster and more efficiently with CMX-RTX.

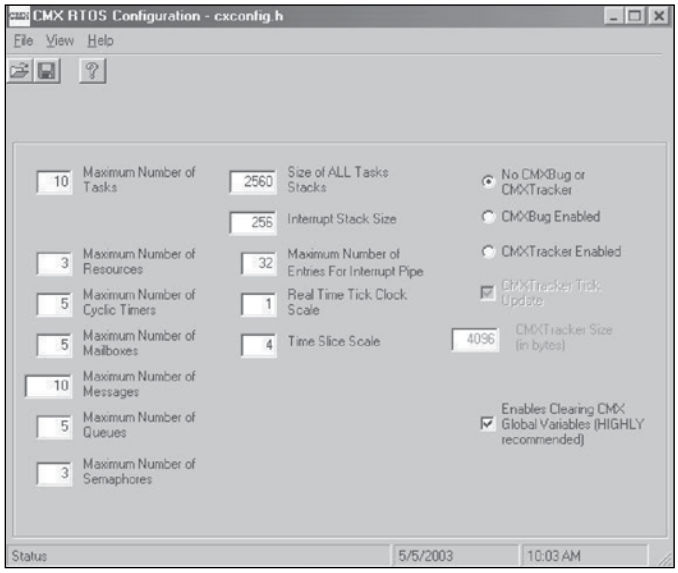
Some RTOS software offers only cooperative scheduling which means that the running task has to call the scheduler to perform a task switch. Others offer time slicing in which each task runs for a certain period of time at which point a task switch takes place no matter what. Also others claim to be fully preemptive, yet they do not allow any interrupt to cause a preemption. All of these models will fail at one point or another.

RTOS/CMX-RTX allows a task of higher priority that is able to run (whether starting or resuming) to preempt the lower priority running task. The scheduler saves the context of the running (lower priority) task and restores the context of the higher priority task so that it is now running. A truly preemptive RTOS allows interrupts to cause an immediate task switch. This means that the interrupts now have the added ability of using the RTOS's functions.

Features

Key features of the RTOS/CMX-RTX for PIC24/dsPIC® Digital Signal Controller (DSC) include:

- The smallest footprint
- The fastest context switch times
- The lowest interrupt latency times
- True preemption
- Scheduler and interrupt handler written in assembly for speed and optimization
- Optional cooperative and time-slicing scheduling
- Nested interrupts
- All functions contained in a library
- Interrupt callable functions
- Scalability
- Free source code provided
- Integrated with TCP/IP CMX-MicroNet™ for optional networking connectivity



CMX-RTX is easy to configure and integrate with your application using the CMX RTOS configuration manager.

RTOS/CMX-RTX Specifications for PIC24/dsPIC DSC Products

Flash

All CMX functions:	3696 bytes
CMX initialize module:	936 bytes
CMX assembly module (scheduler):	645 bytes
RAM, each task control block:	28 bytes
Min. context switch:	92 cycles (starting a task)
	137 cycles (resuming a task)

CMX Functions are contained in a library, thus reducing code size, if not referenced.

Examples of RTOS/CMX-RTX Functionality

Task management
System management
Event management
Memory management
Message management
Queue management
Resource management
Semaphore management
Timer management

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RTOS/CMX-Tiny+™ for PIC24/dsPIC® DSC

Summary

In some cases, well structured linear programming is sufficient for a product. In most cases, however, programmers appreciate not having to worry about structuring their code to perform all necessary tasks in a timely manner. This is where RTOS/CMX-Tiny+ can help. RTOS/CMX-Tiny+ allows tasks (pieces of code that do specific duties) to run quasi-concurrently. This means that tasks will seem to run all at the same time - doing many specific jobs simultaneously.

RTOS/CMX-Tiny+ takes the worry and headaches out of real time programming. The software lets the embedded programmer concentrate on the overall application while taking care of the little details. Finish projects faster and more efficiently with RTOS/CMX-Tiny+.

Some RTOS software offers only cooperative scheduling which means that the running task has to call the scheduler to perform a task switch. Others offer time slicing in which each task runs for a certain period of time at which point a task switch takes place no matter what. Also others claim to be fully preemptive, yet do not allow any interrupt to cause a preemption. All of these models will fail at one point or another.

RTOS/CMX-Tiny+ allows a task of higher priority that is able to run (whether starting or resuming) to preempt the lower priority running task. This will cause the scheduler to save the context of the running (lower priority) task and restore the context of the higher priority task so that it is now running. A truly preemptive RTOS allows interrupts to cause an immediate task switch. This means that the interrupts now have the added ability of using the RTOS's functions.

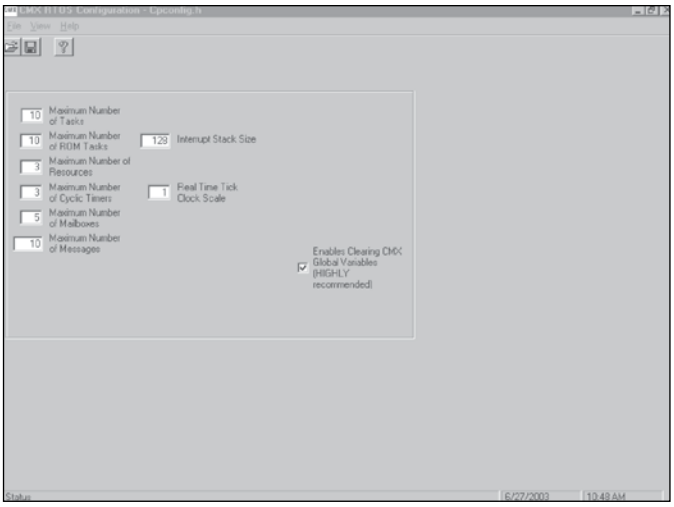
In addition, RTOS/CMX-Tiny+ has been especially designed to offer such a small Flash/RAM footprint that it can be used with only the onboard Flash/RAM of the PIC24/dsPIC Digital Signal Controller (DSC) as a single chip solution. Based upon a scaled down version of the popular RTOS/CMX-RTX™, RTOS/CMX-Tiny+ retains most of the power of RTOS/CMX-RTX, as well as the more frequently used functions.

RTOS CMX-Tiny+ Specifications for PIC24/dsPIC Digital Signal Controller (DSC)

Flash

All CMX functions:	2304 bytes
CMX initialize module:	249 bytes
CMX assembly module (scheduler):	570 bytes
RAM, each task control block:	13 bytes
Flash, Each task bontrol block:	6 bytes
Min. context switch:	71 cycles (starting a task)
	121 cycles (resuming a task)

CMX functions are contained in a library, thus reducing code size, if not referenced.



RTOS/CMX-Tiny+ is easy to configure and integrate with your application using the CMX RTOS configuration manager.

Features

Key features of the RTOS/CMX-Tiny+ for dsPIC DSC include:

- Extremely small Flash/RAM footprint
- Truly preemptive RTOS
- Low-power mode supported
- Full source code with every purchase
- Free technical support and updates
- Low, economical pricing
- No royalties on shipped products
- Backward compatible with CMX-Scheduler™
- Integrated with CMX-MicroNet™ for optional networking connectivity

Examples of RTOS/CMX-RTX Functionality

Task Management
System Management
Event Management
Memory Management
Message Management
Queue Management
Resource Management
Semaphore Management
Timer Management

RTOS/CMX-Scheduler™ for PIC24/dsPIC® DSC

Summary

RTOS/CMX-Scheduler is the result of a special collaboration between CMX and Microchip. Offered in object code only, CMX-Scheduler is available for FREE to embedded systems designers using the PIC24 or dsPIC Digital Signal Controllers (DSCs). RTOS/CMX-Scheduler is specially designed for developers whose designs do not require a full-blown RTOS and/or who are wondering if a kernel might help their application. The perfect entry-level kernel, RTOS/CMX-Scheduler is intuitive to use and easy to implement.

RTOS/CMX-Scheduler offers many growth paths for future designs. Applications developed with the CMX-Scheduler kernel are upwardly compatible with the popular CMX-Tiny+™ or CMX-RTX™ RTOS. RTOS/CMX-Scheduler also is tightly integrated with the unique CMX-MicroNet™ TCP/IP stack for those applications that require networking connectivity.

RTOS/CMX-Scheduler software and documentation is delivered in electronic format and is freely licensed for unlimited product usage on the PIC24 and dsPIC DSC devices.

Features

Key features of the RTOS/CMX-Scheduler include:

- FREE for use on any dsPIC DSC device
- Easy to learn and use
- Truly preemptive kernel
- Supports up to five tasks
- Fast performance
- Free bug fixes and updates
- No royalties on shipped products
- Compatible with RTOS/CMX-Tiny+ and RTOS/CMX-RTX
- Complete electronic documentation
- Integrated with TCP/IP-CMX-MicroNet for optional networking connectivity

RTOS/CMX-Scheduler Specifications for PIC24/dsPIC DSC

All CMX functions:	972 bytes
CMX initialize module:	153 bytes
CMX assembly module:	567 bytes
RAM, each task control block:	11 bytes
Flash, each task control block:	5 bytes
Min. context switch:	81 cycles (starting a task)
	102 cycles (resuming a task)

CMX functions are contained in a library, thus reducing code size, if not referenced.

Functionality

- K_Task_Create – creates a task
- K_Task_Start – starts a task
- K_Task_Wake – wakes a task
- K_Task_Wait – has a task wait with/without a time out
- K_Task_Kill – deletes a task
- K_Task_Coop_Sched – performs a cooperative task switch
- K_Event_Wait – waits on an event
- K_Event_Signal – signals an event from a task
- K_Event_Signal – signals an event from an interrupt
- K_Event_Reset – resets an event for a particular task

TCP/IP-CMX-MicroNet™ for PIC24/dsPIC® DSC

Summary

TCP/IP CMX-MicroNet is an embedded TCP/IP stack specifically designed for optimized use of Flash and RAM resources on Microchip's 16-bit PIC24 microcontrollers and dsPIC® Digital Signal Controllers (DSCs). The software runs directly on the processor with no gateways or PCs required. The stack can be run in Stand-Alone mode or work in conjunction with an RTOS. Using only industry standard protocols, TCP/IP CMX-MicroNet offers true TCP/IP networking via direct, dial-up or Ethernet connectivity and wireless Ethernet (802.11b).

Up to 127 Ethernet sockets and/or PPP or SLIP sockets can be open at a time, however PPP and SLIP cannot be used at the same time. An HTTP Web server, FTP server, SMTP client and DHCP client are also available. The RS-232 link, if used, can either be a direct cable link or through a modem.

TCP/IP CMX-MicroNet offers only industry standard protocols running right on your target processor. TCP/IP CMX-MicroNet offers a low, one-time fee and no royalties on deployed products. Full source code is provided.

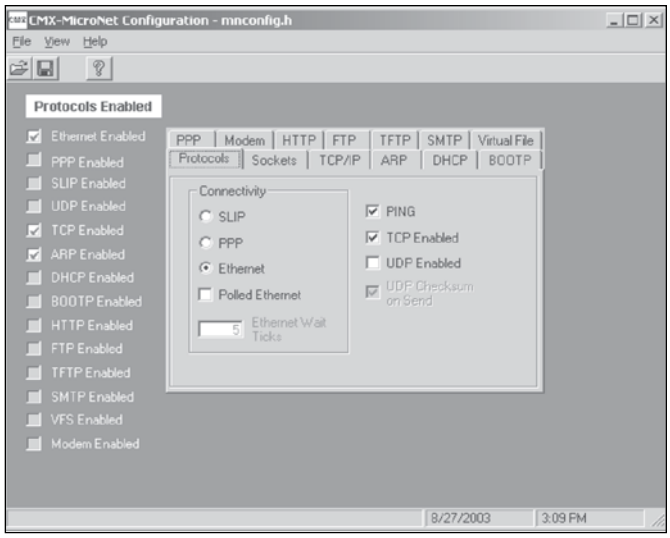
TCP/IP CMX-MicroNet Specifications for PIC24/dsPIC DSCs

Flash

UDP/IP + core	4470 bytes
TCP/IP + core	7827 bytes
UDP/TCP/IP + core	8685 bytes
PPP	6681 bytes
Modem	447 bytes
HTTP server	3888 bytes
Virtual file	885 bytes
Ethernet	2652 bytes
DHCP client	2202 bytes
FTP server	3657 bytes
TFTP client	723 bytes
BOOTP	684 bytes
SMTP	1918 bytes
Utility	1314 bytes

RAM (not including buffer sizes)

UDP/SLIP	56 bytes
TCP/HTTP/PPP	304 bytes
Ethernet	38 bytes



TCP/IP-CMX-MicroNet is easy to configure and integrate with your application.

Features

Key features of TCP/IP CMX-MicroNet include:

- Tested and proven in hundreds of designs worldwide
- Extremely small Flash/RAM requirements
- Software solution does not require additional processor
- Web pages may contain CGI calls and server side includes
- FTP files, including new firmware
- Send E-mail
- Can serve up Java applets
- No proprietary protocols
- Runs stand-alone or with any RTOS
- Economical one time fee
- Full source code provided
- No royalties on shipped products
- Excellent documentation and support

Supported Protocols

TCP PPP UDP SLIP IP DHCP
FTP TFTP SMTP HTTP Web Server

Connectivity

Ethernet, wireless Ethernet, dial-up, direct, (POP3 coming soon)

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Application Solution: Sensorless BLDC Motor Control Using the dsPIC30F

Ready to Use Solution

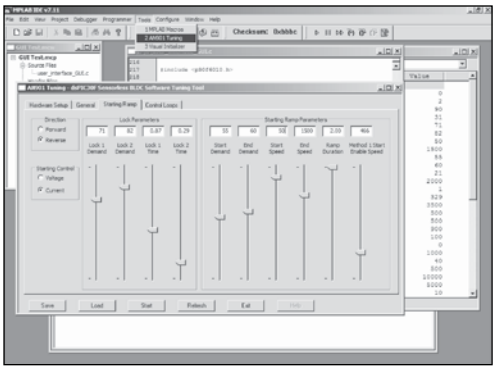
Microchip provides a proven, fully functional and highly flexible solution for using the dsPIC30F to control Brushless DC (BLDC) motors without mechanical Hall-effect position sensors. The software makes extensive use of dsPIC30F peripherals for motor control. The algorithm implemented for sensorless control is particularly suitable for use on fans and pumps. The program is written in C and has been specifically optimized and well-annotated for ease of understanding and program modification/configuration.

Proven Software Source Code

The software can be downloaded from the Microchip web site (www.microchip.com) by searching for source code library part number SWAN0901.

Parameter Tuning User Interface

Manipulation of the source code for different motors can be accomplished through the use a graphical interface developed for this application solution, allowing you to manage/change certain motor specific parameters and control/tune settings/limits, used by the source code.

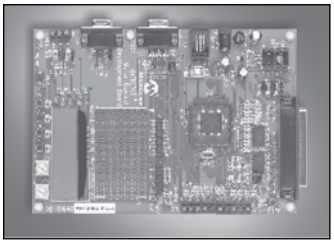


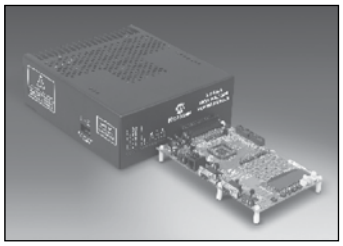
Capabilities of this Application Solution:

- Application includes adjustable parameters and two selectable starting methods to match the particular load
- Back EMF zero-crossing routine precludes the need for position sensing components
- Detects if the sensorless control algorithm gets lost
- Restarts the sensorless control without stopping the motor
- Program code size: 15 KB of program Flash memory or less, depending on the features used
- RAM size: 276 bytes of data RAM memory

Hardware Development Platform:

- MC1 Motor Control Development Board (DM300020)
- MC1L 3-phase Low-voltage Power Module (DM300022)
- 3-Phase BLDC Low-voltage Motor (24V) (AC300020)





Additional Development Support:

- A working example of bringing the hardware and software together: Application Note AN901 support document on the Microchip web site
  - Go to www.microchip.com, search for AN901, download the .pdf document and the .zip source code file
- Motor Control Getting Started Guide (DS51406) available on Microchip's web site
- Microchip's Motor Control Design Center: Extensive design support material; URL: www.microchip.com/motor
- MPLAB® ICD 2 In-Circuit Debugger and Device Programmer (DV164005)

Application Solution:
Using the dsPIC30F for Vector Control of an ACIM

Ready-to-Use Solution

Microchip's AC Induction Motor (ACIM) vector control solution is written for the dsPIC30F family of devices and requires a basic understanding of ACIM characteristics. The software makes extensive use of dsPIC30F peripherals for motor control. The program is written in C and has been specifically optimized and well annotated for ease of understanding and program modification.

Proven Software Source Code

The software can be downloaded from the Microchip web site by searching for source code library part number SWAN0908.

Hardware Development Platform:

- MC1 Motor Control Development Board (DM300020)
- MC1H 3-phase High-Voltage Power Module (DM300021)
- 3-Phase ACIM High-voltage Motor (208/460V) (AC300021)

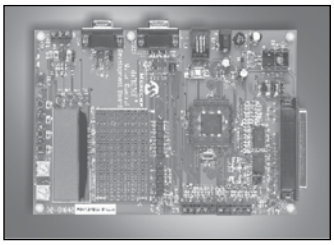
Additional Development Support:

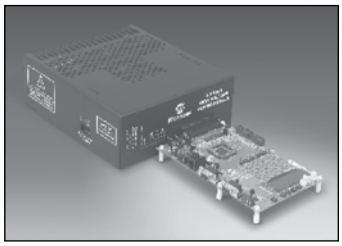
- A working example of bringing the hardware and software together: Application Note AN908 support document on the Microchip web site
  - Go to www.microchip.com, search for AN908, download the .pdf document and the .zip source code file
- Motor Control Getting Started Guide (DS51406): document available on Microchip web site
- Microchip's Motor Control Design Center: Extensive design support material; URL: www.microchip.com/motor
- MPLAB® ICD 2 In-Circuit Debugger and Device Programmer (DV164005)

Capabilities of this Application Solution:

- The software implements vector control of an ACIM, using the indirect flux control method
- With a 50 µsec control loop period, the software requires approximately 9 MIPS of CPU usage (less than one-third of the total available CPU)
- Optional Diagnostic mode can be enabled to allow real-time observation of internal program variables on an oscilloscope; also facilitates control loop adjustment
- Program code size: 8 KB of program Flash memory
- RAM size: 512 bytes of data RAM memory

  NOTE: These memory requirements would be supported by a dsPIC30F2010 – the smallest dsPIC® Digital Signal Controller (DSC) targeted for motor control.





Application Solution:
Sensored BLDC Motor Control Using dsPIC30F2010

Ready to Use Solution

Microchip provides a fully working and highly flexible solution for using the dsPIC30F2010 to control Brushless DC (BLDC) motors with Hall-effect position sensors. The software makes extensive use of dsPIC30F peripherals for motor control. The program is written in C and has been specifically optimized and well annotated for ease of understanding and program modification.

Proven Software Source Code

The software can be downloaded from the Microchip web site by searching for source code library part number SWAN0957.

Hardware Development Platform:

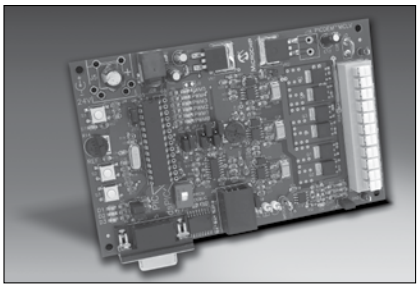
- PICDEM™ MC LV Development Board (DM183021)
- Hurst DMB0224C10002 CLB 6403 24V BLDC Motor (AC300020)

Additional Development Support:

- A working example of bringing the hardware and software together: Application Note AN957 support document on the Microchip web site
  - Go to www.microchip.com, search for AN957, download the .pdf document and the .zip source code file
- Motor Control Getting Started Guide (DS51406): document available on Microchip web site
- Microchip's Motor Control Design Center: Extensive design support material; URL: www.microchip.com/motor
- MPLAB® ICD 2 In Circuit Debugger and Device Programmer (DV164005)

Capabilities of this Application Solution:

- Source code provides both open-loop control and closed-loop control algorithms
- Potentiometer for speed control
- Reference AN901 for BLDC motor details
- Program code size: 2 KB of program Flash memory
- RAM size: 180 bytes of data RAM memory



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Application Solution: An Introduction to AC Induction Motor Control Using the dsPIC30F

Ready-to-Use Solution

Microchip demonstrates how to use the dsPIC30F to control an AC Induction Motor (ACIM). The solution presented requires a basic understanding of ACIM characteristics and is based on the dsPICDEM™ Motor Control Development System, although it can be used with alternative hardware, if needed. The program is written in assembly code and has been specifically optimized and well annotated for ease of understanding and program modification. It provides basic variable speed control of an ACIM.

Proven Software Source Code

The software can be downloaded from the Microchip web site by searching for source code library part number SWAN0984.

Hardware Development Platform:

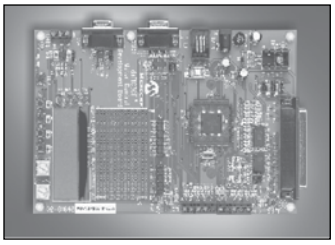
- MC1 Motor Control Development Board (DM300020)
- MC1H 3-phase High-voltage Power Module (DM300021)
- 3-Phase ACIM High-voltage Motor (208/460V) (AC300021)

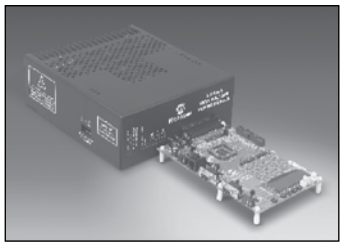
Additional Development Support:

- A working example of bringing the hardware and software together: Application Note AN984 support document on the Microchip web site
  - Go to www.microchip.com, search for AN984, download the .pdf document and the .zip source code file
- Motor Control Getting Started Guide (DS51406): document available on Microchip web site
- Microchip's Motor Control Design Center: Extensive design support material; URL: www.microchip.com/motor
- MPLAB® ICD 2 In-Circuit Debugger and Device Programmer (DV164005)

Capabilities of this Application Solution:

- Supports Sinusoidal waveforms for motor drive
- Provides volts-hertz drive operation for various torque profiles
- Program code size: 1200 bytes of program Flash memory
- RAM size: 86 bytes of data RAM memory





MICROCHIP
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Application Solution: Using the dsPIC30F for Sensorless BLDC Motor Control

Ready to Use Solution

Microchip provides a fully working and highly flexible solution for using the dsPIC30F2010, dsPIC30F3010 or dsPIC30F4012 to control BLDC sensorless motors without mechanical position sensors. The software makes extensive use of dsPIC30F peripherals for motor control. The algorithm implemented for sensorless control is particularly suitable for use on fans and pumps. The program is written in C and has been specifically optimized and well annotated for ease of understanding and programming.

Proven Software Source Code

The software can be downloaded from the Microchip web site by searching for source code library part number SWAN0992.

Hardware Development Platform:

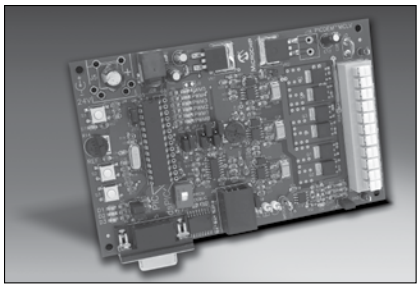
- PICDEM™ MC LV Development Board (DM300021)
- Hurst DMB0224C10002 CLB 6403 24V BLDC Motor (AC300020)

Additional Development Support:

- A working example of bringing the hardware and software together: Application Note AN992 support document on the Microchip web site
  - Go to www.microchip.com, search for AN992, download the .pdf document and the .zip source code file
- Motor Control Getting Started Guide (DS51406): document available on Microchip web site
- Microchip's Motor Control Design Center: Extensive design support material; URL: www.microchip.com/motor
- MPLAB® ICD 2 In-Circuit Debugger and Device Programmer (DV164005)
- Application Note AN901

Capabilities of this Application Solution:

- Based on Application Note AN901
- This solution uses a 28-pin device (dsPIC30F2010, dsPIC30F3010 or dsPIC30F4012) instead of a dsPIC30F6010
- Uses a potentiometer to select the motor speed
- A user interface is available to provide control of up to 45 control parameters
- Program code size: 10 Kbytes of program Flash memory
- RAM size: 300 bytes of data RAM memory



MICROCHIP
www.microchip.com

Application Solution: Sinusoidal Control of PMSM Motors with dsPIC30F DSC

Ready to Use Solution

Microchip provides a fully working and highly flexible solution for using the dsPIC30F2010 to control Brushless DC (BLDC) motors with the use of Hall-effect position sensors. The software makes extensive use of dsPIC30F peripherals for motor control. The program is written in C and has been specifically optimized and well annotated for ease of understanding and program modification.

Proven Software Source Code

The software can be downloaded from the Microchip web site by searching for source code library part number SWAN1017.

Hardware Development Platform:

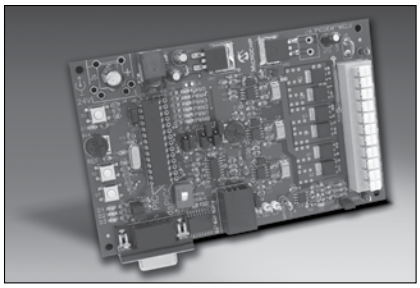
- PICDEM™ MC LV Development Board (DM300021)
- Hurst DMB0224C10002 CLB 6403 24V BLDC Motor (AC300020)

Additional Development Support:

- A working example of bringing the hardware and software together: Application Note AN1017 support document on the Microchip web site
  - Go to www.microchip.com, search for AN1017, download the .pdf document and the .zip source code file
- Motor Control Getting Started Guide (DS51406): document available on Microchip web site
- Microchip's Motor Control Design Center: Extensive design support material; URL: www.microchip.com/motor
- MPLAB® ICD 2 In Circuit Debugger and Device Programmer (DV164005)

Capabilities of this Application Solution:

- Source code provides both open-loop control and closed-loop control algorithms
- Potentiometer for speed control
- Sinusoidal control with Space-Vector Modulation (SVM)
- Four quadrant control
- Optimized PID implementation
- Program code size: 2 KB of program Flash memory
- RAM size: 180 bytes of data RAM memory



MICROCHIP
www.microchip.com

Application Solution:
Sensoreless Field-oriented Control of PMSM Motors

Ready to Use Solution

Microchip provides a fully working and highly-flexible sensorless solution for PMSM motor control using field-oriented control. Applications requiring rapid response to changing loads, high energy efficiency or quieter operation can benefit from this method.
The software makes extensive use of dsPIC® Digital Signal Controller (DSC) resources. Input current vectors are transformed to a coordinate system which is rotated to align with rotor flux. This transformation allows control with conventional techniques such as Proportional and Integral (PI) controllers, similar to a DC motor. The code is compact and can be implemented on all motor-control dsPIC DSCs. To save cost only two current sensors are needed (the third is computed).

Microchip's Data Monitor and Control Interface (DMCI) tool, which is a module within the MPLAB® IDE Integrated Development Environment, can be used to "tune" the algorithm for specific motor configurations.

Proven Software Source Code

The software can be downloaded from the Microchip web site by searching for source code library part number SWAN1078

Hardware Development Platform:

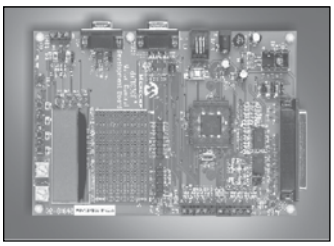
- PICDEM™ MC1 Motor Control Development Board (DM300020)
- PICDEM MC1H 3-Phase High Voltage Power Module (DM300021))

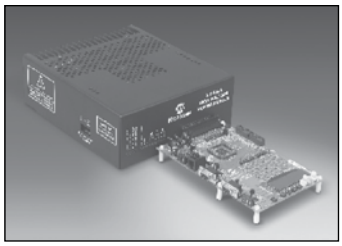
Additional Development Support:

- A working example of bringing the hardware and software together: access Application Note AN1078 on the Microchip web site
  - Go to www.microchip.com, search for AN1078, download the .pdf document and the .zip source code file
- Motor Control Getting Started Guide (DS51406): document available on Microchip web site
- Microchip's Motor Control Design Center: Extensive design support material; URL: www.microchip.com/motor
- MPLAB® ICD 2 In Circuit Debugger and Device Programmer (DV164005)

Capabilities of this Application Solution:

- Source code provides for maximum design flexibility
- Models, algorithms and variables are fully defined
- Control parameters and observe results using MPLAB IDE dynamic data-control interface
- Motor Start-up subroutine is included
- Program code size: 7 Kbytes of Flash memory
- RAM size: 400 bytes of data RAM memory
- 11 MIPS





MICROCHIP
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MPLAB®
Visual Device Initializer

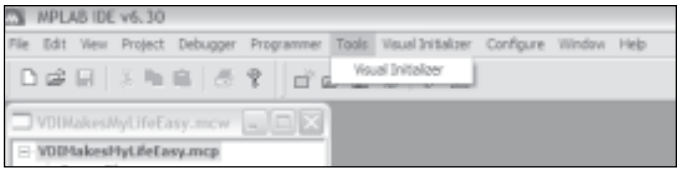
Summary

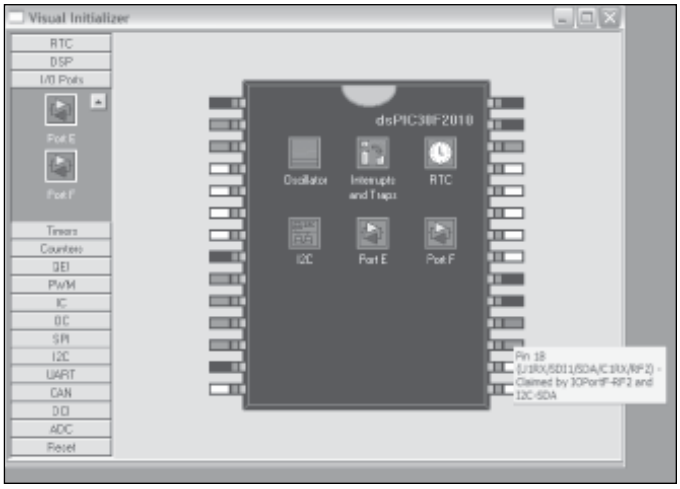
Configuring a powerful 16-bit microcontroller or digital signal controller can be complex and challenging tasks. MPLAB Visual Device Initializer (VDI) allows users to configure the entire processor graphically, and when complete, a mouse-click generates code usable in assembly or C programs.

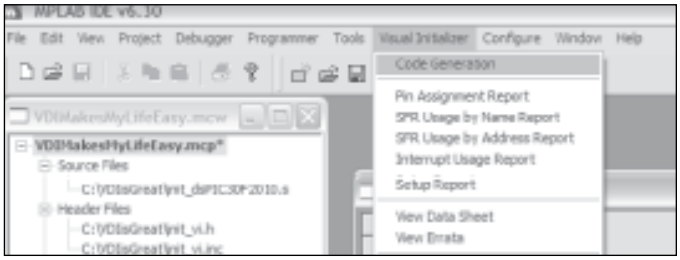
MPLAB VDI does extensive error checking on assignments and conflicts on pins, memories and interrupts as well as selection on operating conditions. The generated code files are integrated with the rest of the application code through the MPLAB IDE Integrated Development Environment project.

The detailed report on resource assignment and configuration simplifies project documentation.

MPLAB VDI is a standard plug-in to MPLAB IDE and can be invoked from within MPLAB IDE under the Tools menu.







Features

Key features of the MPLAB VDI include:

- Drag and drop feature selection
- One click configuration
- Extensive error checking
- Generates initialization code
- Integrates seamlessly in MPLAB IDE project
- Printed reports eases project documentation requirements

MPLAB® C30 C Compiler

Summary

The MPLAB C30 C compiler is a fully ANSI-compliant product with standard libraries for the 16-bit PIC24 microcontroller and dsPIC® Digital Signal Controller (DSC) architectures. It is highly optimizing and takes advantage of many PIC24/dsPIC DSC-specific features to provide efficient software code generation. The MPLAB C30 C compiler also provides extensions that allow for excellent support of the hardware, such as interrupts and peripherals. It is fully integrated with the MPLAB IDE for high level, source debugging.

This compiler comes complete with its own assembler, linker and librarian to write mixed mode C and assembly programs and link the resulting object files into a single executable file.

The MPLAB C30 C compiler is distributed with a complete ANSI C standard library. The library includes functions for string manipulation, dynamic memory allocation, data conversion, timekeeping and math functions (trigonometric, exponential and hyperbolic).

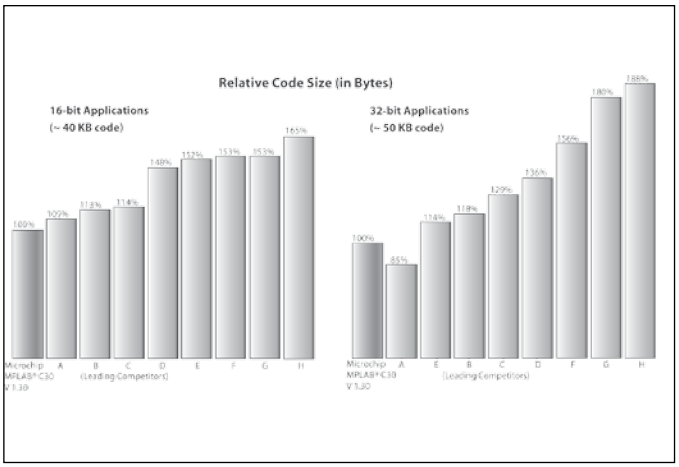
The compiler supports both large and small code and data models. The small code model takes advantage of a more efficient form of call instructions, while the small data model supports the use of compact instructions for accessing data in SFR space.

The MPLAB C30 C compiler includes a powerful command-line driver program. Using the driver program, application programs can be compiled, assembled, and linked in a single step.

Features

Key features of the MPLAB C30 C compiler include:

- ANSI-compliant
- Integrated with MPLAB IDE for easy-to-use project management and source-level debugging
- Generates relocatable object modules for enhanced code reuse
- Fully compatible with object modules generated with MPLAB ASM30 Assembler, allowing complete freedom to mix Assembly and C in a single project
- Interrupt code can be written in C or Assembly
- Flexible memory models take advantage of small memory applications and the storage of data in SFR space



Features (Continued)

- Strong support for inline assembly when total control is absolutely necessary
- Super-efficient code generator engine with multi-level optimization
- Extensive library support, including standard C, math, DSP and PIC24/dsPIC DSC peripheral libraries
- Software libraries and application development tools are available

Package Contents

- MPLAB C30 C Compiler software
- MPLAB IDE software and documentation CD
- *MPLAB ASM30, MPLAB LINK30 and Utilities User's Guide*
- *MPLAB C30 C Compiler User's Guide*
- *dsPIC DSC Language Tools Getting Started*

MICROCHIP
www.microchip.com

MPLAB® REAL ICE™ In-Circuit Emulation System

Summary

MPLAB REAL ICE In-circuit Emulation System is Microchip's next-generation emulation and debugging system. Initially supporting the dsPIC30F601XA, dsPIC33F, PIC24H and PIC24F 16-bit devices, this in-circuit emulation system provides a powerful in-circuit emulation platform for easy and rapid application development and debugging. The emulation is performed using special hardware logic on the target device itself, eliminating the need for a separate emulator device as well as precluding the possibility of the emulator differing from the target device in functionality. The REAL ICE system supports full-speed emulation, communicating with the target device through a traditional In-Circuit Serial Programming™ (ICSP™) interface (default) or a high-speed, low-voltage differential signaling connection (for high noise immunity with longer cable lengths, especially for in-system emulation). Communication with MPLAB IDE on the host workstation is handled through a high-speed USB 2.0 interface

The MPLAB REAL ICE system provides substantial emulation and debugging features on a low-cost and non-intrusive platform. Up to 6 hardware breakpoints and 1000 software breakpoints are supported, depending on the target device. Advanced, device dependant breakpoint features are also included, such as break on address or data match, break on data read or data write, pass counter and freezing peripherals during breaks. In addition, the MPLAB REAL ICE system allows user-configurable tracing of program memory and logging of data memory variables and registers, easily controlled and monitored in real-time via MPLAB IDE.

With extensive over-voltage and over-current protections, rugged probe interface buffers and optically isolated power circuitry, the MPLAB REAL ICE hardware provides a high degree of robustness, making it an ideal emulation platform for use in embedded control applications.

Features

Key features of the MPLAB REAL ICE system include:

- Full speed emulation on target device itself — no separate emulator device needed
- Robust electrical design for safe, low-cost in-circuit emulation
- High speed USB 2.0 PC interface
- Multiple target connections: traditional ICSP interface or LVDS (add-on option)
- Run, Halt and Single-step modes
- 6 hardware breakpoints and other advanced breakpoint features depending on the device
- 1000 software breakpoints (depending on the device)
- Instrumented (user-controlled) Program Memory Trace and Data Memory Log, with run-time updates in MPLAB IDE
- Stopwatch cycle counter
- Logic probe
- In-Circuit Serial Programming and read of on-chip Flash memory

Software Development Tools and Operating Systems

Development Tool	Product Name	Description	Part#	List Price (1)	Devices Supported PIC24F	PIC24H	dsPIC30F	dsPIC33F
Integrated Development Environment	MPLAB® IDE*	Integrated Development Environment	SW007002	Free	√	√	√	√
C Compilers	MPLAB® C30	ANSI C compiler, assembler, linker and librarian	SW006012	$895	√	√	√	√
	MPLAB® C30 Site License	Site License for compiler	SL006012	$8950	√	√	√	√
	Embedded Workbench for dsPIC30F	ISO/ANSI C and Embedded C++ compiler in a professional, extensible IDE, (Windows® NT/2000/Windows XP®) special DSP support included.	EWdsPIC 1	Contact IAR	√	√	√	√
	HI-TECH C	ANSI C Compiler for dsPIC® DSCs and PIC24 MCUs, integrates with MPLAB® IDE	dsPIC/PIC24	Contact HI-TECH	√	√	√	√
Operating Systems	CMX-Tiny+™ for dsPIC® DSC	Preemptive Real-time Operating System (RTOS) for dsPIC30F (from CMX)	CMX-Tiny+ for dsPIC30F	Contact CMX	√	√	√	√
		Preemptive Real-time Operating System (RTOS) for dsPIC30F	SW300032	$3000	√	√	√	√
	CMX-RTX™ for dsPIC® DSC	Fully preemptive Real-time Operating System (RTOS) for dsPIC30F (from CMX)	CMX-RTX for dsPIC30F	Contact CMX	√	√	√	√
		Fully preemptive Real-time Operating System (RTOS) for dsPIC30F	SW300031	$4000	√	√	√	√
	CMX Scheduler™	Multi-tasking, preemptive scheduler for dsPIC30F	SW300030	Free	√	√	√	√
	osCAN for dsPIC® DSC	OSEK/VDX v2.2	—	Contact Vector	—	√	√	√
	FreeRTOS.org™	Portable, open source, mini real time kernel	—	Contact freeRTOS.org™	√	√	√	√
	SEGGER embOS	Real-time operating system for embedded applications	—	Contact SEGGER	√	√	√	√
	Micriμm μC/OS-II	Portable, scalable, preemptive real-time, multitasking kernel	—	Contact Micrium	√	√	√	√
DSP	dsPICworks™	Data analysis and DSP software	SW300023	Free	√	√	√	√
	Digital Filter Design	Full featured graphical IIR and FIR filter design package for dsPIC30F	SW300001	$249	—	—	√	√
	Digital Filter Design Lite	Graphical IIR and FIR filter design package for dsPIC30F	SW300001-LT	$29	—	—	√	√

(1) List price may change without notice.

* Includes MPLAB ASM30, MPLAB SIM, MPLAB VDI.

Development Boards and Reference Designs

Development Tool	Description	Part#	List Price (1)	Devices Supported PIC24F	PIC24H	dsPIC30F	dsPIC33F
Starter Development Boards	Explorer 16 Development Board	DM240001	$129.99	√	√	—	√
	dsPICDEM™ 80-pin Starter Development Board	DM300019	$79.99	—	—	√	—
	16-bit 28-pin Starter Development Board	DM300027	$79.99	√	√	√	√
	dsPICDEM™ 2 Development Board	DM300018	$99.99	√	√	√	√
General Purpose Development Board	dsPICDEM™ 1.1 Plus General Purpose Development Board	DM300024	$299.99	—	—	√	√
Motor Control Development Boards	PICDEM™ MC LV Development Board	DM183021	$129.99	—	—	√	—
	dsPICDEM™ MC1 Motor Control Development Board	DM300020	$300	—	—	√	—
	dsPICDEM™ MC1H 3-Phase High Voltage Power Module	DM300021	$800	—	—	√	√
	3-Phase ACIM High Voltage Motor (208/460V)	AC300021	$120	—	—	√	√
	dsPICDEM™ MC1L 3-Phase Low Voltage Power Module	DM300022	$700	—	—	√	√
	3-Phase BLDC Low Voltage Motor (24V)	AC300020	$120	—	—	√	√
Connectivity Development Boards	dsPICDEM.net™ 1 with FCC/JATE-compliant and Ethernet NIC support	DM300004-1	$389.99	—	—	√	—
	dsPICDEM.net™ 2 with CTR-21-compliant and Ethernet NIC support	DM300004-2	$389.99	—	—	√	—
SMPS Development Board	dsPICDEM™ SMPS Buck Development Board	DM300023	$99.99	—	—	√	—

(1) List price may change without notice.

Hardware Development Tools

Development Tool	Description	Part#	List Price [1]	Devices Supported PIC24F	PIC24H	dsPIC30F	dsPIC33F
MPLAB® ICD 2	In-Circuit Debugger/Programmer	DV164005	$159.99	√	√	√	√
	In-Circuit Debugger/Programmer with dsPICDEM™ 1.1 Plus General Purpose Board	DV164032	$399.99	—	—	√	—
MPLAB® REAL ICE™	In-Circuit Emulator System	DV244005	$499.98	√	√	√	√
	Performance Pak	AC244002	$159.98	√	√	√	√
MPLAB® PM3	Full Featured Device Programmer, Base Unit	DV007004	$895	√	√	√	√
	Socket Module for 18L/28L/40L DIP Devices	AC164301	$189	√	√	√	√
	Socket Module for 16L (.150)/28L (.300) SOIC Devices	AC164302	$189	√	√	√	√
	Socket Module for 28L ML Devices	AC164322	$189	√	√	√	√
	Socket Module for 44L ML Devices	AC164322	$189	√	√	√	√
	Socket Module for 44L TQFP Devices	AC164305	$189	√	√	√	√
	Socket Module for 64L TQFP Devices (PF Package)	AC164313	$189	—	—	√	—
	Socket Module for 64L TQFP Devices (PT Package)	AC164319	$189	√	√	√	√
	Socket Module for 80L TQFP Devices (PF Package)	AC164314	$189	—	—	√	—
	Socket Module for 80L TQFP Devices (PT Package)	AC164320	$189	√	—	√	√

(1) List price may change without notice.

Plug-in Modules, PICtail™ Plus and Adapters for Development Boards

A Plug-in Module (PIM) is a daughter board with a dsPIC® DSC or PIC® MCU soldered on top and header socket strips on the bottom. This method allows for easy swapping of devices onto the various development boards, without having to unsolder and resolder parts.

Development Tool	Description	Part#	List Price[1]	Devices Supported PIC24F	PIC24H	dsPIC30F	dsPIC33F
PICtail™ Plus Daughter Boards	PICtail™ Plus Daughter Board for Secure Digital (SD)/Multimedia Card (MMC) to SPI interface	AC164122	$37.99	√	√	√	√
	Ethernet PICtail™ Plus Daughter Board	AC164123	$39.99	√	√	√	√
	IrDA® Protocol PICtail™ Plus Daughter Board	AC164124	$25.00	√	√	—	√
	Speech Playback PICtail™ Plus Daughter Board	AC164125	$45	√	√	√	√
	Prototype PICtail™ Plus Daughter Board	AC164126	$20	√	√	√	√
Plug-in Modules	PC Board with 100-pin PIC24FJ128GA010 MCU sample; use with DM240001 Development Board	MA240011	$25	√	—	—	—
	PC Board with 100-pin PIC24HJ256GP610 MCU sample; use with DM240001 Development Board	MA240012	$25	—	√	—	—
	PC Board with 44-pin PIC24FJ64GA004 MCU sample; use with DM240001 Development Board	MA240013	$25	√	—	—	—
	PC Board with 100-pin dsPIC33FJ256GP710 DSC sample; use with DM240001 Development Board	MA330011	$25	—	—	—	√
	PC Board with 100-pin dsPIC33FJ256GP710 DSC sample; use with DM300019 Development Board	MA330012	$25	—	—	—	√
	PC board with 100-pin dsPIC33FJ256GP710 motor control DSC sample; use with DM300019 and DM300020 Development Boards	MA330013	$25	—	—	—	√
	PC Board with 80-pin dsPIC30F6010A motor control DSC sample; use with DM300019 and DM300020 Development Boards	MA300015	$25	—	—	√	—
	PC Board with 80-pin dsPIC30F6014A general purpose DSC sample; use with DM300024 and DM300019 Development Boards	MA300014	$25	—	—	√	—
	PC Board with 44-pin SMPS dsPIC30F2023 sample; use with DM300019 Development Board	MA300016	$25	—	—	√	—

(1) List price may change without notice.

Software Libraries and Application Development Tools

Development Tool	Description	Part#	List Price(1)	Devices Supported PIC24F	PIC24H	dsPIC30F	dsPIC33F
dsPIC30F Math Library	Standard math and floating point library (ASM, C Wrapper)	SW300020	Free	√	√	√	√
dsPIC30F Peripheral Library	Peripheral initialization, control and utility routines (C)	SW300021	Free	√	√	√	√
dsPIC30F DSP Library	Essential DSP algorithm suite (Filters, FFT)	SW300022	Free	—	—	√	√
Symmetric Key Embedded Encryption Library	Security encryption software support for AES, triple-DES, SHA-1, RNG and MD5	SW300050 - 5K*	$2500	—	—	√	√
	Evaluation copy of security encryption software support for AES, triple-DES, SHA-1, RNG and MD5	SW300050-EVAL	$5	—	—	√	√
Triple DES/AES Encryption Libraries	Production license for security encryption software support for AES and Triple-DES	SW300052	$5	√	√	√	√
Asymmetric Key Embedded Encryption Library	Security encryption software support for RSA, DSA, Diffie-Hellman, SHA-1, RNG and MD5	SW300055 - 5K*	$2500	—	—	√	√
	Evaluation copy of security encryption software support for RSA, DSA, Diffie-Hellman, SHA-1, RNG and MD5	SW300055-EVAL	$5	—	—	√	√
Noise Suppression Library	Function to suppress noise interference in speech signals	SW300040 - 5K*	$2500	—	—	√	√
	Evaluation copy of function to suppress noise interference in speech signals	SW300040-EVAL	Free	—	—	√	√
Acoustic Echo Cancellation Library	Function to eliminate echo generated from a speaker to a microphone	SW300060 - 5K*	$2500	—	—	√	√
	Evaluation copy of function to eliminate echo generated from a speaker to a microphone	SW300060-EVAL	Free	—	—	√	√
Line Echo Cancellation Library	Function to cancel electrical line echoes caused by 2- or 4-wire conversion hybrids	SW300080-5K	$2500	—	—	√	√
	Function to cancel electrical line echoes caused by 2- or 4-wire conversion hybrids	SW300080-EVAL	Free	—	—	√	√
TCP/IP Library	TCP/IP connectivity and protocol support	CMX-for dsPIC30F	Contact CMX	—	—	√	√
	TCP/IP connectivity and protocol support	SW300024	Free	√	√	√	√
Soft Modem Library	V.22bis/V.22 Soft Modem Library	SW300002	Free	—	—	√	√
	V.32bis Soft Modem Library	SW300003*	$2500	—	—	√	√
	Evaluation copy of V.32bis Soft Modem Library	SW300003-EVAL	Free	—	—	√	√
	V.32 (non-trellis) Soft Modem Library	—	Contact Vocal	—	—	√	√
Speech Recognition System	Automatic speech recognition system including a PC-based speech training sub-system and a speech recognizer software library (16:1 compression)	SW300010 - 5K*	$2500	—	—	√	√
	Evaluation copy of automatic speech recognition system including a PC-based speech training sub-system and a speech recognizer software library (16:1 compression)	SW300010-EVAL	Free	—	—	√	√
SPEEX Speech Encoding/ Decoding Library	Speech library to perform speech compression and decompression	SW300070 - 5K*	$2500	—	—	√	√
	Evaluation copy of speech library to perform speech compression and decompression	SW300070-EVAL	Free	—	—	√	√
G.711 Speech Encoding/ Decoding Library	APCM speech compression and decompression (2:1 compression)	SW300026	Free	√	√	√	√
G.726A Speech Encoding/ Decoding Library	Speech compression and decompression (8:1 compression)	SW300090- 5K*	$2500	—	—	√	√
	Evaluation copy of speech compression and decompression (8:1 compression)	SW300090-EVAL	Free	—	—	√	√
FAT16 File System Library	Implements all the standard FAT16 functions: fopen, fread, fwrite, fseek, etc.	SW300027	Free	√	√	√	√
CANbedded for dsPIC® DSC	CAN driver library for dsPIC30F	—	Contact Vector	—	√	√	√

(1) List price may change without notice

* To license for production quantities greater than 5,000 pieces for a project's lifetime—contact Microchip.

Third Party Contact Information

Company	Phone	E-mail	Web Site
CMX Systems, Inc.	+1 904 880 1840	cmx@cmx.com	www.cmx.com
FreeRTOS.org™	—	—	www.freertos.org
HI-TECH Software	+61 7 3552 777	hitech@htsoft.com	www.htsoft.com
IAR	+46 18 16 78 00	info@iar.se	www.iar.se
Micrium	+1 954 217 2036	info@micruim.com	www.micruim.com
SEGGER	+49 2103 2878 0	info@segger.com	www.segger.com
Vector Informatik GmbH	+49 711 80670 0	info@vector-informatik.com	www.vector-informatik.com
VOCAL Technologies, LTD	+1 716 688 4675	sales@vocal.com	www.vocal.com

Documentation

Note that all the latest revisions of these documents are available from the Microchip web site.

Document Type	Document Title	Document Number
Overview Documents	PIC24H High Performance 16-bit Microcontroller Family Overview	DS70166
	dsPIC30F High Performance 16-bit Digital Signal Controller Family Overview	DS70043
	dsPIC33F High Performance 16-bit Digital Signal Controller Family Overview	DS70155
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