

### FEATURES

**Low Supply Current: 600  $\mu$ A Max**

**OP07 Type Performance**

**Offset Voltage: 20  $\mu$ V Max**

**Offset Voltage Drift: 0.6  $\mu$ V/ $^{\circ}$ C Max**

**Very Low Bias Current**

**25 $^{\circ}$ C: 100 pA Max**

**-55 $^{\circ}$ C to +125 $^{\circ}$ C: 250 pA Max**

**High Common-Mode Rejection: 114 dB Min**

**Extended Industrial Temperature Range: -40 $^{\circ}$ C to +85 $^{\circ}$ C**

### GENERAL DESCRIPTION

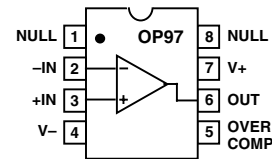
The OP97 is a low power alternative to the industry-standard OP07 precision amplifier. The OP97 maintains the standards of performance set by the OP07 while utilizing only 600  $\mu$ A supply current, less than 1/6 that of an OP07. Offset voltage is an ultralow 25  $\mu$ V, and drift over temperature is below 0.6  $\mu$ V/ $^{\circ}$ C. External offset trimming is not required in the majority of circuits.

Improvements have been made over OP07 specifications in several areas. Notable is bias current, which remains below 250 pA over the full military temperature range. The OP97 is ideal for use in precision long-term integrators or sample-and-hold circuits that must operate at elevated temperatures.

### PIN CONNECTIONS

**8-Lead PDIP (P Suffix)**

**8-Lead SOIC (S Suffix)**



Common-mode rejection and power supply rejection are also improved with the OP97, at 114 dB minimum over wider ranges of common-mode or supply voltage. Outstanding PSR, a supply range specified from  $\pm 2.25$  V to  $\pm 20$  V and the OP97's minimal power requirements combine to make the OP97 a preferred device for portable and battery-powered instruments.

The OP97 conforms to the OP07 pinout, with the null potentiometer connected between Pins 1 and 8 with the wiper to V+. The OP97 will upgrade circuit designs using 725, OP05, OP07, OP12, and 1012 type amplifiers. It may replace 741-type amplifiers in circuits without nulling or where the nulling circuitry has been removed.

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# OP97—SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS (@ $V_S = \pm 15\text{ V}$ , $V_{CM} = 0\text{ V}$ , $T_A = 25^\circ\text{C}$ , unless otherwise noted.)

Parameter	Symbol	Conditions	OP97E			OP97F			Unit
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$V_{OS}$			10	25		30	75	$\mu\text{V}$
Long-Term Offset Voltage Stability	$\Delta V_{OS}/\text{Time}$			0.3			0.3		$\mu\text{V}/\text{Month}$
Input Offset Current	$I_{OS}$			30	100		30	150	pA
Input Bias Current	$I_B$			$\pm 30$	$\pm 100$		$\pm 30$	$\pm 150$	pA
Input Noise Voltage	$e_n$ p-p	0.1 Hz to 10 Hz		0.5			0.5		$\mu\text{V p-p}$
Input Noise Voltage Density	$e_n$	$f_O = 10\text{ Hz}^1$		17	30		17	30	$\text{nV}/\sqrt{\text{Hz}}$
		$f_O = 1000\text{ Hz}^2$		14	22		14	22	$\text{nV}/\sqrt{\text{Hz}}$
Input Noise Current Density	$i_n$	$f_O = 10\text{ Hz}$		20			20		$\text{fA}/\sqrt{\text{Hz}}$
Large-Signal Voltage Gain	$A_{VO}$	$V_O = \pm 10\text{ V}$ ; $R_L = 2\text{ k}\Omega$	300	2000		200	2000		V/mV
Common-Mode Rejection	CMR	$V_{CM} = \pm 13.5\text{ V}$	114	132		110	132		dB
Power-Supply Rejection	PSR	$V_S = \pm 2\text{ V to } \pm 20\text{ V}$	114	132		110	132		dB
Input Voltage Range <sup>3</sup>	IVR		$\pm 13.5$	$\pm 14.0$		$\pm 13.5$	$\pm 14.0$		V
Output Voltage Swing	$V_O$	$R_L = 10\text{ k}\Omega$	$\pm 13$	$\pm 14$		$\pm 13$	$\pm 14$		V
Slew Rate	SR		0.1	0.2		0.1	0.2		V/ $\mu\text{s}$
Differential Input Resistance <sup>4</sup>	$R_{IN}$		30			30			M $\Omega$
Closed-Loop Bandwidth	BW	$A_{VCL} = 1$	0.4	0.9		0.4	0.9		MHz
Supply Current	$I_{SY}$			380	600		380	600	$\mu\text{A}$
Supply Voltage	$V_S$	Operating Range	$\pm 2$	$\pm 15$	$\pm 20$	$\pm 2$	$\pm 15$	$\pm 20$	V

### NOTES

<sup>1</sup>10 Hz noise voltage density is sample tested. Devices 100% tested for noise are available on request.

<sup>2</sup>Sample tested.

<sup>3</sup>Guaranteed by CMR test.

<sup>4</sup>Guaranteed by design.

Specifications subject to change without notice.

## ELECTRICAL CHARACTERISTICS (@ $V_S = \pm 15\text{ V}$ , $V_{CM} = 0\text{ V}$ , $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ for the OP97E/F, unless otherwise noted.)

Parameter	Symbol	Conditions	OP97E			OP97F			Unit
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$V_{OS}$			25	60		60	200	$\mu\text{V}$
Average Temperature Coefficient of $V_{OS}$	$TCV_{OS}$	S-Package		0.2	0.6		0.3	2.0	$\mu\text{V}/^\circ\text{C}$
Input Offset Current	$I_{OS}$			60	250		80	750	pA
Average Temperature Coefficient of $I_{OS}$	$TCI_{OS}$			0.4	2.5		0.6	7.5	$\text{pA}/^\circ\text{C}$
Input Bias Current	$I_B$			$\pm 60$	$\pm 250$		$\pm 80$	$\pm 750$	pA
Average Temperature Coefficient of $I_B$	$TCI_B$			0.4	2.5		0.6	7.5	$\text{pA}/^\circ\text{C}$
Large Signal Voltage Gain	$A_{VO}$	$V_O = 10\text{ V}$ ; $R_L = 2\text{ k}\Omega$	200	1000		150	1000		V/mV
Common-Mode Rejection	CMR	$V_{CM} = \pm 13.5\text{ V}$	108	128		108	128		dB
Power Supply Rejection	PSR	$V_S = \pm 2.5\text{ V to } \pm 20\text{ V}$	108	126		108	128		dB
Input Voltage Range*	IVR		$\pm 13.5$	$\pm 14.0$		$\pm 13.5$	$\pm 14.0$		V
Output Voltage Swing	$V_O$	$R_L = 10\text{ k}\Omega$	$\pm 13$	$\pm 14$		$\pm 13$	$\pm 14$		V
Slew Rate	SR		0.05	0.15		0.05	0.15		V/ $\mu\text{s}$
Supply Current	$I_{SY}$			400	800		400	800	$\mu\text{A}$
Supply Voltage	$V_S$	Operating Range	$\pm 2.5$	$\pm 15$	$\pm 20$	$\pm 2.5$	$\pm 15$	$\pm 20$	V

\*Guaranteed by CMR test.

Specifications subject to change without notice.

**ABSOLUTE MAXIMUM RATINGS<sup>1</sup>**

Supply Voltage	±20 V
Input Voltage <sup>2</sup>	±20 V
Differential Input Voltage <sup>3</sup>	±1 V
Differential Input Current <sup>3</sup>	±10 mA
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	
OP97E, OP97F (P, S)	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

Package Type	$\theta_{JA}$ <sup>4</sup>	$\theta_{JC}$	Unit
8-Lead PDIP (P)	103	43	°C/W
8-Lead SOIC (S)	158	43	°C/W

**NOTES**

<sup>1</sup>Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

<sup>2</sup>For supply voltages less than ±20 V, the absolute maximum input voltage is equal to the supply voltage.

<sup>3</sup>The OP97's inputs are protected by back-to-back diodes. Current-limiting resistors are not used in order to achieve low noise. Differential input voltages greater than 1 V will cause excessive current to flow through the input protection diodes unless limiting resistance is used.

<sup>4</sup> $\theta_{JA}$  is specified for worst-case mounting conditions, i.e.,  $\theta_{JA}$  is specified for device in socket for PDIP package;  $\theta_{JA}$  is specified for device soldered to printed circuit board for SOIC package.

**ORDERING GUIDE**

Model	Temperature Range	Package Description	Package Option*
OP97EP	-40°C to +85°C	8-Lead PDIP	N-8
OP97FP	-40°C to +85°C	8-Lead PDIP	N-8
OP97FS	-40°C to +85°C	8-Lead SOIC	R-8
OP97FS-REEL	-40°C to +85°C	8-Lead SOIC	R-8
OP97FS-REEL7	-40°C to +85°C	8-Lead SOIC	R-8

\*For outline information, see Package Information section.

**CAUTION**

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the OP97 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

