

Features

- Single Power Supply Voltage, 2.3 ~ 3.6 V
- Power Down Features Using CE1#, CE2, LB# and UB#
- Low Power Dissipation
- Data retention Supply Voltage: 1.0V to 3.6V
- Direct TTL Compatibility for All Input and Output
- Wide Operating Temperature Range: -40°C to 85°C
- Standby current (maximum) @ VDD = 3.6 V

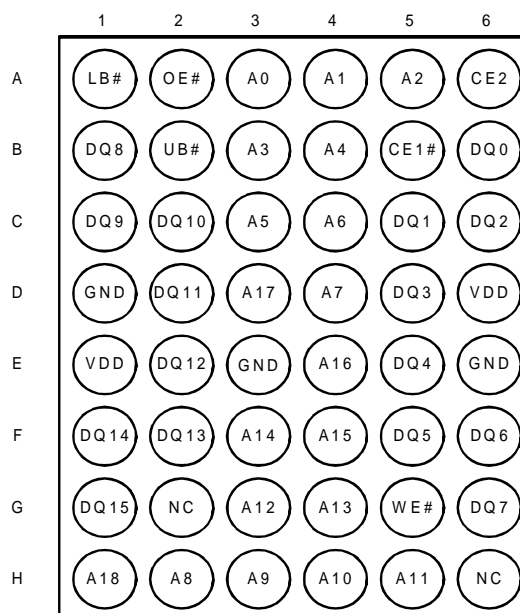
Part Number	IDD _{S2}	
	Typical	Maximum
EM565161BA/BJ-55	2 μA	35 μA
EM565161BA/BJ-70	2 μA	25 μA
EM565161BA/BJ-55E/70E	14 μA	80 μA

Ordering Information

Part Number	Speed	IDD _{S2}	Package
EM565161BJ-70	70 ns	25 μA	6x9 BGA
EM565161BA-70	70 ns	25 μA	8x10 BGA
EM565161BA-70E	70 ns	80 μA	8x10 BGA
EM565161BJ-55	55 ns	35 μA	6x9 BGA
EM565161BA-55	55 ns	35 μA	8x10 BGA
EM565161BA-55E	55 ns	80 μA	8x10 BGA

Pin Assignment

48-Ball BGA (CSP), Top View



Pin Names

Symbol	Function
A0 – A18	Address Inputs
DQ0-DQ15	Data Inputs/Outputs
CE1#,CE2	Chip Enable Input
OE#	Output Enable
WE#	Read/Write Control Input
LB#,UB#	Data Byte Control Inputs
GND	Ground
VDD	Power Supply
NC	No Connection

Overview

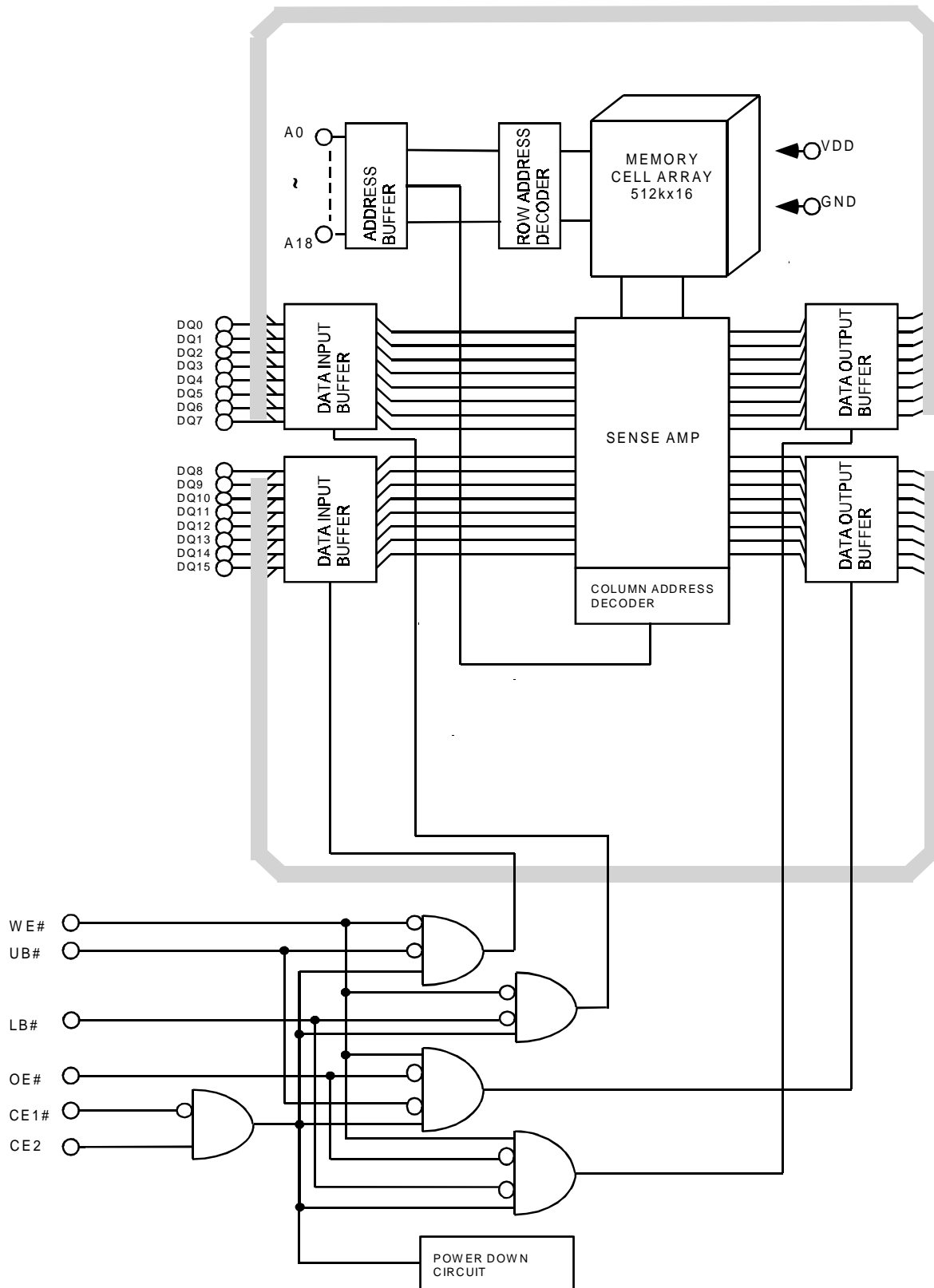
The EM565161 is an 8M-bit SRAM organized as 512K words by 16 bits. It is designed with advanced CMOS technology. This Device operates from a single power supply. Advanced circuit technology provides both high speed and low power. It is automatically placed in low-power mode when CE1# or both UB# and LB# are asserted high or CE2 is asserted low. There are three control inputs. CE1# and CE2 are used to select the device and for data retention control, and output enable (OE#) provides fast memory access. Data byte control pin (LB#,UB#) provides lower and upper byte access. This device is well suited to various microprocessor system applications where high speed, low power and battery backup are required. And, with a guaranteed operating range from -40°C to 85°C, the EM565161 can be used in environments exhibiting extreme temperature conditions.

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Block Diagram



Operating Mode

Mode	CE1#	CE2	OE#	WE#	LB#	UB#	DQ0~DQ7	DQ8~DQ15	Power
Read	L	H	L	H	L	L	D _{OUT}	D _{OUT}	I _{DDO}
					H	L	High-Z	D _{OUT}	I _{DDO}
					L	H	D _{OUT}	High-Z	I _{DDO}
Write	L	H	X	L	L	L	D _{IN}	D _{IN}	I _{DDO}
					H	L	High-Z	D _{IN}	I _{DDO}
					L	H	D _{IN}	High-Z	I _{DDO}
Output Disabled	L	H	H	H	X	X	High-Z	High-Z	I _{DDO}
	L	H	X	X	H	H	High-Z	High-Z	I _{DDO}
Standby	H	X	X	X	X	X	High-Z	High-Z	I _{DDS}
	X	L	X	X	X	X			
	X	X	X	X	H	H			

Note: X=don't care. H=logic high. L=logic low.

Absolute Maximum Ratings

Supply voltage, V _{DD}	-0.3 to +4.6V
Input voltages, V _{IN}	-0.3 to +4.6V
Input and output voltages, V _{I/O}	-0.5 to V _{DD} +0.5V
Operating temperature, T _{OPR}	-40 to +85°C
Storage temperature, T _{STRG}	-55 to +150°C
Soldering Temperature (10s), T _{SOLDER}	240°C
Power dissipation, P _D	1 W

DC Recommended Operating Conditions (Ta=-40°C to 85°C)

Symbol	Parameter	Min	Typ	Max	Unit
V _{DD}	Power Supply Voltage	2.3	3.0	3.6	V
V _{IH}	Input High Voltage	2.2	-	V _{DD} + 0.3 ⁽¹⁾	
V _{IL}	Input Low Voltage	-0.3 ⁽²⁾	-	0.6	
V _{DR}	Data Retention Supply Voltage	1.0	-	3.6	

Note:

(1) Overshoot : V_{DD} +2.0V in case of pulse width ≤ 20ns

(2) Undershoot : -2.0V in case of pulse width ≤ 20ns

DC Characteristics (Ta = -40°C to 85°C, V_{DD} = 2.3V to 3.6V)

Parameter	Symbol	Test Conditions	Min	Typ*	Max	Unit	
Input low current	I _{IL}	I _{IN} = 0V to V _{DD}	-1	-	1	μA	
Output low voltage	V _{OL}	I _{OL} = 2.1 mA	-	-	0.4	V	
Output high voltage	V _{OH}	I _{OH} = -1.0 mA	V _{DD} - 0.15	-	-	V	
Operating current	I _{DD1}	CE1# = V _{IL} and CE2 = V _{IH} and I _{OUT} = 0mA Other Input = V _{IH} / V _{IL}	Cycle time = min	-	12	35	mA
	I _{DD2}		Cycle time = 1μs	-	-	5	
Standby current	I _{DDS1}	CE1# = V _{IH} or CE2 = V _{IL}		-	-	0.3	mA
	I _{DDS2}	CE1# = V _{DD} - 0.2V or UB# and LB# = V _{DD} -0.2V or CE2 = 0.2V	-55	-	2	35	
			-70	-	2	25	
			-55E/70E	-	14	80	

Notes:

* Typical value are measured at T_a = 25°C.

Capacitance (Ta = 25°C; f = 1 MHz)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Input capacitance	C _{IN}	-	8	pF	V _{IN} = GND
Input/Output capacitance	C _{IO}	-	10	pF	V _{IO} = GND

Notes: This parameter is periodically sampled and is not 100% tested.

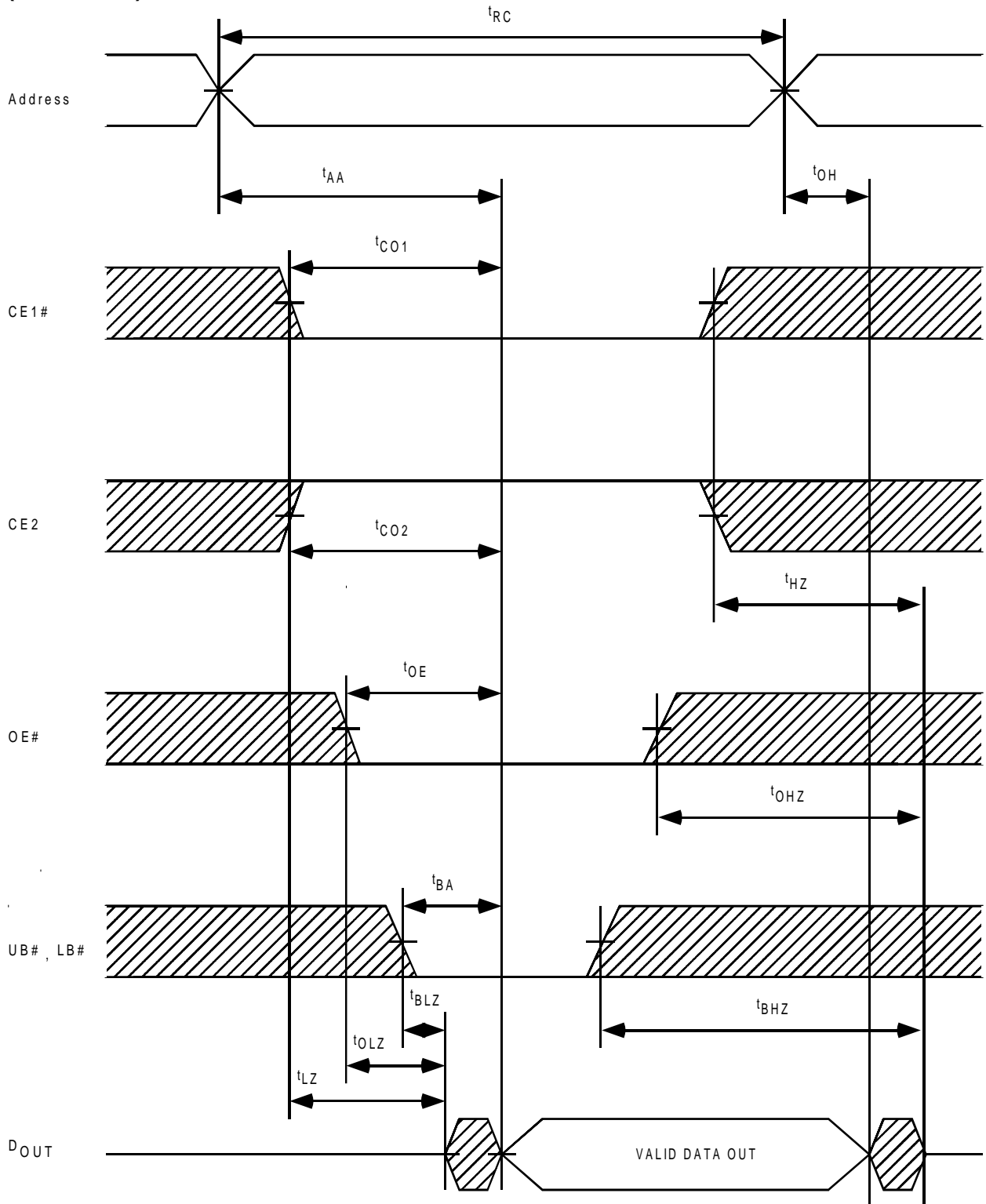
AC Characteristics and Operating Conditions (Ta = -40°C to 85°C, VDD = 2.3V to 3.6V)

Read Cycle						
Symbol	Parameter	EM565161				Unit
		-55		-70		
		Min	Max	Min	Max	
t _{RC}	Read cycle time	55	–	70	–	ns
t _{AA}	Address access time	–	55	–	70	
t _{CO1}	Chip Enable (CE1#) Access Time	–	55	–	70	
t _{CO2}	Chip Enable (CE2) Access Time	–	55	–	70	
t _{OE}	Output enable access time	–	25	–	35	
t _{BA}	Data Byte Control Access Time	–	55	–	70	
t _{LZ}	Chip Enable Low to Output in Low-Z	10	–	10	–	
t _{OLZ}	Output enable Low to Output in Low-Z	5	–	5	–	
t _{BLZ}	Data Byte Control Low to Output in Low-Z	10	–	10	–	
t _{HZ}	Chip Enable High to Output in High-Z	–	20	–	25	
t _{OHZ}	Output Enable High to Output in High-Z	–	20	–	25	
t _{BHZ}	Data Byte Control High to Output in High-Z	–	20	–	25	
t _{OH}	Output Data Hold Time	10	–	10	–	
Write Cycle						
Symbol	Parameter	EM565161				Unit
		-55		-70		
		Min	Max	Min	Max	
t _{WC}	Write cycle time	55	–	70	–	ns
t _{WP}	Write pulse width	45	–	55	–	
t _{CW}	Chip Enable to end of write	45	–	60	–	
t _{BW}	Data Byte Control to end of Write	45	–	60	–	
t _{AS}	Address setup time	0	–	0	–	
t _{WR}	Write Recovery time	0	–	0	–	
t _{WHZ}	WE# Low to Output in High-Z	–	20	–	20	
t _{OW}	WE# High to Output in Low-Z	5	–	5	–	
t _{DS}	Data Setup Time	25	–	30	–	
t _{DH}	Data Hold Time	0	–	0	–	

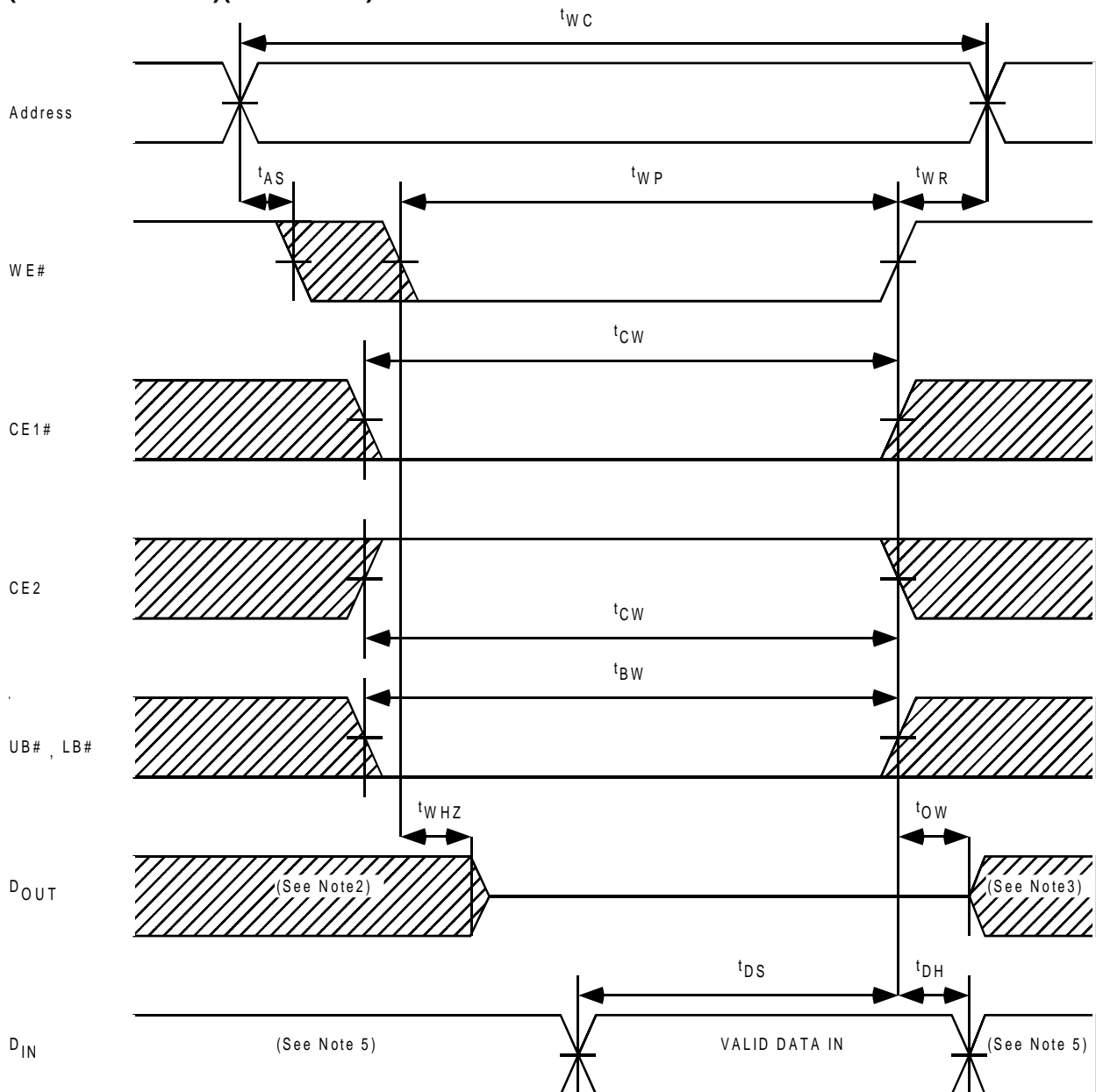
AC Test Condition

- Output load : 60pF + one TTL gate
- Input pulse level : 0.4V, 2.4V
- Timing measurements : 0.5 x VDD
- t_R, t_F : 5ns

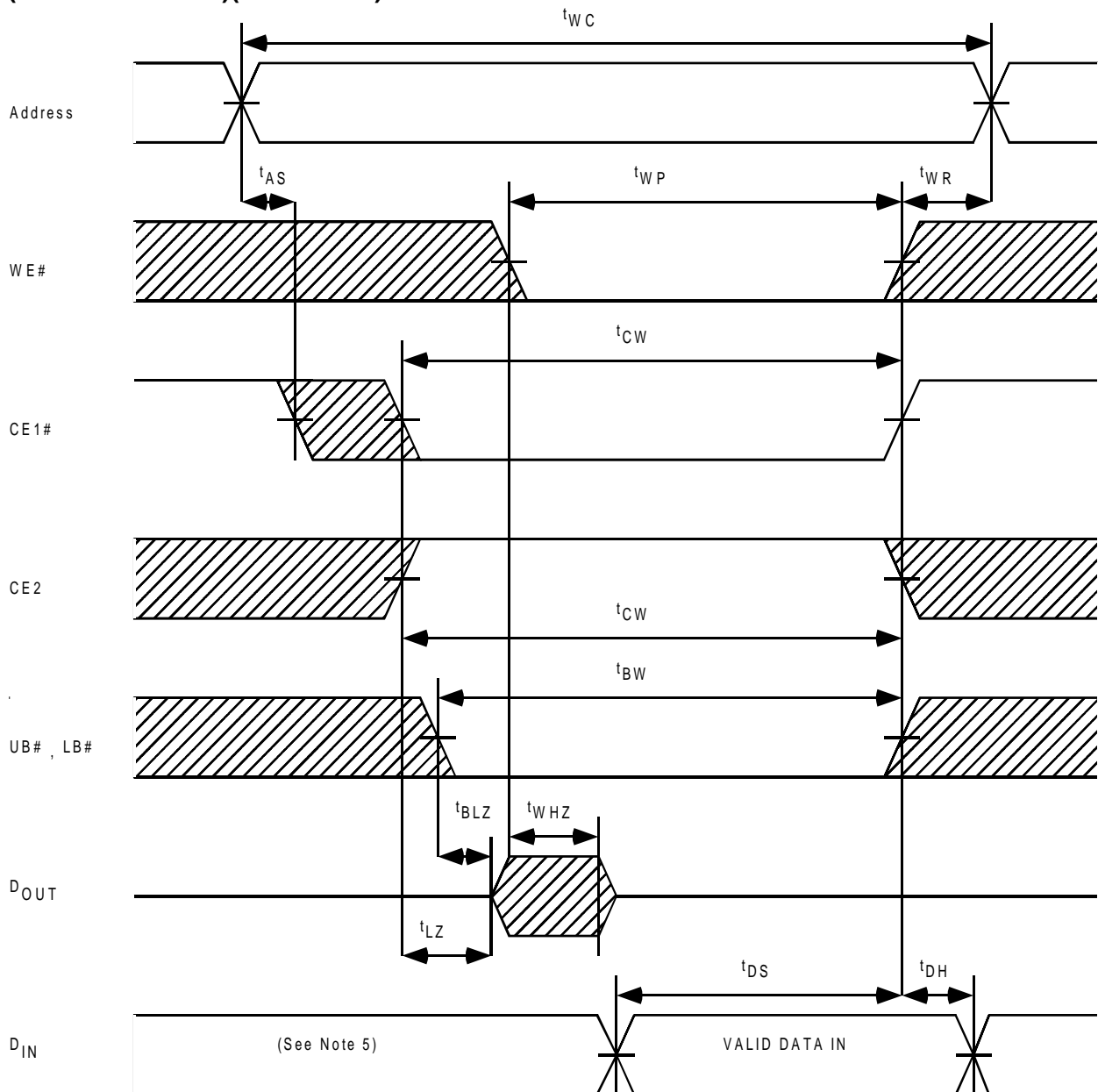
Read Cycle (See Note 1)



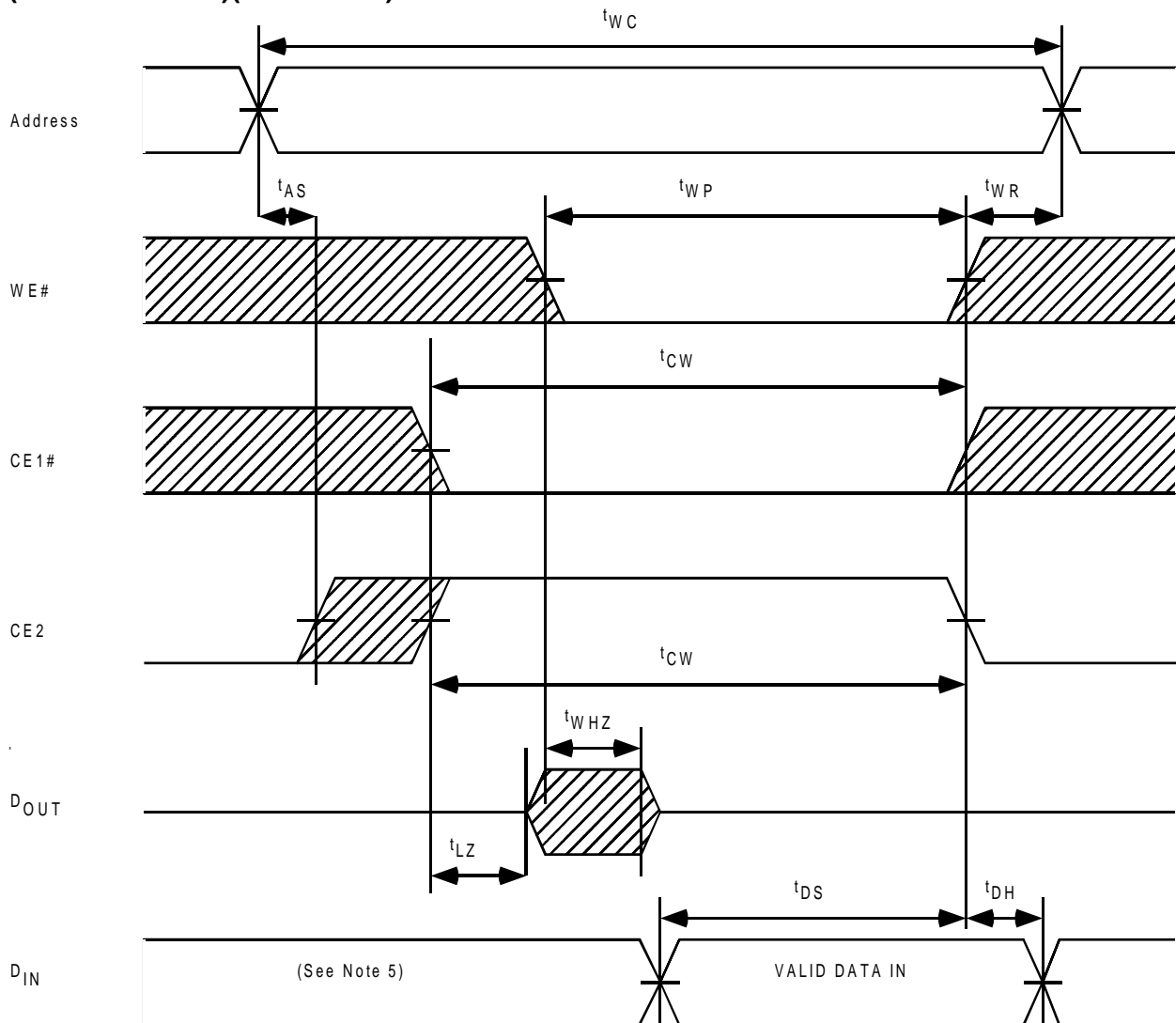
Write Cycle1 (WE# Controlled)(See Note 4)



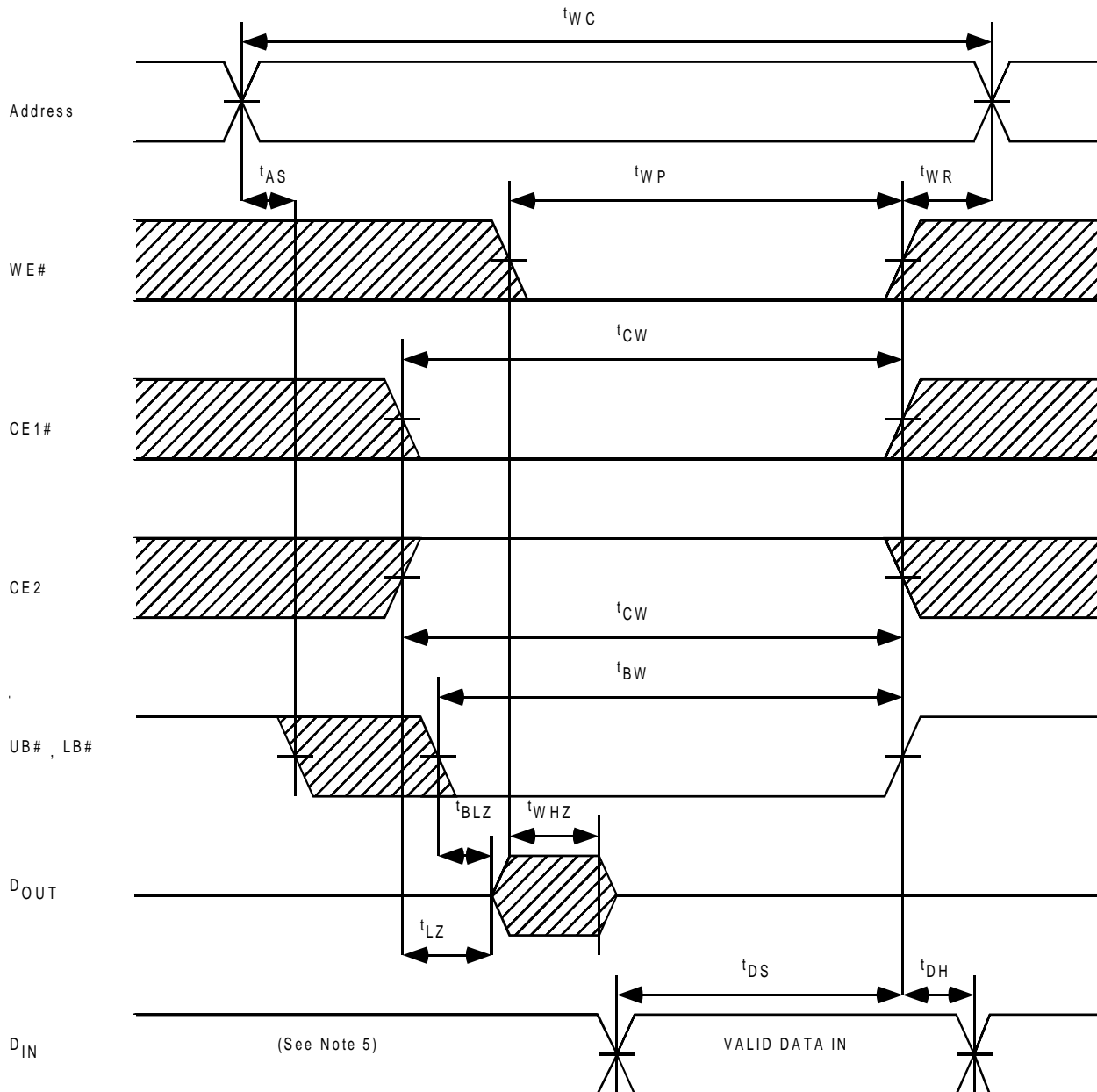
Write Cycle 2 (CE1# Controlled)(See Note 4)



Write Cycle 3 (CE2 Controlled)(See Note 4)



Write Cycle4 (UB#, LB# Controlled)(See Note 4)



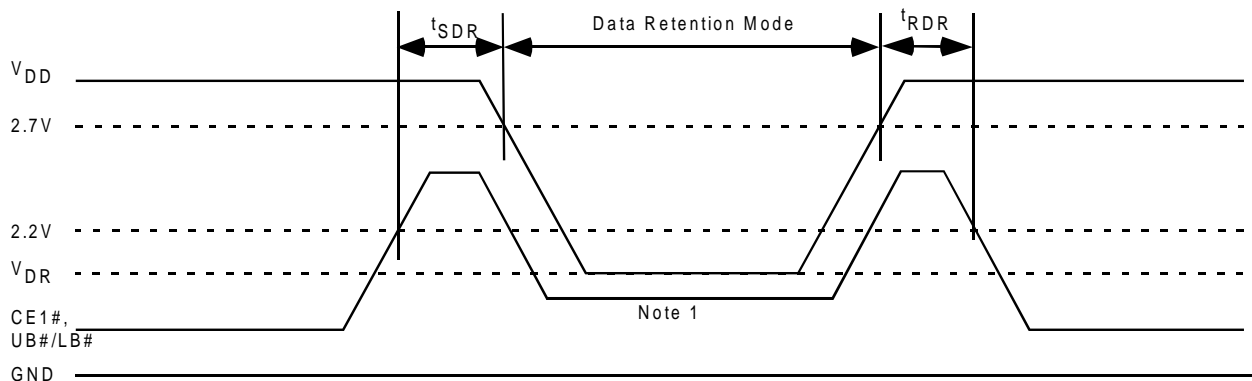
Note:

1. $WE\#$ remains HIGH for the read cycle.
2. If $CE1\#$ goes LOW (or $CE2$ goes HIGH) with or after $WE\#$ goes LOW, the outputs will remain at high impedance.
3. If $CE1\#$ goes HIGH (or $CE2$ goes LOW) coincident with or before $WE\#$ goes HIGH, the outputs will remain at high impedance.
4. If $OE\#$ is HIGH during the write cycle, the outputs will remain at high impedance.
5. Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

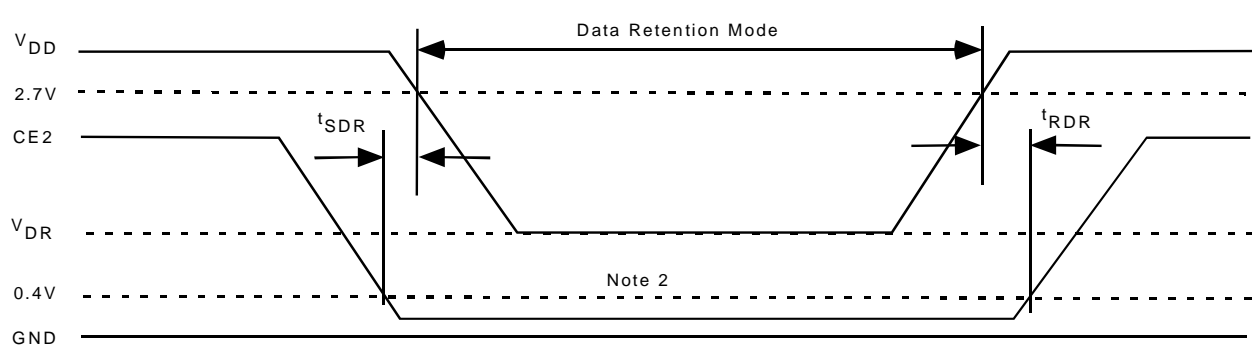
Data Retention Characteristics (Ta = -40°C to 85°C)

Symbol	Parameter		Min	Typ	Max	Unit
V _{DR}	Data Retention Supply Voltage	CE1# ≥ V _{DD} - 0.2V or UB# = LB# ≥ V _{DD} - 0.2V or CE2 ≤ 0.2V, VIN ≥ V _{DD} - 0.2V or VIN ≤ 0.2V	1.0	-	3.6	V
t _{SDR}	Chip Deselect to Data Retention Mode Time		0	-	-	ns
t _{RDR}	Recovery Time		t _{RC}	-	-	ns

CE1# or UB#/LB# Controlled Data Retention Mode



CE2 Controlled Data Retention Mode



Note:

1. CE1# ≥ V_{DD} - 0.2V or UB# = LB# ≥ V_{DD} - 0.2V
2. CE2 ≤ 0.2V

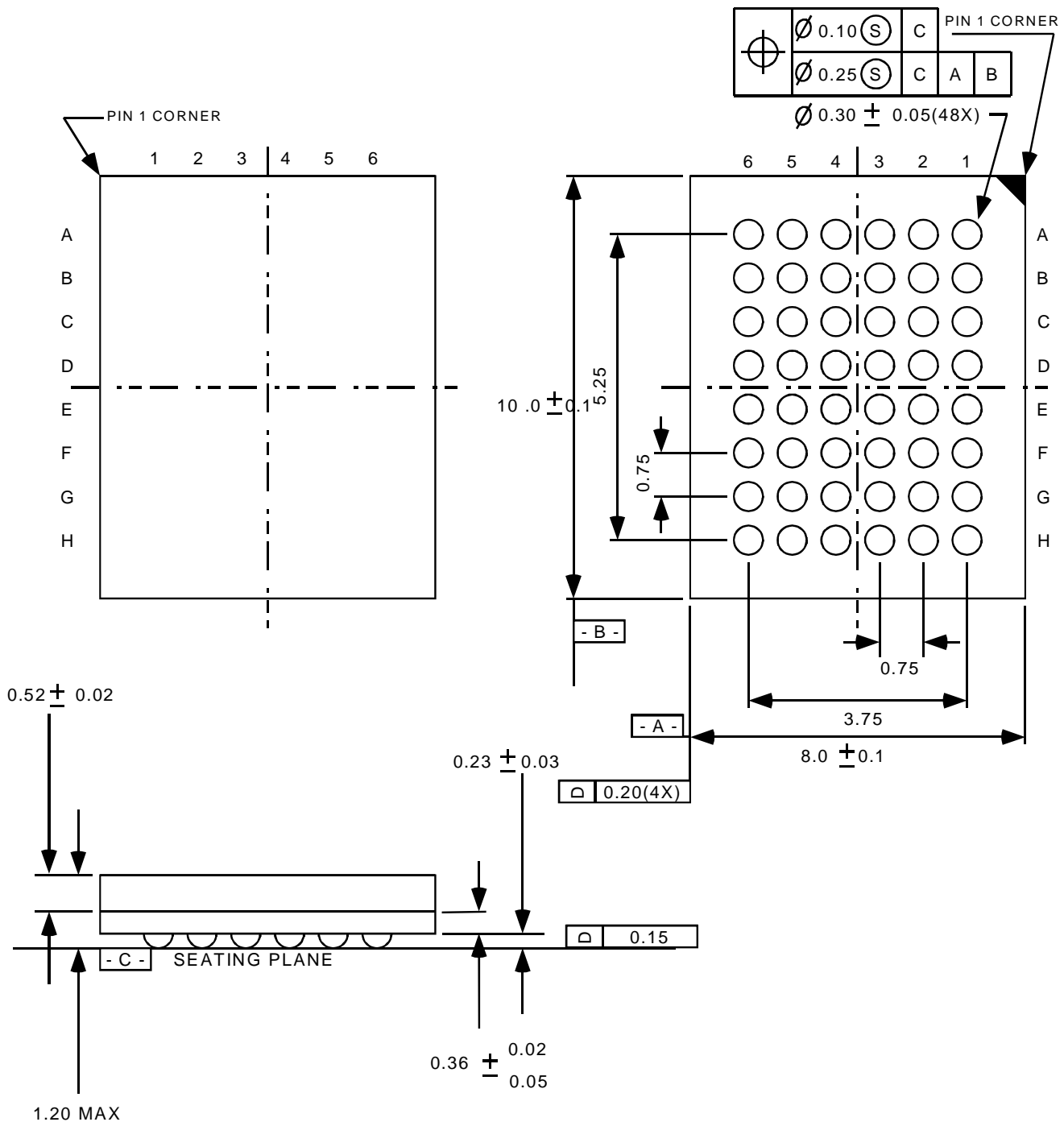
Package Diagrams

48-Ball (8mm x 10mm) BGA

Units in mm

TOP VIEW

BOTTOM VIEW



Package Diagrams
48-Ball (6mm x 9mm) BGA
Units in mm

