



**P-Channel Enhancement-Mode Vertical DMOS FETs**

**Ordering Information**

BV <sub>DSS</sub> / BV <sub>DGS</sub>	R <sub>DS(ON)</sub> (max)	V <sub>GS(th)</sub> (max)	I <sub>D(ON)</sub> (min)	Order Number / Package	
				TO-243AA*	Die†
-20V	2.0Ω	-2.4V	-2.0A	TP2502N8	TP2502ND

\* Same as SOT-89. Product supplied on 2000 piece carrier tape reels.

† MIL visual screening available.

**Product marking for TO-243AA**

**TP5L\***

Where \* = 2-week alpha date code

**Features**

- Low threshold — -2.4V max.
- High input impedance
- Low input capacitance — 125pF max.
- Fast switching speeds
- Low on resistance
- Free from secondary breakdown
- Low input and output leakage
- Complementary N- and P-channel devices

**Applications**

- Logic level interfaces – ideal for TTL and CMOS
- Solid state relays
- Battery operated systems
- Photo voltaic drives
- Analog switches
- General purpose line drivers
- Telecom switches

**Absolute Maximum Ratings**

Drain-to-Source Voltage	BV <sub>DSS</sub>
Drain-to-Gate Voltage	BV <sub>DGS</sub>
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

\* Distance of 1.6 mm from case for 10 seconds.

**Low Threshold DMOS Technology**

These low threshold enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

**Package Option**

**TO-243AA  
(SOT-89)**

Note: See Package Outline section for dimensions.

11/12/01

Supertex Inc. does not recommend the use of its products in life support applications and will not knowingly sell its products for use in such applications unless it receives an adequate "products liability indemnification insurance agreement." Supertex does not assume responsibility for use of devices described and limits its liability to the replacement of devices determined to be defective due to workmanship. No responsibility is assumed for possible omissions or inaccuracies. Circuitry and specifications are subject to change without notice. For the latest product specifications, refer to the Supertex website: <http://www.supertex.com>. For complete liability information on all Supertex products, refer to the most current databook or to the Legal/Disclaimer page on the Supertex website.

## Thermal Characteristics

Package	$I_D$ (continuous)*	$I_D$ (pulsed)	Power Dissipation @ $T_A = 25^\circ\text{C}$	$\theta_{jc}$ $^\circ\text{C/W}$	$\theta_{ja}$ $^\circ\text{C/W}$	$I_{DR}^*$	$I_{DRM}$
TO-243AA	-630mA	-3.3A	1.6W <sup>†</sup>	15	78 <sup>†</sup>	-630mA	-3.3A

\*  $I_D$  (continuous) is limited by max rated  $T_j$ .

<sup>†</sup> Mounted on FR5 board, 25mm x 25mm x 1.57mm. Significant  $P_D$  increase possible on ceramic substrate.

## Electrical Characteristics (@ 25°C unless otherwise specified)

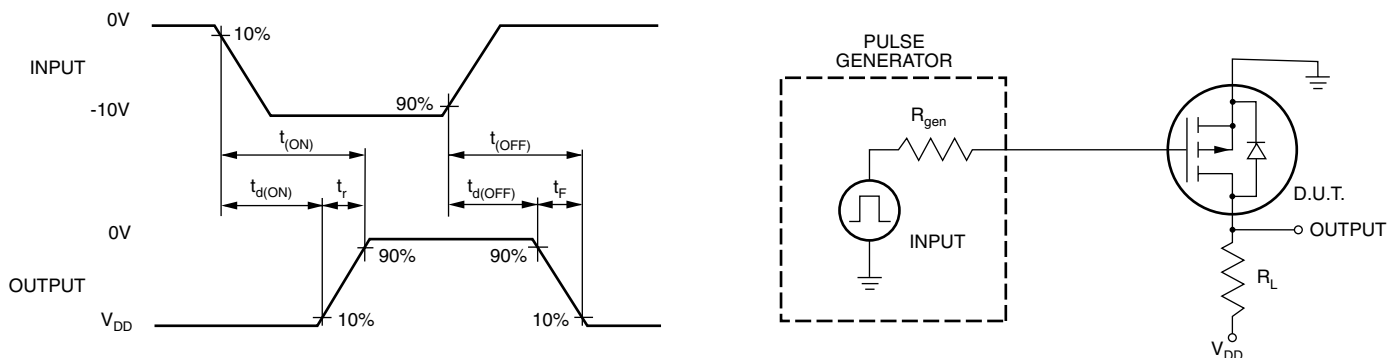
Symbol	Parameter	Min	Typ	Max	Unit	Conditions
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	-20			V	$V_{GS} = 0V, I_D = -2.0mA$
$V_{GS(th)}$	Gate Threshold Voltage	-1.0		-2.4	V	$V_{GS} = V_{DS}, I_D = -1.0mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature		3.0	4.5	mV/ $^\circ\text{C}$	$V_{GS} = V_{DS}, I_D = -1.0mA$
$I_{GSS}$	Gate Body Leakage			-100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
$I_{DSS}$	Zero Gate Voltage Drain Current			-100	$\mu\text{A}$	$V_{GS} = 0V, V_{DS} = \text{Max Rating}$
				-10	mA	$V_{GS} = 0V, V_{DS} = 0.8 \text{ Max Rating}$ $T_A = 125^\circ\text{C}$
$I_{D(ON)}$	ON-State Drain Current	-0.4	-0.7		A	$V_{GS} = -5.0V, V_{DS} = -15V$
		-2.0	-3.3			$V_{GS} = -10V, V_{DS} = -15V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance		2.0	3.5	$\Omega$	$V_{GS} = -5.0V, I_D = -250mA$
			1.5	2.0		$V_{GS} = -10V, I_D = -1.0A$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature		0.75	1.2	%/ $^\circ\text{C}$	$V_{GS} = -10V, I_D = -1.0A$
$G_{FS}$	Forward Transconductance	0.3	0.65		$\text{S}$	$V_{DS} = -15V, I_D = -1.0A$
$C_{ISS}$	Input Capacitance			125	pF	$V_{GS} = 0V, V_{DS} = -20V$ $f = 1.0 \text{ MHz}$
$C_{OSS}$	Common Source Output Capacitance			70		
$C_{RSS}$	Reverse Transfer Capacitance			25		
$t_{d(ON)}$	Turn-ON Delay Time			10	ns	$V_{DD} = -20V,$ $I_D = -1.0A,$ $R_{GEN} = 25\Omega$
$t_r$	Rise Time			11		
$t_{d(OFF)}$	Turn-OFF Delay Time			15		
$t_f$	Fall Time			12		
$V_{SD}$	Diode Forward Voltage Drop		-1.3	-2.0	V	$V_{GS} = 0V, I_{SD} = -1.5A$
$t_{rr}$	Reverse Recovery Time		300		ns	$V_{GS} = 0V, I_{SD} = -1.5A$

### Notes:

1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300 $\mu\text{s}$  pulse, 2% duty cycle.)

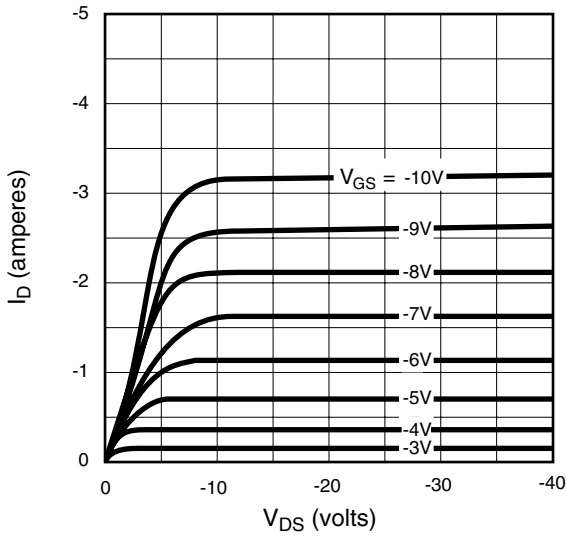
2. All A.C. parameters sample tested.

## Switching Waveforms and Test Circuit

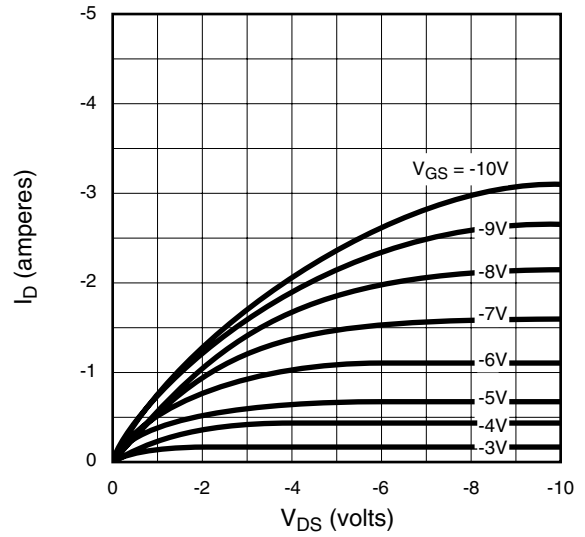


# Typical Performance Curves

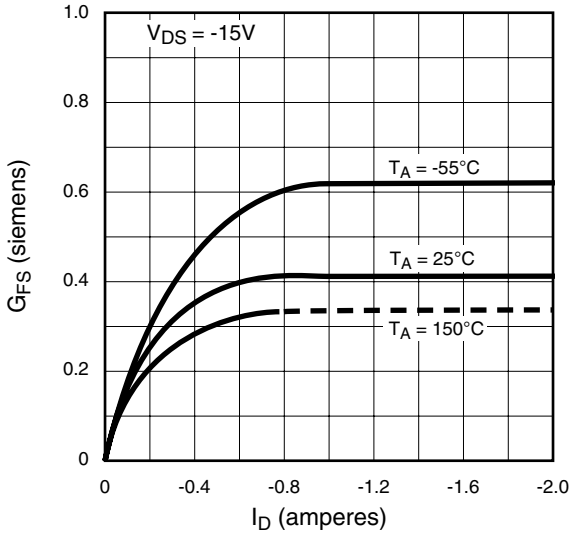
Output Characteristics



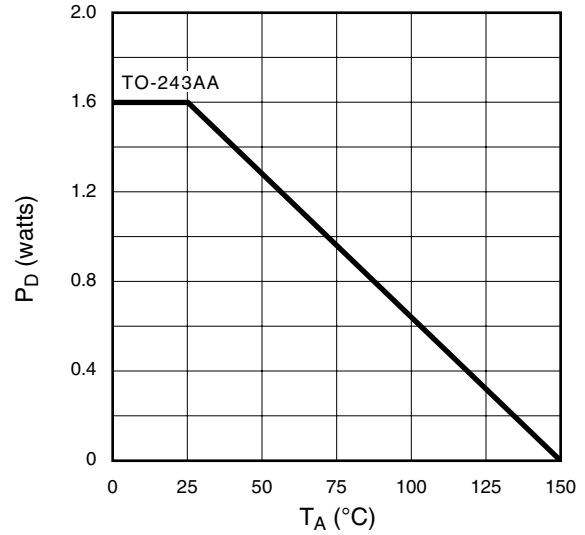
Saturation Characteristics



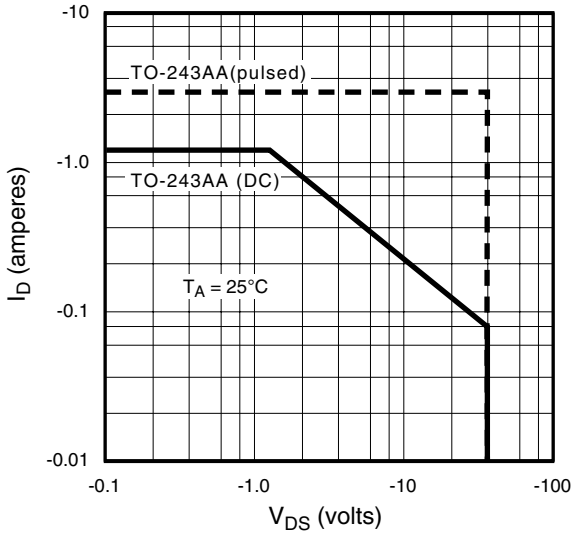
Transconductance vs. Drain Current



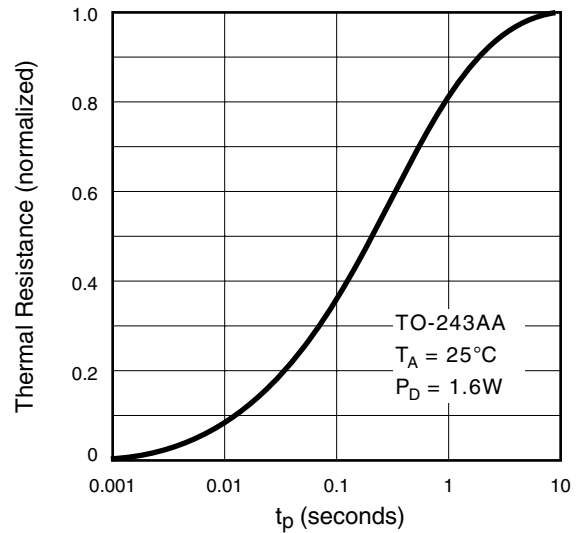
Power Dissipation vs. Ambient Temperature



Maximum Rated Safe Operating Area



Thermal Response Characteristics



# Typical Performance Curves

