80960CA-33, -25, -16

32-BIT HIGH-PERFORMANCE EMBEDDED PROCESSOR

- *Two Instructions/Clock Sustained Execution*
- *Four 59 Mbytes/s DMA Channels with Data Chaining*
- *Demultiplexed 32-bit Burst Bus with Pipelining*

- **32-bit Parallel Architecture**
  - **Two Instructions/clock Execution**
  - **Load/Store Architecture**
  - **Sixteen 32-bit Global Registers**
  - **Sixteen 32-bit Local Registers**
  - **Manipulates 64-bit Bit Fields**
  - **11 Addressing Modes**
  - **Full Parallel Fault Model**
  - **Supervisor Protection Model**
- **Fast Procedure Call/Return Model**
  - **Full Procedure Call in 4 Clocks**
- **On-Chip Register Cache**
  - **Caches Registers on Call/Ret**
  - **Minimum of 6 Frames Provided**
  - **Up to 15 Programmable Frames**
- **On-Chip Instruction Cache**
  - **1 Kbyte Two-Way Set Associative**
  - **128-bit Path to Instruction Sequencer**
  - **Cache-Lock Modes**
  - **Cache-Off Mode**
- **High Bandwidth On-Chip Data RAM**
  - **1 Kbyte On-Chip Data RAM**
  - **Sustains 128 bits per Clock Access**
- **Four On-Chip DMA Channels**
  - **59 Mbytes/s Fly-by Transfers**
  - **32 Mbytes/s Two-Cycle Transfers**
  - **Data Chaining**
  - **Data Packing/Unpacking**
  - **Programmable Priority Method**
- **32-Bit Demultiplexed Burst Bus**
  - **128-bit Internal Data Paths to *and* from Registers**
  - **Burst Bus for DRAM Interfacing**
  - **Address Pipelining Option**
  - **Fully Programmable Wait States**
  - **Supports 8-, 16- or 32-bit Bus Widths**
  - **Supports Unaligned Accesses**
  - **Supervisor Protection Pin**
- **Selectable Big or Little Endian Byte Ordering**
- **High-Speed Interrupt Controller**
  - **Up to 248 External Interrupts**
  - **32 Fully Programmable Priorities**
  - **Multi-mode 8-bit Interrupt Port**
  - **Four Internal DMA Interrupts**
  - **Separate, Non-maskable Interrupt Pin**
  - **Context Switch in 750 ns Typical**

November 1993 **Order Number: 270727-006**

80960CA-33, -25, -16
32-BIT HIGH-PERFORMANCE EMBEDDED PROCESSOR

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1.0 PURPOSE

This document provides electrical characteristics for the 33, 25 and 16 MHz versions of the 80960CA. For a detailed description of any 80960CA functional topic—other than parametric performance—consult the *80960CA Product Overview* (Order No. 270669) or the *i960® CA Microprocessor User's Manual* (Order No. 270710). To obtain data sheet updates and errata, please call Intel's FaxBACK® data-on-demand system (1-800-628-2283 or 916-356-3105). Other information can be obtained from Intel's technical BBS (916-356-3600).

2.0 80960CA OVERVIEW

The 80960CA is the second-generation member of the 80960 family of embedded processors. The 80960CA is object code compatible with the 32-bit 80960 Core Architecture while including Special Function Register extensions to control on-chip peripherals and instruction set extensions to shift 64-bit operands and configure on-chip hardware. Multiple 128-bit internal buses, on-chip instruction caching and a sophisticated instruction scheduler allow the processor to sustain execution of two instructions every clock and peak at execution of three instructions per clock.

A 32-bit demultiplexed and pipelined burst bus provides a 132 Mbyte/s bandwidth to a system's high-speed external memory sub-system. In addition, the 80960CA's on-chip caching of instructions, procedure context and critical program data substantially decouple system performance from the wait states associated with accesses to the system's slower, cost sensitive, main memory subsystem.

The 80960CA bus controller integrates full wait state and bus width control for highest system performance with minimal system design complexity. Unaligned access and Big Endian byte order support reduces the cost of porting existing applications to the 80960CA.

The processor also integrates four complete data-chaining DMA channels and a high-speed interrupt controller on-chip. DMA channels perform: single-cycle or two-cycle transfers, data packing and unpacking and data chaining. Block transfers—in addition to source or destination synchronized transfers—are provided.

The interrupt controller provides full programmability of 248 interrupt sources into 32 priority levels with a typical interrupt task switch ("latency") time of 750 ns.

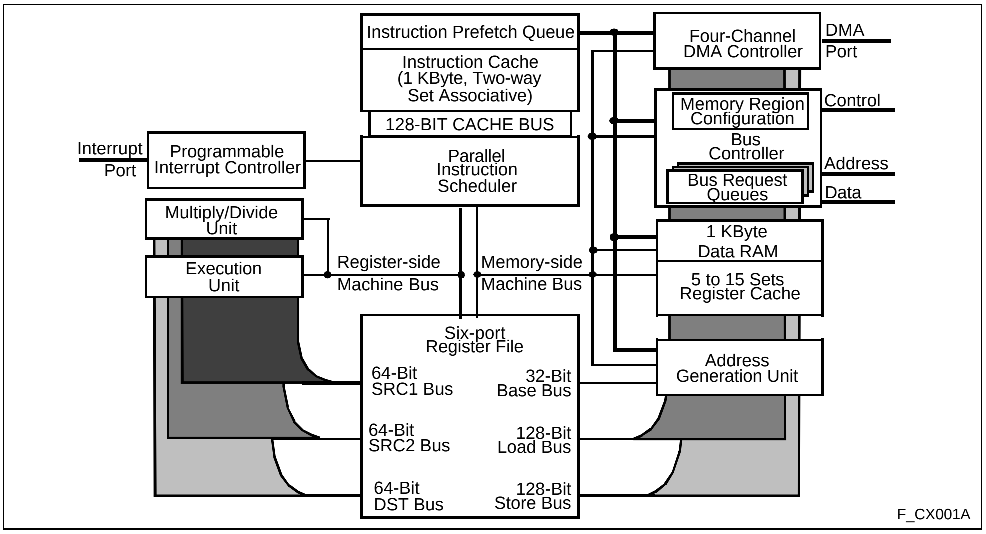


Figure 1. 80960CA Block Diagram

2.1 The C-Series Core

The C-Series core is a very high performance microarchitectural implementation of the 80960 Core Architecture. The C-Series core can sustain execution of two instructions per clock (66 MIPs at 33 MHz). To achieve this level of performance, Intel has incorporated state-of-the-art silicon technology and innovative microarchitectural constructs into the implementation of the C-Series core. Factors that contribute to the core's performance include:

- Parallel instruction decoding allows issuance of up to three instructions per clock
- Single-clock execution of most instructions
- Parallel instruction decode allows sustained, simultaneous execution of two single-clock instructions every clock cycle
- Efficient instruction pipeline minimizes pipeline break losses
- Register and resource scoreboarding allow simultaneous multi-clock instruction execution
- Branch look-ahead and prediction allows many branches to execute with no pipeline break
- Local Register Cache integrated on-chip caches Call/Return context
- Two-way set associative, 1 Kbyte integrated instruction cache
- 1 Kbyte integrated Data RAM sustains a four-word (128-bit) access every clock cycle

2.2 Pipelined, Burst Bus

A 32-bit high performance bus controller interfaces the 80960CA to external memory and peripherals. The Bus Control Unit features a maximum transfer rate of 132 Mbytes per second (at 33 MHz). Internally programmable wait states and 16 separately configurable memory regions allow the processor to interface with a variety of memory subsystems with a minimum of system complexity and a maximum of performance. The Bus Controller's main features include:

- Demultiplexed, Burst Bus to exploit most efficient DRAM access modes
- Address Pipelining to reduce memory cost while maintaining performance
- 32-, 16- and 8-bit modes for I/O interfacing ease
- Full internal wait state generation to reduce system cost
- Little and Big Endian support to ease application development
- Unaligned access support for code portability
- Three-deep request queue to decouple the bus from the core

2.3 Flexible DMA Controller

A four-channel DMA controller provides high speed DMA control for data transfers involving peripherals and memory. The DMA provides advanced features such as data chaining, byte assembly and disassembly and a high performance fly-by mode capable of transfer speeds of up to 59 Mbytes per second at 33 MHz. The DMA controller features a performance and flexibility which is only possible by integrating the DMA controller and the 80960CA core.

2.4 Priority Interrupt Controller

A programmable-priority interrupt controller manages up to 248 external sources through the 8-bit external interrupt port. The Interrupt Unit also handles the four internal sources from the DMA controller and a single non-maskable interrupt input. The 8-bit interrupt port can also be configured to provide individual interrupt sources that are level or edge triggered.

Interrupts in the 80960CA are prioritized and signaled within 270 ns of the request. If the interrupt is of higher priority than the processor priority, the context switch to the interrupt routine typically is complete in another 480 ns. The interrupt unit provides the mechanism for the low latency and high throughput interrupt service which is essential for embedded applications.

2.5 Instruction Set Summary

Table 1 summarizes the 80960CA instruction set by logical groupings. See the *i960® CA Microprocessor User's Manual* for a complete description of the instruction set.

Table 1. 80960CA Instruction Set

Data Movement	Arithmetic	Logical	Bit and Bit Field and Byte
Load Store Move Load Address	Add Subtract Multiply Divide Remainder Modulo Shift *Extended Shift Extended Multiply Extended Divide Add with Carry Subtract with Carry Rotate	And Not And And Not Or Exclusive Or Not Or Or Not Nor Exclusive Nor Not Nand	Set Bit Clear Bit Not Bit Alter Bit Scan For Bit Span Over Bit Extract Modify Scan Byte for Equal
Comparison	**Branch**	**Call/Return**	**Fault**
Compare Conditional Compare Compare and Increment Compare and Decrement Test Condition Code Check Bit	Unconditional Branch Conditional Branch Compare and Branch	Call Call Extended Call System Return Branch and Link	Conditional Fault Synchronize Faults
Debug	**Processor Management**	**Atomic**	
Modify Trace Controls Mark Force Mark	Flush Local Registers Modify Arithmetic Controls Modify Process Controls *System Control *DMA Control	Atomic Add Atomic Modify	

NOTES:
Instructions marked by (*) are 80960CA extensions to the 80960 instruction set.

3.0 PACKAGE INFORMATION

3.1 Package Introduction

This section describes the pins, pinouts and thermal characteristics for the 80960CA in the 168-pin Ceramic Pin Grid Array (PGA) package and the 196-pin Plastic Quad Flat Package (PQFP). For complete package specifications and information, see the *Packaging* Handbook (Order No. 240800).

3.2 Pin Descriptions

The 80960CA pins are described in this section. Table 2 presents the legend for interpreting the pin descriptions in the following tables. Pins associated with the 32-bit demultiplexed processor bus are described in Table 3. Pins associated with basic processor configuration and control are described in Table 4. Pins associated with the 80960CA DMA Controller and Interrupt Unit are described in Table 5.

All pins float while the processor is in the ONCE mode.

Table 2. Pin Description Nomenclature

Symbol	Description
I	Input only pin
O	Output only pin
I/O	Pin can be either an input or output
–	Pins “must be” connected as described
S(...)	Synchronous. Inputs must meet setup and hold times relative to PCLK2:1 for proper operation. All outputs are synchronous to PCLK2:1. S(E) Edge sensitive input S(L) Level sensitive input
A(...)	Asynchronous. Inputs may be asynchronous to PCLK2:1. A(E) Edge sensitive input A(L) Level sensitive input
H(...)	While the processor’s bus is in the Hold Acknowledge or Bus Backoff state, the pin: H(1) is driven to V_{CC} H(0) is driven to V_{SS} H(Z) floats H(Q) continues to be a valid input
R(...)	While the processor’s $\overline{\text{RESET}}$ pin is low, the pin: R(1) is driven to V_{CC} R(0) is driven to V_{SS} R(Z) floats R(Q) continues to be a valid output

Table 3. 80960CA Pin Description — External Bus Signals (Sheet 1 of 3)

Name	Type	Description
A31:2	**O** S H(Z) R(Z)	**ADDRESS BUS** carries the physical address' upper 30 bits. A31 is the most significant address bit; A2 is the least significant. During a bus access, A31:2 identify all external addresses to word (4-byte) boundaries. The byte enable signals indicate the selected byte in each word. During burst accesses, A3:2 increment to indicate successive data cycles.
D31:0	**I/O** S(L) H(Z) R(Z)	**DATA BUS** carries 32-, 16- or 8-bit data quantities depending on bus width configuration. The least significant bit of the data is carried on D0 and the most significant on D31. When the bus is configured for 8-bit data, the lower 8 data lines, D7:0 are used. For 16-bit data bus widths, D15:0 are used. For 32-bit bus widths the full data bus is used.
$\overline{\text{BE3:0}}$	**O** S H(Z) R(1)	**BYTE ENABLES** select which of the four bytes addressed by A31:2 are active during an access to a memory region configured for a 32-bit data-bus width. $\overline{\text{BE3}}$ applies to D31:24; $\overline{\text{BE2}}$ applies to D23:16; $\overline{\text{BE1}}$ applies to D15:8 $\overline{\text{BE0}}$ applies to D7:0. 32-bit bus: $\overline{\text{BE3}}$ –Byte Enable 3 –enable D31:24 $\overline{\text{BE2}}$ –Byte Enable 2 –enable D23:16 $\overline{\text{BE1}}$ –Byte Enable 1 –enable D15:8 $\overline{\text{BE0}}$ –Byte Enable 0 –enable D7:0 For accesses to a memory region configured for a 16-bit data-bus width, the processor uses the $\overline{\text{BE3}}$, $\overline{\text{BE1}}$ and $\overline{\text{BE0}}$ pins as $\overline{\text{BHE}}$, A1 and $\overline{\text{BLE}}$ respectively. 16-bit bus: $\overline{\text{BE3}}$ –Byte High Enable ($\overline{\text{BHE}}$) –enable D15:8 $\overline{\text{BE2}}$ –Not used (driven high or low) $\overline{\text{BE1}}$ –Address Bit 1 (A1) $\overline{\text{BE0}}$ –Byte Low Enable ($\overline{\text{BLE}}$) –enable D7:0 For accesses to a memory region configured for an 8-bit data-bus width, the processor uses the $\overline{\text{BE1}}$ and $\overline{\text{BE0}}$ pins as A1 and A0 respectively. 8-bit bus: $\overline{\text{BE3}}$ –Not used (driven high or low) $\overline{\text{BE2}}$ –Not used (driven high or low) $\overline{\text{BE1}}$ –Address Bit 1 (A1) $\overline{\text{BE0}}$ –Address Bit 0 (A0)
W/$\overline{\text{R}}$	**O** S H(Z) R(0)	**WRITE/READ** is asserted for read requests and deasserted for write requests. The W/$\overline{\text{R}}$ signal changes in the same clock cycle as $\overline{\text{ADS}}$. It remains valid for the entire access in non-pipelined regions. In pipelined regions, W/$\overline{\text{R}}$ is not guaranteed to be valid in the last cycle of a read access.
$\overline{\text{ADS}}$	**O** S H(Z) R(1)	**ADDRESS STROBE** indicates a valid address and the start of a new bus access. $\overline{\text{ADS}}$ is asserted for the first clock of a bus access.

Table 3. 80960CA Pin Description — External Bus Signals (Sheet 2 of 3)

Name	Type	Description
READY	**I** S(L) H(Z) R(Z)	**READY** is an input which signals the termination of a data transfer. READY is used to indicate that read data on the bus is valid or that a write-data transfer has completed. The READY signal works in conjunction with the internally programmed wait-state generator. If READY is enabled in a region, the pin is sampled after the programmed number of wait-states has expired. If the READY pin is deasserted, wait states continue to be inserted until READY becomes asserted. This is true for the N_{RAD}, N_{RDD}, N_{WAD} and N_{WDD} wait states. The N_{XDA} wait states cannot be extended.
BTERM	**I** S(L) H(Z) R(Z)	**BURST TERMINATE** is an input which breaks up a burst access and causes another address cycle to occur. The BTERM signal works in conjunction with the internally programmed wait-state generator. If READY and BTERM are enabled in a region, the BTERM pin is sampled after the programmed number of wait states has expired. When BTERM is asserted, a new ADS signal is generated and the access is completed. The READY input is ignored when BTERM is asserted. BTERM must be externally synchronized to satisfy BTERM setup and hold times.
WAIT	**O** S H(Z) R(1)	**WAIT** indicates internal wait state generator status. WAIT is asserted when wait states are being caused by the internal wait state generator and not by the READY or BTERM inputs. WAIT can be used to derive a write-data strobe. WAIT can also be thought of as a READY output that the processor provides when it is inserting wait states.
BLAST	**O** S H(Z) R(0)	**BURST LAST** indicates the last transfer in a bus access. BLAST is asserted in the last data transfer of burst and non-burst accesses after the wait state counter reaches zero. BLAST remains asserted until the clock following the last cycle of the last data transfer of a bus access. If the READY or BTERM input is used to extend wait states, the BLAST signal remains asserted until READY or BTERM terminates the access.
DT/R	**O** S H(Z) R(0)	**DATA TRANSMIT/RECEIVE** indicates direction for data transceivers. DT/R is used in conjunction with DEN to provide control for data transceivers attached to the external bus. When DT/R is asserted, the signal indicates that the processor receives data. Conversely, when deasserted, the processor sends data. DT/R changes only while DEN is high.
DEN	**O** S H(Z) R(1)	**DATA ENABLE** indicates data cycles in a bus request. DEN is asserted at the start of the bus request first data cycle and is deasserted at the end of the last data cycle. DEN is used in conjunction with DT/R to provide control for data transceivers attached to the external bus. DEN remains asserted for sequential reads from pipelined memory regions. DEN is deasserted when DT/R changes.
LOCK	**O** S H(Z) R(1)	**BUS LOCK** indicates that an atomic read-modify-write operation is in progress. LOCK may be used to prevent external agents from accessing memory which is currently involved in an atomic operation. LOCK is asserted in the first clock of an atomic operation and deasserted in the clock cycle following the last bus access for the atomic operation. To allow the most flexibility for memory system enforcement of locked accesses, the processor acknowledges a bus hold request when LOCK is asserted. The processor performs DMA transfers while LOCK is active.
HOLD	**I** S(L) H(Z) R(Z)	**HOLD REQUEST** signals that an external agent requests access to the external bus. The processor asserts HOLDA after completing the current bus request. HOLD, HOLDA and BREQ are used together to arbitrate access to the processor's external bus by external bus agents.

Table 3. 80960CA Pin Description — External Bus Signals (Sheet 3 of 3)

Name	Type	Description
$\overline{\text{BOFF}}$	**I** S(L) H(Z) R(Z)	**BUS BACKOFF**, when asserted, suspends the current access and causes the bus pins to float. When $\overline{\text{BOFF}}$ is deasserted, the $\overline{\text{ADS}}$ signal is asserted on the next clock cycle and the access is resumed.
HOLDA	**O** S H(1) R(Q)	**HOLD ACKNOWLEDGE** indicates to a bus requestor that the processor has relinquished control of the external bus. When HOLDA is asserted, the external address bus, data bus and bus control signals are floated. HOLD, $\overline{\text{BOFF}}$, HOLDA and BREQ are used together to arbitrate access to the processor's external bus by external bus agents. Since the processor grants HOLD requests and enters the Hold Acknowledge state even while $\overline{\text{RESET}}$ is asserted, the state of the HOLDA pin is independent of the $\overline{\text{RESET}}$ pin.
BREQ	**O** S H(Q) R(0)	**BUS REQUEST** is asserted when the bus controller has a request pending. BREQ can be used by external bus arbitration logic in conjunction with HOLD and HOLDA to determine when to return mastership of the external bus to the processor.
D/$\overline{\text{C}}$	**O** S H(Z) R(Z)	**DATA OR CODE** is asserted for a data request and deasserted for instruction requests. D/$\overline{\text{C}}$ has the same timing as W/$\overline{\text{R}}$.
$\overline{\text{DMA}}$	**O** S H(Z) R(Z)	**DMA ACCESS** indicates whether the bus request was initiated by the DMA controller. $\overline{\text{DMA}}$ is asserted for any DMA request. $\overline{\text{DMA}}$ is deasserted for all other requests.
$\overline{\text{SUP}}$	**O** S H(Z) R(Z)	**SUPERVISOR ACCESS** indicates whether the bus request is issued while in supervisor mode. $\overline{\text{SUP}}$ is asserted when the request has supervisor privileges and is deasserted otherwise. $\overline{\text{SUP}}$ can be used to isolate supervisor code and data structures from non-supervisor requests.

Table 4. 80960CA Pin Description — Processor Control Signals (Sheet 1 of 2)

Name	Type	Description
RESET	**I** A(L) H(Z) R(Z)	**RESET** causes the chip to reset. When RESET is asserted, all external signals return to the reset state. When RESET is deasserted, initialization begins. When the 2-x clock mode is selected, RESET must remain asserted for 32 CLKIN cycles before being deasserted to guarantee correct processor initialization. When the 1-x clock mode is selected, RESET must remain asserted for 10,000 CLKIN cycles before being deasserted to guarantee correct processor initialization. The CLKMODE pin selects 1-x or 2-x input clock division of the CLKIN pin. The processor's Hold Acknowledge bus state functions while the chip is reset. If the processor's bus is in the Hold Acknowledge state when RESET is asserted, the processor will internally reset, but maintains the Hold Acknowledge state on external pins until the Hold request is removed. If a Hold request is made while the processor is in the reset state, the processor bus will grant HOLDA and enter the Hold Acknowledge state.
FAIL	**O** S H(Q) R(0)	**FAIL** indicates failure of the processor's self-test performed at initialization. When RESET is deasserted and the processor begins initialization, the FAIL pin is asserted. An internal self-test is performed as part of the initialization process. If this self-test passes, the FAIL pin is deasserted; otherwise it remains asserted. The FAIL pin is reasserted while the processor performs an external bus self-confidence test. If this self-test passes, the processor deasserts the FAIL pin and branches to the user's initialization routine; otherwise the FAIL pin remains asserted. Internal self-test and the use of the FAIL pin can be disabled with the STEST pin.
STEST	**I** S(L) H(Z) R(Z)	**SELF TEST** causes the processor's internal self-test feature to be enabled or disabled at initialization. STEST is read on the rising edge of RESET. When asserted, the processor's internal self-test and external bus confidence tests are performed during processor initialization. When deasserted, only the bus confidence tests are performed during initialization.
ONCE	**I** A(L) H(Z) R(Z)	**ON CIRCUIT EMULATION**, when asserted, causes all outputs to be floated. ONCE is continuously sampled while RESET is low and is latched on the rising edge of RESET. To place the processor in the ONCE state: (1) assert RESET and ONCE (order does not matter) (2) wait for at least 16 CLKIN periods in 2-x mode—or 10,000 CLKIN periods in 1-x mode—after V_{CC} and CLKIN are within operating specifications (3) deassert RESET (4) wait at least 32 CLKIN periods (The processor will now be latched in the ONCE state as long as RESET is high.) To exit the ONCE state, bring V_{CC} and CLKIN to operating conditions, then assert RESET and bring ONCE high prior to deasserting RESET. CLKIN must operate within the specified operating conditions of the processor until Step 4 above has been completed. CLKIN may then be changed to DC to achieve the lowest possible ONCE mode leakage current. ONCE can be used by emulator products or for board testers to effectively make an installed processor transparent in the board.

Table 4. 80960CA Pin Description — Processor Control Signals (Sheet 2 of 2)

Name	Type	Description
CLKIN	**I** A(E) H(Z) R(Z)	**CLOCK INPUT** is an input for the external clock needed to run the processor. The external clock is internally divided as prescribed by the CLKMODE pin to produce PCLK2:1.
CLKMODE	**I** A(L) H(Z) R(Z)	**CLOCK MODE** selects the division factor applied to the external clock input (CLKIN). When CLKMODE is high, CLKIN is divided by one to create PCLK2:1 and the processor's internal clock. When CLKMODE is low, CLKIN is divided by two to create PCLK2:1 and the processor's internal clock. CLKMODE should be tied high or low in a system as the clock mode is not latched by the processor. If left unconnected, the processor will internally pull the CLKMODE pin low, enabling the 2-x clock mode.
PCLK2:1	**O** S H(Q) R(Q)	**PROCESSOR OUTPUT CLOCKS** provide a timing reference for all processor inputs and outputs. All input and output timings are specified in relation to PCLK2 and PCLK1. PCLK2 and PCLK1 are identical signals. Two output pins are provided to allow flexibility in the system's allocation of capacitive loading on the clock. PCLK2:1 may also be connected at the processor to form a single clock signal.
V_{SS}	–	**GROUND** connections must be connected externally to a V_{SS} board plane.
V_{CC}	–	**POWER** connections must be connected externally to a V_{CC} board plane.
V_{CCPLL}	–	**V_{CCPLL}** is a separate V_{CC} supply pin for the phase lock loop used in 1-x clock mode. Connecting a simple lowpass filter to V_{CCPLL} may help reduce clock jitter (T_{CP}) in noisy environments. Otherwise, V_{CCPLL} should be connected to V_{CC}. This pin is implemented starting with the D-stepping. See Table 13 for die stepping information.
NC	–	**NO CONNECT** pins must not be connected in a system.

Table 5. 80960CA Pin Description — DMA and Interrupt Unit Control Signals

Name	Type	Description
$\overline{\text{DREQ3:0}}$	**I** A(L) H(Z) R(Z)	**DMA REQUEST** causes a DMA transfer to be requested. Each of the four signals requests a transfer on a single channel. $\overline{\text{DREQ0}}$ requests channel 0, $\overline{\text{DREQ1}}$ requests channel 1, etc. When two or more channels are requested simultaneously, the channel with the highest priority is serviced first. The channel priority mode is programmable.
$\overline{\text{DACK3:0}}$	**O** S H(1) R(1)	**DMA ACKNOWLEDGE** indicates that a DMA transfer is being executed. Each of the four signals acknowledges a transfer for a single channel. $\overline{\text{DACK0}}$ acknowledges channel 0, $\overline{\text{DACK1}}$ acknowledges channel 1, etc. $\overline{\text{DACK3:0}}$ are asserted when the requesting device of a DMA is accessed.
$\overline{\text{EOP}}$/$\overline{\text{TC3:0}}$	**I/O** A(L) H(Z/Q) R(Z)	**END OF PROCESS/TERMINAL COUNT** can be programmed as either an input ($\overline{\text{EOP3:0}}$) or as an output ($\overline{\text{TC3:0}}$), but not both. Each pin is individually programmable. When programmed as an input, $\overline{\text{EOPx}}$ causes the termination of a current DMA transfer for the channel corresponding to the $\overline{\text{EOPx}}$ pin. $\overline{\text{EOP0}}$ corresponds to channel 0, $\overline{\text{EOP1}}$ corresponds to channel 1, etc. When a channel is configured for source *and* destination chaining, the EOP pin for that channel causes termination of only the current buffer transferred and causes the next buffer to be transferred. $\overline{\text{EOP3:0}}$ are asynchronous inputs. When programmed as an output, the channel's $\overline{\text{TCx}}$ pin indicates that the channel byte count has reached 0 and a DMA has terminated. $\overline{\text{TCx}}$ is driven with the same timing as $\overline{\text{DACKx}}$ during the last DMA transfer for a buffer. If the last bus request is executed as multiple bus accesses, $\overline{\text{TCx}}$ will stay asserted for the entire bus request.
$\overline{\text{XINT7:0}}$	**I** A(E/L) H(Z) R(Z)	**EXTERNAL INTERRUPT PINS** cause interrupts to be requested. These pins can be configured in three modes: **Dedicated Mode:** each pin is a dedicated external interrupt source. Dedicated inputs can be individually programmed to be level (low) or edge (falling) activated. **Expanded Mode:** the eight pins act together as an 8-bit vectored interrupt source. The interrupt pins in this mode are level activated.Since the interrupt pins are active low, the vector number requested is the one's complement of the positive logic value place on the port. This eliminates glue logic to interface to combinational priority encoders which output negative logic. **Mixed Mode:** $\overline{\text{XINT7:5}}$ are dedicated sources and $\overline{\text{XINT4:0}}$ act as the five most significant bits of an expanded mode vector. The least significant bits are set to 010 internally.
$\overline{\text{NMI}}$	**I** A(E) H(Z) R(Z)	**NON-MASKABLE INTERRUPT** causes a non-maskable interrupt event to occur. $\overline{\text{NMI}}$ is the highest priority interrupt recognized. $\overline{\text{NMI}}$ is an edge (falling) activated source.

3.3 80960CA Mechanical Data

3.3.1 80960CA PGA Pinout

Tables 6 and 7 list the 80960CA pin names with package location. Figure 2 depicts the complete 80960CA PGA pinout as viewed from the top side of the component (i.e., pins facing down). Figure 3 shows the complete 80960CA PGA pinout as viewed from the pin-side of the package (i.e., pins facing up). See **Section 4.0, ELECTRICAL SPECIFICATIONS** for specifications and recommended connections.

Table 6. 80960CA PGA Pinout — In Signal Order

Address Bus		Data Bus		Bus Control		Processor Control		I/O	
Signal	**Pin**	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**	**Pin**
A31	S15	D31	R3	$\overline{\text{BE3}}$	S5	$\overline{\text{RESET}}$	A16	$\overline{\text{DREQ3}}$	A7
A30	Q13	D30	Q5	$\overline{\text{BE2}}$	S6			$\overline{\text{DREQ2}}$	B6
A29	R14	D29	S2	$\overline{\text{BE1}}$	S7	$\overline{\text{FAIL}}$	A2	$\overline{\text{DREQ1}}$	A6
A28	Q14	D28	Q4	$\overline{\text{BE0}}$	R9			$\overline{\text{DREQ0}}$	B5
A27	S16	D27	R2			STEST	B2		
A26	R15	D26	Q3	W/$\overline{\text{R}}$	S10			$\overline{\text{DACK3}}$	A10
A25	S17	D25	S1			$\overline{\text{ONCE}}$	C3	$\overline{\text{DACK2}}$	A9
A24	Q15	D24	R1	$\overline{\text{ADS}}$	R6			$\overline{\text{DACK1}}$	A8
A23	R16	D23	Q2			CLKIN	C13	$\overline{\text{DACK0}}$	B8
A22	R17	D22	P3	$\overline{\text{READY}}$	S3	CLKMODE	C14		
A21	Q16	D21	Q1	$\overline{\text{BTERM}}$	R4	PLCK1	B14	$\overline{\text{EOP/TC3}}$	A14
A20	P15	D20	P2			PLCK2	B13	$\overline{\text{EOP/TC2}}$	A13
A19	P16	D19	P1	$\overline{\text{WAIT}}$	S12			$\overline{\text{EOP/TC1}}$	A12
A18	Q17	D18	N2	$\overline{\text{BLAST}}$	S8	**V_{SS}**		$\overline{\text{EOP/TC0}}$	A11
A17	P17	D17	N1			*Location*			
A16	N16	D16	M1	DT/$\overline{\text{R}}$	S11	C7, C8, C9, C10, C11, C12, F15, G3, G15, H3, H15, J3, J15, K3, K15, L3, L15, M3, M15, Q7, Q8, Q9, Q10, Q11		$\overline{\text{XINT7}}$	C17
A15	N17	D15	L1	$\overline{\text{DEN}}$	S9			$\overline{\text{XINT6}}$	C16
A14	M17	D14	L2					$\overline{\text{XINT5}}$	B17
A13	L16	D13	K1	$\overline{\text{LOCK}}$	S14			$\overline{\text{XINT4}}$	C15
A12	L17	D12	J1					$\overline{\text{XINT3}}$	B16
A11	K17	D11	H1			**V_{CC}**		$\overline{\text{XINT2}}$	A17
A10	J17	D10	H2	HOLD	R5	*Location*		$\overline{\text{XINT1}}$	A15
A9	H17	D9	G1	HOLDA	S4	B7, B9, B11, B12, C6, E15, F3, F16, G2, H16, J2, J16, K2, K16, M2, M16, N3, N15, Q6, R7, R8, R10, R11		$\overline{\text{XINT0}}$	B15
A8	G17	D8	F1	$\overline{\text{BREQ}}$	R13				
A7	G16	D7	E1					$\overline{\text{NMI}}$	D15
A6	F17	D6	F2	D/$\overline{\text{C}}$	S13				
A5	E17	D5	D1	$\overline{\text{DMA}}$	R12				
A4	E16	D4	E2	$\overline{\text{SUP}}$	Q12	V_{CCPLL}	B10		
A3	D17	D3	C1			**No Connect**			
A2	D16	D2	D2	$\overline{\text{BOFF}}$	B1	*Location*			
		D1	C2			A1, A3, A4, A5, B3, B4, C4, C5, D3			
		D0	E3						

Table 7. 80960CA PGA Pinout — In Pin Order

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	NC	C1	D3	G1	D9	M1	D16	R1	D24
A2	$\overline{\text{FAIL}}$	C2	D1	G2	V_{CC}	M2	V_{CC}	R2	D27
A3	NC	C3	$\overline{\text{ONCE}}$	G3	V_{SS}	M3	V_{SS}	R3	D31
A4	NC	C4	NC	G15	V_{SS}	M15	V_{SS}	R4	$\overline{\text{BTERM}}$
A5	NC	C5	NC	G16	A7	M16	V_{CC}	R5	HOLD
A6	$\overline{\text{DREQ1}}$	C6	V_{CC}	G17	A8	M17	A14	R6	$\overline{\text{ADS}}$
A7	$\overline{\text{DREQ3}}$	C7	V_{SS}					R7	V_{CC}
A8	$\overline{\text{DACK1}}$	C8	V_{SS}	H1	D11	N1	D17	R8	V_{CC}
A9	$\overline{\text{DACK2}}$	C9	V_{SS}	H2	D10	N2	D18	R9	$\overline{\text{BE0}}$
A10	$\overline{\text{DACK3}}$	C10	V_{SS}	H3	V_{SS}	N3	V_{CC}	R10	V_{CC}
A11	$\overline{\text{EOP}}/\overline{\text{TC0}}$	C11	V_{SS}	H15	V_{SS}	N15	V_{CC}	R11	V_{CC}
A12	$\overline{\text{EOP}}/\overline{\text{TC1}}$	C12	V_{SS}	H16	V_{CC}	N16	A16	R12	$\overline{\text{DMA}}$
A13	$\overline{\text{EOP}}/\overline{\text{TC2}}$	C13	CLKIN	H17	A9	N17	A15	R13	BREQ
A14	$\overline{\text{EOP}}/\overline{\text{TC3}}$	C14	CLKMODE					R14	A29
A15	$\overline{\text{XINT1}}$	C15	$\overline{\text{XINT4}}$	J1	D12	P1	D19	R15	A26
A16	$\overline{\text{RESET}}$	C16	$\overline{\text{XINT6}}$	J2	V_{CC}	P2	D20	R16	A23
A17	$\overline{\text{XINT2}}$	C17	$\overline{\text{XINT7}}$	J3	V_{SS}	P3	D22	R17	A22
				J15	V_{SS}	P15	A20		
B1	$\overline{\text{BOFF}}$	D1	D5	J16	V_{CC}	P16	A19	S1	D25
B2	STEST	D2	D2	J17	A10	P17	A17	S2	D29
B3	NC	D3	NC					S3	$\overline{\text{READY}}$
B4	NC	D15	$\overline{\text{NMI}}$	K1	D13	Q1	D21	S4	HOLDA
B5	$\overline{\text{DREQ0}}$	D16	A2	K2	V_{CC}	Q2	D23	S5	$\overline{\text{BE3}}$
B6	$\overline{\text{DREQ2}}$	D17	A3	K3	V_{SS}	Q3	D26	S6	$\overline{\text{BE2}}$
B7	V_{CC}			K15	V_{SS}	Q4	D28	S7	$\overline{\text{BE1}}$
B8	$\overline{\text{DACK0}}$	E1	D7	K16	V_{CC}	Q5	D30	S8	$\overline{\text{BLAST}}$
B9	V_{CC}	E2	D4	K17	A11	Q6	V_{CC}	S9	$\overline{\text{DEN}}$
B10	V_{CCPLL}	E3	D0			Q7	V_{SS}	S10	W/$\overline{\text{R}}$
B11	V_{CC}	E15	V_{CC}	L1	D15	Q8	V_{SS}	S11	DT/$\overline{\text{R}}$
B12	V_{CC}	E16	A4	L2	D14	Q9	V_{SS}	S12	$\overline{\text{WAIT}}$
B13	PCLK2	E17	A5	L3	V_{SS}	Q10	V_{SS}	S13	D/$\overline{\text{C}}$
B14	PCLK1			L15	V_{SS}	Q11	V_{SS}	S14	$\overline{\text{LOCK}}$
B15	$\overline{\text{XINT0}}$	F1	D8	L16	A13	Q12	$\overline{\text{SUP}}$	S15	A31
B16	$\overline{\text{XINT3}}$	F2	D6	L17	A12	Q13	A30	S16	A27
B17	$\overline{\text{XINT5}}$	F3	V_{CC}			Q14	A28	S17	A25
		F15	V_{SS}			Q15	A24		
		F16	V_{CC}			Q16	A21		
		F17	A6			Q17	A18		

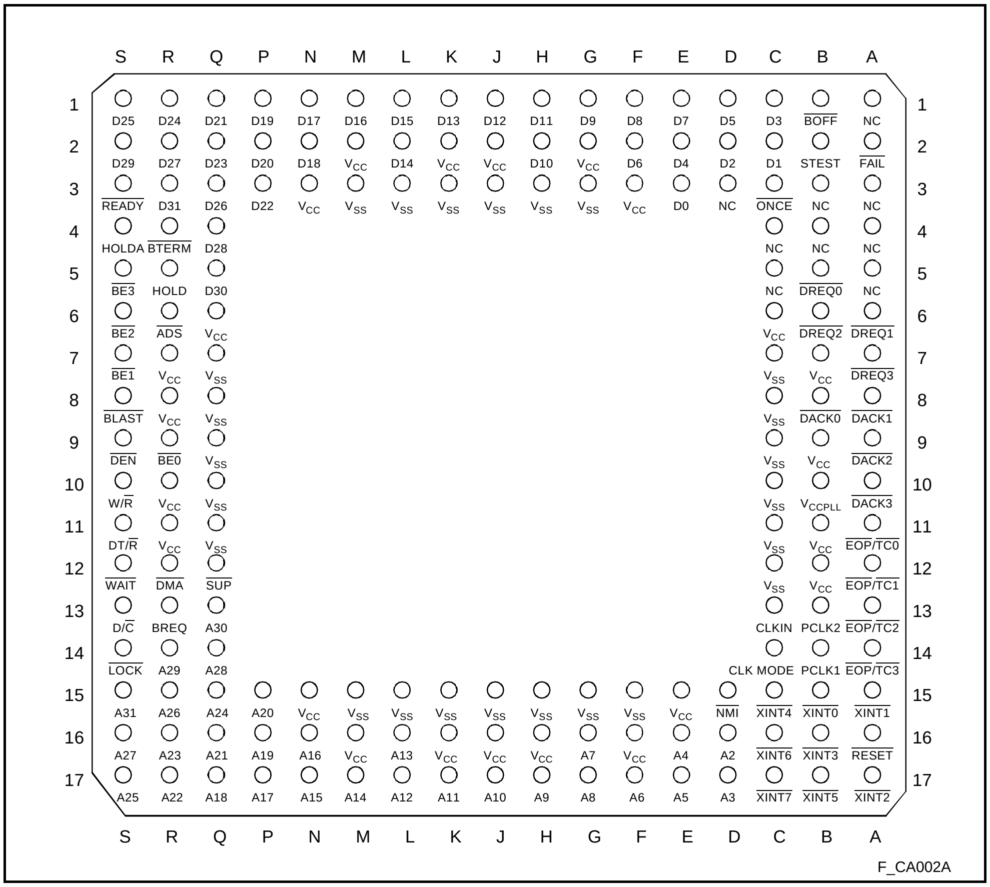
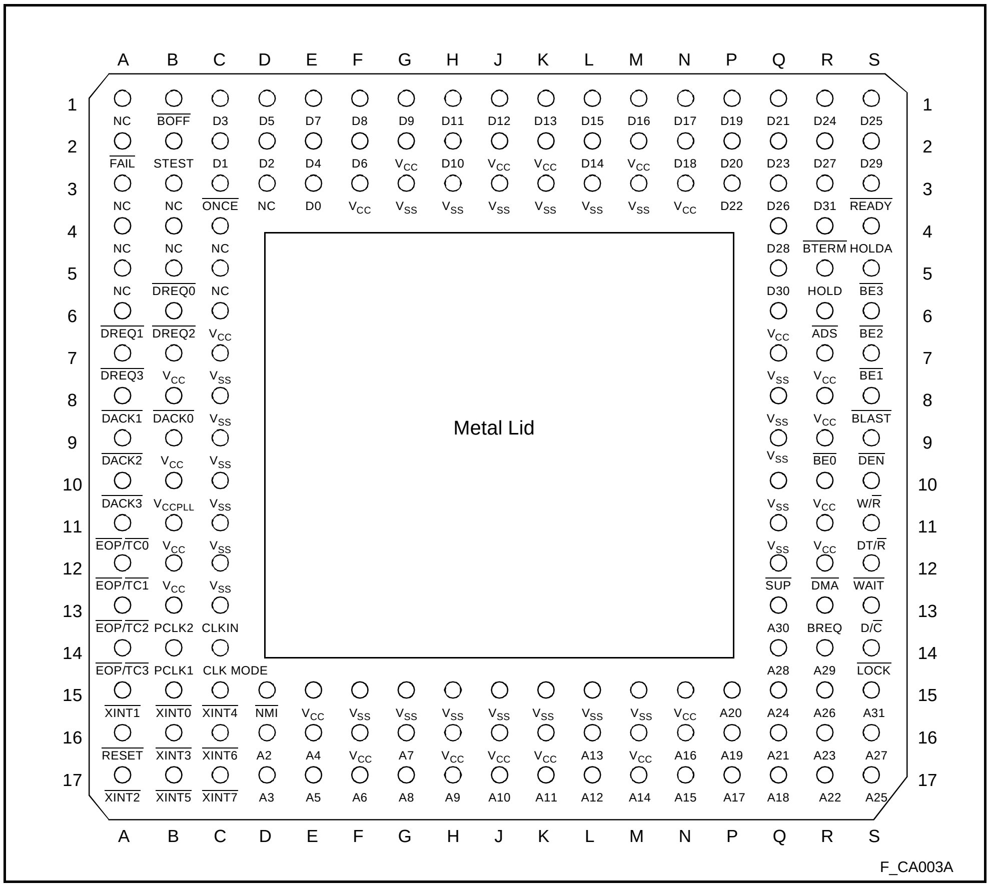


Figure 2. 80960CA PGA Pinout — View from Top (Pins Facing Down)



	A	B	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S
1	NC	$\overline{BOFF}$	D3	D5	D7	D8	D9	D11	D12	D13	D15	D16	D17	D19	D21	D24	D25
2	$\overline{FAIL}$	STEST	D1	D2	D4	D6	V_{CC}	D10	V_{CC}	V_{CC}	D14	V_{CC}	D18	D20	D23	D27	D29
3	NC	NC	$\overline{ONCE}$	NC	D0	V_{CC}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{CC}	D22	D26	D31	READY
4	NC	NC	NC												D28	$\overline{BTERM}$	HOLDA
5	NC	$\overline{DREQ0}$	NC												D30	HOLD	$\overline{BE3}$
6	$\overline{DREQ1}$	$\overline{DREQ2}$	V_{CC}												V_{CC}	$\overline{ADS}$	$\overline{BE2}$
7	$\overline{DREQ3}$	V_{CC}	V_{SS}												V_{SS}	V_{CC}	$\overline{BE1}$
8	$\overline{DACK1}$	$\overline{DACK0}$	V_{SS}												V_{SS}	V_{CC}	$\overline{BLAST}$
9	$\overline{DACK2}$	V_{CC}	V_{SS}												V_{SS}	$\overline{BE0}$	$\overline{DEN}$
10	$\overline{DACK3}$	V_{CCPLL}	V_{SS}												V_{SS}	V_{CC}	$W/\overline{R}$
11	$\overline{EOP/TC0}$	V_{CC}	V_{SS}												V_{SS}	V_{CC}	$DT/\overline{R}$
12	$\overline{EOP/TC1}$	V_{CC}	V_{SS}												$\overline{SUP}$	$\overline{DMA}$	$\overline{WAIT}$
13	$\overline{EOP/TC2}$	PCLK2	CLKIN												A30	BREQ	$D/\overline{C}$
14	$\overline{EOP/TC3}$	PCLK1	CLK MODE												A28	A29	$\overline{LOCK}$
15	$\overline{XINT1}$	$\overline{XINT0}$	$\overline{XINT4}$	$\overline{NMI}$	V_{CC}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{CC}	A20	A24	A26	A31
16	$\overline{RESET}$	$\overline{XINT3}$	$\overline{XINT6}$	A2	A4	V_{CC}	A7	V_{CC}	V_{CC}	V_{CC}	A13	V_{CC}	A16	A19	A21	A23	A27
17	$\overline{XINT2}$	$\overline{XINT5}$	$\overline{XINT7}$	A3	A5	A6	A8	A9	A10	A11	A12	A14	A15	A17	A18	A22	A25

Figure 3. 80960CA PGA Pinout — View from Bottom (Pins Facing Up)

3.3.2 80960CA PQFP Pinout

Tables 8 and 9 list the 80960CA pin names with package location. Figure 4 shows the 80960CA PQFP pinout as viewed from the top side.

See **Section 4.0, ELECTRICAL SPECIFICATIONS** for specifications and recommended connections.

Table 8. 80960CA PQFP Pinout — In Signal Order

Address Bus		Data Bus		Bus Control		Processor Control		I/O	
Signal	**Pin**	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**	**Pin**
A31	153	D31	186	$\overline{\text{BE3}}$	176	$\overline{\text{RESET}}$	91	$\overline{\text{DREQ3}}$	60
A30	152	D30	187	$\overline{\text{BE2}}$	175	$\overline{\text{FAIL}}$	45	$\overline{\text{DREQ2}}$	59
A29	151	D29	188	$\overline{\text{BE1}}$	172	STEST	46	$\overline{\text{DREQ1}}$	58
A28	145	D28	189	$\overline{\text{BE0}}$	170	$\overline{\text{ONCE}}$	43	$\overline{\text{DREQ0}}$	57
A27	144	D27	191			CLKIN	87		
A26	143	D26	192	W/$\overline{\text{R}}$	164	CLKMODE	85	$\overline{\text{DACK3}}$	65
A25	142	D25	194			PCLK2	74	$\overline{\text{DACK2}}$	64
A24	141	D24	195	$\overline{\text{ADS}}$	178	PCLK1	78	$\overline{\text{DACK1}}$	63
A23	139	D23	3			**V_{SS}**		$\overline{\text{DACK0}}$	62
A22	138	D22	4	$\overline{\text{READY}}$	182	*Location*			
A21	137	D21	5	$\overline{\text{BTERM}}$	184	2, 7, 16, 24, 30, 38, 39, 49, 56, 70, 75, 77, 81, 83, 88, 89, 92, 98, 105, 109, 110, 121, 125, 131, 135, 147, 150, 161, 165, 173, 174, 185, 196		$\overline{\text{EOP}}$/$\overline{\text{TC3}}$	69
A20	136	D20	6					$\overline{\text{EOP}}$/$\overline{\text{TC2}}$	68
A19	134	D19	8	$\overline{\text{WAIT}}$	162			$\overline{\text{EOP}}$/$\overline{\text{TC1}}$	67
A18	133	D18	9	$\overline{\text{BLAST}}$	169			$\overline{\text{EOP}}$/$\overline{\text{TC0}}$	66
A17	132	D17	10						
A16	130	D16	11	DT/$\overline{\text{R}}$	163			$\overline{\text{XINT7}}$	107
A15	129	D15	13	$\overline{\text{DEN}}$	167	**V_{CC}**		$\overline{\text{XINT6}}$	106
A14	128	D14	14			*Location*		$\overline{\text{XINT5}}$	102
A13	124	D13	15	$\overline{\text{LOCK}}$	156	1, 12, 20, 28, 32, 37, 44, 50, 61, 71, 79, 82, 96, 99, 103, 115, 127, 140, 148, 154, 168, 171, 180, 190		$\overline{\text{XINT4}}$	101
A12	123	D12	17					$\overline{\text{XINT3}}$	100
A11	122	D11	18	HOLD	181			$\overline{\text{XINT2}}$	95
A10	120	D10	19	HOLDA	179			$\overline{\text{XINT1}}$	94
A9	119	D9	21	BREQ	155			$\overline{\text{XINT0}}$	93
A8	118	D8	22			V_{CCPLL}	72		
A7	117	D7	23	D/$\overline{\text{C}}$	159	**No Connect**		$\overline{\text{NMI}}$	108
A6	116	D6	25	$\overline{\text{DMA}}$	160	*Location*			
A5	114	D5	26	$\overline{\text{SUP}}$	158	29, 31, 41, 42, 47, 48, 51, 52, 53, 54, 55, 73, 76, 80, 84, 86, 90, 97, 104, 126, 146, 149, 157, 166, 177, 183, 193			
A4	113	D4	27						
A3	112	D3	33	$\overline{\text{BOFF}}$	40				
A2	111	D2	34						
		D1	35						
		D0	36						

Table 9. 80960CA PQFP Pinout — In Pin Order

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	V_{CC}	34	D2	67	$\overline{\text{EOP}}/\overline{\text{TC1}}$	100	$\overline{\text{XINT3}}$	133	A18	166	NC
2	V_{SS}	35	D1	68	$\overline{\text{EOP}}/\overline{\text{TC2}}$	101	$\overline{\text{XINT4}}$	134	A19	167	$\overline{\text{DEN}}$
3	D23	36	D0	69	$\overline{\text{EOP}}/\overline{\text{TC3}}$	102	$\overline{\text{XINT5}}$	135	V_{SS}	168	V_{CC}
4	D22	37	V_{CC}	70	V_{SS}	103	V_{CC}	136	A20	169	$\overline{\text{BLAST}}$
5	D21	38	V_{SS}	71	V_{CC}	104	NC	137	A21	170	$\overline{\text{BE0}}$
6	D20	39	V_{SS}	72	V_{CCPLL}	105	V_{SS}	138	A22	171	V_{CC}
7	V_{SS}	40	$\overline{\text{BOFF}}$	73	NC	106	$\overline{\text{XINT6}}$	139	A23	172	$\overline{\text{BE1}}$
8	D19	41	NC	74	PCLK2	107	$\overline{\text{XINT7}}$	140	V_{CC}	173	V_{SS}
9	D18	42	NC	75	V_{SS}	108	$\overline{\text{NMI}}$	141	A24	174	V_{SS}
10	D17	43	$\overline{\text{ONCE}}$	76	NC	109	V_{SS}	142	A25	175	$\overline{\text{BE2}}$
11	D16	44	V_{CC}	77	V_{SS}	110	V_{SS}	143	A26	176	$\overline{\text{BE3}}$
12	V_{CC}	45	$\overline{\text{FAIL}}$	78	PCLK1	111	A2	144	A27	177	NC
13	D15	46	STEST	79	V_{CC}	112	A3	145	A28	178	$\overline{\text{ADS}}$
14	D14	47	NC	80	NC	113	A4	146	NC	179	HOLDA
15	D13	48	NC	81	V_{SS}	114	A5	147	V_{SS}	180	V_{CC}
16	V_{SS}	49	V_{SS}	82	V_{CC}	115	V_{CC}	148	V_{CC}	181	HOLD
17	D12	50	V_{CC}	83	V_{SS}	116	A6	149	NC	182	$\overline{\text{READY}}$
18	D11	51	NC	84	NC	117	A7	150	V_{SS}	183	NC
19	D10	52	NC	85	CLKMODE	118	A8	151	A29	184	$\overline{\text{BTERM}}$
20	V_{CC}	53	NC	86	NC	119	A9	152	A30	185	V_{SS}
21	D9	54	NC	87	CLKIN	120	A10	153	A31	186	D31
22	D8	55	NC	88	V_{SS}	121	V_{SS}	154	V_{CC}	187	D30
23	D7	56	V_{SS}	89	V_{SS}	122	A11	155	BREQ	188	D29
24	V_{SS}	57	$\overline{\text{DREQ0}}$	90	NC	123	A12	156	$\overline{\text{LOCK}}$	189	D28
25	D6	58	$\overline{\text{DREQ1}}$	91	$\overline{\text{RESET}}$	124	A13	157	NC	190	V_{CC}
26	D5	59	$\overline{\text{DREQ2}}$	92	V_{SS}	125	V_{SS}	158	$\overline{\text{SUP}}$	191	D27
27	D4	60	$\overline{\text{DREQ3}}$	93	$\overline{\text{XINT0}}$	126	NC	159	D/$\overline{\text{C}}$	192	D26
28	V_{CC}	61	V_{CC}	94	$\overline{\text{XINT1}}$	127	V_{CC}	160	$\overline{\text{DMA}}$	193	NC
29	NC	62	$\overline{\text{DACK0}}$	95	$\overline{\text{XINT2}}$	128	A14	161	V_{SS}	194	D25
30	V_{SS}	63	$\overline{\text{DACK1}}$	96	V_{CC}	129	A15	162	$\overline{\text{WAIT}}$	195	D24
31	NC	64	$\overline{\text{DACK2}}$	97	NC	130	A16	163	DT/$\overline{\text{R}}$	196	V_{SS}
32	V_{CC}	65	$\overline{\text{DACK3}}$	98	V_{SS}	131	V_{SS}	164	W/$\overline{\text{R}}$		
33	D3	66	$\overline{\text{EOP}}/\overline{\text{TC0}}$	99	V_{CC}	132	A17	165	V_{SS}		

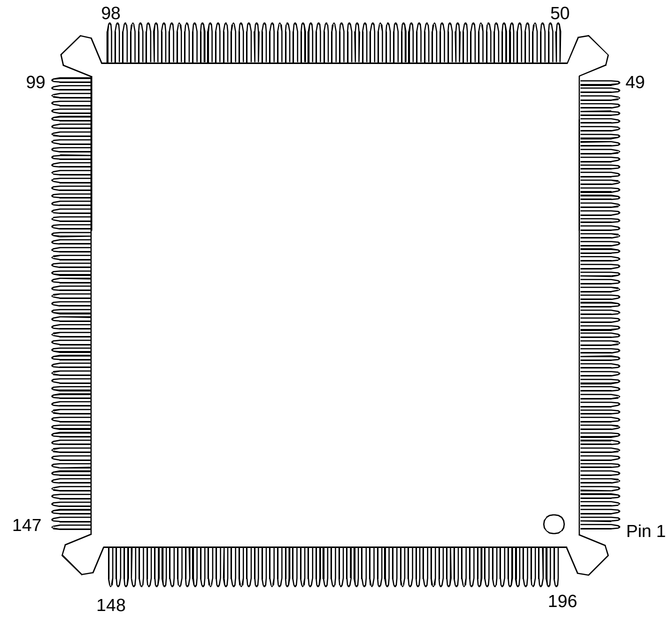


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Figure 4. 80960CA PQFP Pinout (View from Top Side)

3.4 Package Thermal Specifications

The 80960CA is specified for operation when T_C (case temperature) is within the range of $0^oC–100^oC$. T_C may be measured in any environment to determine whether the 80960CA is within specified operating range. Case temperature should be measured at the center of the top surface, opposite the pins. Refer to Figure 5.

T_A (ambient temperature) can be calculated from θ_{CA} (thermal resistance from case to ambient) using the following equation:

$$T_A = T_C - P^*\theta_{CA}$$

Table 10 shows the maximum T_A allowable (without exceeding T_C) at various airflows and operating frequencies (f_{PCLK}).

Note that T_A is greatly improved by attaching fins or a heatsink to the package. P (maximum power consumption) is calculated by using the typical I_{CC} as tabulated in **Section 4.4, DC Specifications** and V_{CC} of 5V.

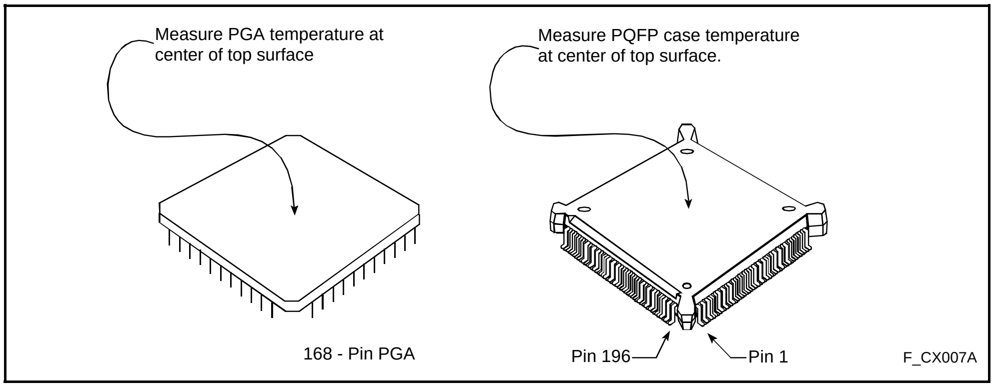


Figure 5. Measuring 80960CA PGA and PQFP Case Temperature

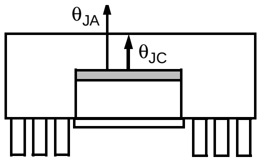
Table 10. Maximum T_A at Various Airflows in ^oC (PGA Package Only)

		Airflow-ft/min (m/sec)					
	f_{PCLK} (MHz)	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
T_A with Heatsink*	33	51	66	79	81	85	87
	25	61	73	83	85	88	89
	16	74	82	89	90	92	93
T_A without Heatsink*	33	36	47	59	66	73	75
	25	49	58	67	73	78	80
	16	66	72	78	82	86	87

NOTES:
*0.285” high unidirectional heatsink (Al alloy 6061, 50 mil fin width, 150 mil center-to-center fin spacing).

Table 11. 80960CA PGA Package Thermal Characteristics

Parameter	Thermal Resistance — °C/Watt					
	Airflow — ft./min (m/sec)					
	0 (0)	200 (1.01)	400 (2.03)	600 (3.07)	800 (4.06)	1000 (5.07)
θ Junction-to-Case (Case measured as shown in Figure 5)	1.5	1.5	1.5	1.5	1.5	1.5
θ Case-to-Ambient (No Heatsink)	17	14	11	9	7.1	6.6
θ Case-to-Ambient (With Heatsink)*	13	9	5.5	5	3.9	3.4



NOTES:

1. This table applies to 80960CA PGA plugged into socket or soldered directly to board.
2. $\theta_{JA} = \theta_{JC} + \theta_{CA}$

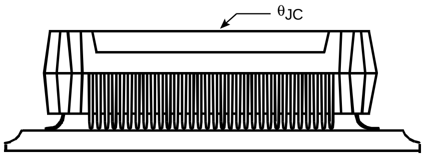
*0.285” high unidirectional heatsink (Al alloy 6061, 50 mil fin width, 150 mil center-to-center fin spacing).

Table 12. 80960CA PQFP Package Thermal Characteristics

Parameter	Thermal Resistance — °C/Watt						
	Airflow — ft./min (m/sec)						
	0 (0)	50 (0.25)	100 (0.50)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)
θ Junction-to-Case (Case Measured as shown in Figure 5)	5	5	5	5	5	5	5
θ Case-to-Ambient (No Heatsink)	19	18	17	15	12	10	9

NOTES:

1. This table applies to 80960CA PQFP soldered directly to board.
2. $\theta_{JA} = \theta_{JC} + \theta_{CA}$



3.5 Stepping Register Information

Upon reset, register g0 contains die stepping information. Figure 6 shows how g0 is configured. The most significant byte contains an ASCII 0. The upper middle byte contains an ASCII C. The lower middle byte contains an ASCII A. The least significant byte contains the stepping number in ASCII. g0 retains this information until it is overwritten by the user program.

ASCII	00	43	41	Stepping Number
DECIMAL	0	C	A	Stepping Number
	MSB			LSB

Figure 6. Register g0

Table 13 contains a cross reference of the number in the least significant byte of register g0 to the die stepping number.

Table 13. Die Stepping Cross Reference

g0 Least Significant Byte	Die Stepping
01	B
02	C-1
03	C-2,C-3
04	D

3.6 Suggested Sources for 80960CA Accessories

The following is a list of suggested sources for 80960CA accessories. This is not an endorsement of any kind, nor is it a warranty of the performance of any of the listed products and/or companies.

Sockets

1. 3M Textool Test and Interconnection
   Products Department
   P.O. Box 2963
   Austin, TX 78769-2963
2. Augat, Inc.
   Interconnection Products Group
   33 Perry Avenue
   P.O. box 779
   Attleboro, MA 02703
   (508) 699-7646
3. Concept Manufacturing, Inc.
   (Decoupling Sockets)
   41484 Christy Street
   Fremont, CA 94538
   (415) 651-3804

Heatsinks/Fins

1. Thermalloy, Inc.
   2021 West Valley View Lane
   Dallas, TX 75234-8993
   (214) 243-4321
   FAX: (214) 241-4656
2. E G & G Division
   60 Audubon Road
   Wakefield, MA 01880
   (617) 245-5900

4.0 ELECTRICAL SPECIFICATIONS

4.1 Absolute Maximum Ratings

Parameter	Maximum Rating
Storage Temperature	–65°C to +150°C
Case Temperature Under Bias	–65°C to +110°C
Supply Voltage wrt. V_{SS}	–0.5V to + 6.5V
Voltage on Other Pins wrt. V_{SS}	–0.5V to V_{CC} + 0.5V

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

***WARNING:** *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

4.2 Operating Conditions

Table 14. Operating Conditions (80960CA-33, -25, -16)

Symbol	Parameter		Min	Max	Units	Notes
V_{CC}	Supply Voltage	80960CA-33	4.75	5.25	V	
		80960CA-25	4.50	5.50	V	
		80960CA-16	4.50	5.50	V	
f_{CLK2x}	Input Clock Frequency (2-x Mode)	80960CA-33	0	66.66	MHz	
		80960CA-25	0	50	MHz	
		80960CA-16	0	32	MHz	
f_{CLK1x}	Input Clock Frequency (1-x Mode)	80960CA-33	8	33.33	MHz	(1)
		80960CA-25	8	25	MHz	
		80960CA-16	8	16	MHz	
T_C	Case Temperature Under Bias	PGA Package	0	100	°C	
	80960CA-33, -25, -16	196-Pin PQFP	0	100	°C	

NOTES:

1. When in the 1-x input clock mode, CLKIN is an input to an internal phase-locked loop and must maintain a minimum frequency of 8 MHz for proper processor operation. However, in the 1-x mode, CLKIN may still be stopped when the processor either is in a reset condition or is reset. If CLKIN is stopped, the specified RESET low time must be provided once CLKIN restarts and has stabilized.

4.3 Recommended Connections

Power and ground connections must be made to multiple V_{CC} and V_{SS} (GND) pins. Every 80960CA-based circuit board should include power (V_{CC}) and ground (V_{SS}) planes for power distribution. Every V_{CC} pin must be connected to the power plane, and every V_{SS} pin must be connected to the ground plane. Pins identified as "NC" **must not** be connected in the system.

Liberal decoupling capacitance should be placed near the 80960CA. The processor can cause transient power surges when its numerous output buffers transition, particularly when connected to large capacitive loads.

Low inductance capacitors and interconnects are recommended for best high frequency electrical performance. Inductance can be reduced by shortening the board traces between the processor and decoupling capacitors as much as possible. Capacitors specifically designed for PGA packages will offer the lowest possible inductance.

For reliable operation, always connect unused inputs to an appropriate signal level. In particular, any unused interrupt (XINT, NMI) or DMA (DREQ) input should be connected to V_{CC} through a pull-up resistor, as should BTERM if not used. Pull-up resistors should be in the range of 20 KΩ for each pin tied high. If READY or HOLD are not used, the unused input should be connected to ground. **N.C. pins must always remain unconnected.** Refer to the *i960® Cx Microprocessor User's Manual* (Order Number 270710) for more information.

4.4 DC Specifications

Table 15. DC Characteristics

(80960CA-33, -25, -16 under the conditions described in **Section 4.2, Operating Conditions**.)

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input Low Voltage for all pins except $\overline{\text{RESET}}$	– 0.3	+0.8	V	
V_{IH}	Input High Voltage for all pins except $\overline{\text{RESET}}$	2.0	V_{CC} + 0.3	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 5 mA
V_{OH}	Output High Voltage I_{OH} = –1 mA I_{OH} = – 200 µA	 2.4 V_{CC} – 0.5		 V V	
V_{ILR}	Input Low Voltage for $\overline{\text{RESET}}$	– 0.3	1.5	V	
V_{IHR}	Input High Voltage for $\overline{\text{RESET}}$	3.5	V_{CC} + 0.3	V	
I_{LI1}	Input Leakage Current for each pin *except*: $\overline{\text{BTERM}}$, $\overline{\text{ONCE}}$, $\overline{\text{DREQ3:0}}$, STEST, $\overline{\text{EOP3:0/TC3:0}}$, $\overline{\text{NMI}}$, $\overline{\text{XINT7:0}}$, $\overline{\text{BOFF}}$, $\overline{\text{READY}}$, HOLD, CLKMODE		±15	µA	0 ≤ V_{IN} ≤ V_{CC} (1)
I_{LI2}	Input Leakage Current for: $\overline{\text{BTERM}}$, $\overline{\text{ONCE}}$, $\overline{\text{DREQ3:0}}$, STEST, $\overline{\text{EOP3:0/TC3:0}}$, $\overline{\text{NMI}}$, $\overline{\text{XINT7:0}}$, $\overline{\text{BOFF}}$	0	– 300	µA	V_{IN} = 0.45V (2)
I_{LI3}	Input Leakage Current for: $\overline{\text{READY}}$, HOLD, CLKMODE	0	500	µA	V_{IN} = 2.4V (3,7)
I_{LO}	Output Leakage Current		±15	µA	0.45 ≤ V_{OUT} ≤ V_{CC}
I_{CC}	Supply Current (80960CA-33): I_{CC} Max I_{CC}Typ		 900 750	 mA mA	 (4) (5)
I_{CC}	Supply Current (80960CA-25): I_{CC} Max I_{CC}Typ		 750 600	 mA mA	 (4) (5)
I_{CC}	Supply Current (80960CA-16): I_{CC} Max I_{CC}Typ		 550 400	 mA mA	 (4) (5)
I_{ONCE}	ONCE-mode Supply Current		100	mA	
C_{IN}	Input Capacitance for: CLKIN, $\overline{\text{RESET}}$, $\overline{\text{ONCE}}$, $\overline{\text{READY}}$, HOLD, $\overline{\text{DREQ3:0}}$, $\overline{\text{BOFF}}$, $\overline{\text{XINT7:0}}$, $\overline{\text{NMI}}$, $\overline{\text{BTERM}}$, CLKMODE	0	12	pF	F_C = 1 MHz
C_{OUT}	Output Capacitance of each output pin		12	pF	F_C = 1 MHz (6)
$C_{I/O}$	I/O Pin Capacitance		12	pF	F_C = 1 MHz

NOTES:
1. No pullup or pulldown.
2. These pins have internal pullup resistors.
3. These pins have internal pulldown resistors.
4. Measured at worst case frequency, V_{CC} and temperature, with device operating and outputs loaded to the test conditions described in **Section 4.5.1, AC Test Conditions.**
5. I_{CC} Typical is not tested.
6. Output Capacitance is the capacitive load of a floating output.
7. CLKMODE pin has a pulldown resistor only when $\overline{\text{ONCE}}$ pin is deasserted.

4.5 AC Specifications

Table 16. 80960CA AC Characteristics (33 MHz)

(80960CA-33 only, under the conditions described in **Section 4.2, Operating Conditions** and **Section 4.5.1, AC Test Conditions**.)

Symbol	Parameter		Min	Max	Units	Notes
Input Clock (1,9)						
T_F	CLKIN Frequency		0	66.66	MHz	
T_C	CLKIN Period	In 1-x Mode (f_{CLK1x}) In 2-x Mode (f_{CLK2x})	30 15	125 ∞	ns ns	(11)
T_{CS}	CLKIN Period Stability	In 1-x Mode (f_{CLK1x})		±0.1%	Δ	(12)
T_{CH}	CLKIN High Time	In 1-x Mode (f_{CLK1x}) In 2-x Mode (f_{CLK2x})	6 6	62.5 ∞	ns ns	(11)
T_{CL}	CLKIN Low Time	In 1-x Mode (f_{CLK1x}) In 2-x Mode (f_{CLK2x})	6 6	62.5 ∞	ns ns	(11)
T_{CR}	CLKIN Rise Time		0	6	ns	
T_{CF}	CLKIN Fall Time		0	6	ns	
Output Clocks (1,8)						
T_{CP}	CLKIN to PCLK2:1 Delay	In 1-x Mode (f_{CLK1x}) In 2-x Mode (f_{CLK2x})	– 2 2	2 25	ns ns	(3,12) (3)
T	PCLK2:1 Period	In 1-x Mode (f_{CLK1x}) In 2-x Mode (f_{CLK2x})	T_C $2T_C$		ns ns	(12) (3)
T_{PH}	PCLK2:1 High Time		(T/2) – 2	T/2	ns	(12)
T_{PL}	PCLK2:1 Low Time		(T/2) – 2	T/2	ns	(12)
T_{PR}	PCLK2:1 Rise Time		1	4	ns	(3)
T_{PF}	PCLK2:1 Fall Time		1	4	ns	(3)
Synchronous Outputs (8)						
T_{OH} T_{OV}	Output Valid Delay, Output Hold					(6,10)
	T_{OH1}, T_{OV1}	A31:2	3	14	ns	
	T_{OH2}, T_{OV2}	BE3:0	3	16	ns	
	T_{OH3}, T_{OV3}	ADS	6	18	ns	
	T_{OH4}, T_{OV4}	W/R	3	18	ns	
	T_{OH5}, T_{OV5}	D/C, SUP, DMA	4	16	ns	
	T_{OH6}, T_{OV6}	BLAST, WAIT	5	16	ns	
	T_{OH7}, T_{OV7}	DEN	3	16	ns	
	T_{OH8}, T_{OV8}	HOLDA, BREQ	4	16	ns	
	T_{OH9}, T_{OV9}	LOCK	4	16	ns	
	T_{OH10}, T_{OV10}	DACK3:0	4	18	ns	
	T_{OH11}, T_{OV11}	D31:0	3	16	ns	
	T_{OH12}, T_{OV12}	DT/R	T/2 + 3	T/2 + 14	ns	
	T_{OH13}, T_{OV13}	FAIL	2	14	ns	
	T_{OH14}, T_{OV14}	EOP3:0/TC3:0	3	18	ns	(6,10)
T_{OF}	Output Float for all outputs		3	22	ns	(6)
Synchronous Inputs (1,9,10)						
T_{IS}	Input Setup					
	T_{IS1}	D31:0	3		ns	
	T_{IS2}	BOFF	17		ns	
	T_{IS3}	BTERM/READY	7		ns	
	T_{IS4}	HOLD	7		ns	
T_{IH}	Input Hold					
	T_{IH1}	D31:0	5		ns	
	T_{IH2}	BOFF	5		ns	
	T_{IH3}	BTERM/READY	2		ns	
	T_{IH4}	HOLD	3		ns	

Table 16. 80960CA AC Characteristics (33 MHz) (Continued)

(80960CA-33 only, under the conditions described in **Section 4.2, Operating Conditions** and **Section 4.5.1, AC Test Conditions**.)

Symbol	Parameter	Min	Max	Units	Notes
Relative Output Timings (1,2,3,8)					
T_{AVSH1}	A31:2 Valid to $\overline{\text{ADS}}$ Rising	T – 4	T + 4	ns	
T_{AVSH2}	$\overline{\text{BE3:0}}$, W/$\overline{\text{R}}$, $\overline{\text{SUP}}$, D/$\overline{\text{C}}$, $\overline{\text{DMA}}$, $\overline{\text{DACK3:0}}$ Valid to $\overline{\text{ADS}}$ Rising	T – 6	T + 6	ns	
T_{AVEL1}	A31:2 Valid to $\overline{\text{DEN}}$ Falling	T – 4	T + 4	ns	
T_{AVEL2}	$\overline{\text{BE3:0}}$, W/$\overline{\text{R}}$, $\overline{\text{SUP}}$, $\overline{\text{INST}}$, $\overline{\text{DMA}}$, $\overline{\text{DACK3:0}}$ Valid to $\overline{\text{DEN}}$ Falling	T – 6	T + 6	ns	
T_{NLQV}	$\overline{\text{WAIT}}$ Falling to Output Data Valid	± 4		ns	
T_{DVNH}	Output Data Valid to $\overline{\text{WAIT}}$ Rising	N*T – 4	N*T + 4	ns	(4)
T_{NLNH}	$\overline{\text{WAIT}}$ Falling to $\overline{\text{WAIT}}$ Rising	N*T ± 4		ns	(4)
T_{NHQX}	Output Data Hold after $\overline{\text{WAIT}}$ Rising	(N+1)*T–8	(N+1)*T+6	ns	(5)
T_{EHTV}	DT/$\overline{\text{R}}$ Hold after $\overline{\text{DEN}}$ High	T/2 – 7	∞	ns	(6)
T_{TVEL}	DT/$\overline{\text{R}}$ Valid to $\overline{\text{DEN}}$ Falling	T/2 – 4		ns	
Relative Input Timings (1,2,3)					
T_{IS5}	$\overline{\text{RESET}}$ Input Setup (2-x Clock Mode)	6		ns	(13)
T_{IH5}	$\overline{\text{RESET}}$ Input Hold (2-x Clock Mode)	5		ns	(13)
T_{IS6}	$\overline{\text{DREQ3:0}}$ Input Setup	12		ns	(7)
T_{IH6}	$\overline{\text{DREQ3:0}}$ Input Hold	7		ns	(7)
T_{IS7}	XINT7:0, $\overline{\text{NMI}}$ Input Setup	7		ns	(15)
T_{IH7}	XINT7:0, $\overline{\text{NMI}}$ Input Hold	3		ns	(15)
T_{IS8}	$\overline{\text{RESET}}$ Input Setup (1-x Clock Mode)	3		ns	(14)
T_{IH8}	$\overline{\text{RESET}}$ Input Hold (1-x Clock Mode)	T/4 + 1		ns	(14)

NOTES:

1. See **Section 4.5.2, AC Timing Waveforms** for waveforms and definitions.
2. See Figure 16 for capacitive derating information for output delays and hold times.
3. See Figure 17 for capacitive derating information for rise and fall times.
4. Where N is the number of N_{RAD}, N_{RDD}, N_{WAD} or N_{WDD} wait states that are programmed in the Bus Controller Region Table. $\overline{\text{WAIT}}$ never goes active when there are no wait states in an access.
5. N = Number of wait states inserted with $\overline{\text{READY}}$.
6. Output Data and/or DT/$\overline{\text{R}}$ may be driven indefinitely following a cycle if there is no subsequent bus activity.
7. Since asynchronous inputs are synchronized internally by the 80960CA, they have no required setup or hold times to be recognized and for proper operation. However, to guarantee recognition of the input at a particular edge of PCLK2:1, the setup times shown must be met. Asynchronous inputs must be active for at least two consecutive PCLK2:1 rising edges to be seen by the processor.
8. These specifications are guaranteed by the processor.
9. These specifications must be met by the system for proper operation of the processor.
10. This timing is dependent upon the loading of PCLK2:1. Use the derating curves of **Section 4.5.3, Derating Curves** to adjust the timing for PCLK2:1 loading.
11. In the 1-x input clock mode, the maximum input clock period is limited to 125 ns while the processor is operating. When the processor is in reset, the input clock may stop even in 1-x mode.
12. When in the 1-x input clock mode, these specifications assume a stable input clock with a period variation of less than ± 0.1% between adjacent cycles.
13. In 2-x clock mode, $\overline{\text{RESET}}$ is an asynchronous input which has no required setup and hold time for proper operation. However, to guarantee the device exits reset synchronized to a particular clock edge, the $\overline{\text{RESET}}$ pin must meet setup and hold times to the falling edge of the CLKIN. (See Figure 22.)
14. In 1-x clock mode, $\overline{\text{RESET}}$ is an asynchronous input which has no required setup and hold time for proper operation. However, to guarantee the device exits reset synchronized to a particular clock edge, the $\overline{\text{RESET}}$ pin must meet setup and hold times to the rising edge of the CLKIN. (See Figure 23.)
15. The interrupt pins are synchronized internally by the 80960CA. They have no required setup or hold times for proper operation. These pins are sampled by the interrupt controller every other clock and must be active for at least three consecutive PCLK2:1 rising edges when asserting them asynchronously. To guarantee recognition at a particular clock edge, the setup and hold times shown must be met for two consecutive PCLK2:1 rising edges.

Table 17. 80960CA AC Characteristics (25 MHz)

(80960CA-25 only, under conditions described in **Section 4.2, Operating Conditions** and **Section 4.5.1, AC Test Conditions**.)

Symbol	Parameter		Min	Max	Units	Notes
Input Clock (1,9)						
T_F	CLKIN Frequency		0	50	MHz	
T_C	CLKIN Period	In 1-x Mode (f_{CLK1x}) In 2-x Mode (f_{CLK2x})	40 20	125 ∞	ns ns	(11)
T_{CS}	CLKIN Period Stability	In 1-x Mode (f_{CLK1x})		±0.1%	Δ	(12)
T_{CH}	CLKIN High Time	In 1-x Mode (f_{CLK1x}) In 2-x Mode (f_{CLK2x})	8 8	62.5 ∞	ns ns	(11)
T_{CL}	CLKIN Low Time	In 1-x Mode (f_{CLK1x}) In 2-x Mode (f_{CLK2x})	8 8	62.5 ∞	ns ns	(11)
T_{CR}	CLKIN Rise Time		0	6	ns	
T_{CF}	CLKIN Fall Time		0	6	ns	
Output Clocks (1,8)						
T_{CP}	CLKIN to PCLK2:1 Delay	In 1-x Mode (f_{CLK1x}) In 2-x Mode (f_{CLK2x})	– 2 2	2 25	ns ns	(3,12) (3)
T	PCLK2:1 Period	In 1-x Mode (f_{CLK1x}) In 2-x Mode (f_{CLK2x})	T_C $2T_C$		ns ns	(12) (3)
T_{PH}	PCLK2:1 High Time		(T/2) – 3	T/2	ns	(12)
T_{PL}	PCLK2:1 Low Time		(T/2) – 3	T/2	ns	(12)
T_{PR}	PCLK2:1 Rise Time		1	4	ns	(3)
T_{PF}	PCLK2:1 Fall Time		1	4	ns	(3)
Synchronous Outputs (8)						
T_{OH} T_{OV}	Output Valid Delay, Output Hold					(6,10)
	T_{OH1}, T_{OV1}	A31:2	3	16	ns	
	T_{OH2}, T_{OV2}	BE3:0	3	18	ns	
	T_{OH3}, T_{OV3}	ADS	6	20	ns	
	T_{OH4}, T_{OV4}	W/R	3	20	ns	
	T_{OH5}, T_{OV5}	D/C, SUP, DMA	4	18	ns	
	T_{OH6}, T_{OV6}	BLAST, WAIT	5	18	ns	
	T_{OH7}, T_{OV7}	DEN	3	18	ns	
	T_{OH8}, T_{OV8}	HOLDA, BREQ	4	18	ns	
	T_{OH9}, T_{OV9}	LOCK	4	18	ns	
	T_{OH10}, T_{OV10}	DACK3:0	4	20	ns	
	T_{OH11}, T_{OV11}	D31:0	3	18	ns	
	T_{OH12}, T_{OV12}	DT/R	T/2 + 3	T/2 + 16	ns	
	T_{OH13}, T_{OV13}	FAIL	2	16	ns	
	T_{OH14}, T_{OV14}	EOP3:0/TC3:0	3	20	ns	(6,10)
T_{OF}	Output Float for all outputs		3	22	ns	(6)
Synchronous Inputs (1,9,10)						
T_{IS}	Input Setup					
	T_{IS1}	D31:0	5		ns	
	T_{IS2}	BOFF	19		ns	
	T_{IS3}	BTERM/READY	9		ns	
	T_{IS4}	HOLD	9		ns	
T_{IH}	Input Hold					
	T_{IH1}	D31:0	5		ns	
	T_{IH2}	BOFF	7		ns	
	T_{IH3}	BTERM/READY	2		ns	
	T_{IH4}	HOLD	5		ns	

Table 17. 80960CA AC Characteristics (25 MHz) (Continued)

(80960CA-25 only, under conditions described in **Section 4.2, Operating Conditions** and **Section 4.5.1, AC Test Conditions**.)

Symbol	Parameter	Min	Max	Units	Notes
Relative Output Timings (1,2,3,8)					
T_{AVSH1}	A31:2 Valid to ADS Rising	T – 4	T + 4	ns	
T_{AVSH2}	BE3:0, W/R, SUP, D/C, DMA, DACK3:0 Valid to ADS Rising	T – 6	T + 6	ns	
T_{AVEL1}	A31:2 Valid to DEN Falling	T – 4	T + 4	ns	
T_{AVEL2}	BE3:0, W/R, SUP, INST, DMA, DACK3:0 Valid to DEN Falling	T – 6	T + 6	ns	
T_{NLQV}	WAIT Falling to Output Data Valid	± 4		ns	
T_{DVNH}	Output Data Valid to WAIT Rising	N*T – 4	N*T + 4	ns	(4)
T_{NLNH}	WAIT Falling to WAIT Rising	N*T ± 4		ns	(4)
T_{NHQX}	Output Data Hold after WAIT Rising	(N+1)*T–8	(N+1)*T+6	ns	(5)
T_{EHTV}	DT/R Hold after DEN High	T/2 – 7	∞	ns	(6)
T_{TVEL}	DT/R Valid to DEN Falling	T/2 – 4		ns	
Relative Input Timings (1,2,3)					
T_{IS5}	RESET Input Setup (2-x Clock Mode)	8		ns	(13)
T_{IH5}	RESET Input Hold (2-x Clock Mode)	7		ns	(13)
T_{IS6}	DREQ3:0 Input Setup	14		ns	(7)
T_{IH6}	DREQ3:0 Input Hold	9		ns	(7)
T_{IS7}	XINT7:0, NMI Input Setup	9		ns	(15)
T_{IH7}	XINT7:0, NMI Input Hold	5		ns	(15)
T_{IS8}	RESET Input Setup (1-x Clock Mode)	3		ns	(14)
T_{IH8}	RESET Input Hold (1-x Clock Mode)	T/4 + 1		ns	(14)

NOTES:

1. See **Section 4.5.2, AC Timing Waveforms** for waveforms and definitions.
2. See Figure 16 for capacitive derating information for output delays and hold times.
3. See Figure 17 for capacitive derating information for rise and fall times.
4. Where N is the number of N_{RAD}, N_{RDD}, N_{WAD} or N_{WDD} wait states that are programmed in the Bus Controller Region Table. WAIT never goes active when there are no wait states in an access.
5. N = Number of wait states inserted with READY.
6. Output Data and/or DT/R may be driven indefinitely following a cycle if there is no subsequent bus activity.
7. Since asynchronous inputs are synchronized internally by the 80960CA, they have no required setup or hold times to be recognized and for proper operation. However, to guarantee recognition of the input at a particular edge of PCLK2:1, the setup times shown must be met. Asynchronous inputs must be active for at least two consecutive PCLK2:1 rising edges to be seen by the processor.
8. These specifications are guaranteed by the processor.
9. These specifications must be met by the system for proper operation of the processor.
10. This timing is dependent upon the loading of PCLK2:1. Use the derating curves of **Section 4.5.3, Derating Curves** to adjust the timing for PCLK2:1 loading.
11. In the 1-x input clock mode, the maximum input clock period is limited to 125 ns while the processor is operating. When the processor is in reset, the input clock may stop even in 1-x mode.
12. When in the 1-x input clock mode, these specifications assume a stable input clock with a period variation of less than ± 0.1% between adjacent cycles.
13. In 2-x clock mode, RESET is an asynchronous input which has no required setup and hold time for proper operation. However, to guarantee the device exits reset synchronized to a particular clock edge, the RESET pin must meet setup and hold times to the falling edge of the CLKIN. (See Figure 22.)
14. In 1-x clock mode, RESET is an asynchronous input which has no required setup and hold time for proper operation. However, to guarantee the device exits reset synchronized to a particular clock edge, the RESET pin must meet setup and hold times to the rising edge of the CLKIN. (See Figure 23.)
15. The interrupt pins are synchronized internally by the 80960CA. They have no required setup or hold times for proper operation. These pins are sampled by the interrupt controller every other clock and must be active for at least three consecutive PCLK2:1 rising edges when asserting them asynchronously. To guarantee recognition at a particular clock edge, the setup and hold times shown must be met for two consecutive PCLK2:1 rising edges.

Table 18. 80960CA AC Characteristics (16 MHz)

(80960CA-16 only, under conditions described in **Section 4.2, Operating Conditions** and **Section 4.5.1, AC Test Conditions**.)

Symbol	Parameter		Min	Max	Units	Notes
Input Clock (1,9)						
T_F	CLKIN Frequency		0	32	MHz	
T_C	CLKIN Period	In 1-x Mode (f_{CLK1x})	62.5	125	ns	(11)
		In 2-x Mode (f_{CLK2x})	31.25	∞	ns	
T_{CS}	CLKIN Period Stability	In 1-x Mode (f_{CLK1x})		±0.1%	Δ	(12)
T_{CH}	CLKIN High Time	In 1-x Mode (f_{CLK1x})	10	62.5	ns	(11)
		In 2-x Mode (f_{CLK2x})	10	∞	ns	
T_{CL}	CLKIN Low Time	In 1-x Mode (f_{CLK1x})	10	62.5	ns	(11)
		In 2-x Mode (f_{CLK2x})	10	∞	ns	
T_{CR}	CLKIN Rise Time		0	6	ns	
T_{CF}	CLKIN Fall Time		0	6	ns	
Output Clocks (1,8)						
T_{CP}	CLKIN to PCLK2:1 Delay	In 1-x Mode (f_{CLK1x})	– 2	2	ns	(3,12)
		In 2-x Mode (f_{CLK2x})	2	25	ns	(3)
T	PCLK2:1 Period	In 1-x Mode (f_{CLK1x})	T_C		ns	(12)
		In 2-x Mode (f_{CLK2x})	$2T_C$		ns	(3)
T_{PH}	PCLK2:1 High Time		(T/2) – 4	T/2	ns	(12)
T_{PL}	PCLK2:1 Low Time		(T/2) – 4	T/2	ns	(12)
T_{PR}	PCLK2:1 Rise Time		1	4	ns	(3)
T_{PF}	PCLK2:1 Fall Time		1	4	ns	(3)
Synchronous Outputs (8)						
T_{OH} T_{OV}	Output Valid Delay, Output Hold					(6,10)
	T_{OH1}, T_{OV1}	A31:2	3	18	ns	
	T_{OH2}, T_{OV2}	BE3:0	3	20	ns	
	T_{OH3}, T_{OV3}	ADS	6	22	ns	
	T_{OH4}, T_{OV4}	W/R	3	22	ns	
	T_{OH5}, T_{OV5}	D/C, SUP, DMA	4	20	ns	
	T_{OH6}, T_{OV6}	BLAST, WAIT	5	20	ns	
	T_{OH7}, T_{OV7}	DEN	3	20	ns	
	T_{OH8}, T_{OV8}	HOLDA, BREQ	4	20	ns	
	T_{OH9}, T_{OV9}	LOCK	4	20	ns	
	T_{OH10}, T_{OV10}	DACK3:0	4	22	ns	
	T_{OH11}, T_{OV11}	D31:0	3	20	ns	
	T_{OH12}, T_{OV12}	DT/R	T/2 + 3	T/2 + 18	ns	
	T_{OH13}, T_{OV13}	FAIL	2	18	ns	
	T_{OH14}, T_{OV14}	EOP3:0/TC3:0	3	22	ns	(6,10)
T_{OF}	Output Float for all outputs		3	22	ns	(6)
Synchronous Inputs (1,9,10)						
T_{IS}	Input Setup					
	T_{IS1}	D31:0	5		ns	
	T_{IS2}	BOFF	21		ns	
	T_{IS3}	BTERM/READY	9		ns	
	T_{IS4}	HOLD	9		ns	
T_{IH}	Input Hold					
	T_{IH1}	D31:0	5		ns	
	T_{IH2}	BOFF	7		ns	
	T_{IH3}	BTERM/READY	2		ns	
	T_{IH4}	HOLD	5		ns	

Table 18. 80960CA AC Characteristics (16 MHz) (Continued)

(80960CA-16 only, under conditions described in **Section 4.2, Operating Conditions** and **Section 4.5.1, AC Test Conditions**.)

Symbol	Parameter	Min	Max	Units	Notes
Relative Output Timings (1,2,3,8)					
T_{AVSH1}	A31:2 Valid to $\overline{\text{ADS}}$ Rising	T – 4	T + 4	ns	
T_{AVSH2}	$\overline{\text{BE3:0}}$, W/$\overline{\text{R}}$, $\overline{\text{SUP}}$, D/$\overline{\text{C}}$, $\overline{\text{DMA}}$, $\overline{\text{DACK3:0}}$ Valid to $\overline{\text{ADS}}$ Rising	T – 6	T + 6	ns	
T_{AVEL1}	A31:2 Valid to $\overline{\text{DEN}}$ Falling	T – 6	T + 6	ns	
T_{AVEL2}	$\overline{\text{BE3:0}}$, W/$\overline{\text{R}}$, $\overline{\text{SUP}}$, $\overline{\text{INST}}$, $\overline{\text{DMA}}$, $\overline{\text{DACK3:0}}$ Valid to $\overline{\text{DEN}}$ Falling	T – 6	T + 6	ns	
T_{NLQV}	$\overline{\text{WAIT}}$ Falling to Output Data Valid	± 4		ns	
T_{DVNH}	Output Data Valid to $\overline{\text{WAIT}}$ Rising	N*T – 4	N*T + 4	ns	(4)
T_{NLNH}	$\overline{\text{WAIT}}$ Falling to $\overline{\text{WAIT}}$ Rising	N*T ± 4		ns	(4)
T_{NHQX}	Output Data Hold after $\overline{\text{WAIT}}$ Rising	(N+1)*T–8	(N+1)*T+6	ns	(5)
T_{EHTV}	DT/$\overline{\text{R}}$ Hold after $\overline{\text{DEN}}$ High	T/2 – 7	∞	ns	(6)
T_{TVEL}	DT/$\overline{\text{R}}$ Valid to $\overline{\text{DEN}}$ Falling	T/2 – 4		ns	
Relative Input Timings (1,2,3)					
T_{IS5}	$\overline{\text{RESET}}$ Input Setup (2-x Clock Mode)	10		ns	(13)
T_{IH5}	$\overline{\text{RESET}}$ Input Hold (2-x Clock Mode)	9		ns	(13)
T_{IS6}	$\overline{\text{DREQ3:0}}$ Input Setup	16		ns	(7)
T_{IH6}	$\overline{\text{DREQ3:0}}$ Input Hold	11		ns	(7)
T_{IS7}	$\overline{\text{XINT7:0}}$, $\overline{\text{NMI}}$ Input Setup	9		ns	(15)
T_{IH7}	$\overline{\text{XINT7:0}}$, $\overline{\text{NMI}}$ Input Hold	5		ns	(15)
T_{IS8}	$\overline{\text{RESET}}$ Input Setup (1-x Clock Mode)	3		ns	(14)
T_{IH8}	$\overline{\text{RESET}}$ Input Hold (1-x Clock Mode)	T/4 + 1		ns	(14)

NOTES:

1. See **Section 4.5.2, AC Timing Waveforms** for waveforms and definitions.
2. See Figure 16 for capacitive derating information for output delays and hold times.
3. See Figure 17 for capacitive derating information for rise and fall times.
4. Where N is the number of N_{RAD}, N_{RDD}, N_{WAD} or N_{WDD} wait states that are programmed in the Bus Controller Region Table. $\overline{\text{WAIT}}$ never goes active when there are no wait states in an access.
5. N = Number of wait states inserted with $\overline{\text{READY}}$.
6. Output Data and/or DT/$\overline{\text{R}}$ may be driven indefinitely following a cycle if there is no subsequent bus activity.
7. Since asynchronous inputs are synchronized internally by the 80960CA, they have no required setup or hold times to be recognized and for proper operation. However, to guarantee recognition of the input at a particular edge of PCLK2:1, the setup times shown must be met. Asynchronous inputs must be active for at least two consecutive PCLK2:1 rising edges to be seen by the processor.
8. These specifications are guaranteed by the processor.
9. These specifications must be met by the system for proper operation of the processor.
10. This timing is dependent upon the loading of PCLK2:1. Use the derating curves of **Section 4.5.3, Derating Curves** to adjust the timing for PCLK2:1 loading.
11. In the 1-x input clock mode, the maximum input clock period is limited to 125 ns while the processor is operating. When the processor is in reset, the input clock may stop even in 1-x mode.
12. When in the 1-x input clock mode, these specifications assume a stable input clock with a period variation of less than ± 0.1% between adjacent cycles.
13. In 2-x clock mode, $\overline{\text{RESET}}$ is an asynchronous input which has no required setup and hold time for proper operation. However, to guarantee the device exits reset synchronized to a particular clock edge, the $\overline{\text{RESET}}$ pin must meet setup and hold times to the falling edge of the CLKIN. (See Figure 22.)
14. In 1-x clock mode, $\overline{\text{RESET}}$ is an asynchronous input which has no required setup and hold time for proper operation. However, to guarantee the device exits reset synchronized to a particular clock edge, the $\overline{\text{RESET}}$ pin must meet setup and hold times to the rising edge of the CLKIN. (See Figure 23.)
15. The interrupt pins are synchronized internally by the 80960CA. They have no required setup or hold times for proper operation. These pins are sampled by the interrupt controller every other clock and must be active for at least three consecutive PCLK2:1 rising edges when asserting them asynchronously. To guarantee recognition at a particular clock edge, the setup and hold times shown must be met for two consecutive PCLK2:1 rising edges.

4.5.1 AC Test Conditions

The AC Specifications in Section 4.5 are tested with the 50 pF load shown in Figure 7. Figure 16 shows how timings vary with load capacitance.

Specifications are measured at the 1.5V crossing point, unless otherwise indicated. Input waveforms are assumed to have a rise and fall time of ≤ 2 ns from 0.8V to 2.0V. See **Section 4.5.2, AC Timing Waveforms** for AC spec definitions, test points and illustrations.

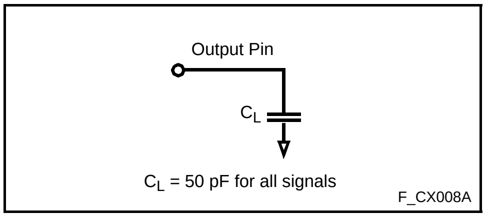


Figure 7. AC Test Load

4.5.2 AC Timing Waveforms

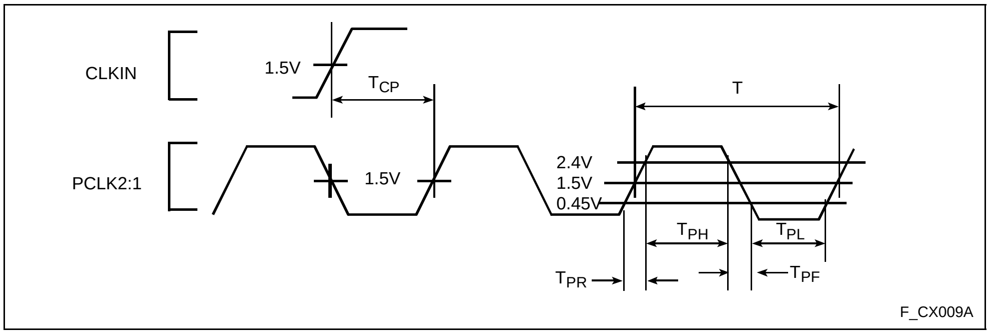


Figure 8. Input and Output Clocks Waveform

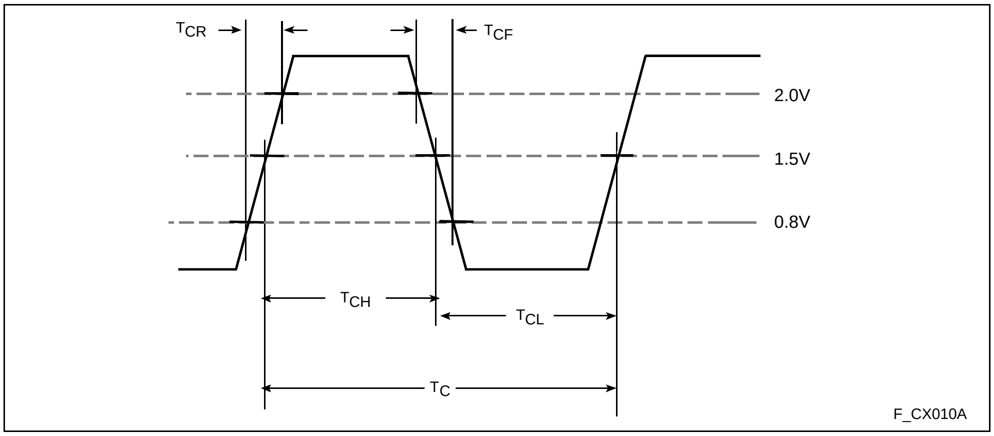


Figure 9. CLKIN Waveform

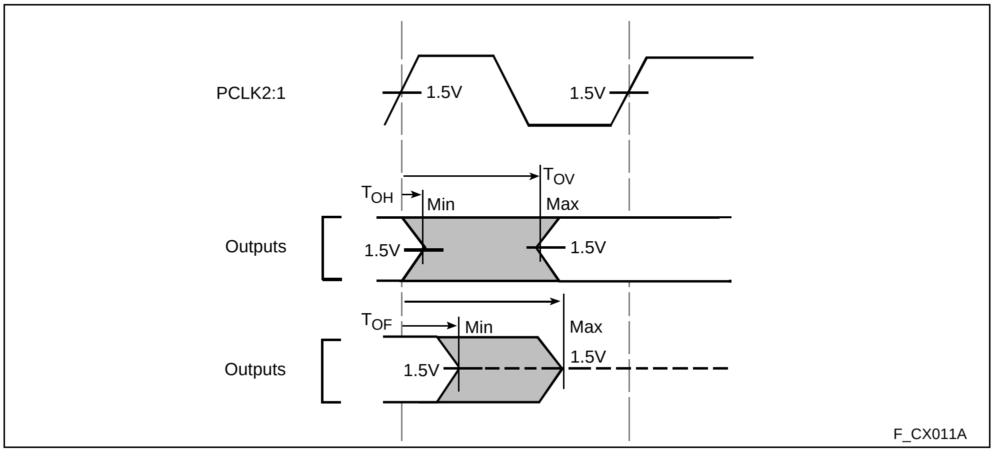


Figure 10. Output Delay and Float Waveform

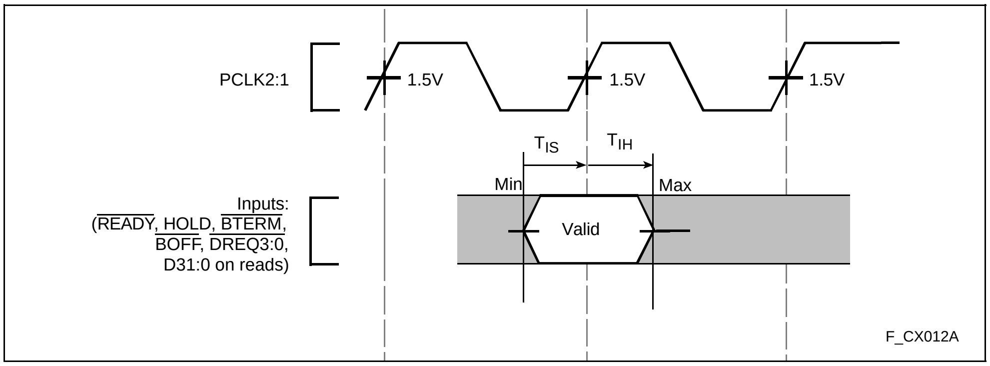


Figure 11. Input Setup and Hold Waveform

T_{OV} T_{OH}	- OUTPUT DELAY - The maximum output delay is referred to as the Output Valid Delay (T_{OV}). The minimum output delay is referred to as the Output Hold (T_{OH}).
T_{OF}	- OUTPUT FLOAT DELAY - The output float condition occurs when the maximum output current becomes less that I_{LO} in magnitude.
T_{IS} T_{IH}	- INPUT SETUP AND HOLD - The input setup and hold requirements specify the sampling window during which synchronous inputs must be stable for correct processor operation.

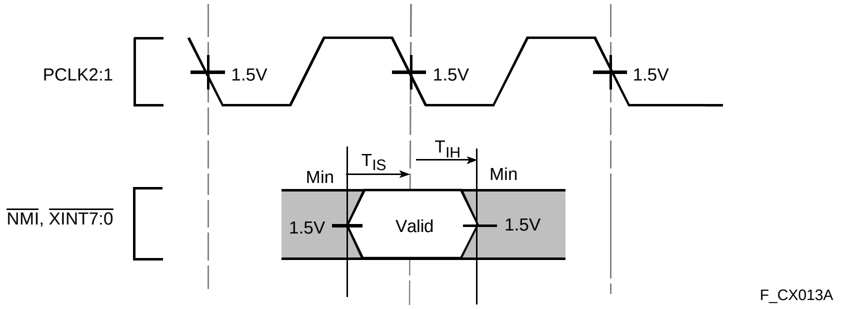
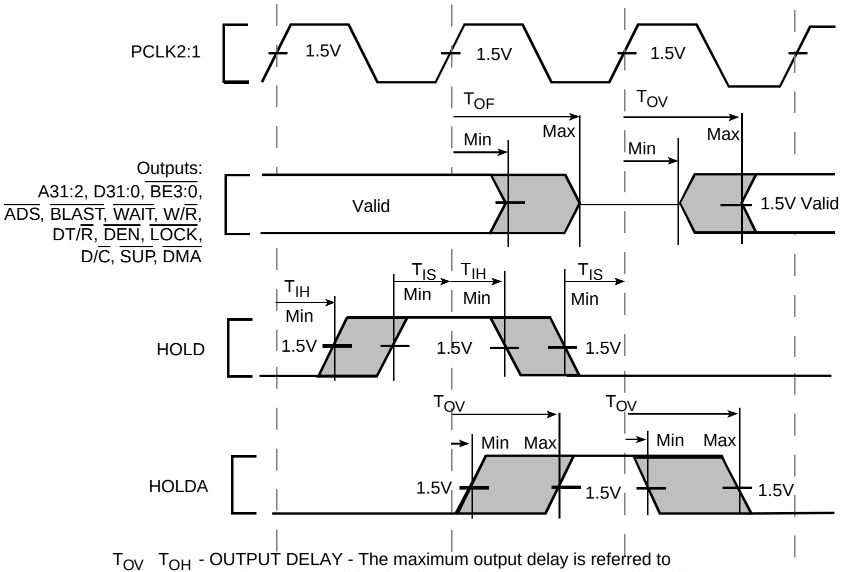


Figure 12. $\overline{\text{NMI}}$, $\overline{\text{XINT7:0}}$ Input Setup and Hold Waveform



T_{OV} T_{OH} - OUTPUT DELAY - The maximum output delay is referred to as the Output Valid Delay (T_{OV}). The minimum output delay is referred to as the Output Hold (T_{OH}).

T_{OF} - OUTPUT FLOAT DELAY - The output float condition occurs when the maximum output current becomes less that I_{LO} in magnitude.

T_{IS} T_{IH} - INPUT SETUP AND HOLD - The input setup and hold requirements specify the sampling window during which synchronous inputs must be stable for correct processor operation.

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Figure 13. Hold Acknowledge Timings

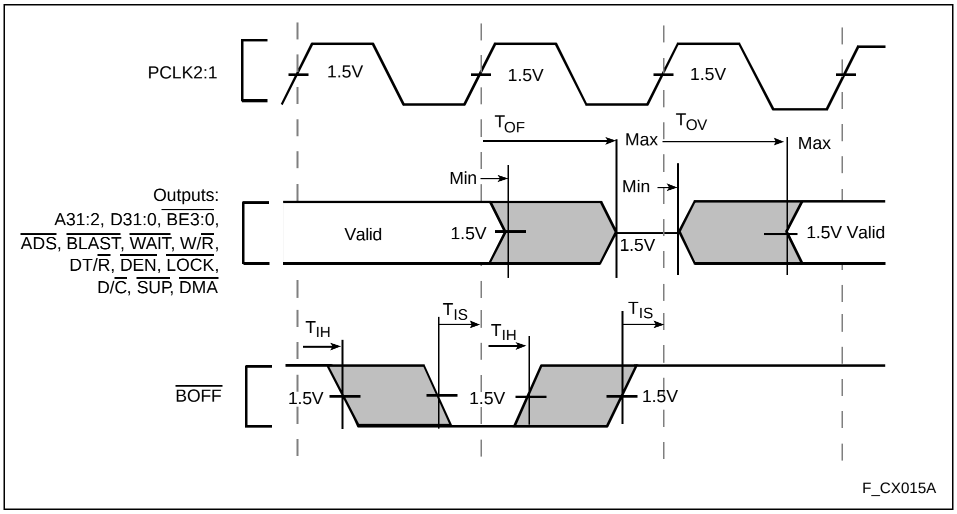


Figure 14. Bus Backoff ($\overline{\text{BOFF}}$) Timings

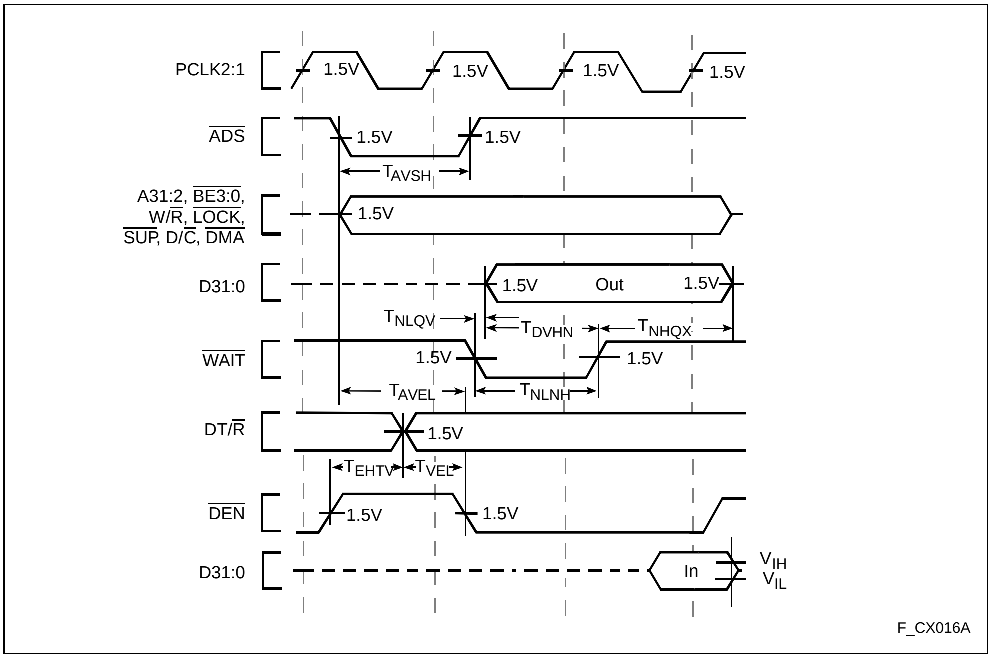


Figure 15. Relative Timings Waveforms

4.5.3 Derating Curves

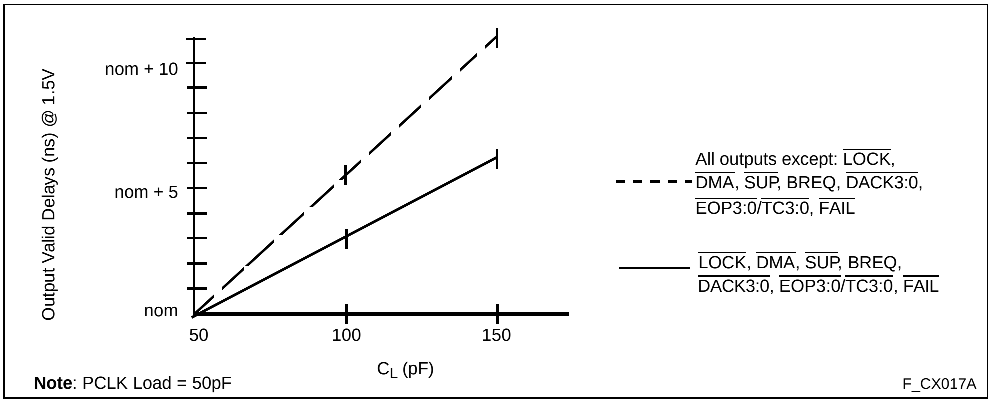
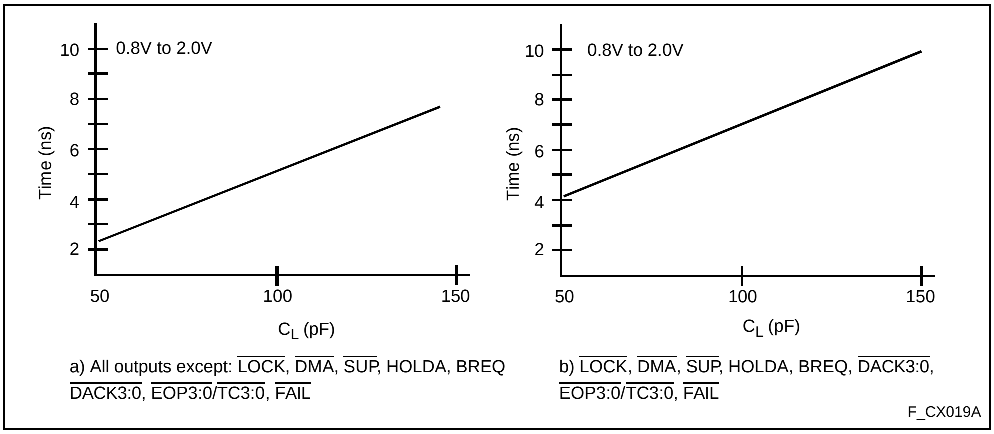


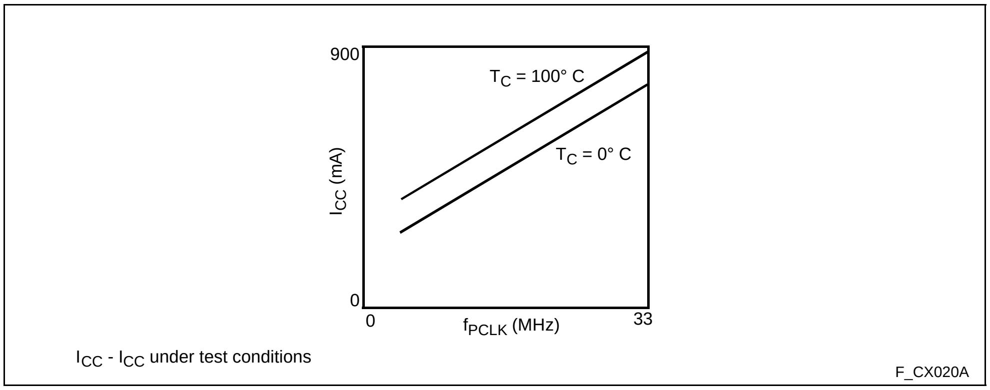
Figure 16. Output Delay or Hold vs. Load Capacitance



a) All outputs except: $\overline{\text{LOCK}}$, $\overline{\text{DMA}}$, $\overline{\text{SUP}}$, HOLDA, BREQ $\overline{\text{DACK3:0}}$, $\overline{\text{EOP3:0}}$/$\overline{\text{TC3:0}}$, $\overline{\text{FAIL}}$

b) $\overline{\text{LOCK}}$, $\overline{\text{DMA}}$, $\overline{\text{SUP}}$, HOLDA, BREQ, $\overline{\text{DACK3:0}}$, $\overline{\text{EOP3:0}}$/$\overline{\text{TC3:0}}$, $\overline{\text{FAIL}}$

Figure 17. Rise and Fall Time Derating at Highest Operating Temperature and Minimum V_{CC}



I_{CC} - I_{CC} under test conditions

Figure 18. I_{CC} vs. Frequency and Temperature

5.0 RESET, BACKOFF AND HOLD ACKNOWLEDGE

Table 19 lists the condition of each processor output pin while $\overline{\text{RESET}}$ is asserted (low).

Table 19. Reset Conditions

Pins	State During Reset (HOLDA inactive)[1]
A31:2	Floating
D31:0	Floating
$\overline{\text{BE3:0}}$	Driven high (Inactive)
W/$\overline{\text{R}}$	Driven low (Read)
$\overline{\text{ADS}}$	Driven high (Inactive)
$\overline{\text{WAIT}}$	Driven high (Inactive)
$\overline{\text{BLAST}}$	Driven low (Active)
DT/$\overline{\text{R}}$	Driven low (Receive)
$\overline{\text{DEN}}$	Driven high (Inactive)
$\overline{\text{LOCK}}$	Driven high (Inactive)
BREQ	Driven low (Inactive)
D/$\overline{\text{C}}$	Floating
$\overline{\text{DMA}}$	Floating
$\overline{\text{SUP}}$	Floating
$\overline{\text{FAIL}}$	Driven low (Active)
$\overline{\text{DACK3:0}}$	Driven high (Inactive)
$\overline{\text{EOP3:0}}$/$\overline{\text{TC3:0}}$	Floating (Set to input mode)

NOTES:

1. With regard to bus output pin state only, the Hold Acknowledge state takes precedence over the reset state. Although asserting the $\overline{\text{RESET}}$ pin will internally reset the processor, the processor's bus output pins will not enter the reset state if it has granted Hold Acknowledge to a previous HOLD request (HOLDA is active). Furthermore, the processor will grant new HOLD requests and enter the Hold Acknowledge state even while in reset.
   For example, if HOLDA is inactive and the processor is in the reset state, then HOLD is asserted, the processor's bus pins enter the Hold Acknowledge state and HOLDA is granted. The processor will not be able to perform memory accesses until the HOLD request is removed, even if the $\overline{\text{RESET}}$ pin is brought high. This operation is provided to simplify boot-up synchronization among multiple processors sharing the same bus.

Table 20 lists the condition of each processor output pin while HOLDA is asserted (low).

Table 20. Hold Acknowledge and Backoff Conditions

Pins	State During HOLDA
A31:2	Floating
D31:0	Floating
$\overline{\text{BE3:0}}$	Floating
W/$\overline{\text{R}}$	Floating
$\overline{\text{ADS}}$	Floating
$\overline{\text{WAIT}}$	Floating
$\overline{\text{BLAST}}$	Floating
DT/$\overline{\text{R}}$	Floating
$\overline{\text{DEN}}$	Floating
$\overline{\text{LOCK}}$	Floating
BREQ	Driven (High or low)
D/$\overline{\text{C}}$	Floating
$\overline{\text{DMA}}$	Floating
$\overline{\text{SUP}}$	Floating
$\overline{\text{FAIL}}$	Driven high (Inactive)
$\overline{\text{DACK3:0}}$	Driven high (Inactive)
$\overline{\text{EOP3:0}}$/$\overline{\text{TC3:0}}$	Driven (If output)

6.0 BUS WAVEFORMS

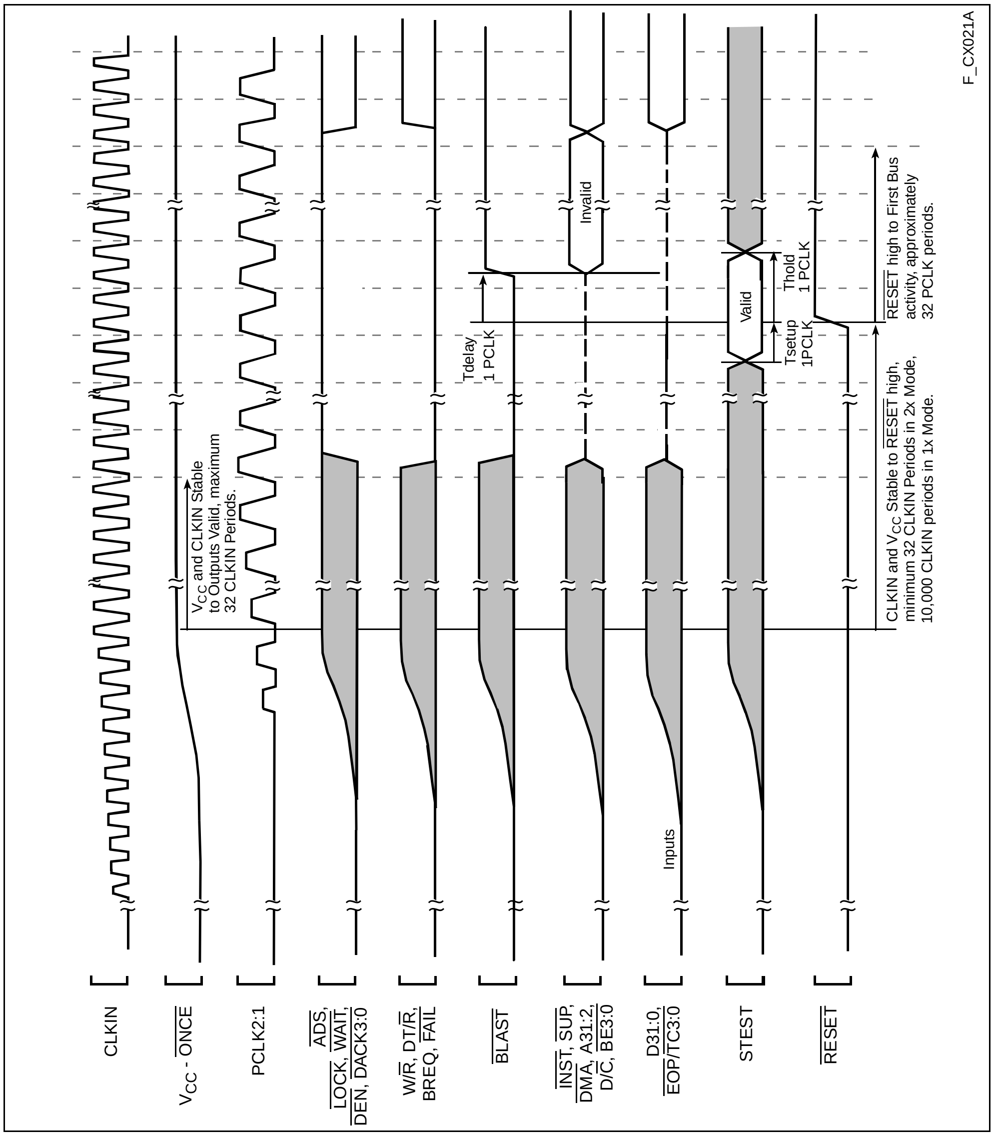


Figure 19. Cold Reset Waveform

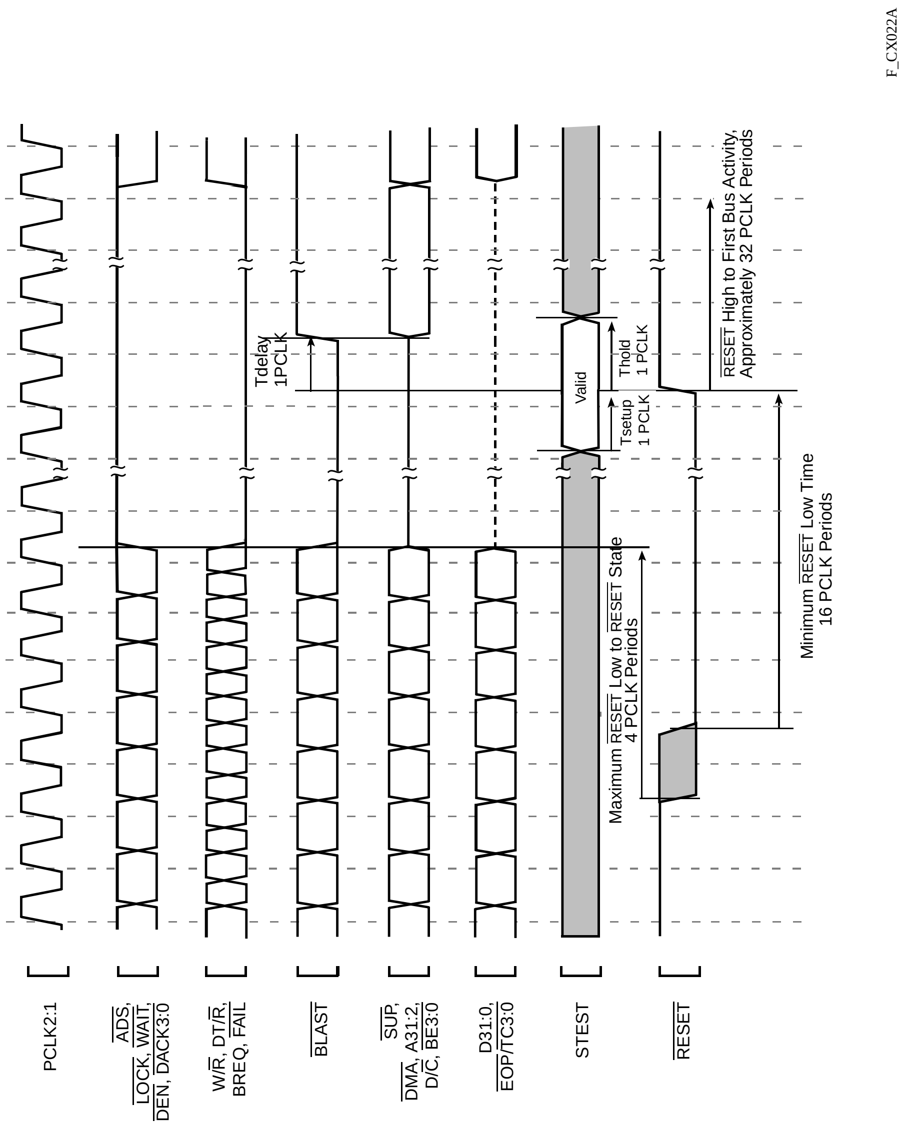


Figure 20. Warm Reset Waveform

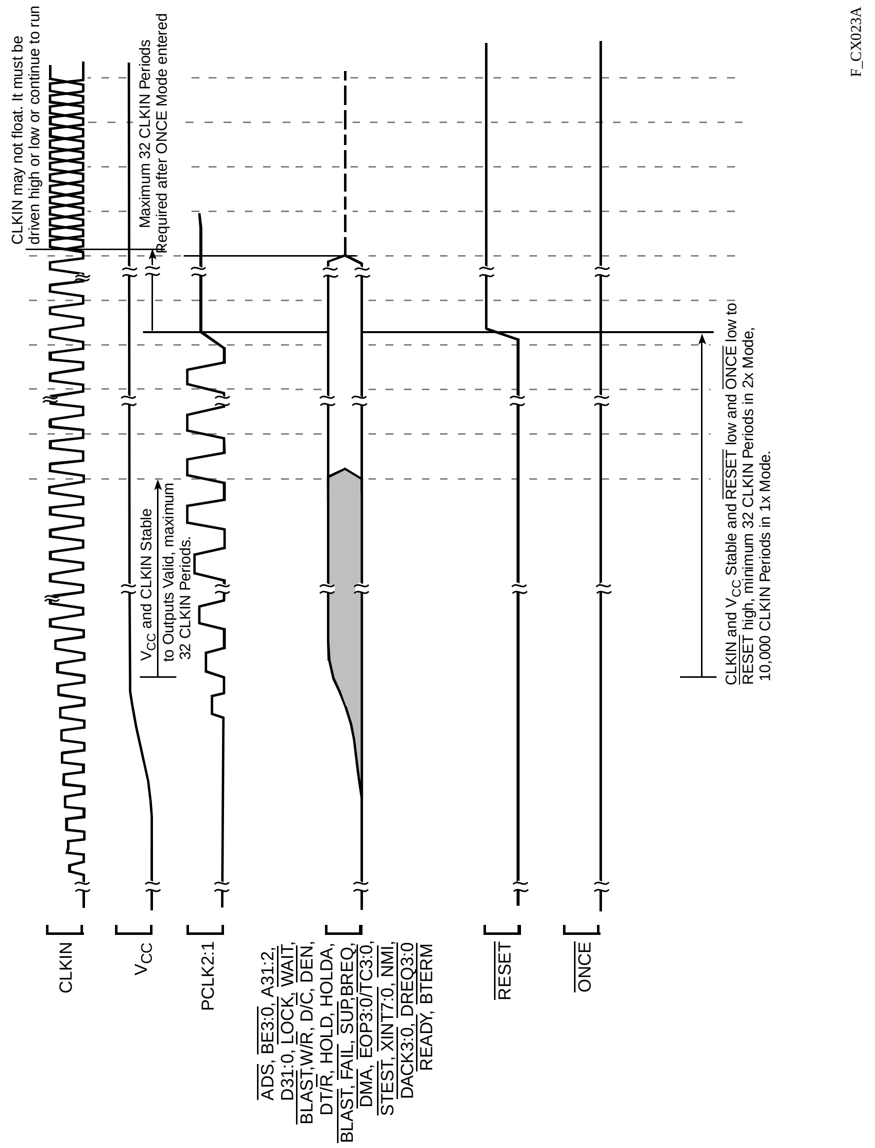
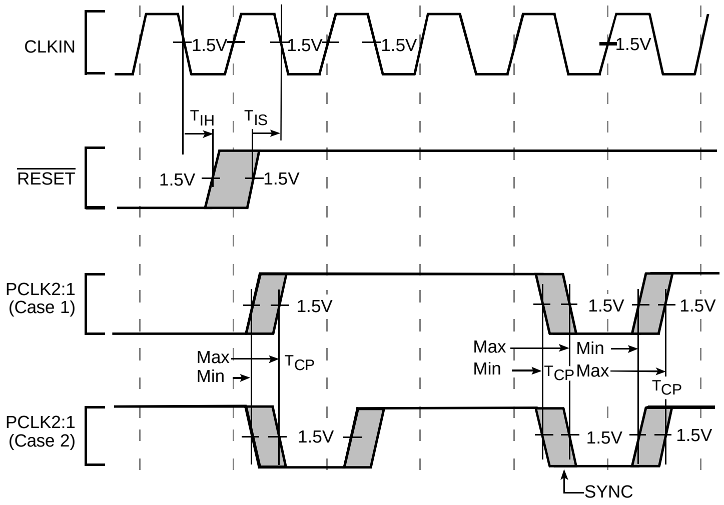


Figure 21. Entering the ONCE State



Note: Case 1 and Case 2 show two possible polarities of PCLK2:1

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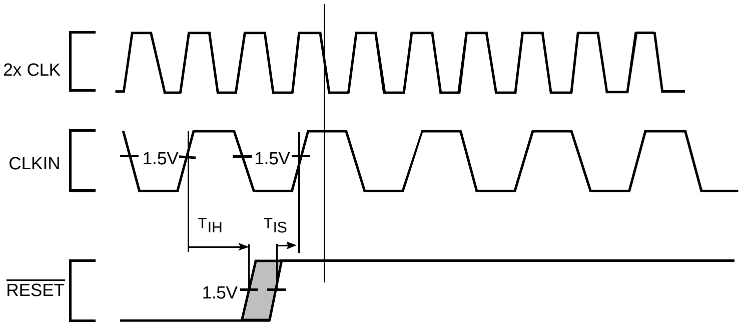
Figure 22. Clock Synchronization in the 2-x Clock Mode



Note: In 1x clock mode, the $\overline{\text{RESET}}$ pin is actually sampled on the falling edge of 2xCLK. 2xCLK is an internal signal generated by the PLL and is not available on an external pin. Therefore, $\overline{\text{RESET}}$ is specified relative to the rising edge of CLKIN. The $\overline{\text{RESET}}$ pin is sampled when PCLK is high.

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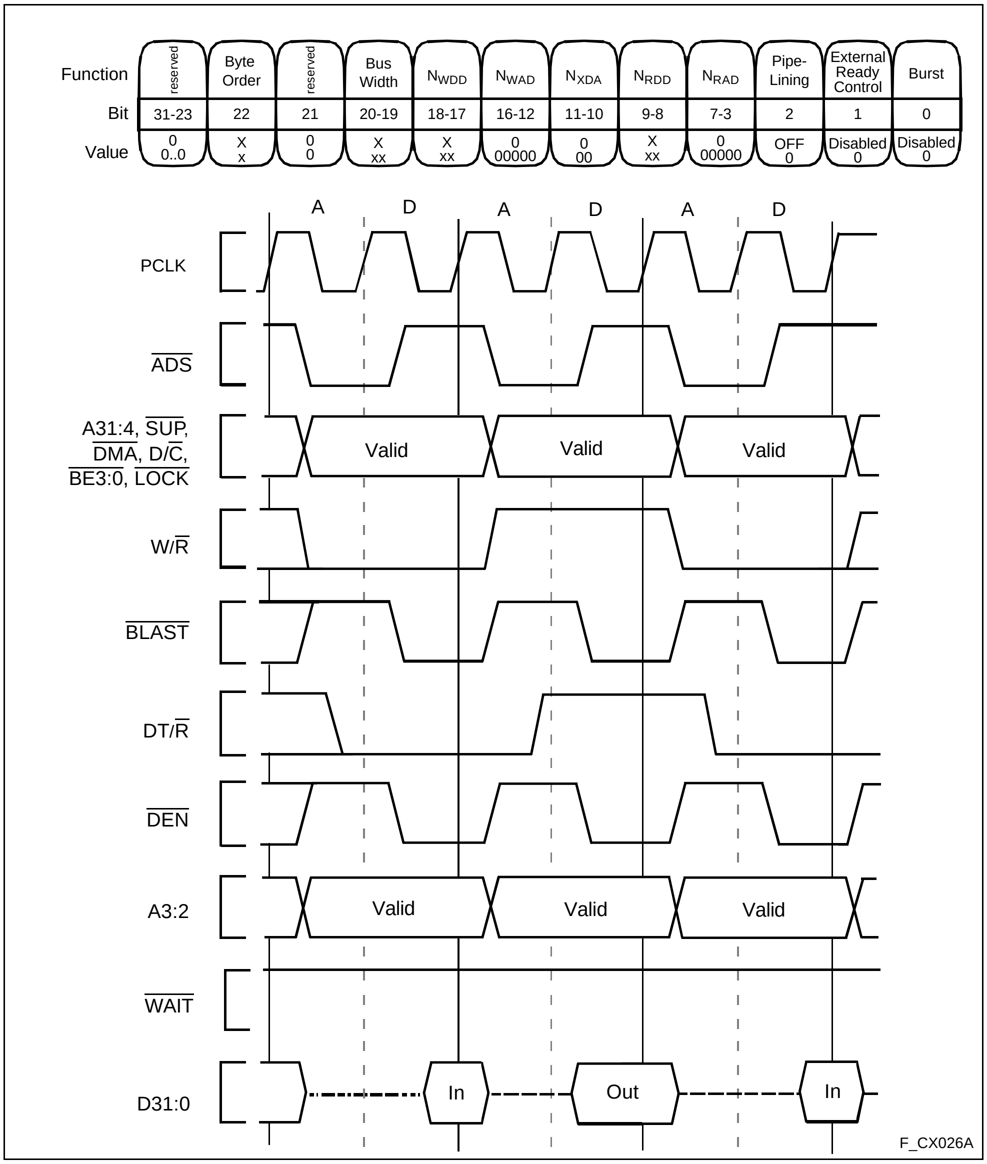
Figure 23. Clock Synchronization in the 1-x Clock Mode



Function	reserved	Byte Order	reserved	Bus Width	N_{WDD}	N_{WAD}	N_{XDA}	N_{RDD}	N_{RAD}	Pipe-Lining	External Ready Control	Burst
Bit	31-23	22	21	20-19	18-17	16-12	11-10	9-8	7-3	2	1	0
Value	0 0..0	X x	0 0	X xx	X xx	0 00000	0 00	X xx	0 00000	OFF 0	Disabled 0	Disabled 0

Figure 24. Non-Burst, Non-Pipelined Requests Without Wait States

Function	reserved	Byte Order	reserved	Bus Width	N_{WDD}	N_{WAD}	N_{XDA}	N_{RDD}	N_{RAD}	Pipe-Lining	External Ready Control	Burst
Bit	31-23	22	21	20-19	18-17	16-12	11-10	9-8	7-3	2	1	0
Value	0 0..0	X x	0 0	X xx	X xx	X xxxxx	1 01	X xx	3 00011	OFF 0	Disabled 0	Disabled 0

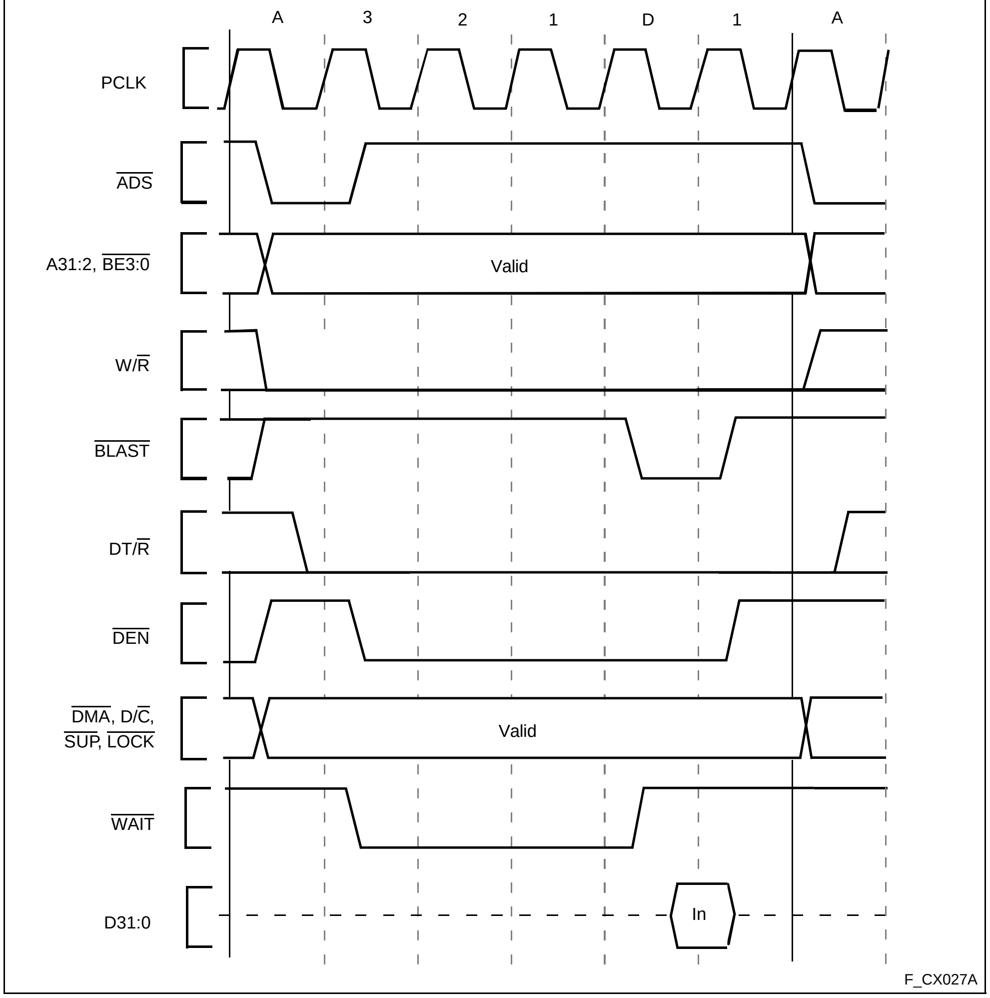
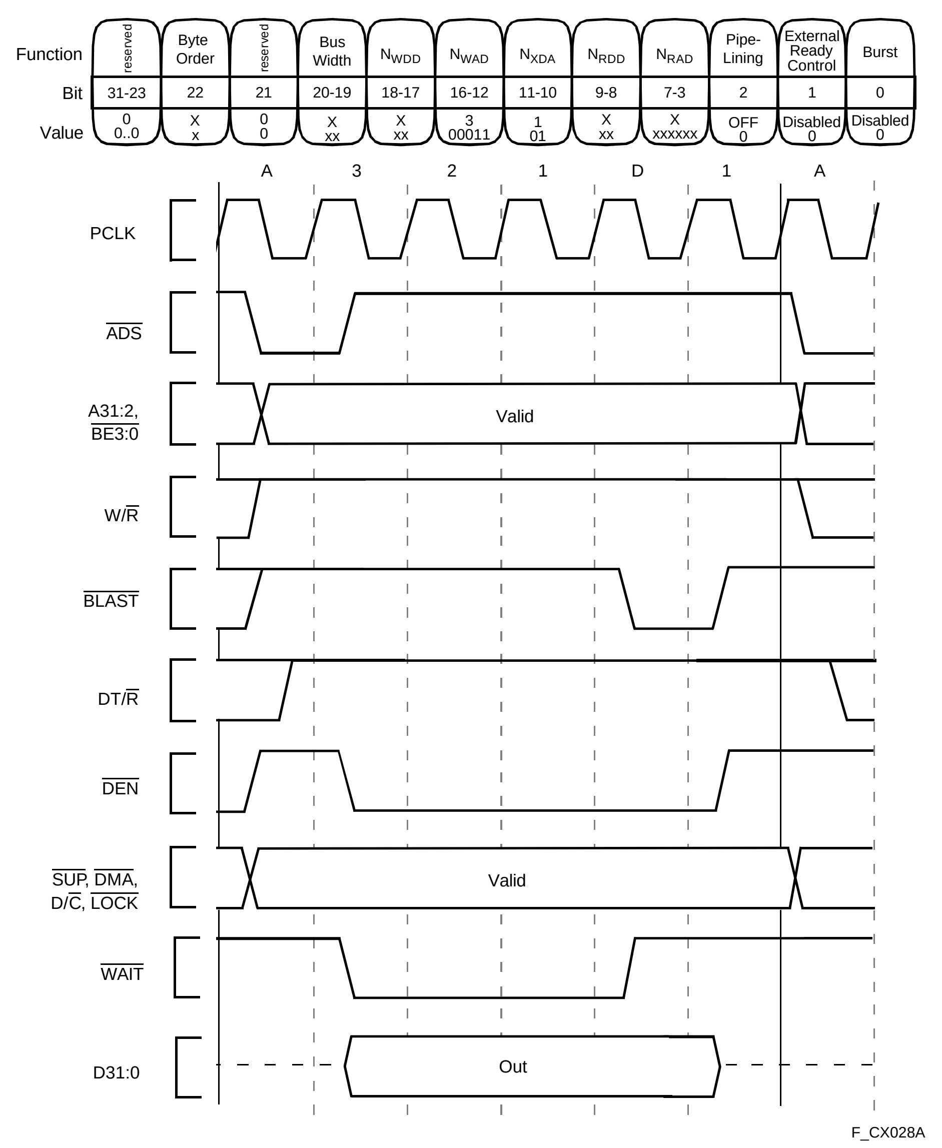


Figure 25. Non-Burst, Non-Pipelined Read Request With Wait States



Function	reserved	Byte Order	reserved	Bus Width	N_{WDD}	N_{WAD}	N_{XDA}	N_{RDD}	N_{RAD}	Pipe-Lining	External Ready Control	Burst
Bit	31-23	22	21	20-19	18-17	16-12	11-10	9-8	7-3	2	1	0
Value	0 0..0	X x	0 0	X xx	X xx	3 00011	1 01	X xx	X xxxxxx	OFF 0	Disabled 0	Disabled 0

Figure 26. Non-Burst, Non-Pipelined Write Request With Wait States

Function	reserved	Byte Order	reserved	Bus Width	N_{WDD}	N_{WAD}	N_{XDA}	N_{RDD}	N_{RAD}	Pipe-Lining	External Ready Control	Burst
Bit	31-23	22	21	20-19	18-17	16-12	11-10	9-8	7-3	2	1	0
Value	0 0..0	X x	0 0	32-Bit 10	X xx	X xxxxx	0 00	0 00	0 00000	OFF 0	Disabled 0	Enabled 1

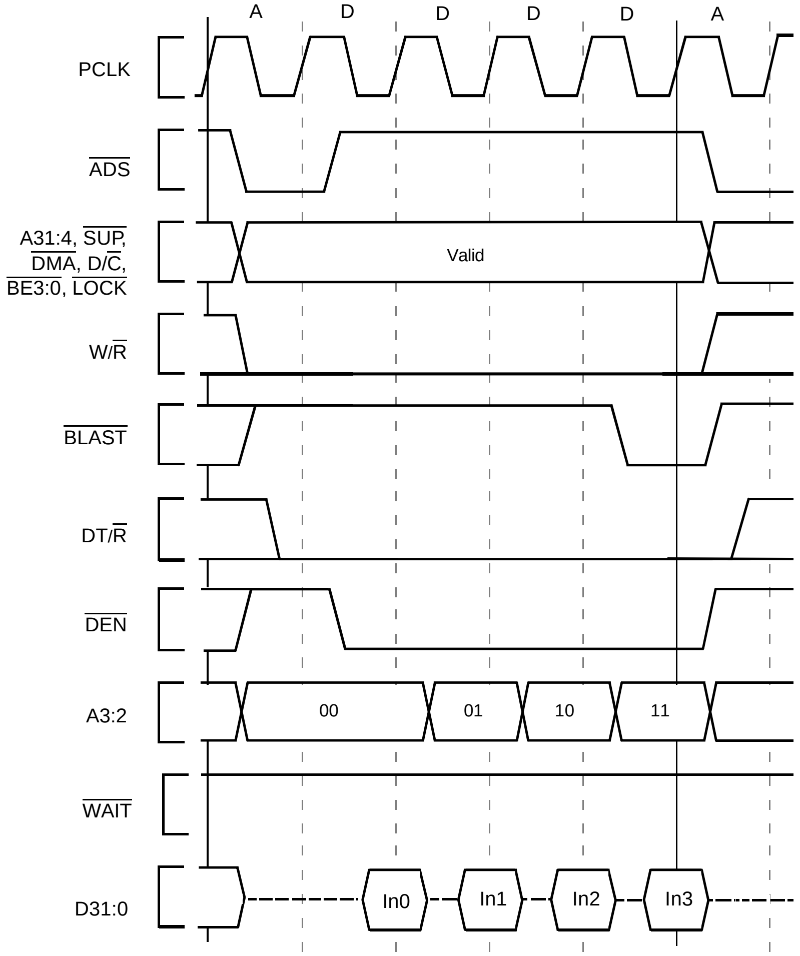
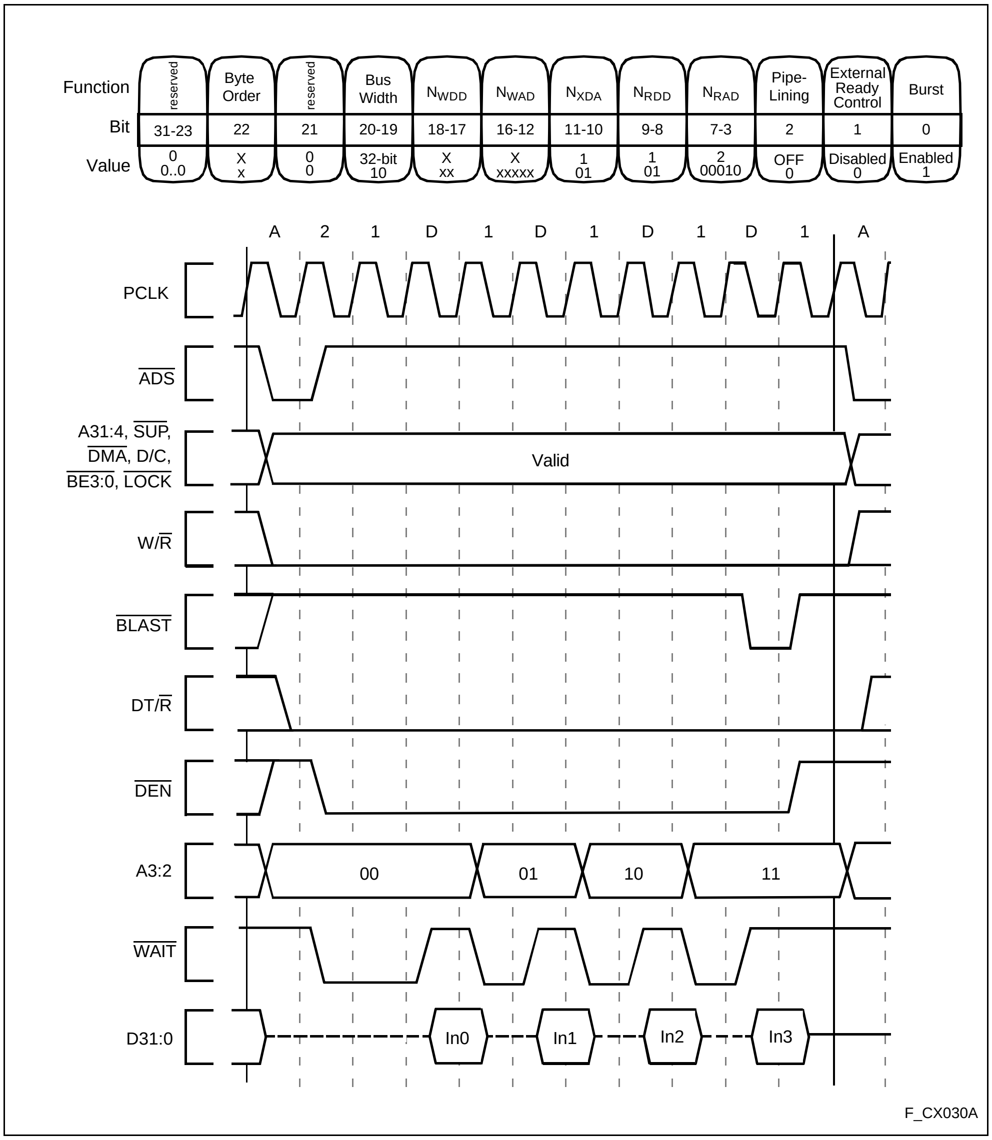
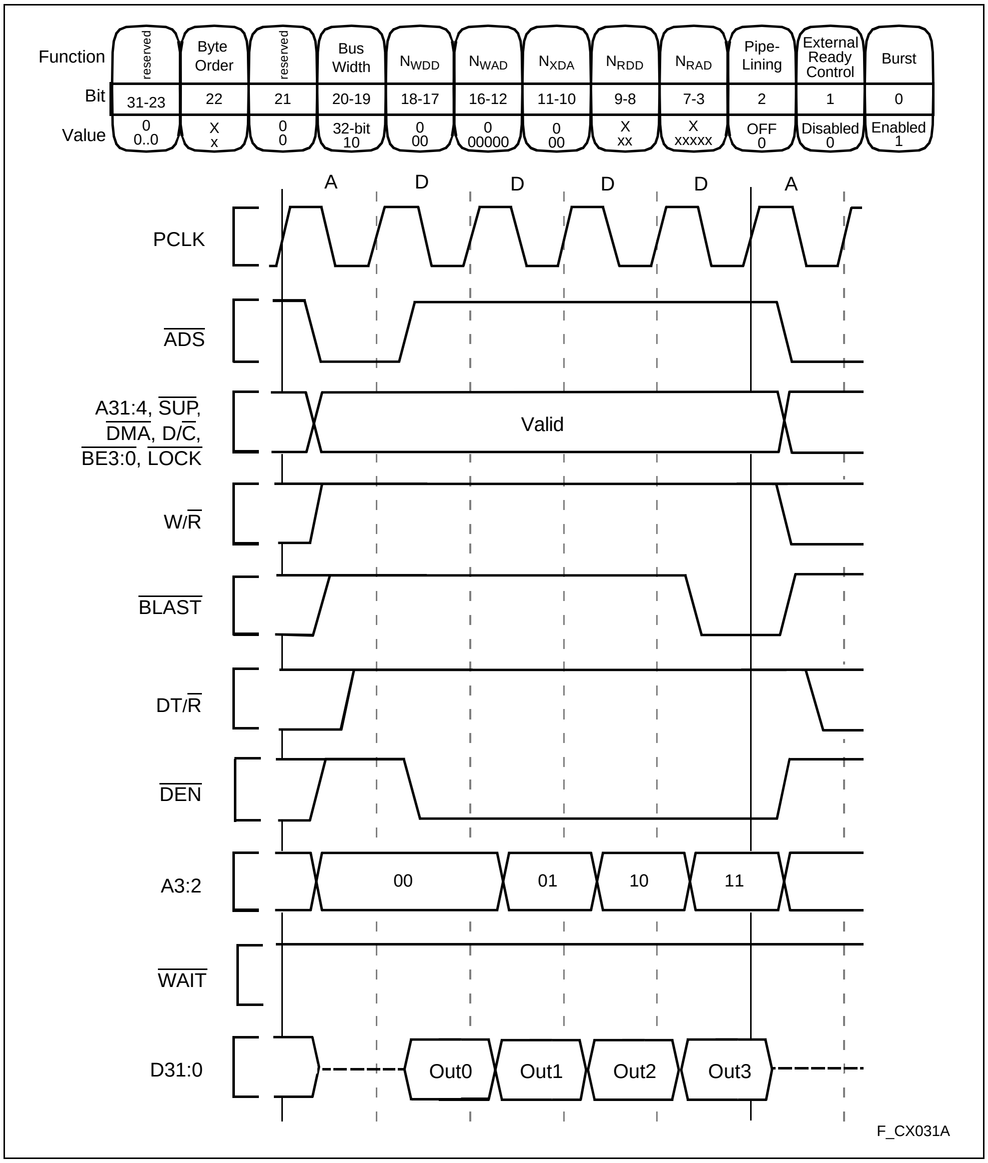


Figure 27. Burst, Non-Pipelined Read Request Without Wait States, 32-Bit Bus



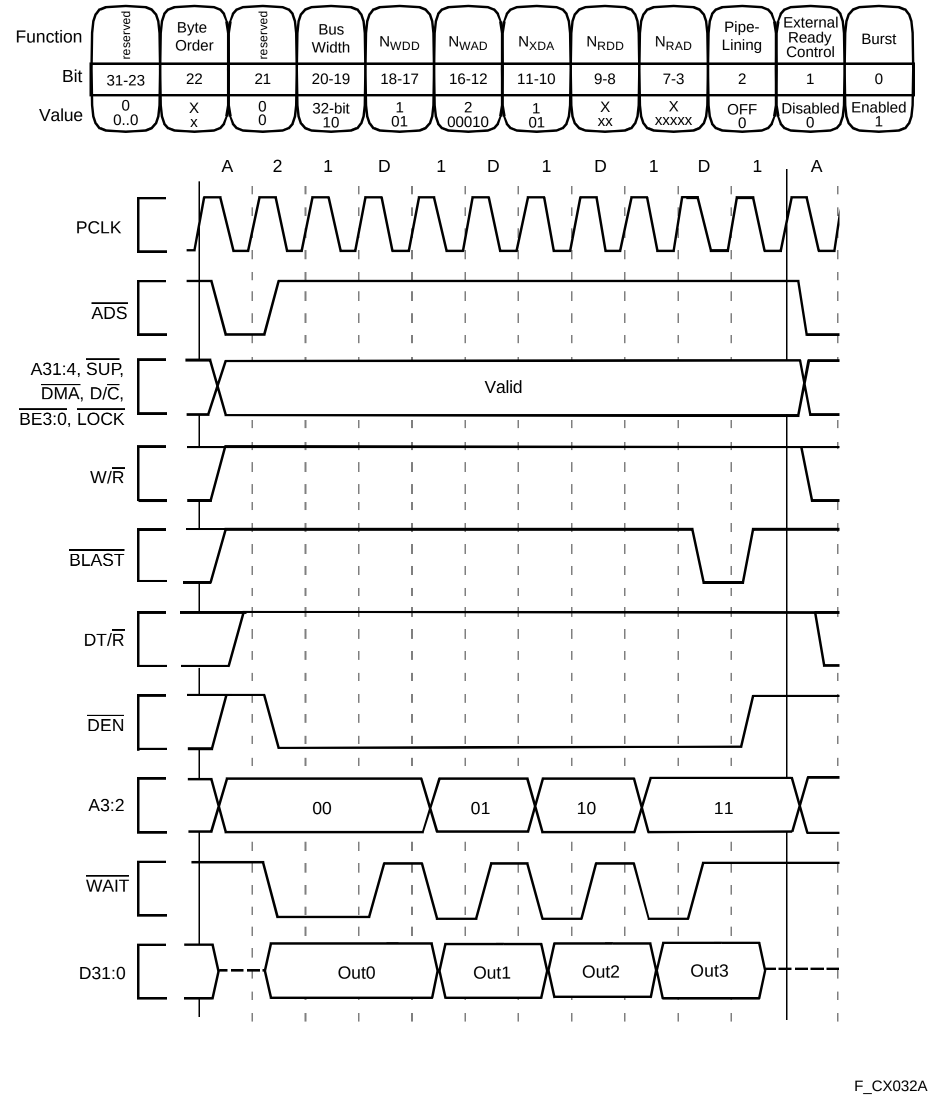
Function	reserved	Byte Order	reserved	Bus Width	N_{WDD}	N_{WAD}	N_{XDA}	N_{RDD}	N_{RAD}	Pipe-Lining	External Ready Control	Burst
Bit	31-23	22	21	20-19	18-17	16-12	11-10	9-8	7-3	2	1	0
Value	0 0..0	X x	0 0	32-bit 10	X xx	X xxxxx	1 01	1 01	2 00010	OFF 0	Disabled 0	Enabled 1

Figure 28. Burst, Non-Pipelined Read Request With Wait States, 32-Bit Bus



Function	reserved	Byte Order	reserved	Bus Width	N_{WDD}	N_{WAD}	N_{XDA}	N_{RDD}	N_{RAD}	Pipe-Lining	External Ready Control	Burst
Bit	31-23	22	21	20-19	18-17	16-12	11-10	9-8	7-3	2	1	0
Value	0 0..0	X x	0 0	32-bit 10	0 00	0 00000	0 00	X xx	X xxxxx	OFF 0	Disabled 0	Enabled 1

Figure 29. Burst, Non-Pipelined Write Request Without Wait States, 32-Bit Bus



Function	reserved	Byte Order	reserved	Bus Width	N_{WDD}	N_{WAD}	N_{XDA}	N_{RDD}	N_{RAD}	Pipe-Lining	External Ready Control	Burst
Bit	31-23	22	21	20-19	18-17	16-12	11-10	9-8	7-3	2	1	0
Value	0 0..0	X x	0 0	32-bit 10	1 01	2 00010	1 01	X xx	X xxxxx	OFF 0	Disabled 0	Enabled 1

Figure 30. Burst, Non-Pipelined Write Request With Wait States, 32-Bit Bus

Function	reserved	Byte Order	reserved	Bus Width	N_{WDD}	N_{WAD}	N_{XDA}	N_{RDD}	N_{RAD}	Pipe-Lining	External Ready Control	Burst
Bit	31-23	22	21	20-19	18-17	16-12	11-10	9-8	7-3	2	1	0
Value	0 0..0	X x	0 0	16-bit 01	X xx	X xxxxx	1 01	1 01	2 00010	OFF 0	Disabled 0	Enabled 1

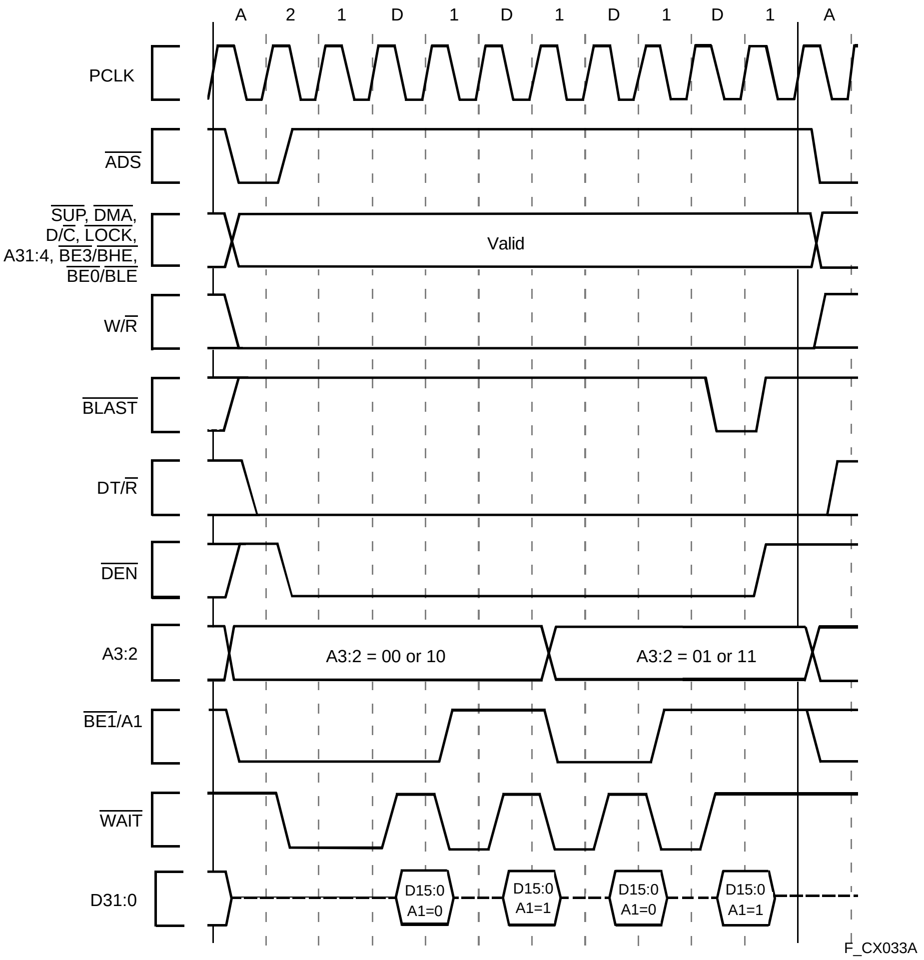


Figure 31. Burst, Non-Pipelined Read Request With Wait States, 16-Bit Bus

Function	reserved	Byte Order	reserved	Bus Width	N_{WDD}	N_{WAD}	N_{XDA}	N_{RDD}	N_{RAD}	Pipe-Lining	External Ready Control	Burst
Bit	31-23	22	21	20-19	18-17	16-12	11-10	9-8	7-3	2	1	0
Value	0 0..0	X x	0 0	8-bit 00	X xx	X xxxxx	1 01	1 01	2 00010	OFF 0	Disabled 0	Enabled 1

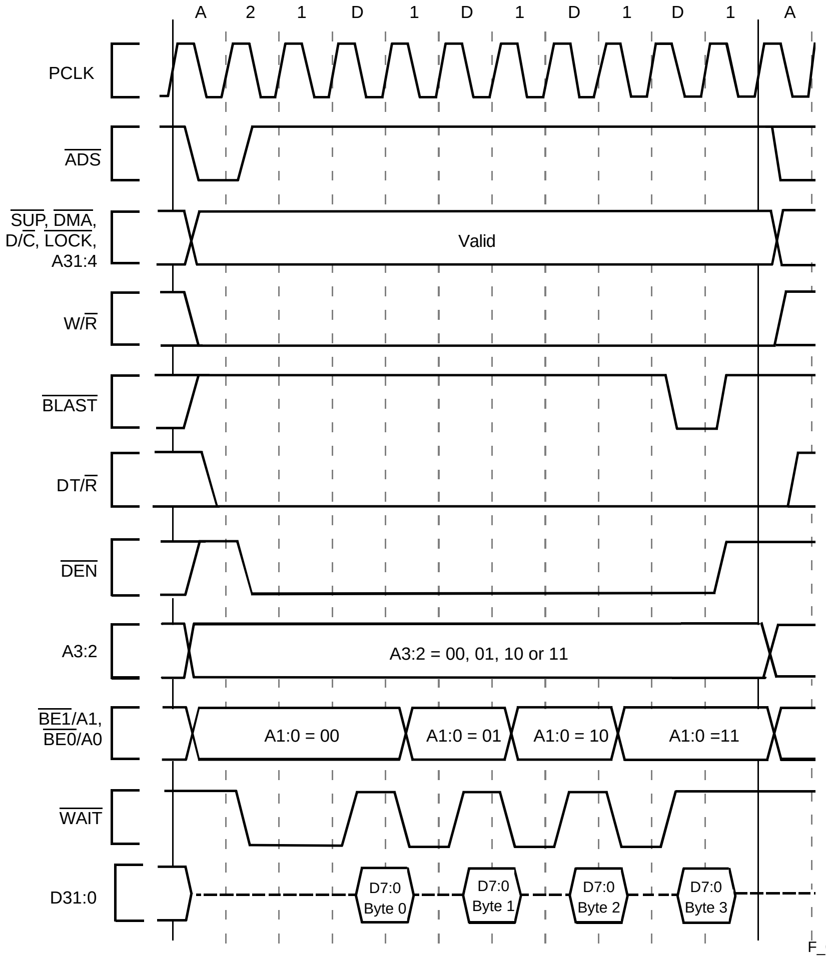
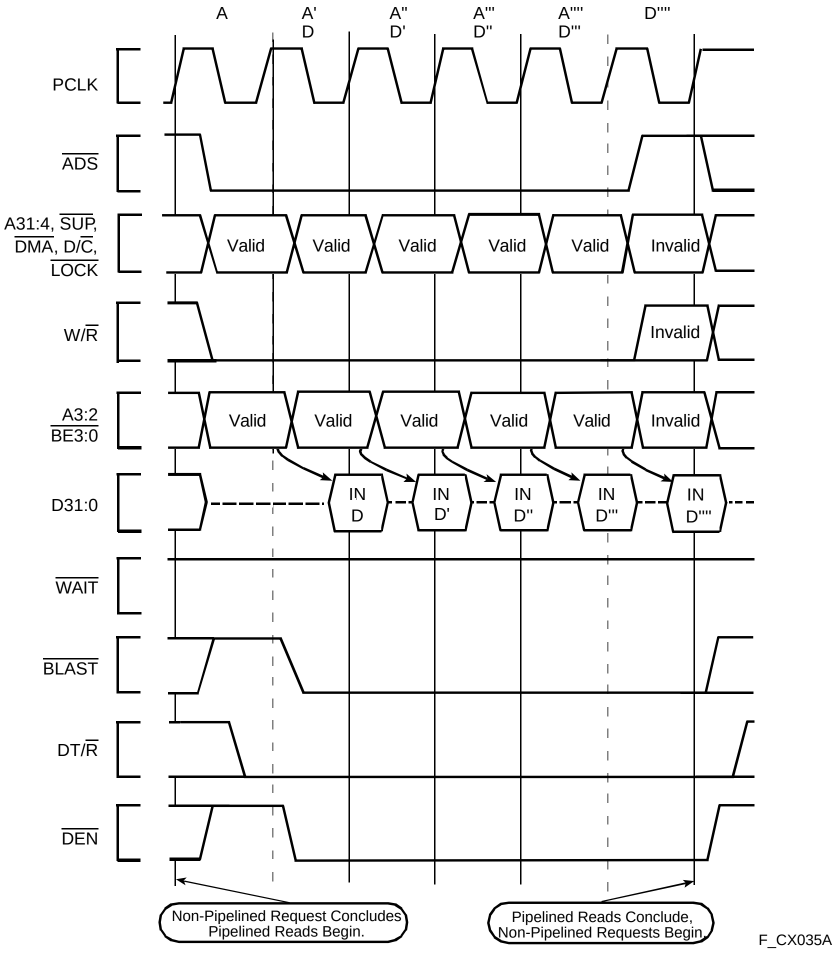


Figure 32. Burst, Non-Pipelined Read Request With Wait States, 8-Bit Bus

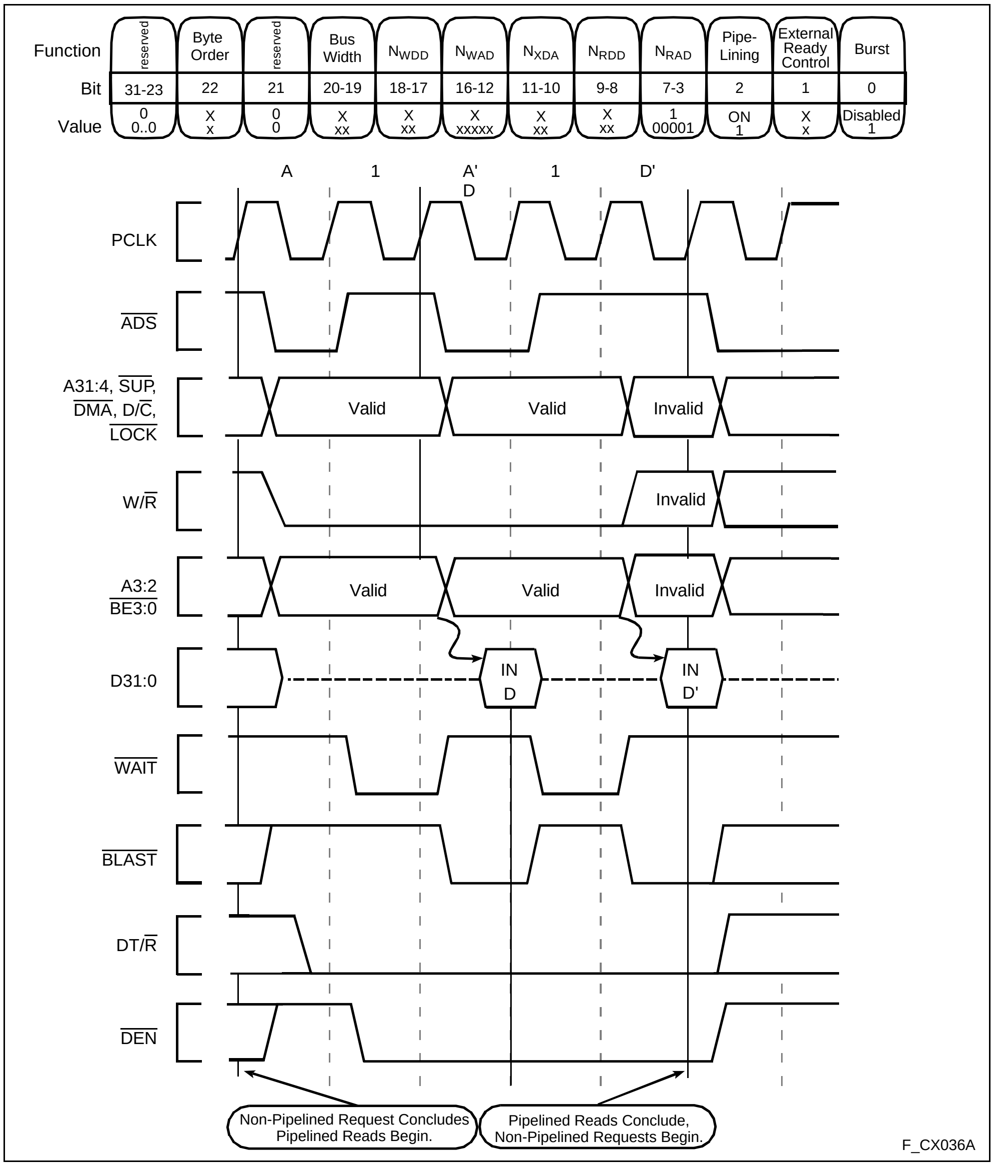
Function	reserved	Byte Order	reserved	Bus Width	N_{WDD}	N_{WAD}	N_{XDA}	N_{RDD}	N_{RAD}	Pipe-Lining	External Ready Control	Burst
Bit	31-23	22	21	20-19	18-17	16-12	11-10	9-8	7-3	2	1	0
Value	0 0..0	X x	0 0	X xx	X xx	X xxxxx	X xx	X xx	0 00000	ON 1	X x	Disabled 0



Non-Pipelined Request Concludes
Pipelined Reads Begin.

Pipelined Reads Conclude,
Non-Pipelined Requests Begin.

Figure 33. Non-Burst, Pipelined Read Request Without Wait States, 32-Bit Bus



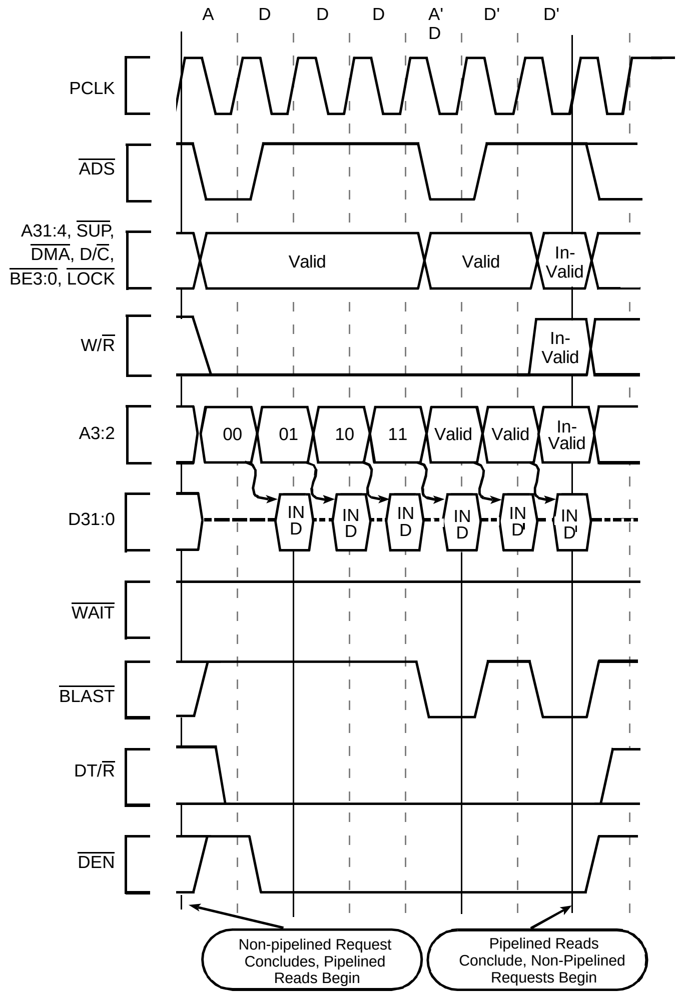
Function	reserved	Byte Order	reserved	Bus Width	N_{WDD}	N_{WAD}	N_{XDA}	N_{RDD}	N_{RAD}	Pipe-Lining	External Ready Control	Burst
Bit	31-23	22	21	20-19	18-17	16-12	11-10	9-8	7-3	2	1	0
Value	0 0..0	X x	0 0	X xx	X xx	X xxxxx	X xx	X xx	1 00001	ON 1	X x	Disabled 1

Non-Pipelined Request Concludes Pipelined Reads Begin.

Pipelined Reads Conclude, Non-Pipelined Requests Begin.

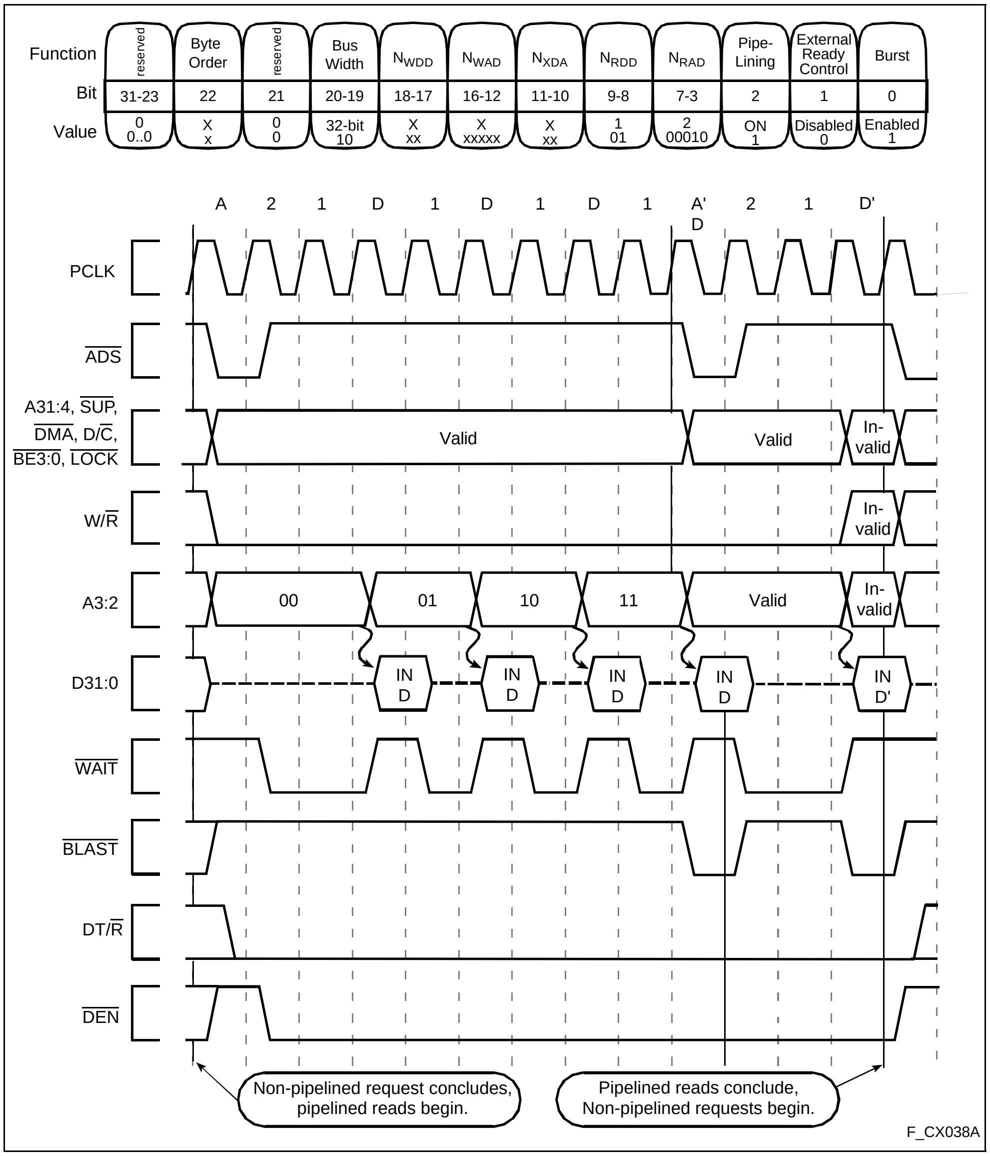
Figure 34. Non-Burst, Pipelined Read Request With Wait States, 32-Bit Bus

Function	reserved	Byte Order	reserved	Bus Width	N_{WDD}	N_{WAD}	N_{XDA}	N_{RDD}	N_{RAD}	Pipe-Lining	External Ready Control	Burst
Bit	31-23	22	21	20-19	18-17	16-12	11-10	9-8	7-3	2	1	0
Value	0 0..0	X x	0 0	32-bit 10	X xx	X xxxxx	X xx	0 00	0 00000	ON 1	Disabled 0	Enabled 1



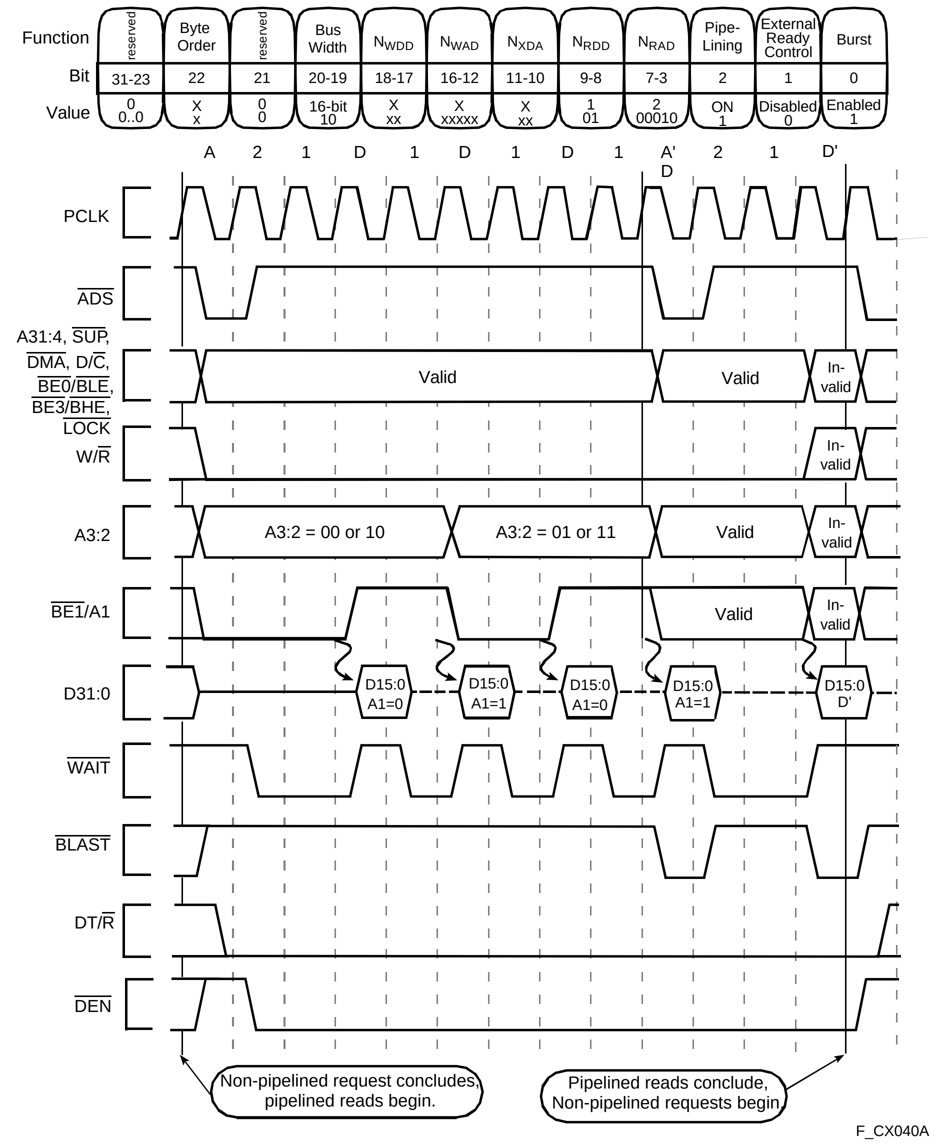
F_CX037A

Figure 35. Burst, Pipelined Read Request Without Wait States, 32-Bit Bus



Function	reserved	Byte Order	reserved	Bus Width	N_{WDD}	N_{WAD}	N_{XDA}	N_{RDD}	N_{RAD}	Pipe-Lining	External Ready Control	Burst
Bit	31-23	22	21	20-19	18-17	16-12	11-10	9-8	7-3	2	1	0
Value	0 0..0	X x	0 0	32-bit 10	X xx	X xxxxx	X xx	1 01	2 00010	ON 1	Disabled 0	Enabled 1

Figure 36. Burst, Pipelined Read Request With Wait States, 32-Bit Bus



Function	reserved	Byte Order	reserved	Bus Width	N_{WDD}	N_{WAD}	N_{XDA}	N_{RDD}	N_{RAD}	Pipe-Lining	External Ready Control	Burst
Bit	31-23	22	21	20-19	18-17	16-12	11-10	9-8	7-3	2	1	0
Value	0 0..0	X x	0 0	16-bit 10	X xx	X xxxxx	X xx	1 01	2 00010	ON 1	Disabled 0	Enabled 1

Figure 37. Burst, Pipelined Read Request With Wait States, 16-Bit Bus

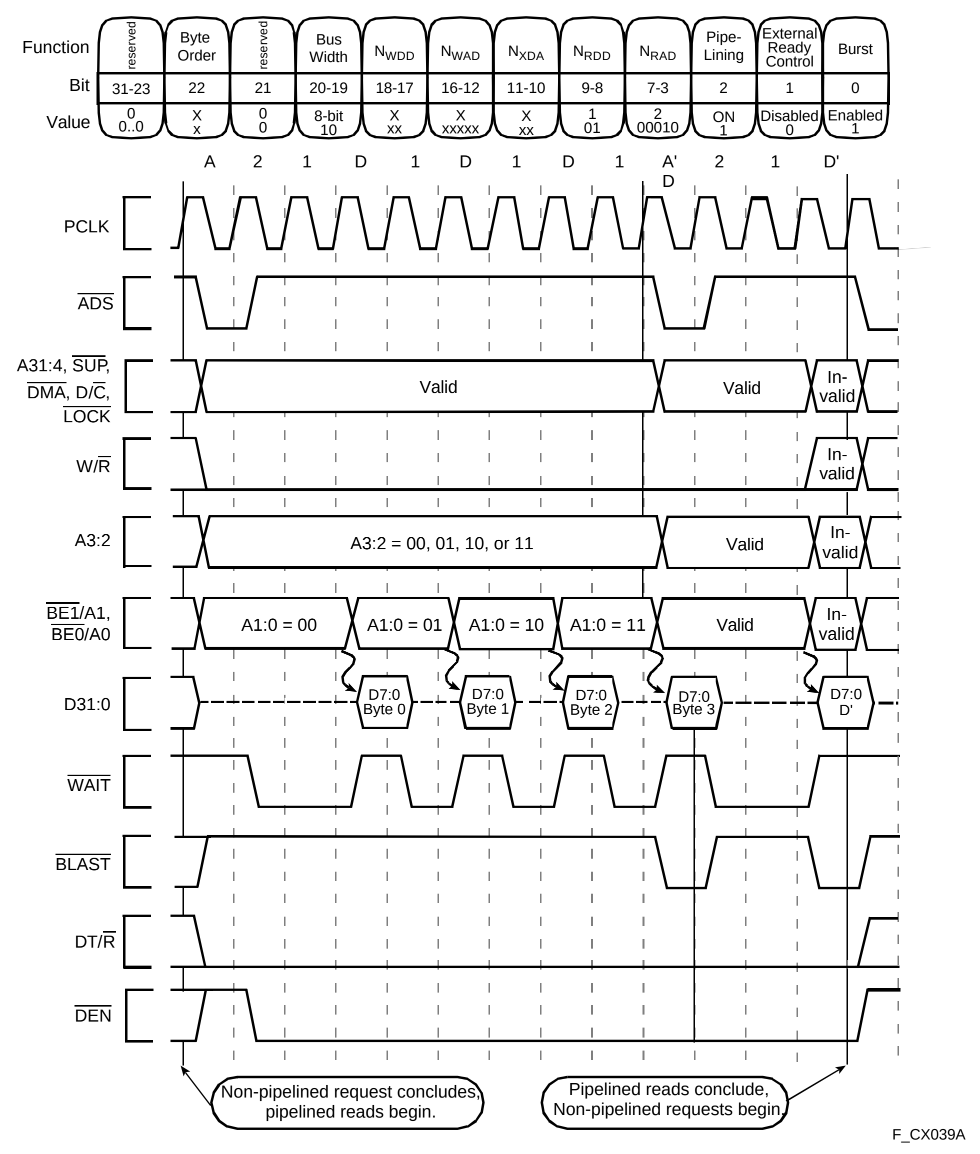


Figure 38. Burst, Pipelined Read Request With Wait States, 8-Bit Bus

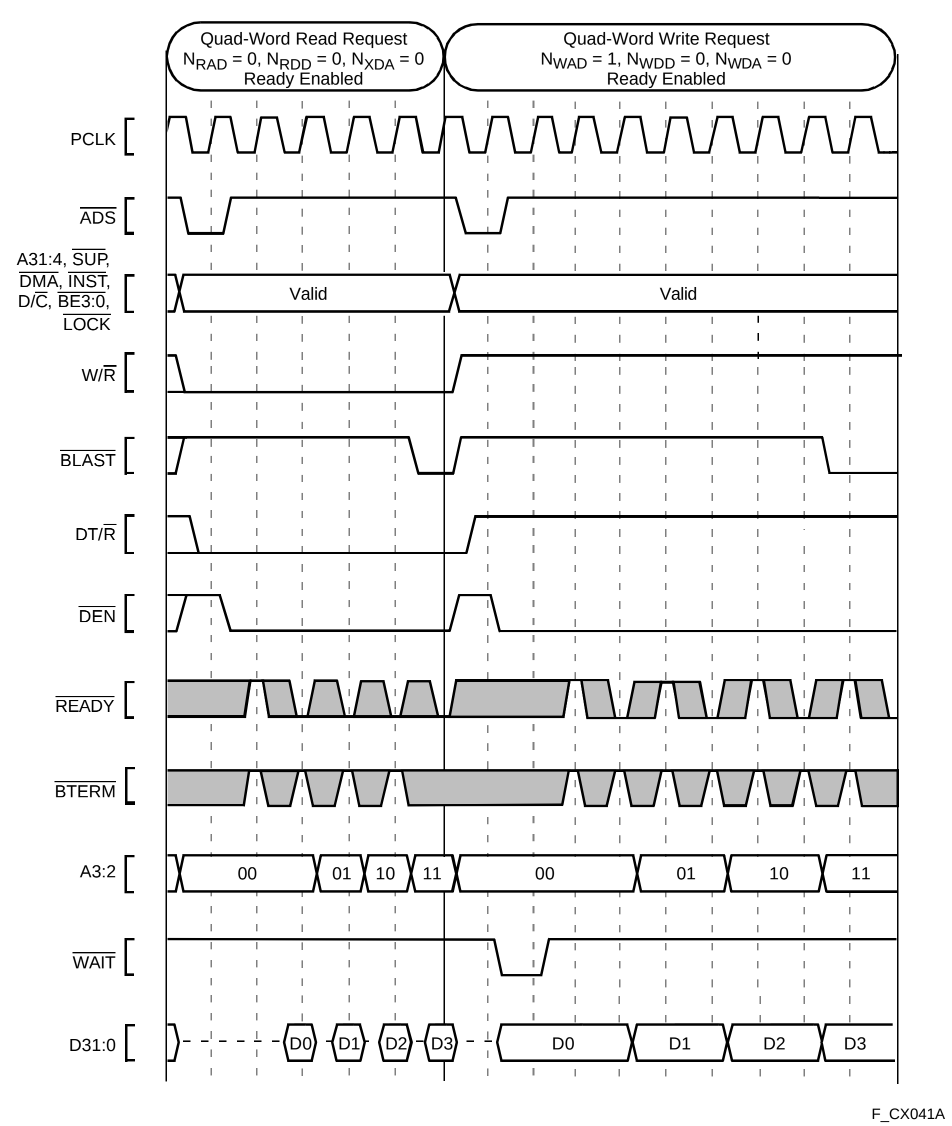
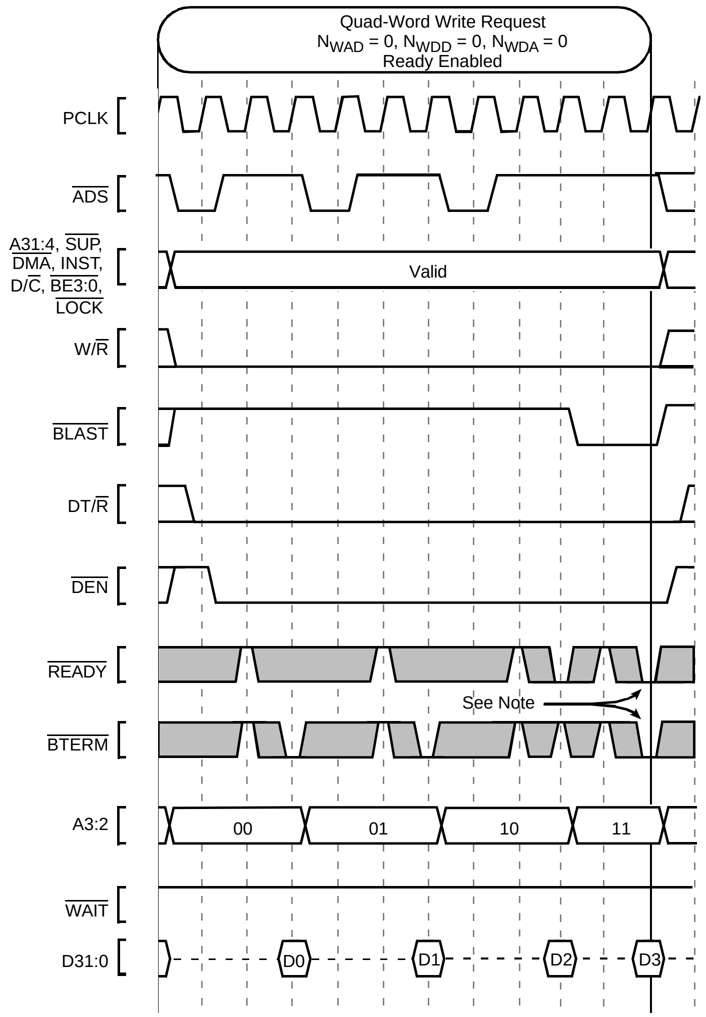


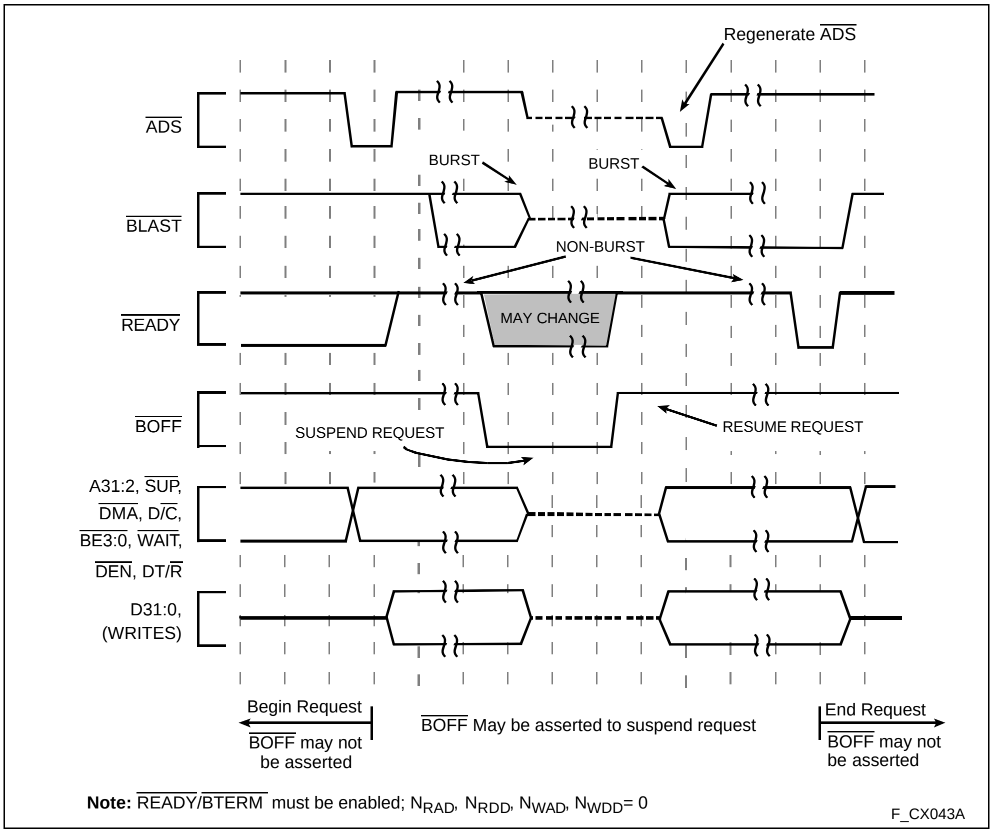
Figure 39. Using External READY



Note: $\overline{\text{READY}}$ adds memory access time to data transfers, whether or not the bus access is a burst access. $\overline{\text{BTERM}}$ interrupts a bus access, whether or not the bus access has more data transfers pending. Either the $\overline{\text{READY}}$ signal or the $\overline{\text{BTERM}}$ signal will terminate a bus access if the signal is asserted during the last (or only) data transfer of the bus access.

F_CX042A

Figure 40. Terminating a Burst with $\overline{\text{BTERM}}$



Note: $\overline{\text{READY}}/\overline{\text{BTERM}}$ must be enabled; N_{RAD}, N_{RDD}, N_{WAD}, N_{WDD}= 0

Figure 41. $\overline{\text{BOFF}}$ Functional Timing

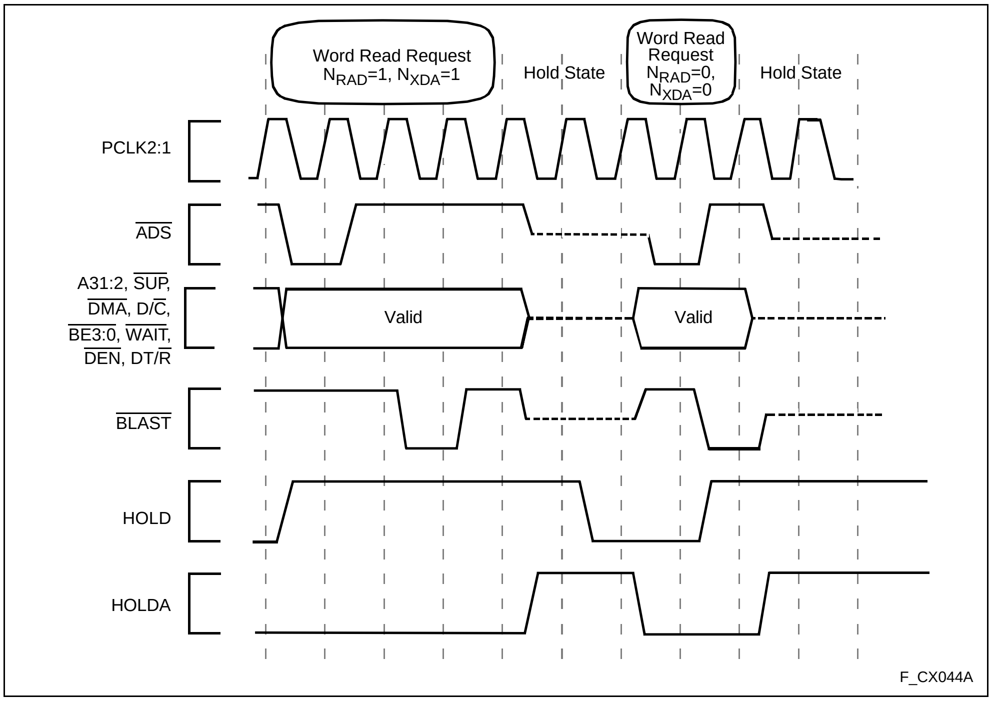
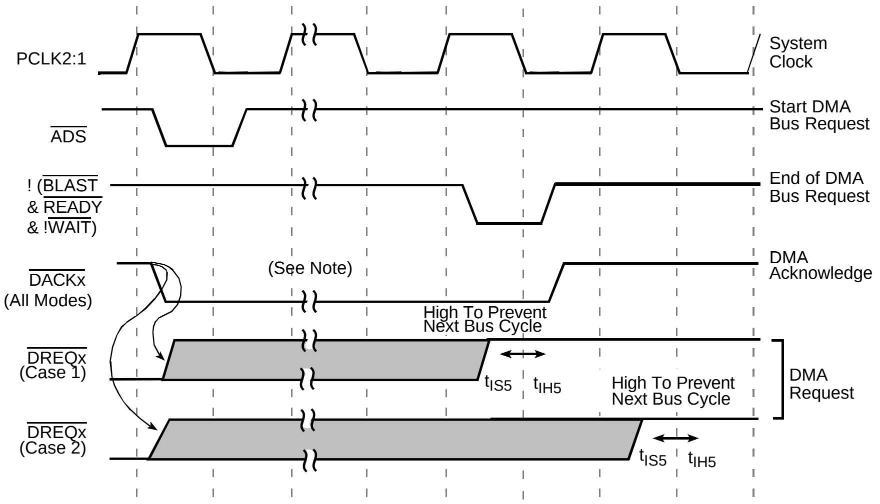


Figure 42. HOLD Functional Timing

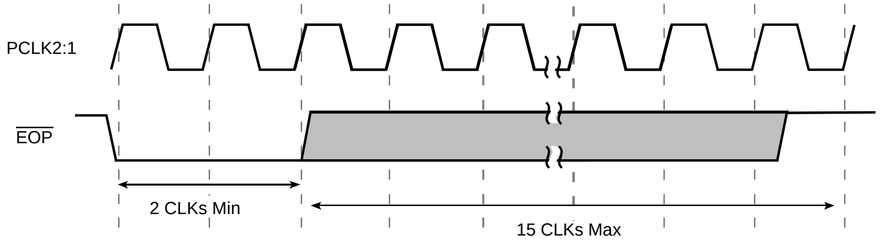


Note:

1. Case 1: $\overline{\text{DREQ}}$ must deassert before $\overline{\text{DACK}}$ deasserts. Applications are Fly-By and some packing and unpacking modes in which loads are followed by loads or stores are followed by stores.
2. Case 2: $\overline{\text{DREQ}}$ must be deasserted by the second clock (rising edge) after $\overline{\text{DACK}}$ is driven high. Applications are non Fly-By transfers and adjacent load-stores or store-loads.
3. $\overline{\text{DACKx}}$ is asserted for the duration of a DMA bus request. The request may consist of multiple bus accesses (defined by $\overline{\text{ADS}}$ and $\overline{\text{BLAST}}$. Refer to *i960® Cx Microprocessor User's Manual* for "access", "request" definitions.

F_CX018A

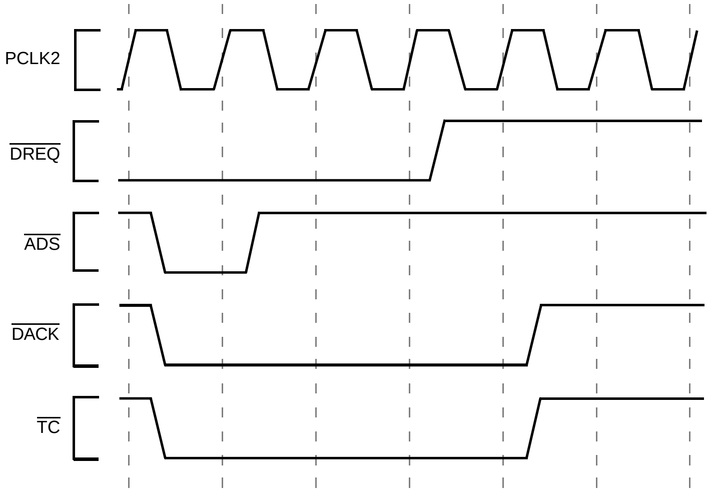
Figure 43. $\overline{\text{DREQ}}$ and $\overline{\text{DACK}}$ Functional Timing



Note: $\overline{\text{EOP}}$ has the same AC Timing Requirements as $\overline{\text{DREQ}}$ to prevent unwanted DMA requests. $\overline{\text{EOP}}$ is NOT edge triggered. $\overline{\text{EOP}}$ must be held for a minimum of 2 clock cycles then deasserted within 15 clock cycles.

F_CX045A

Figure 44. $\overline{\text{EOP}}$ Functional Timing



Note: Terminal Count becomes active during the last bus request of a buffer transfer. If the last LOAD/STORE bus request is executed as multiple bus accesses, the TC will be active for the entire bus request. Refer to the *i960® Cx Microprocessor User's Manual* for further information.

F_CX046A

Figure 45. Terminal Count Functional Timing

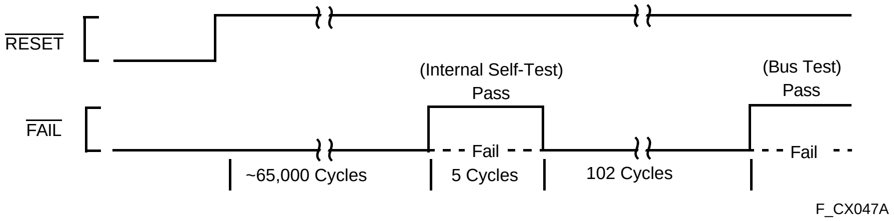


Figure 46. FAIL Functional Timing

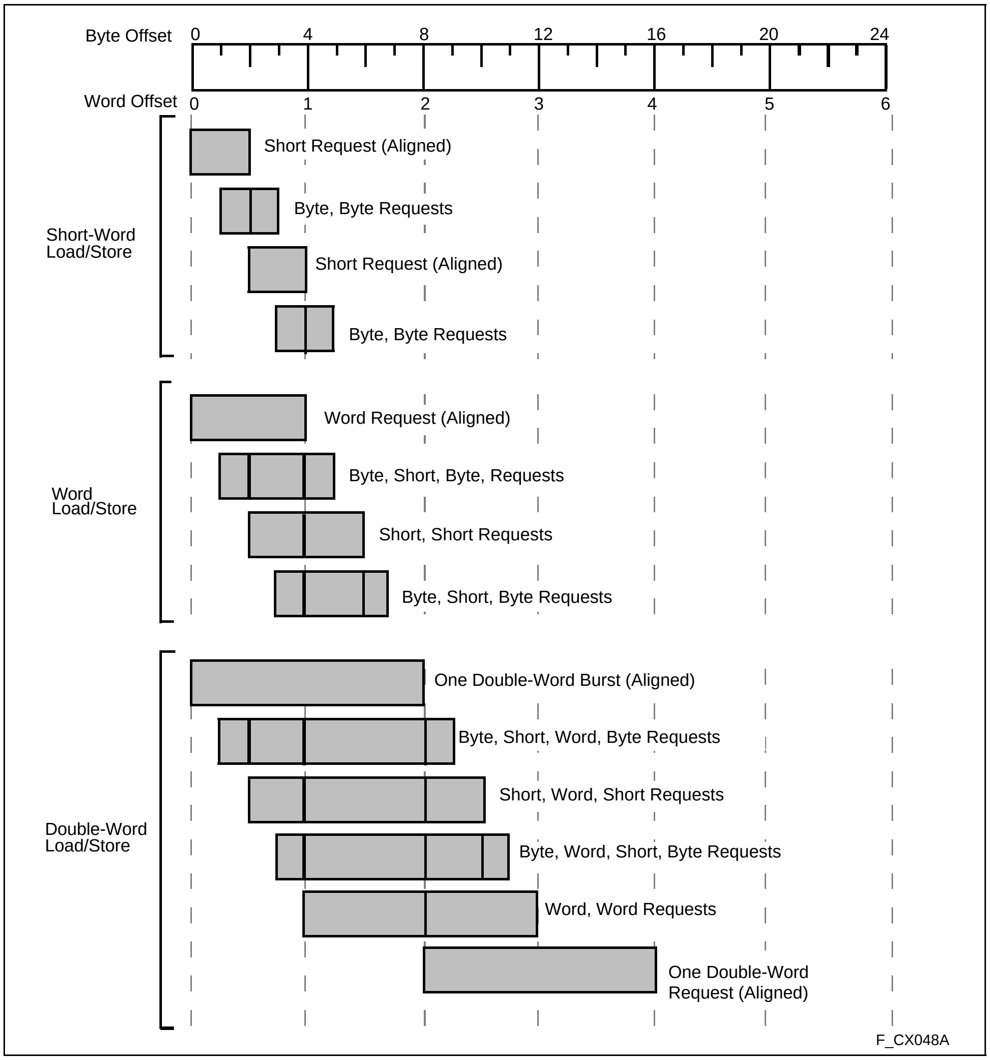


Figure 47. A Summary of Aligned and Unaligned Transfers for Little Endian Regions

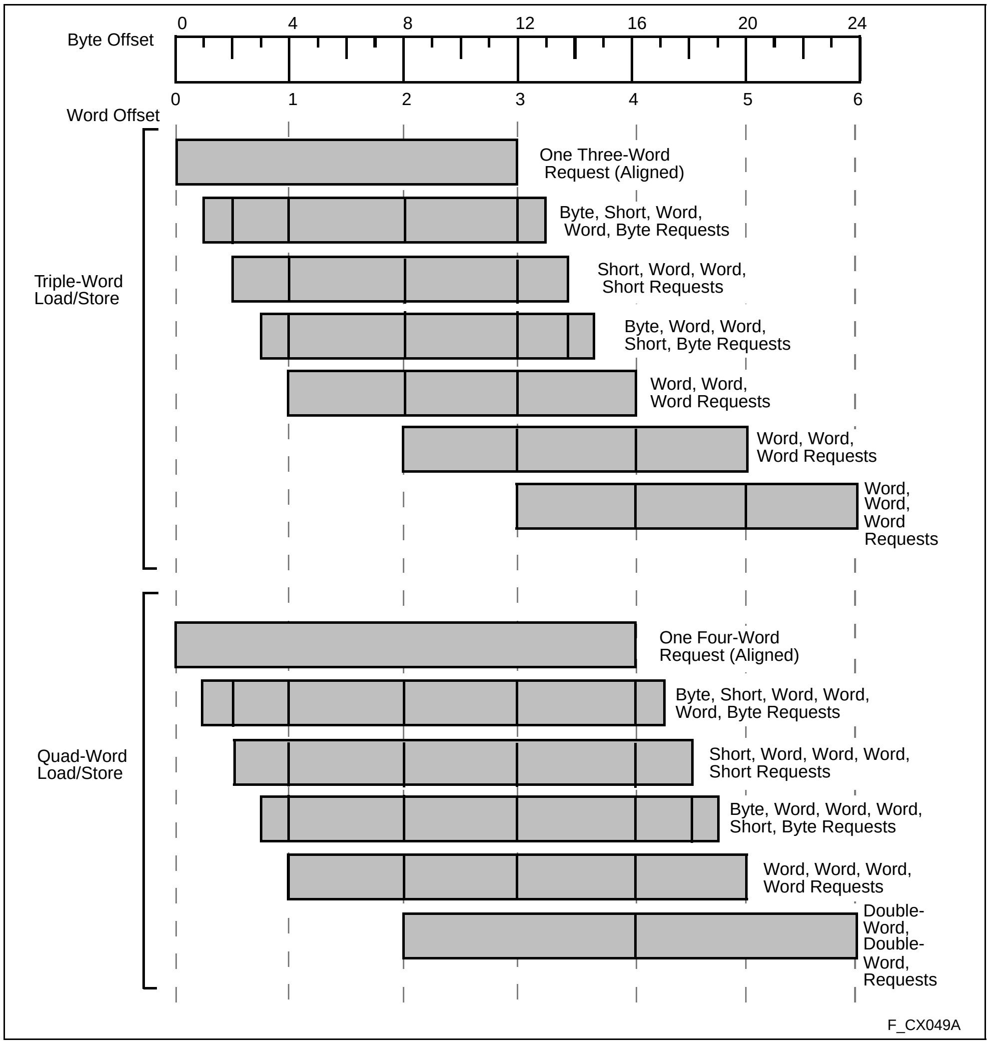


Figure 48. A Summary of Aligned and Unaligned Transfers for Little Endian Regions (Continued)

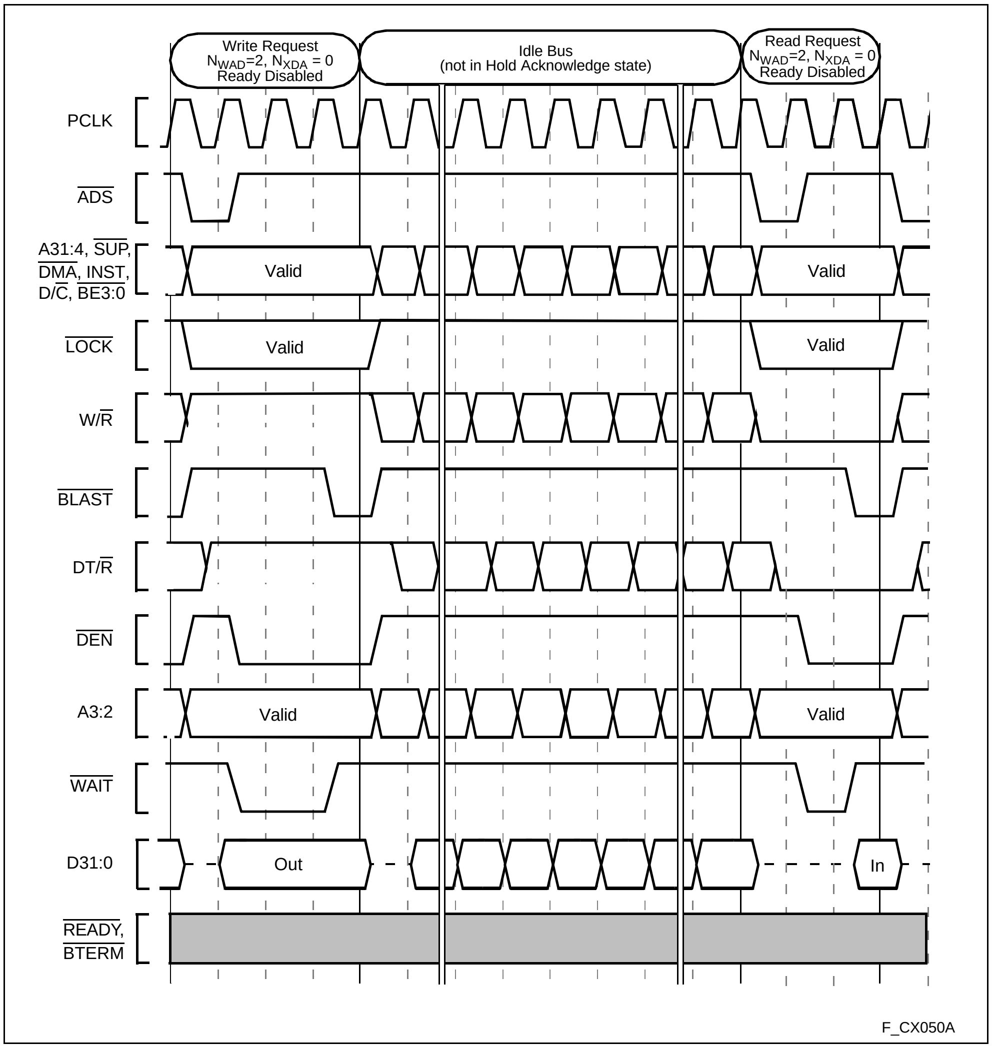


Figure 49. Idle Bus Operation

7.0 REVISION HISTORY

This data sheet supersedes data sheet 270727-005. Specification changes in the 80960CA data sheet are a result of design changes. The sections significantly changed since the previous revision are:

Section	Last Rev.	Description
Table 11. 80960CA PGA Package Thermal Characteristics	-005	Removed references and notes pertaining to $\theta_{J\text{-}CAP}$ and $\theta_{J\text{-}PIN}$.
Table 12. 80960CA PQFP package Thermal Characteristics	-005	Removed references and notes pertaining to θ_{JL} and θ_{JB}.
3.3 80960CA Mechanical Data	-005	Removed section containing information on Package Dimensions. Moved section header to encompass Pinout tables and diagrams.
3.7 Suggested Sources for 80960CA Accessories	-005	Removed entire section containing information about 80960CA accessories.
Tables 16, 17 and18 80960CA AC Characteristics (33-, 25- and 16MHz, respectively)	-005	T_{TVEL} maximum deleted. T_{NHQX} and T_{EHTV} minimums changed: WAS: IS: T_{NHQX} (N+1)*T-6 (N+1)*T-8 T_{EHTV} T/2 - 6 T/2 - 7
All	-005	All timing diagrams and waveforms have been redrawn to conform to consistent format. Data sheet formatting has been changed to conform to corporate standards. Specific formatting changes are not itemized in this revision history.