CS4362

114 dB, 192 kHz 6-Channel D/A Converter

Features

- 24-bit Conversion
- Up to 192 kHz Sample Rates
- 114 dB Dynamic Range
- -100 dB THD+N
- Supports PCM or DSD Data Formats
- Selectable Digital Filters
- Volume Control with Soft Ramp
  - 1 dB Step Size
  - Zero Crossing Click-free Transitions
- Dedicated DSD inputs
- Low Clock Jitter Sensitivity
- Simultaneous Support for Two Synchronous Sample Rates for DVD Audio
- µC or Stand-Alone Operation

Description

The CS4362 is a complete 6-channel digital-to-analog system including digital interpolation, fifth-order delta-sigma digital-to-analog conversion, digital de-emphasis, volume control and analog filtering. The advantages of this architecture include: ideal differential linearity, no distortion mechanisms due to resistor matching errors, no linearity drift over time and temperature and a high tolerance to clock jitter.

The CS4362 accepts PCM data at sample rates from 4 kHz to 192 kHz, DSD audio data, and operates over a wide power supply range. These features are ideal for multi-channel audio systems including DVD players. SACD players, A/V receivers, digital TV's, mixing consoles, and effects processors.

ORDERING INFORMATION

CS4362-KQZ, Lead Free	-10 to 70 °C	48-pin LQFP
CDB4362	Evaluation Board	

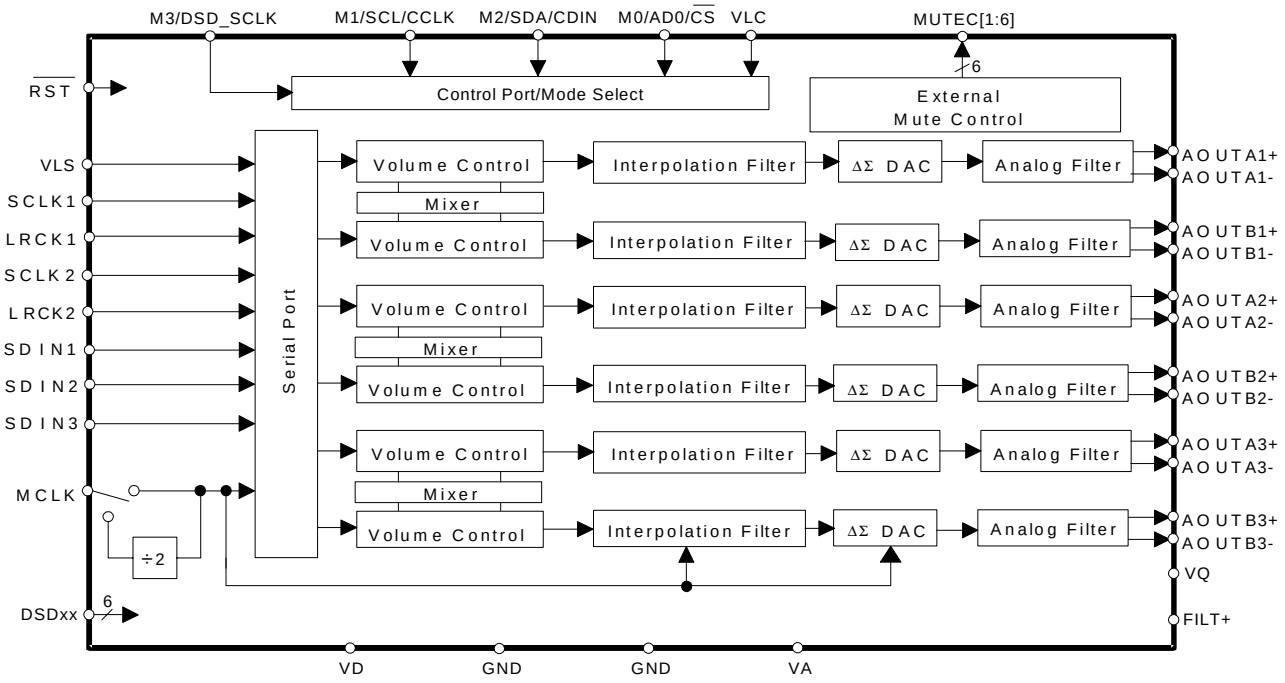


TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1. CHARACTERISTICS AND SPECIFICATIONS

ANALOG CHARACTERISTICS (Full-Scale Output Sine Wave, 997 Hz; Measurement Bandwidth 10 Hz to 20 kHz, unless otherwise specified; Test load R_L = 3 kΩ, C_L = 100 pF, VA = 5 V, VD = 3.3 V (see Figure 5)

For Single speed Mode Fs = 48 kHz, SCLK = 3.072 MHz, MCLK = 12.288 MHz;
For Double Speed Mode Fs = 96 kHz, SCLK = 6.144 MHz, MCLK = 12.288 MHz;
For Quad Speed Mode Fs = 192 kHz, SCLK = 12.288 MHz, MCLK = 24.576 MHz;
For Direct Stream Digital Mode Fs = 128 x 48 kHz, DSD_SCLK = 6.144 MHz, MCLK = 12.288 MHz).

Parameters			Symbol	Min	Typ	Max	Unit
CS4362-KQZ Dynamic Performance - All PCM modes and DSD (Note 1)							
Specified Temperature Range			T_A	-10	-	70	°C
Dynamic Range (Note 2)	24-bit	unweighted		105	111	-	dB
		A-Weighted		108	114	-	dB
	16-bit	unweighted		-	94	-	dB
	(Note 3)	A-Weighted		-	97	-	dB
Total Harmonic Distortion + Noise		(Note 2)	THD+N				
	24-bit	0 dB		-	-100	-94	dB
		-20 dB		-	-91	-	dB
		-60 dB		-	-51	-	dB
	16-bit	0 dB		-	-94	-	dB
	(Note 3)	-20 dB		-	-74	-	dB
		-60 dB		-	-34	-	dB
Idle Channel Noise / Signal-to-noise ratio				-	114	-	dB
Interchannel Isolation		(1 kHz)		-	90	-	dB

Notes: 1. CS4362-KQZ parts are tested at 25 °C.
2. One-half LSB of triangular PDF dither is added to data.
3. Performance limited by 16-bit quantization noise.

ANALOG CHARACTERISTICS (Continued)

Parameters	Symbol	Min	Typ	Max	Units
Analog Output - All PCM modes and DSD					
Full Scale Differential Output Voltage (Note 4)	V_{FS}	86% V_A	91% V_A	96% V_A	Vpp
Quiescent Voltage	V_Q	-	50% V_A	-	VDC
Max Current from V_Q	I_{QMAX}	-	1	-	µA
Interchannel Gain Mismatch		-	0.1	-	dB
Gain Drift		-	100	-	ppm/°C
Output Impedance (Note 4)	Z_{OUT}	-	100	-	Ω
AC-Load Resistance	R_L	3	-	-	kΩ
Load Capacitance	C_L	-	-	100	pF

POWER AND THERMAL CHARACTERISTICS

Parameters		Symbol	Min	Typ	Max	Units
Power Supplies						
Power Supply Current	normal operation, V_A= 5 V	I_A	-	50	55	mA
(Note 5)	V_D= 5 V	I_D	-	38	60	mA
	V_D= 3.3 V	I_D	-	25	40	mA
	Interface current, VLC=5 V (Note 6, 7)	I_{LC}	-	2	-	µA
	VLS=5 V	I_{LS}	-	84	-	µA
	power-down state (all supplies) (Note 8)	I_{pd}	-	200	-	µA
Power Dissipation	(Note 5)					
VA = 5 V, VD = 3.3 V	normal operation		-	335	410	mW
	power-down (Note 8)		-	1	-	mW
VA = 5 V, VD = 5 V	normal operation		-	440	575	mW
	power-down (Note 8)		-	1	-	mW
Package Thermal Resistance		θ_{JA}	-	48	-	°C/Watt
		θ_{JC}	-	15	-	°C/Watt
Power Supply Rejection Ratio (Note 9)	(1 kHz)	PSRR	-	60	-	dB
	(60 Hz)		-	40	-	dB

Notes:
4. V_{FS} is tested under load R_L and includes attenuation due to Z_{OUT}
5. Current consumption increases with increasing FS within a given speed mode and is signal dependant. Max values are based on highest FS and highest MCLK.
6. I_{LC} measured with no external loading on the SDA pin.
7. This specification is violated when the VLC supply is greater than VD and when pin 16 (M1/SDA) is tied or pulled low. Logic tied to pin 16 needs to be able to sink this current.
8. Power down mode is defined as $\overline{RST}$ pin = Low with all clock and data lines held static.
9. Valid with the recommended capacitor values on FILT+ and VQ as shown in Figures 5 and 6.

ANALOG FILTER RESPONSE

Parameter		Fast Roll-Off Min	Fast Roll-Off Typ	Fast Roll-Off Max	Slow Roll-Off (Note 10) Min	Slow Roll-Off (Note 10) Typ	Slow Roll-Off (Note 10) Max	Unit
Combined Digital and On-chip Analog Filter Response - Single Speed Mode (Note 11)								
Passband (Note 12)	to -0.01 dB corner	0	-	.454	0	-	0.417	Fs
	to -3 dB corner	0	-	.499	0	-	0.499	Fs
Frequency Response 10 Hz to 20 kHz		-0.01	-	+0.01	-0.01	-	+0.01	dB
StopBand		.547	-	-	.583	-	-	Fs
StopBand Attenuation	(Note 13)	90	-	-	64	-	-	dB
Group Delay		-	12/Fs	-	-	6.5/Fs	-	s
Passband Group Delay Deviation	0 - 20 kHz	-	-	±0.41/Fs		-	±0.14/Fs	s
De-emphasis Error (Note 14)	Fs = 32 kHz	-	-	±0.23	-	-	±0.23	dB
(Relative to 1 kHz)	Fs = 44.1 kHz	-	-	±0.14	-	-	±0.14	dB
	Fs = 48 kHz	-	-	±0.09	-	-	±0.09	dB
Combined Digital and On-chip Analog Filter Response - Double Speed Mode - 96 kHz (Note 11)								
Passband (Note 12)	to -0.01 dB corner	0	-	.430	0	-	.296	Fs
	to -3 dB corner	0	-	.499	0	-	.499	Fs
Frequency Response 10 Hz to 20 kHz		-0.01	-	0.01	-0.01	-	0.01	dB
StopBand		.583	-	-	.792	-	-	Fs
StopBand Attenuation	(Note 13)	80	-	-	70	-	-	dB
Group Delay		-	4.6/Fs	-	-	3.9/Fs	-	s
Passband Group Delay Deviation	0 - 20 kHz	-	-	±0.03/Fs		-	±0.01/Fs	s
Combined Digital and On-chip Analog Filter Response - Quad Speed Mode - 192 kHz (Note 11)								
Passband (Note 12)	to -0.01 dB corner	0	-	.105	0	-	.104	Fs
	to -3 dB corner	0	-	.490	0	-	.481	Fs
Frequency Response 10 Hz to 20 kHz		-0.01	-	0.01	-0.01	-	0.01	dB
StopBand		.635	-	-	.868	-	-	Fs
StopBand Attenuation	(Note 13)	90	-	-	75	-	-	dB
Group Delay		-	4.7/Fs	-	-	4.2/Fs	-	s
Passband Group Delay Deviation	0 - 20 kHz	-	-	±0.01/Fs		-	±0.01/Fs	s
Combined Digital and On-chip Analog Filter Response - DSD Mode (Note 11)								
Passband (Note 12)	to -0.1 dB corner	-	-	-	0	-	20	kHz
	to -3 dB corner	-	-	-	0	-	120	kHz
Frequency Response 10 Hz to 20 kHz		-	-	-	-.01	-	0.1	dB

Notes: 10. Slow Roll-Off interpolation filter is only available in control port mode.

11. Filter response is not tested but is guaranteed by design.

12. Response is clock dependent and will scale with Fs. Note that the response plots (Figures 9 to 32) have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.

13. Single and Double Speed Mode Measurement Bandwidth is from stopband to 3 Fs.
Quad Speed Mode Measurement Bandwidth is from stopband to 1.34 Fs.

14. De-emphasis is available only in Single Speed Mode; Only 44.1 kHz De-emphasis is available in Stand-Alone Mode

DIGITAL CHARACTERISTICS (For KQZ T_A = -10 to +70 °C; VLC = VLS = 1.8 V to 5.5 V)

Parameters		Symbol	Min	Typ	Max	Units
High-Level Input Voltage	Serial Data Port	V_{IH}	70% VLS	-	-	V
	Control Port	V_{IH}	70% VLC	-	-	V
Low-Level Input Voltage	Serial Data Port	V_{IL}	-	-	20% VLS	V
	Control Port	V_{IL}	-	-	20% VLC	V
Input Leakage Current	(Note 7)	I_{in}	-	-	±10	µA
Input Capacitance			-	8	-	pF
Maximum MUTEC Drive Current			-	3	-	mA
MUTEC High-Level Output Voltage		V_{OH}	-	VA	-	V
MUTEC Low-Level Output Voltage		V_{OL}	-	0	-	V

ABSOLUTE MAXIMUM RATINGS (GND = 0 V; all voltages with respect to ground.)

Parameters		Symbol	Min	Max	Units
DC Power Supply	Analog power	VA	-0.3	6.0	V
	Digital internal power	VD	-0.3	6.0	V
	Serial data port interface power	VLS	-0.3	6.0	V
	Control port interface power	VLC	-0.3	6.0	V
Input Current, Any Pin Except Supplies		I_{in}	-	±10	mA
Digital Input Voltage	Serial data port interface	V_{IND-S}	-0.3	VLS+ 0.4	V
	Control port interface	V_{IND-C}	-0.3	VLC+ 0.4	V
Ambient Operating Temperature (power applied)		T_A	-55	125	°C
Storage Temperature		T_{stg}	-65	150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS (GND = 0 V; all voltages with respect to ground.)

Parameters		Symbol	Min	Typ	Max	Units
DC Power Supply	Analog power	VA	4.5	5.0	5.5	V
	Digital internal power	VD	3.0	3.3	5.5	V
	Serial data port interface power	VLS	1.8	5.0	5.5	V
	Control port interface power	VLC	1.8	5.0	5.5	V

SWITCHING CHARACTERISTICS (For KQZ T_A = -10 to +70 °C; VLS = 1.8 V to 5.5 V; Inputs: Logic 0 = GND, Logic 1 = VLS, C_L = 30 pF)

Parameters		Symbol	Min	Typ	Max	Units
MCLK Frequency	(Note 15)					
	Single Speed Mode		1.024	-	51.2	MHz
	Double Speed Mode		6.400	-	51.2	MHz
	Quad Speed Mode		6.400	-	51.2	MHz
MCLK Duty Cycle			40	50	60	%
Input Sample Rate	Single Speed Mode	Fs	4	-	50	kHz
	Double Speed Mode	Fs	50	-	100	kHz
	Quad Speed Mode	Fs	100	-	200	kHz
LRCK Duty Cycle			45	50	55	%
SCLK Pulse Width Low		t_{sclkl}	20	-	-	ns
SCLK Pulse Width High		t_{sclkh}	20	-	-	ns
SCLK Period		t_{sclkw}	$\frac{2}{MCLK}$	-	-	ns
	(Note 16)	t_{sclkw}	$\frac{4}{MCLK}$	-	-	ns
SCLK rising to LRCK edge delay		t_{slrd}	20	-	-	ns
SCLK rising to LRCK edge setup time		t_{slrs}	20	-	-	ns
SDATA valid to SCLK rising setup time		t_{sdlrs}	20	-	-	ns
SCLK rising to SDATA hold time		t_{sdh}	20	-	-	ns
LRCK1 to LRCK2 frequency ratio	(Note 17)		0.25	1.00	4.00	

Notes: 15. See Table 5 on page 26 for suggested MCLK frequencies

16. This serial clock is available only in Control Port Mode when the MCLK Divide bit is enabled.

17. The higher frequency LRCK must be an exact integer multiple (1, 2, or 4) of the lower frequency LRCK

.

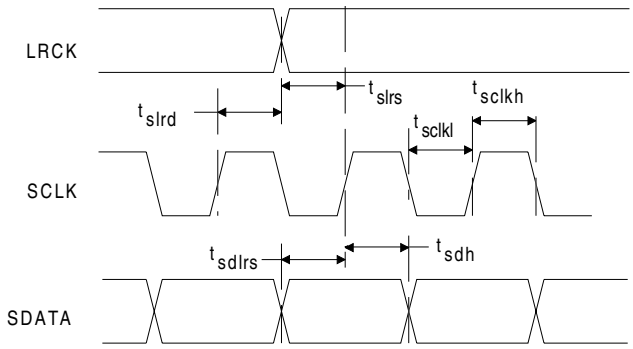


Figure 1. Serial Mode Input Timing

DSD - SWITCHING CHARACTERISTICS (T_A= -10 to 70°C; Logic 0 = GND; VLS = 1.8 V to 5.5 V; Logic 1 = VLS Volts; C_L = 30 pF)

Parameter		Symbol	Min	Typ	Max	Unit
Master Clock Frequency	(Note 18)		4.096	-	38.4	MHz
MCLK Duty Cycle	(All DSD modes)		40	50	60	%
DSD_SCLK Pulse Width Low		t_{sclkl}	20	-	-	ns
DSD_SCLK Pulse Width High		t_{sclkh}	20	-	-	ns
DSD_SCLK Frequency	(64x Oversampled)		1.024	-	3.2	MHz
	(128x Oversampled)		2.048	-	6.4	MHz
DSD_L / _R valid to DSD_SCLK rising setup time		t_{sdlrs}	20	-	-	ns
DSD_SCLK rising to DSD_L or DSD_R hold time		t_{sdh}	20	-	-	ns

Note: 18. Min is 4 times 64x DSD or 2 times 128x DSD, and Max is 12 times 64x DSD or 6 times 128x DSD. The proper MCLK to DSD_SCLK ratio must be set either by the DIF registers or the M0:2 pins

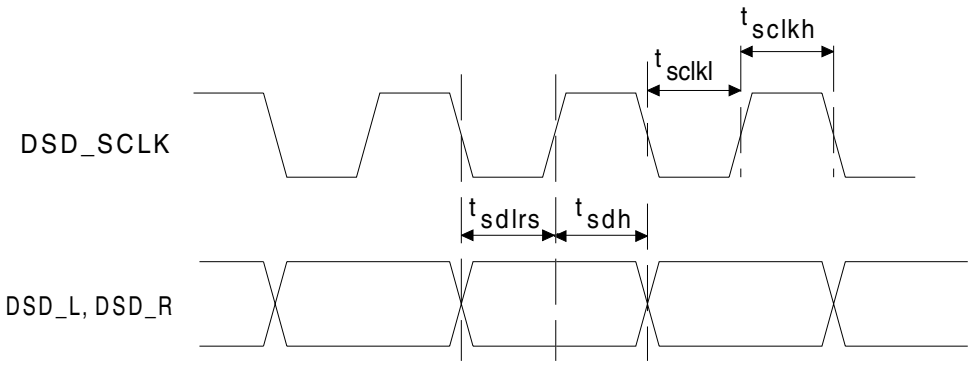


Figure 2. Direct Stream Digital - Serial Audio Input Timing

SWITCHING CHARACTERISTICS - CONTROL PORT - I²C FORMAT

(For KQZ T_A = -10 to +70 °C; VLC = 1.8 V to 5.5 V; Inputs: Logic 0 = GND, Logic 1 = VLC, C_L = 30 pF)

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f_{scl}	-	100	kHz
$\overline{RST}$ Rising Edge to Start	t_{irs}	500	-	ns
Bus Free Time Between Transmissions	t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	µs
Clock Low time	t_{low}	4.7	-	µs
Clock High Time	t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling (Note 19)	t_{hdd}	0	-	µs
SDA Setup time to SCL Rising	t_{sud}	250	-	ns
Rise Time of SCL and SDA	t_{rc}, t_{rc}	-	1	µs
Fall Time SCL and SDA	t_{fc}, t_{fc}	-	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	µs
Acknowledge Delay from SCL Falling (Note 20)	t_{ack}	-	(Note 21)	ns

Notes: 19. Data must be held for sufficient time to bridge the transition time, t_{fc}, of SCL.

20. The acknowledge delay is based on MCLK and can limit the maximum transaction speed.

21. $\frac{15}{256 \times Fs}$ for Single-Speed Mode, $\frac{15}{128 \times Fs}$ for Double-Speed Mode, $\frac{15}{64 \times Fs}$ for Quad-Speed Mode.

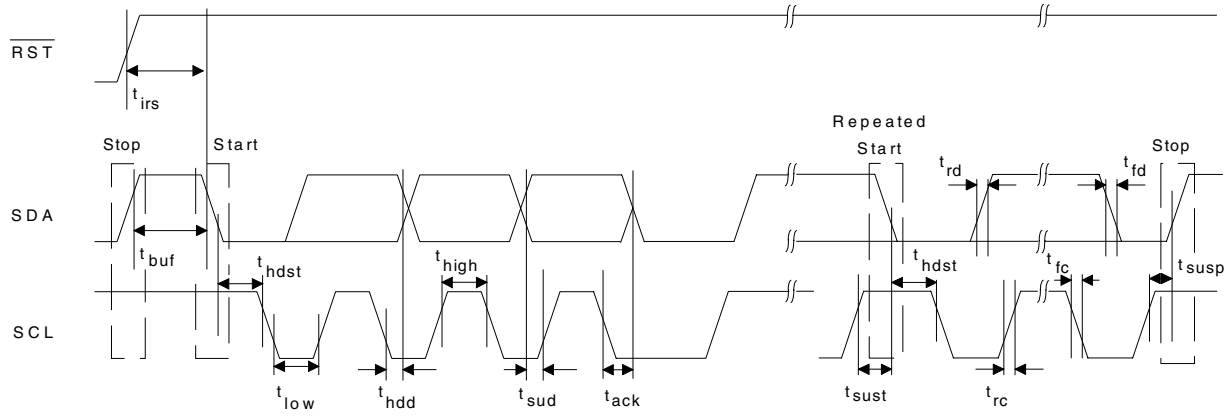


Figure 3. Control Port Timing - I²C Format

SWITCHING CHARACTERISTICS - CONTROL PORT - SPI™ FORMAT

(For KQZ T_A = -10 to +70 °C; VLC = 1.8 V to 5.5 V; Inputs: Logic 0 = GND, Logic 1 = VLC, C_L = 30 pF)

Parameter		Symbol	Min	Max	Unit
CCLK Clock Frequency		f_{sclk}	-	$\frac{MCLK}{2}$	MHz
$\overline{RST}$ Rising Edge to CS Falling		t_{srs}	500	-	ns
CCLK Edge to $\overline{CS}$ Falling	(Note 22)	t_{spi}	500	-	ns
$\overline{CS}$ High Time Between Transmissions		t_{csh}	1.0	-	µs
$\overline{CS}$ Falling to CCLK Edge		t_{css}	20	-	ns
CCLK Low Time		t_{scl}	$\frac{1}{MCLK}$	-	ns
CCLK High Time		t_{sch}	$\frac{1}{MCLK}$	-	ns
CDIN to CCLK Rising Setup Time		t_{dsu}	40	-	ns
CCLK Rising to DATA Hold Time	(Note 23)	t_{dh}	15	-	ns
Rise Time of CCLK and CDIN	(Note 24)	t_{r2}	-	100	ns
Fall Time of CCLK and CDIN	(Note 24)	t_{f2}	-	100	ns

Notes: 22. t_{spi} only needed before first falling edge of $\overline{CS}$ after $\overline{RST}$ rising edge. t_{spi} = 0 at all other times.

23. Data must be held for sufficient time to bridge the transition time of CCLK.

24. For F_{SCK} < 1 MHz.

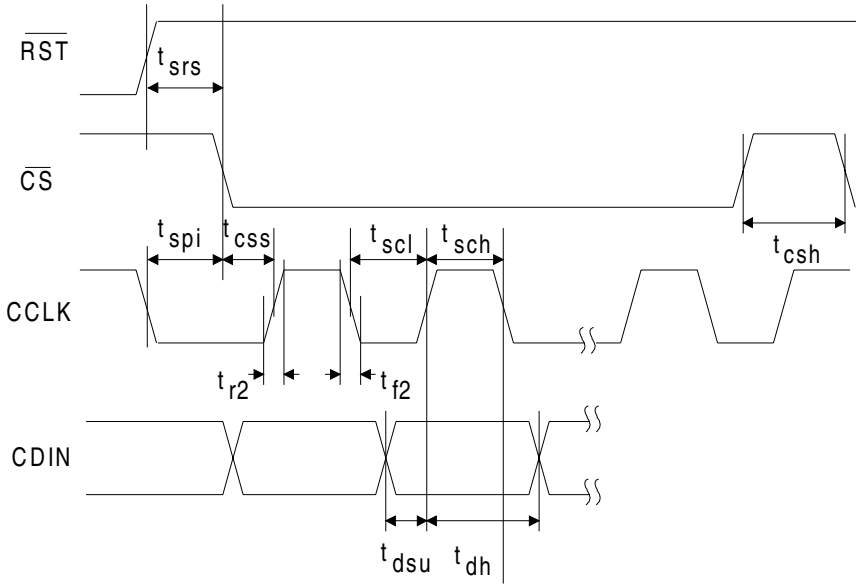


Figure 4. Control Port Timing - SPI Format

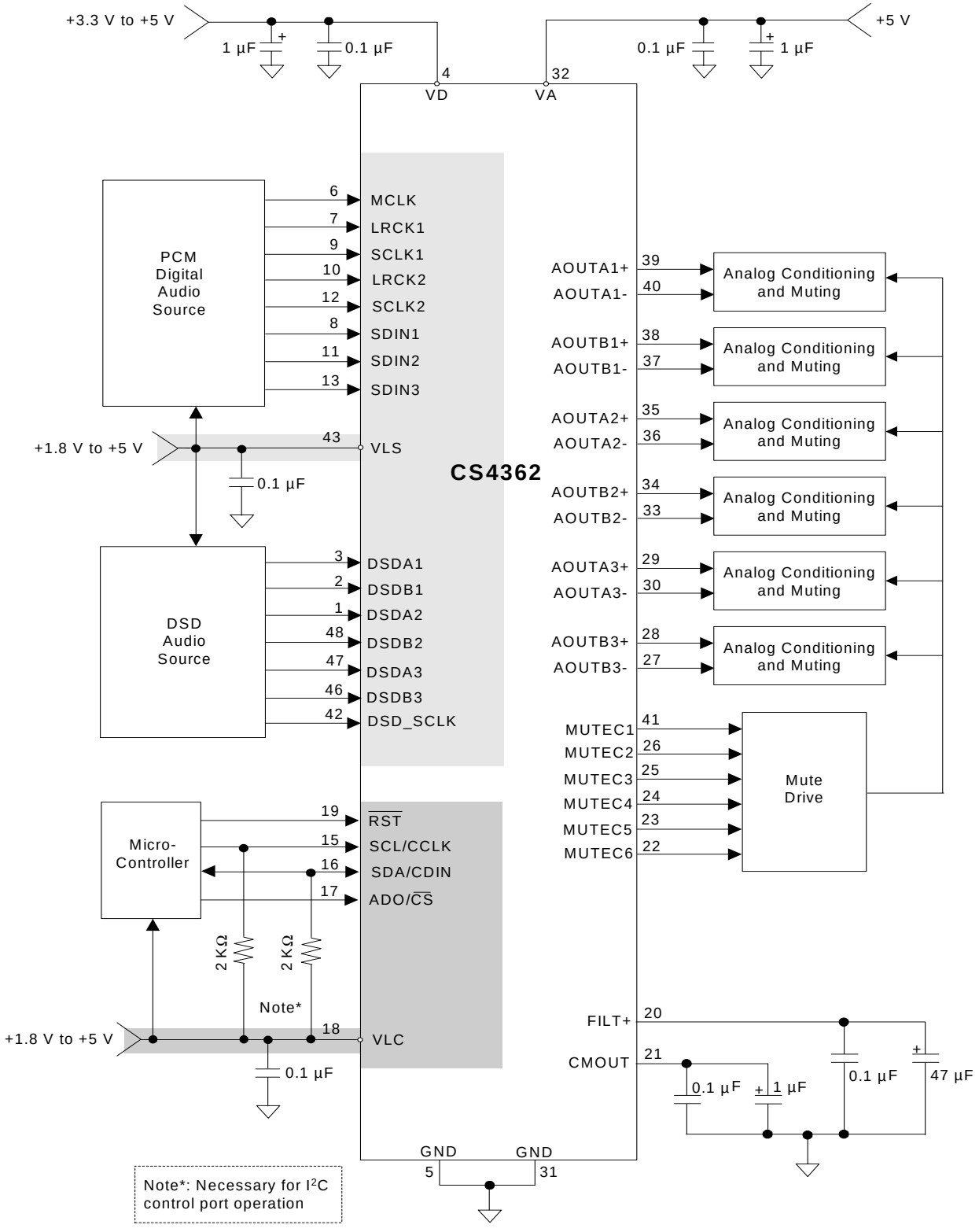


Figure 5. Typical Connection Diagram Control Port

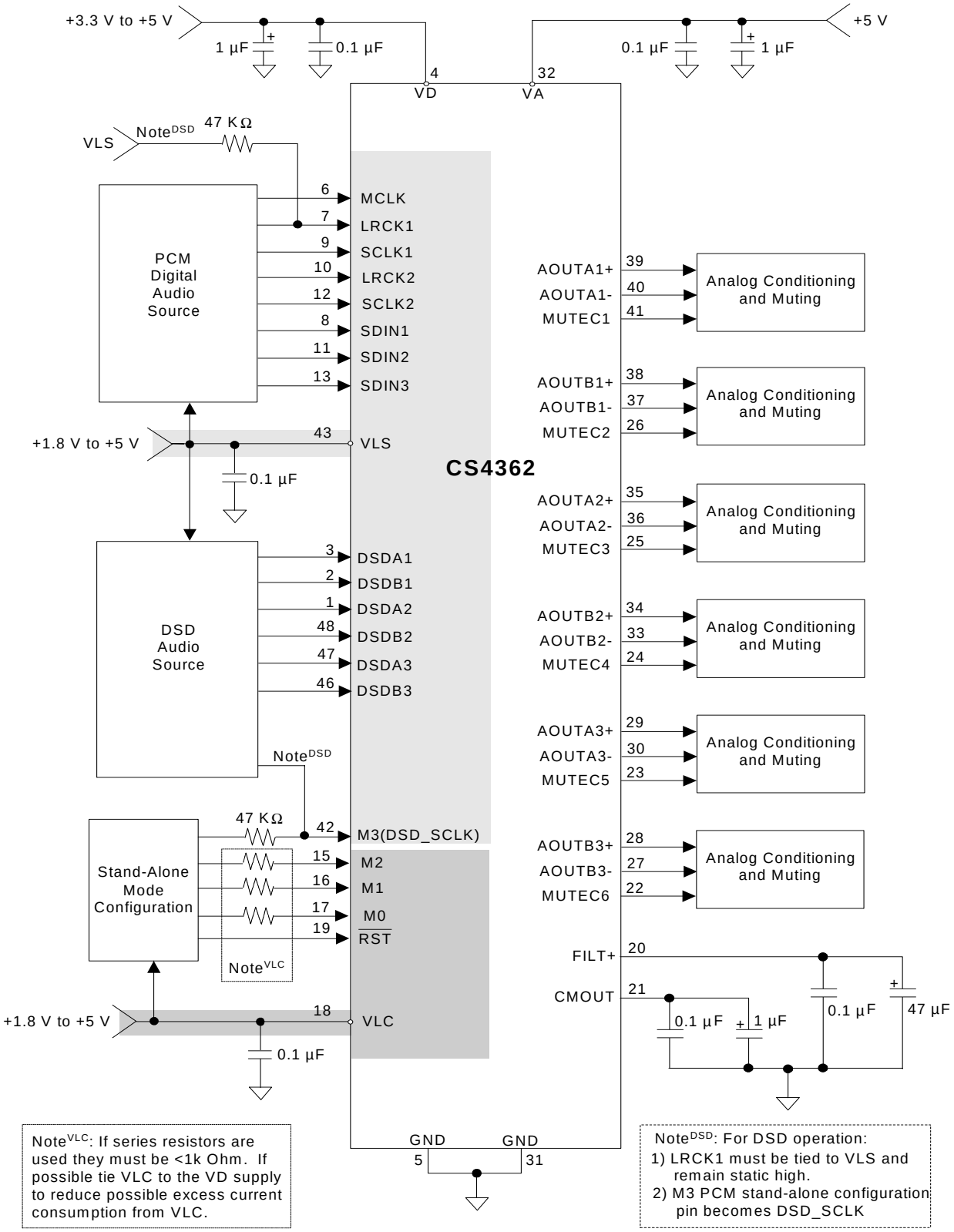


Figure 6. Typical Connection Diagram Stand-Alone

2. REGISTER QUICK REFERENCE

Addr	Function	7	6	5	4	3	2	1	0
01h	Mode Control 1	CPEN	FREEZE	MCLKDIV	Reserved	DAC3_DIS	DAC2_DIS	DAC1_DIS	PDN
	default	0	0	0	0	0	0	0	1
02h	Mode Control 2	Reserved	DIF2	DIF1	DIF0	Reserved	SDIN3CLK	SDIN2CLK	SDIN1CLK
	default	0	0	0	0	0	0	0	0
03h	Mode Control 3	SZC1	SZC0	SNGLVOL	RMP_UP	MUTEC+/-	AMUTE	MUTEC1	MUTEC0
	default	1	0	0	0	0	1	0	0
04h	Filter Control	Reserved	Reserved	Reserved	FILT_SEL	Reserved	DEM1	DEM0	RMP_DN
	default	0	0	0	0	0	0	0	0
05h	Invert Control	Reserved	Reserved	INV_B3	INV_A3	INV_B2	INV_A2	INV_B1	INV_A1
	default	0	0	0	0	0	0	0	0
06h	Mixing Control Pair 1 (AOUTx1)	P1_A=B	P1ATAPI4	P1ATAPI3	P1ATAPI2	P1ATAPI1	P1ATAPI0	P1FM1	P1FM0
	default	0	0	1	0	0	1	0	0
07h	Vol. Control A1	A1_MUTE	A1_VOL6	A1_VOL5	A1_VOL4	A1_VOL3	A1_VOL2	A1_VOL1	A1_VOL0
	default	0	0	0	0	0	0	0	0
08h	Vol. Control B1	B1_MUTE	B1_VOL6	B1_VOL5	B1_VOL4	B1_VOL3	B1_VOL2	B1_VOL1	B1_VOL0
	default	0	0	0	0	0	0	0	0
09h	Mixing Control Pair 2 (AOUTx2)	P2_A=B	P2ATAPI4	P2ATAPI3	P2ATAPI2	P2ATAPI1	P2ATAPI0	P2FM1	P2FM0
	default	0	0	1	0	0	1	0	0
0Ah	Vol. Control A2	A2_MUTE	A2_VOL6	A2_VOL5	A2_VOL4	A2_VOL3	A2_VOL2	A2_VOL1	A2_VOL0
	default	0	0	0	0	0	0	0	0
0Bh	Vol. Control B2	B2_MUTE	B2_VOL6	B2_VOL5	B2_VOL4	B2_VOL3	B2_VOL2	B2_VOL1	B2_VOL0
	default	0	0	0	0	0	0	0	0
0Ch	Mixing Control Pair 3 (AOUTx3)	P3_A=B	P3ATAPI4	P3ATAPI3	P3ATAPI2	P3ATAPI1	P3ATAPI0	P3FM1	P3FM0
	default	0	0	1	0	0	1	0	0
0Dh	Vol. Control A3	A3_MUTE	A3_VOL6	A3_VOL5	A3_VOL4	A3_VOL3	A3_VOL2	A3_VOL1	A3_VOL0
	default	0	0	0	0	0	0	0	0
0Eh	Vol. Control B3	B3_MUTE	B3_VOL6	B3_VOL5	B3_VOL4	B3_VOL3	B3_VOL2	B3_VOL1	B3_VOL0
	default	0	0	0	0	0	0	0	0
12h	Chip Revision	PART3	PART2	PART1	PART0	Reserved	Reserved	Reserved	Reserved
	default	1	1	1	0	-	-	-	-

3. REGISTER DESCRIPTION

Note: All registers are read/write in I^2C mode and write only in SPI, unless otherwise noted.

3.1 Mode Control 1 (address 01h)

7	6	5	4	3	2	1	0
CPEN	FREEZE	MCLKDIV	Reserved	DAC3_DIS	DAC2_DIS	DAC1_DIS	PDN
0	0	0	0	0	0	0	1

3.1.1 CONTROL PORT ENABLE (CPEN)

Default = 0
0 - Disabled
1 - Enabled

Function:

This bit defaults to 0, allowing the device to power-up in Stand-Alone mode. The Control port mode can be accessed by setting this bit to 1. This will allow the operation of the device to be controlled by the registers and the pin definitions will conform to Control Port Mode. To accomplish a clean power-up, the user should write this bit within 10 ms following the release of Reset.

3.1.2 FREEZE CONTROLS (FREEZE)

Default = 0
0 - Disabled
1 - Enabled

Function:

This function allows modifications to be made to the registers without the changes taking effect until the FREEZE is disabled. To make multiple changes in the Control port registers take effect simultaneously, enable the FREEZE Bit, make all register changes, then Disable the FREEZE bit.

3.1.3 MASTER CLOCK DIVIDE ENABLE (MCLKDIV)

Default = 0
0 - Disabled
1 - Enabled

Function:

The MCLKDIV bit enables a circuit which divides the externally applied MCLK signal by 2 prior to all other internal circuitry.

3.1.4 DAC PAIR DISABLE (DACX_DIS)

Default = 0
0 - Enabled
1 - Disabled

Function:

When enabled the respective DAC channel pair*x* (AOUTAx and AOUTBx) will remain in a reset state. It is advised that changes to these bits be made while the power down bit is enabled to eliminate the possibility of audible artifacts.

3.1.5 POWER DOWN (PDN)

Default = 1
0 - Disabled
1 - Enabled

Function:

The entire device will enter a low-power state when this function is enabled, and the contents of the control registers are retained in this mode. The power-down bit defaults to 'enabled' on power-up and must be disabled before normal operation in Control Port mode can occur.

3.2 Mode Control 2 (address 02h)

7	6	5	4	3	2	1	0
Reserved	DIF2	DIF1	DIF0	Reserved	SDIN3CLK	SDIN2CLK	SDIN1CLK
0	0	0	0	0	0	0	0

3.2.1 DIGITAL INTERFACE FORMAT (DIF)

*Default = 000 - Format 0 (*Left Justified, up to 24-bit data*)*

Function:

These bits select the interface format for the serial audio input. The Functional Mode bits determine whether PCM or DSD mode is selected.

PCM Mode: The required relationship between the Left/Right clock, serial clock and serial data is defined by the Digital Interface Format and the options are detailed in Figures 33-38.

DIF2	DIF1	DIF0	DESCRIPTION	Format	FIGURE
0	0	0	Left Justified, up to 24-bit data	0	33
0	0	1	I^2S, up to 24-bit data	1	34
0	1	0	Right Justified, 16-bit data	2	35
0	1	1	Right Justified, 24-bit data	3	36
1	0	0	Right Justified, 20-bit data	4	37
1	0	1	Right Justified, 18-bit data	5	38
1	1	0	Reserved		
1	1	1	Reserved		

Table 1. Digital Interface Formats - PCM Mode

DSD Mode: The relationship between the oversampling ratio of the DSD audio data and the required Master clock to DSD data rate is defined by the Digital Interface Format pins. An additional write of 99h to register 00h and 80h to register 1Ah is required to access the modes denoted with *.

DIF2	DIF1	DIFO	DESCRIPTION	Note
0	0	0	64x oversampled DSD data with a 4x MCLK to DSD data rate	
0	0	1	64x oversampled DSD data with a 6x MCLK to DSD data rate	*
0	1	0	64x oversampled DSD data with a 8x MCLK to DSD data rate	*
0	1	1	64x oversampled DSD data with a 12x MCLK to DSD data rate	*
1	0	0	128x oversampled DSD data with a 2x MCLK to DSD data rate	
1	0	1	128x oversampled DSD data with a 3x MCLK to DSD data rate	*
1	1	0	128x oversampled DSD data with a 4x MCLK to DSD data rate	*
1	1	1	128x oversampled DSD data with a 6x MCLK to DSD data rate	*

Table 2. Digital Interface Formats - DSD Mode

3.2.2 SERIAL AUDIO DATA CLOCK SOURCE (SDINXCLK)

Default = 0
0 - SDINx clocked by SCLK1 and LRCK1
1 - SDINx clocked by SCLK2 and LRCK2

Function:

The SDINxCLK bit specifies which SCLK/LRCK input pair is used to clock in the data on the given SDINx line. For more details see "Clock Source Selection" on page 28.

3.3 Mode Control 3 (address 03h)

7	6	5	4	3	2	1	0
SZC1	SZC0	SNGLVOL	RMP_UP	Reserved	AMUTE	MUTEC1	MUTEC0
1	0	0	0	0	1	0	0

3.3.1 SOFT RAMP AND ZERO CROSS CONTROL (SZC)

Default = 10
00 - Immediate Change
01 - Zero Cross
10 - Soft Ramp
11 - Soft Ramp on Zero Crossings

Function:

Immediate Change

When Immediate Change is selected all level changes will take effect immediately in one step.

Zero Cross

Zero Cross Enable dictates that signal level changes, either by attenuation changes or muting, will occur on a signal zero crossing to minimize audible artifacts. The requested level change will occur after a timeout period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel.

Soft Ramp

Soft Ramp allows level changes, both muting and attenuation, to be implemented by incrementally ramping, in 1/8 dB steps, from the current level to the new level at a rate of 1 dB per 8 left/right clock periods.

Soft Ramp on Zero Crossing

Soft Ramp and Zero Cross Enable dictates that signal level changes, either by attenuation changes or muting, will occur in 1/8 dB steps and be implemented on a signal zero crossing. The 1/8 dB level change will occur after a timeout period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel.

3.3.2 SINGLE VOLUME CONTROL (SNGLVOL)

Default = 0
0 - Disabled
1 - Enabled

Function:

The individual channel volume levels are independently controlled by their respective Volume Control Bytes when this function is disabled. The volume on all channels is determined by the A1 Channel Volume Control Byte, and the other Volume Control Bytes are ignored when this function is enabled.

3.3.3 SOFT VOLUME RAMP-UP AFTER ERROR (RMP_UP)

Default = 0
0 - Disabled
1 - Enabled

Function:

An un-mute will be performed after executing a filter mode change, after a LRCK/MCLK ratio change or error, and after changing the Functional Mode. When this feature is enabled, this un-mute is effected, similar to attenuation changes, by the Soft and Zero Cross bits in the Mode Control 3 register. When disabled, an immediate un-mute is performed in these instances.

Note: For best results, it is recommended that this feature be used in conjunction with the RMP_DN bit.

3.3.4 MUTEC POLARITY (MUTEC+/-)

Default = 0
0 - Active High
1 - Active Low

Function:

The active polarity of the MUTEC pin(s) is determined by this register. When set to 0 (default) the MUTEC pins are high when active. When set to 1 the MUTEC pin(s) are low when active.

Note: When the on board mute circuitry is designed for active low, the MUTEC outputs will be high (un-muted) for the period of time during reset and before this bit is enabled to 1.

3.3.5 AUTO-MUTE (AMUTE)

Default = 1
0 - Disabled
1 - Enabled

Function:

The Digital-to-Analog converter output will mute following the reception of 8192 consecutive audio samples of static 0 or -1. A single sample of non-static data will release the mute. Detection and muting is done independently for each channel. The quiescent voltage on the output will be retained and the Mute Control pin will go active during the mute period. The muting function is affected, similar to volume control changes, by the Soft and Zero Cross bits in the Mode Control 3 register.

3.3.6 MUTE PIN CONTROL(MUTEC1, MUTEC0)

Default = 00
00 - Six mute control signals
01, 10 - One mute control signal
11 - Three mute control signals

Function:

Selects how the internal mute control signals are routed to the MUTEC1 through MUTEC6 pins. When set to '00', there is one mute control signal for each channel: AOUT1A on MUTEC1, AOUT1B on MUTEC2, etc. When set to either '01' or '10', there is a single mute control signal on the MUTEC1 pin. When set to '11', there are three mute control signals, one for each stereo pair: AOUT1A and AOUT1B on MUTEC1, AOUT2A and AOUT2B on MUTEC2, and AOUT3A and AOUT3B on MUTEC3.

3.4 Filter Control (address 04h)

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	FILT_SEL	Reserved	DEM1	DEM0	RMP_DN
0	0	0	0	0	0	0	0

3.4.1 INTERPOLATION FILTER SELECT (FILT_SEL)

Default = 0
0 - Fast roll-off
1 - Slow roll-off

Function:

This Function allows the user to select whether the interpolation filter has a fast or slow roll off. For filter characteristics please see Section 1.

3.4.2 DE-EMPHASIS CONTROL (DEM)

Default = 00
00 - Disabled
01 - 44.1 kHz
10 - 48 kHz
11 - 32 kHz

Function:

Selects the appropriate digital filter to maintain the standard 15 µs/50 µs digital de-emphasis filter response at 32, 44.1 or 48 kHz sample rates. (see Figure 39)

De-emphasis is only available in Single Speed Mode.

3.4.3 SOFT RAMP-DOWN BEFORE FILTER MODE CHANGE (RMP_DN)

Default = 0
0 - Disabled
1 - Enabled

Function:

A mute will be performed prior to executing a filter mode change. When this feature is enabled, this mute is effected, similar to attenuation changes, by the Soft and Zero Cross bits in the Mode Control 3 register. When disabled, an immediate mute is performed prior to executing a filter mode change.

Note: For best results, it is recommended that this feature be used in conjunction with the RMP_UP bit.

3.5 Invert control (address 05h)

7	6	5	4	3	2	1	0
Reserved	Reserved	INV_B3	INV_A3	INV_B2	INV_A2	INV_B1	INV_A1
0	0	0	0	0	0	0	0

3.5.1 INVERT SIGNAL POLARITY (INV_XX)

Default = 0
0 - Disabled
1 - Enabled

Function:

When enabled, these bits will invert the signal polarity of their respective channels.

3.6 Mixing Control Pair 1 (Channels A1 & B1)(address 06h)
Mixing Control Pair 2 (Channels A2 & B2)(address 09h)
Mixing Control Pair 3 (Channels A3 & B3)(address 0Ch)

7	6	5	4	3	2	1	0
Px_A=B	PxATAPI4	PxATAPI3	PxATAPI2	PxATAPI1	PxATAPI0	PxFM1	PxFM0
0	0	1	0	0	1	0	0

3.6.1 CHANNEL A VOLUME = CHANNEL B VOLUME (A=B)

Default = 0
0 - Disabled
1 - Enabled

Function:

The AOUTAx and AOUTBx volume levels are independently controlled by the A and the B Channel Volume Control Bytes when this function is disabled. The volume on both AOUTAx and AOUTBx are determined by the A Channel Attenuation and Volume Control Bytes (per A-B pair), and the B Channel Bytes are ignored when this function is enabled.

3.6.2 ATAPI CHANNEL MIXING AND MUTING (ATAPI)

Default = 01001 - AOUTAx=aL, AOUTBx=bR (Stereo)

Function:

The CS4362 implements the channel mixing functions of the ATAPI CD-ROM specification. The ATAPI functions are applied per A-B pair. Refer to Table 3 and Figure 41 for additional information.

ATAPI4	ATAPI3	ATAPI2	ATAPI1	ATAPI0	AOUTAx	AOUTBx
0	0	0	0	0	MUTE	MUTE
0	0	0	0	1	MUTE	bR
0	0	0	1	0	MUTE	bL
0	0	0	1	1	MUTE	b[(L+R)/2]
0	0	1	0	0	aR	MUTE
0	0	1	0	1	aR	bR
0	0	1	1	0	aR	bL
0	0	1	1	1	aR	b[(L+R)/2]
0	1	0	0	0	aL	MUTE
0	1	0	0	1	aL	bR
0	1	0	1	0	aL	bL
0	1	0	1	1	aL	b[(L+R)/2]
0	1	1	0	0	a[(L+R)/2]	MUTE
0	1	1	0	1	a[(L+R)/2]	bR
0	1	1	1	0	a[(L+R)/2]	bL
0	1	1	1	1	a[(L+R)/2]	b[(L+R)/2]
1	0	0	0	0	MUTE	MUTE
1	0	0	0	1	MUTE	bR
1	0	0	1	0	MUTE	bL
1	0	0	1	1	MUTE	[(aL+bR)/2]
1	0	1	0	0	aR	MUTE
1	0	1	0	1	aR	bR
1	0	1	1	0	aR	bL
1	0	1	1	1	aR	[(bL+aR)/2]
1	1	0	0	0	aL	MUTE
1	1	0	0	1	aL	bR
1	1	0	1	0	aL	bL
1	1	0	1	1	aL	[(aL+bR)/2]
1	1	1	0	0	[(aL+bR)/2]	MUTE
1	1	1	0	1	[(aL+bR)/2]	bR
1	1	1	1	0	[(bL+aR)/2]	bL
1	1	1	1	1	[(aL+bR)/2]	[(aL+bR)/2]

Table 3. ATAPI Decode

3.6.3 FUNCTIONAL MODE (FM)

Default = 00
00 - Single-Speed Mode (4 to 50 kHz sample rates)
01 - Double-Speed Mode (50 to 100 kHz sample rates)
10 - Quad-Speed Mode (100 to 200 kHz sample rates)
11 - Direct Stream Digital Mode

Function:

Selects the required range of input sample rates or DSD Mode. All DAC pairs set to the same SCLK/LRCK pair (section 3.2.2) are required to be set to the same functional mode setting before a speed mode change is accepted. When DSD mode is selected for any channel pair then all pairs will switch to DSD mode.

3.7 Volume control (addresses 07h, 08h, 0Ah, 0Bh, 0Dh, 0Eh)

7	6	5	4	3	2	1	0
xx_MUTE	xx_VOL6	xx_VOL5	xx_VOL4	xx_VOL3	xx_VOL2	xx_VOL1	xx_VOL0
0	0	0	0	0	0	0	0

3.7.1 MUTE (MUTE)

Default = 0
0 - Disabled
1 - Enabled

Function:

The Digital-to-Analog converter output will mute when enabled. The quiescent voltage on the output will be retained. The muting function is effected, similar to attenuation changes, by the Soft and Zero Cross bits. The MUTE pins will go active during the mute period according to the MUTEC bits.

3.7.2 VOLUME CONTROL (XX_VOL)

Default = 0 (No attenuation)

Function:

The Digital Volume Control registers allow independent control of the signal levels in 1 dB increments from 0 to -127 dB. Volume settings are decoded as shown in Table 4. The volume changes are implemented as dictated by the Soft and Zero Cross bits. All volume settings less than -127 dB are equivalent to enabling the MUTE bit.

Binary Code	Decimal Value	Volume Setting
0000000	0	0 dB
0010100	20	-20 dB
0101000	40	-40 dB
0111100	60	-60 dB
1011010	90	-90 dB

Table 4. Example Digital Volume Settings

3.8 Chip Revision (address 12h)

7	6	5	4	3	2	1	0
PART3	PART2	PART1	PART0	Reserved	Reserved	Reserved	Reserved
1	1	1	0	-	-	-	-

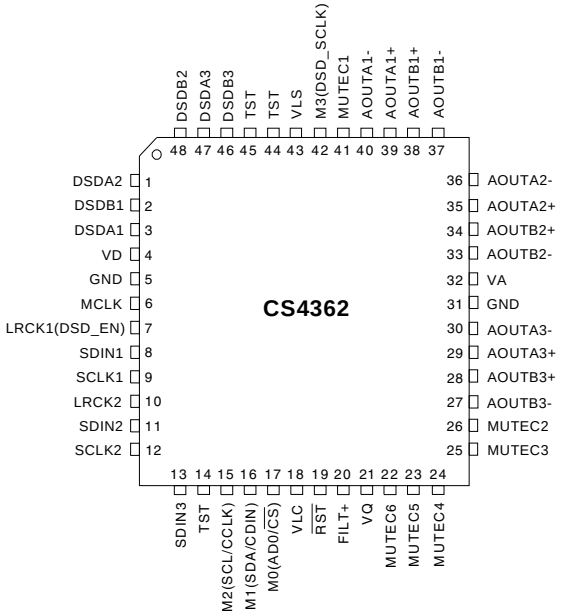
3.8.1 PART NUMBER ID (PART) [READ ONLY]

1110 - CS4362

Function:

This read-only register can be used to identify the model number of the device.

4. PIN DESCRIPTION



Pin Name	#	Pin Description
VD	4	**Digital Power** (*Input*) **-** Positive power supply for the digital section. Refer to the Recommended Operating Conditions for appropriate voltages.
GND	5 31	**Ground** (*Input*) - Ground reference. Should be connected to analog ground.
MCLK	6	**Master Clock** (*Input*) - Clock source for the delta-sigma modulator and digital filters. Table 5 illustrates several standard audio sample rates and the required master clock frequencies.
LRCK1 **LRCK2**	7 10	**Left Right Clock** (*Input*) - Determines which channel, Left or Right, is currently active on the serial audio data line. The frequency of the left/right clock must be at the audio sample rate, Fs.
SDIN1 **SDIN2** **SDIN3**	8 11 13	**Serial Data Input** (*Input*) - Input for two's complement serial audio data.
SCLK1 **SCLK2**	9 12	**Serial Clock** (*Input*) - Serial clocks for the serial audio interface.
TST	14 44 45	**Test -** These pins need to be tied to analog ground.
$\overline{\text{RST}}$	19	**Reset** (*Input*) - The device enters a low power mode and all internal registers are reset to their default settings when low.
VA	32	**Analog Power** (*Input*) **-** Positive power supply for the analog section. Refer to the Recommended Operating Conditions for appropriate voltages.
VLS	43	**Serial Audio Interface Power** (*Input*) **-** Determines the required signal level for the serial audio interface. Refer to the Recommended Operating Conditions for appropriate voltages.
VLC	18	**Control Port Power** (*Input*) **-** Determines the required signal level for the control port and stand alone configuration pins. Refer to the Recommended Operating Conditions for appropriate voltages.

Pin Name	#	Pin Description
VQ	21	**Quiescent Voltage** (*Output*) - Filter connection for internal quiescent voltage. VQ must be capacitively coupled to analog ground, as shown in the Typical Connection Diagram. The nominal voltage level is specified in the Analog Characteristics and Specifications section. VQ presents an appreciable source impedance and any current drawn from this pin will alter device performance. However, VQ can be used to bias the analog circuitry assuming there is no AC signal component and the DC current is less then the maximum specified in the Analog Characteristics and Specifications section.
FILT+	20	**Positive Voltage Reference** (*Output*) **-** Positive reference voltage for the internal sampling circuits. Requires the capacitive decoupling to analog ground as shown in the Typical Connection Diagram.
AOUTA1 +,- **AOUTB1 +,-** **AOUTA2 +,-** **AOUTB2 +,-** **AOUTA3 +,-** **AOUTB3 +,-**	39,40 38,37 35,36 34,33 29,30 28,27	**Differential Analog Output** (*Output*) - The full scale differential analog output level is specified in the Analog Characteristics specification table.
MUTEC1 **MUTEC2** **MUTEC3** **MUTEC4** **MUTEC5** **MUTEC6**	41 26 25 24 23 22	**Mute Control** (*Output*) - The Mute Control pins go high during power-up initialization, reset, muting, power-down or if the master clock to left/right clock frequency ratio is incorrect. These pins are intended to be used as a control for external mute circuits on the line outputs to prevent the clicks and pops that can occur in any single supply system. Use of Mute Control is not mandatory but recommended for designs requiring the absolute minimum in extraneous clicks and pops.
Stand Alone Definitions		
M0 **M1** **M2** **M3**	17 16 15 42	**Mode Selection** (*Input*) - Determines the operational mode of the device as detailed in Tables 6 and 7.
Control Port Definitions		
SCL/CCLK	15	**Serial Control Port Clock** (*Input*) - Serial clock for the serial control port. Requires an external pull-up resistor to the logic interface voltage in I^2C mode as shown in the Typical Connection Diagram.
SDA/CDIN	16	**Serial Control Port Data** (*Input/Output*) - SDA is a data I/O line in I^2C mode and is open drain, requiring an external pull-up resistor to the logic interface voltage, as shown in the Typical Connection Diagram; CDIN is the input data line for the control port interface in SPI mode.
AD0/$\overline{\text{CS}}$	17	**Address Bit 0 (I^2C) / Control Port Chip Select (SPI)** (*Input*) - AD0 is a chip address pin in I^2C mode; $\overline{\text{CS}}$ is the chip select signal for SPI mode.
DSD Definitions		
DSDA1 **DSDB1** **DSDA2** **DSDB2** **DSDA3** **DSDB3**	3 2 1 48 47 46	**Direct Stream Digital Input** (*Input)* - Input for Direct Stream Digital serial audio data.
DSD_SCLK	42	**DSD Serial Clock** *(Input)* - Serial clock for the Direct Stream Digital serial audio interface.
DSD_EN	7	**DSD Enable** *(Input)* - When held at logic '1' the device will enter DSD mode (Stand-Alone mode only).

Mode (sample-rate range)	Sample Rate (kHz)	MCLK (MHz)				Control port only modes
MCLK Ratio		**256x**	**384x**	**512x**	**768x**	**1024x***
Single Speed (4 to 50 kHz)	32	8.1920	12.2880	16.3840	24.5760	32.7680
	44.1	11.2896	16.9344	22.5792	33.8688	45.1584
	48	12.2880	18.4320	24.5760	36.8640	49.1520
MCLK Ratio		**128x**	**192x**	**256x**	**384x**	**512x***
Double Speed (50 to 100 kHz)	64	8.1920	12.2880	16.3840	24.5760	32.7680
	88.2	11.2896	16.9344	22.5792	33.8688	45.1584
	96	12.2880	18.4320	24.5760	36.8640	49.1520
MCLK Ratio		**64x**	**96x**	**128x**	**192x**	**256x***
Quad Speed (100 to 200 kHz)	176.4	11.2896	16.9344	22.5792	33.8688	45.1584
	192	12.2880	18.4320	24.5760	36.8640	49.1520

Table 5. Common Clock Frequencies

*Note: These modes are only available in control port mode by setting the MCLKDIV bit = 1.

M1 (DIF1)	M0 (DIF0)	DESCRIPTION	FORMAT	FIGURE
0	0	Left Justified, up to 24-bit data	0	33
0	1	I^2S, up to 24-bit data	1	34
1	0	Right Justified, 16-bit Data	2	35
1	1	Right Justified, 24-bit Data	3	36

Table 6. Digital Interface Format, Stand-Alone Mode Options

M3	M2 (DEM)	DESCRIPTION
0	0	Single-Speed without De-Emphasis (4 to 50 kHz sample rates)
0	1	Single-Speed with 44.1 kHz De-Emphasis; see Figure 39
1	0	Double-Speed (50 to 100 kHz sample rates)
1	1	Quad-Speed (100 to 200 kHz sample rates)

Table 7. Mode Selection, Stand-Alone Mode Options

DSD_Mode (LRCK1)	M2	M1	M0	DESCRIPTION
1	0	0	0	64x oversampled DSD data with a 4x MCLK to DSD data rate
1	0	0	1	Reserved
1	0	1	0	Reserved
1	0	1	1	Reserved
1	1	0	0	128x oversampled DSD data with a 2x MCLK to DSD data rate
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

Table 8. Direct Stream Digital (DSD), Stand-Alone Mode Options

5. APPLICATIONS

5.1 Grounding and Power Supply Decoupling

As with any high resolution converter, the CS4362 requires careful attention to power supply and grounding arrangements to optimize performance. Figures 5 & 6 show the recommended power arrangement with VA, VD, VLS and VLC connected to clean supplies. Decoupling capacitors should be located as close to the device package as possible. If desired, all supply pins may be connected to the same supply, but a decoupling capacitor should still be placed on each supply pin (see Section 1 for recommended voltages).

5.2 Oversampling Modes

The CS4362 operates in one of three oversampling modes based on the input sample rate. Mode selection is determined by the M3 and M2 pins in Stand-Alone mode or the FM bits in Control Port mode. Single-Speed mode supports input sample rates up to 50 kHz and uses a 128x oversampling ratio. Double-Speed mode supports input sample rates up to 100 kHz and uses an oversampling ratio of 64x. Quad-Speed mode supports input sample rates up to 200 kHz and uses an oversampling ratio of 32x.

5.3 Recommended Power-up Sequence

1. Hold $\overline{\text{RST}}$ low until the power supply, master, and left/right clocks are stable. In this state, the control port is reset to its default settings and VQ will remain low.

2. Bring $\overline{\text{RST}}$ high. The device will remain in a low power state with VQ low and will initiate the Stand-Alone power-up sequence. The control port will be accessible at this time. If Control Port operation is desired, write the CPEN bit prior to the completion of the Stand-Alone power-up sequence, approximately 512 LRCK cycles in Single-Speed Mode (1024 LRCK cycles in Double-Speed Mode, and 2048 LRCK cycles in Quad-Speed Mode). Writing this bit will halt the Stand-Alone power-up sequence and initialize the control port to its default settings. The desired register settings can be loaded while keeping the PDN bit set to 1.

3. If Control Port Mode is selected via the CPEN bit, set the RMP_UP and RMP_DN bits in registers 03h and 04h to 1, set the format and Mode control bits to the desired settings, and then set the PDN bit to 0 which will initiate the power-up sequence.

5.4 Analog Output and Filtering

The application note “Design Notes for a 2-Pole Filter with Differential Input” discusses the second-order Butterworth filter and differential to single-ended converter which was implemented on the CS4362 evaluation board, CDB4362, as seen in Figure 42. The CS4362 does not include phase or amplitude compensation for an external filter. Therefore, the DAC system phase and amplitude response will be dependent on the external analog circuitry.

5.5 Interpolation Filter

To accommodate the increasingly complex requirements of digital audio systems, the CS4362 incorporates selectable interpolation filters for each mode of operation. A “fast” and a “slow” roll-off filter is available in each of Single, Double, and Quad Speed modes. These filters have been designed to accommodate a variety of musical tastes and styles. The FILT_SEL bit is used to select which filter is used (see the control port section for more details).

When in stand-alone mode, only the “fast” roll-off filter is available.

Filter specifications can be found in Section 1, and filter response plots can be found in Figures 9 to 32.

5.6 Clock Source Selection

The CS4362 has two serial clock and two left/right clock inputs. The SDINxCLK bits in the control port allow the user to set which SCLK/LRCK pair is used to latch the data for each SDINx pin. The clocks applied to LRCK1 and LRCK2 must be derived from the same MCLK and must be exact frequency multiples of each other as specified in the "Switching Characteristics" table on page 8. When using both SCLK1/LRCK1 and SCLK2/LRCK2, if either SCLK/LRCK pair loses synchronization then both SCLK/LRCK pairs will go through a retime period where the device is re-evaluating clock ratios. During the retime period all DAC pairs are temporarily inactive, outputs are muted, and the mute control pins will go active according to the MUTEC bits.

If unused, SCLK2 and LRCK2 should be tied static low and SDINx bits should all be set to SCLK1/LRCK1.

In stand-alone mode all DAC pairs use SCLK1 and LRCK1 for timing and SCLK2/LRCK2 should be tied to ground.

5.7 Using DSD mode

In stand-alone mode, DSD operation is selected by holding DSD_EN(LRCK1) high and applying the DSD data and clocks to the appropriate pins. The M2:0 pins set the expected DSD rate and MCLK ratio.

In control-port mode the FM bits set the device into DSD mode (DSD_EN pin is not required to be held high). The DIF register then controls the expected DSD rate and MCLK ratio. To access the full range of DSD clocking modes (other than 64x DSD 4x MCLK and 128x DSD 2x MCLK) the following additional register sequence needs to be written:
99h to register 00h
80h to register 1Ah
00h to register 00h

When exiting DSD mode the following additional sequence needs to be written:
99h to register 00h
00h to register 1Ah
00h to register 00h

During DSD operation, the PCM related pins should either be tied low or remain active with clocks (except LRCK1 in Stand-Alone mode). When the DSD related pins are not being used they should either be tied static low, or remain active with clocks (except M3 in Stand-Alone mode).

5.8 Recommended Procedure for Switching Operational Modes

For systems where the absolute minimum in clicks and pops is required, it is recommended that the MUTE bits are set prior to changing significant DAC functions (such as changing sample rates or clock sources). The mute bits may then be released after clocks have settled and the proper CS4362 modes have been set.

It is required that the CS4362 be held in reset if the minimum high/low time specs of MCLK can not be met during clock source changes.

6. CONTROL PORT INTERFACE

The control port is used to load all the internal settings. The operation of the control port may be completely asynchronous with the audio sample rate. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

The CS4362 has MAP auto increment capability, enabled by the INCR bit in the MAP register, which is the MSB. If INCR is 0, then the MAP will stay constant for successive writes. If INCR is set to 1, then MAP will auto increment after each byte is written from register 01h to 08h and then from 09h and 11h, allowing block reads or writes of successive registers in two separate sections (the counter will not auto-increment to register 09h from register 08h).

6.1 Enabling the Control Port

On the CS4362 the control port pins are shared with stand-alone configuration pins. To enable the control port, the user must set the CPEN bit. This is done by performing a I^2C or SPI write. Once the control port is enabled, these pins are dedicated to control port functionality.

To prevent audible artifacts the CPEN bit (see Section 3.1.1) should be set prior to the completion of the Stand-Alone power-up sequence, approximately 1024 LRCK cycles. Writing this bit will halt the Stand-Alone power-up sequence and initialize the control port to its default settings. Note, the CP_EN bit can be set any time after $\overline{RST}$ goes high; however, setting this bit after the Stand-Alone power-up sequence has completed can cause audible artifacts.

6.2 Format Selection

The control port has 2 formats: SPI and I^2C, with the CS4362 operating as a slave device.

If I^2C operation is desired, AD0/$\overline{CS}$ should be tied to VLC or GND. If the CS4362 ever detects a high to low transition on AD0/$\overline{CS}$ after power-up and after the control port is activated , SPI format will be selected.

6.3 I^2C Format

In I^2C Format, SDA is a bidirectional data line. Data is clocked into and out of the part by the clock, SCL, with a clock to data relationship as shown in Figure 7. The receiving device should send an acknowledge (ACK) after each byte received. There is no $\overline{CS}$ pin. Pin AD0 forms the partial chip address and should be tied to VLC or GND as required. The upper 6 bits of the 7 bit address field must be 001100.

Note: MCLK is required during all I^2C transactions. Please see reference 4 for further details.

6.3.1 Writing in I^2C Format

To communicate with the CS4362, initiate a START condition of the bus. Next, send the chip address. The eighth bit of the address byte is the R/$\overline{W}$ bit (low for a write). The next byte is the Memory Address Pointer, MAP, which selects the register to be read or written. The MAP is then followed by the data to be written. To write multiple registers, continue providing a clock and data, waiting for the CS4362 to acknowledge between each byte. To end the transaction, send a STOP condition.

6.3.2 Reading in I^2C Format

To communicate with the CS4362, initiate a START condition of the bus. Next, send the chip address. The eighth bit of the address byte is the R/$\overline{W}$ bit (high for a read). The contents of the register pointed to by the MAP will be output after the chip address. To read multiple registers, continue providing a clock and issue an ACK after each byte. To end the transaction, send a STOP condition.

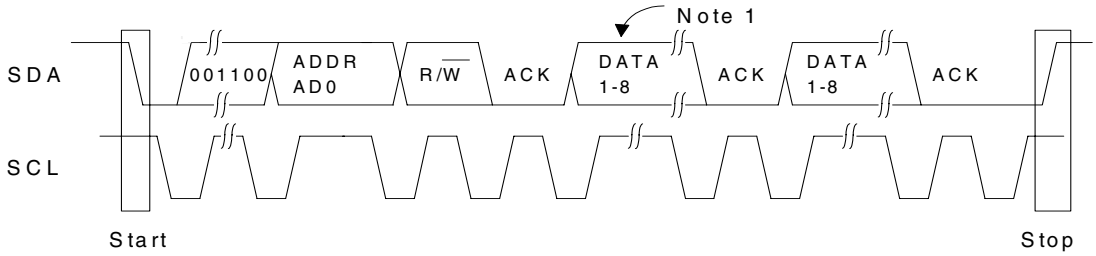
6.4 SPI Format

In SPI format, $\overline{CS}$ is the CS4362 chip select signal, CCLK is the control port bit clock, CDIN is the input data line from the microcontroller and the chip address is 0011000. $\overline{CS}$, CCLK and CDIN are all inputs and data is clocked in on the rising edge of CCLK.

Note that the CS4362 is write-only when in SPI format.

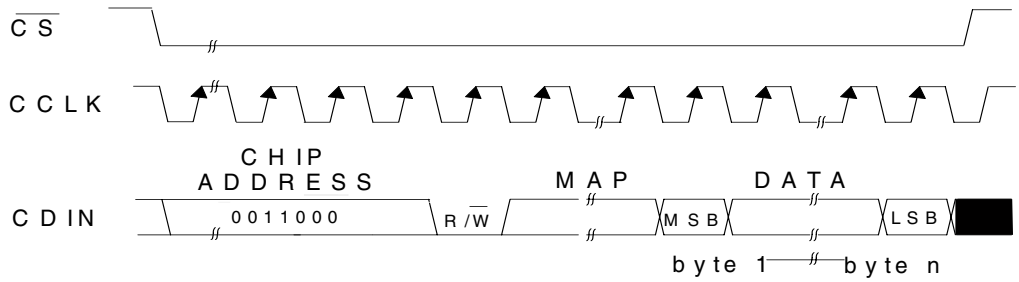
6.4.1 Writing in SPI

Figure 8 shows the operation of the control port in SPI format. To write to a register, bring $\overline{CS}$ low. The first 7 bits on CDIN form the chip address and must be 0011000. The eighth bit is a read/write indicator (R/$\overline{W}$), which must be low to write. The next 8 bits form the Memory Address Pointer (MAP), which is set to the address of the register that is to be updated. The next 8 bits are the data which will be placed into register designated by the MAP. To write multiple registers, keep $\overline{CS}$ low and continue providing clocks on CCLK. End the read transaction by setting $\overline{CS}$ high.



Note: If operation is a write, this byte contains the Memory Address Pointer, MAP.

Figure 7. Control Port Timing, I²C Format



MAP = Memory Address Pointer

Figure 8. Control Port Timing, SPI Format

6.5 Memory Address Pointer (MAP)

7	6	5	4	3	2	1	0
INCR	Reserved	Reserved	MAP4	MAP3	MAP2	MAP1	MAP0
0	0	0	0	0	0	0	0

6.5.1 INCR (AUTO MAP INCREMENT ENABLE)

Default = '0'
0 - Disabled
1 - Enabled

Note: When Auto Map Increment is enabled, the register must be written it two separate blocks: from register 01h to 08h and then from 09h and 11h. The counter will not auto-increment to register 09h from register 08h

6.5.2 MAP4-0 (MEMORY ADDRESS POINTER)

Default = '00000'

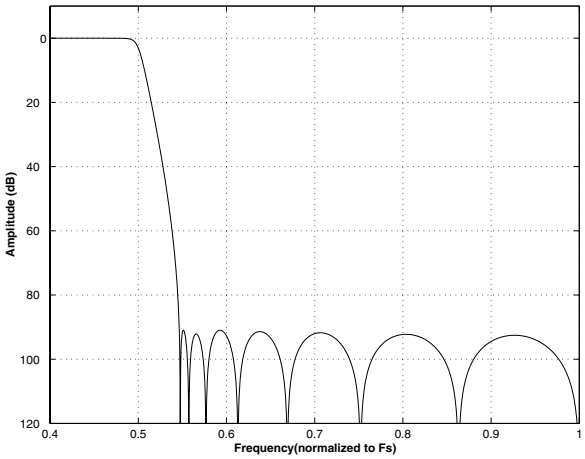


Figure 9. Single Speed (fast) Stopband Rejection

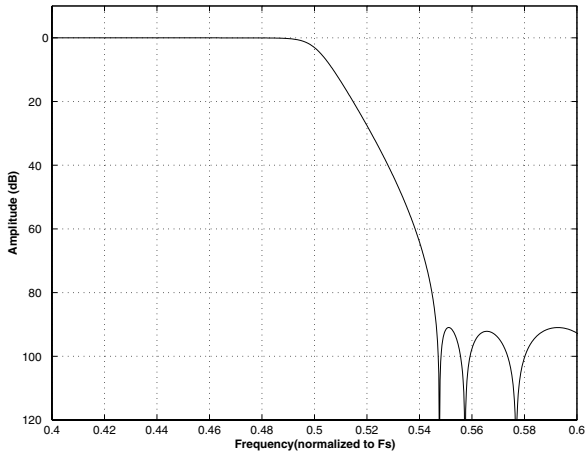


Figure 10. Single Speed (fast) Transition Band

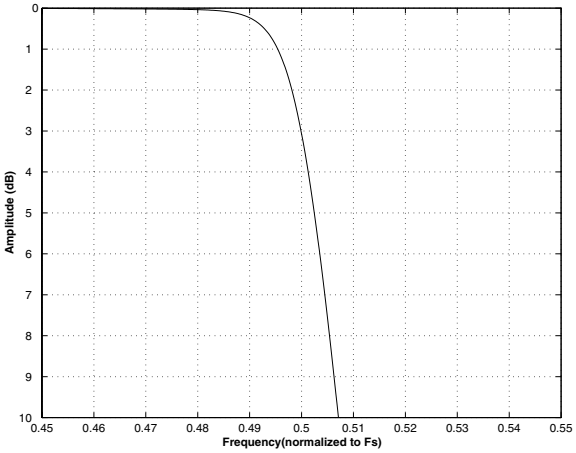


Figure 11. Single Speed (fast) Transition Band (detail)

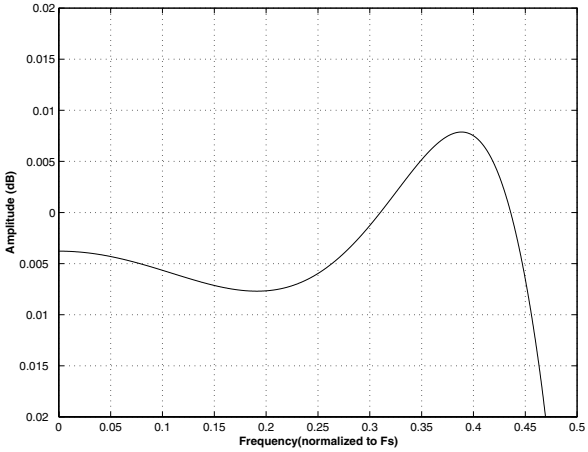


Figure 12. Single Speed (fast) Passband Ripple

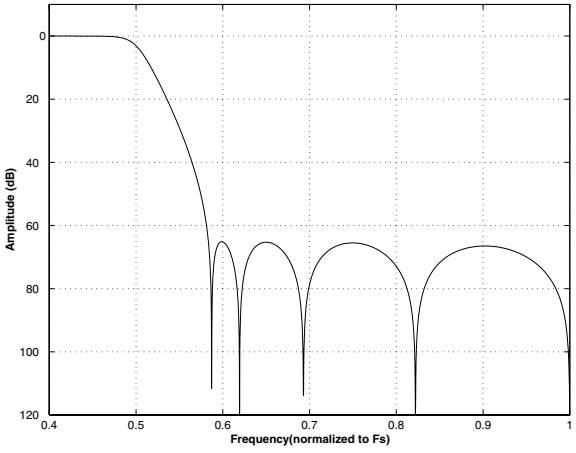


Figure 13. Single Speed (slow) Stopband Rejection

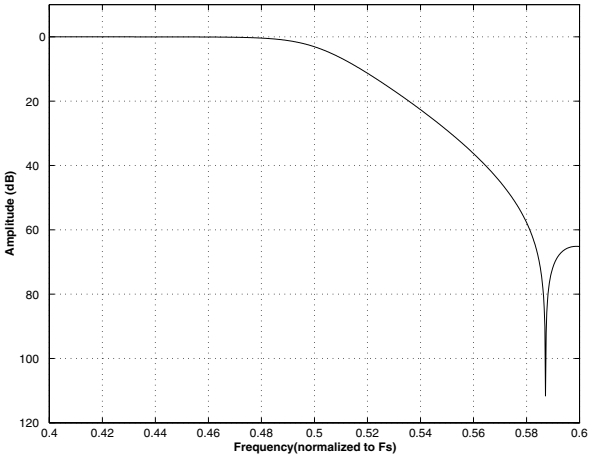


Figure 14. Single Speed (slow) Transition Band

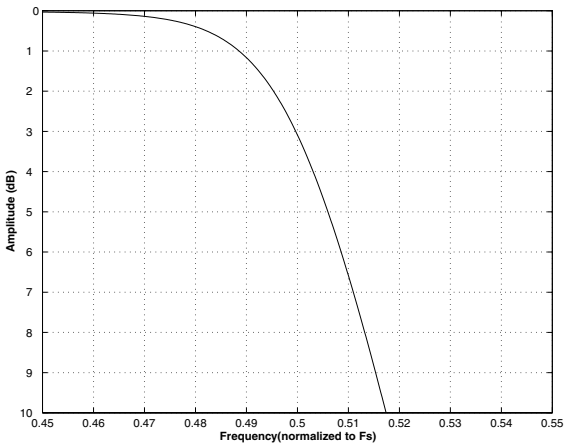


Figure 15. Single Speed (slow) Transition Band (detail)

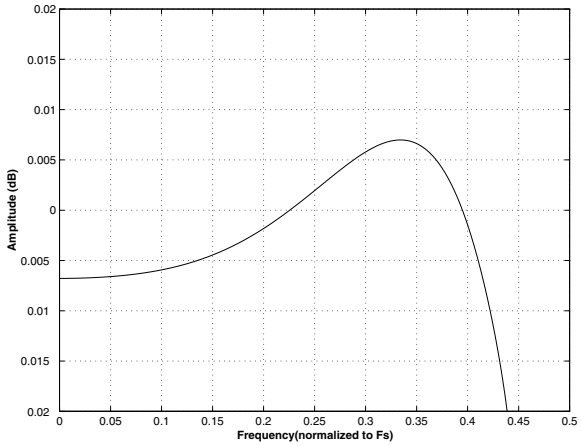


Figure 16. Single Speed (slow) Passband Ripple

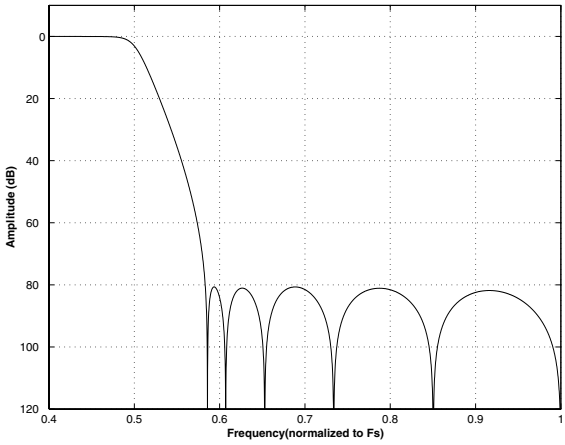


Figure 17. Double Speed (fast) Stopband Rejection

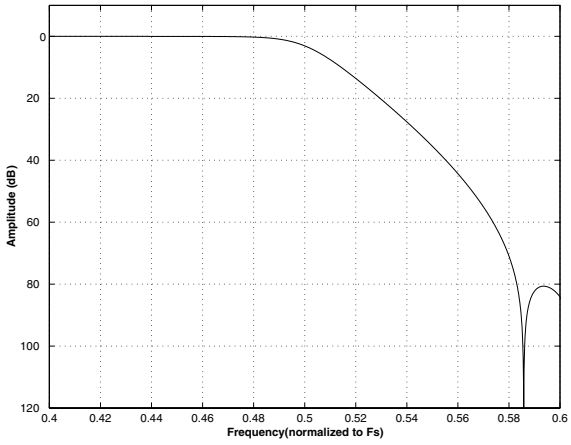


Figure 18. Double Speed (fast) Transition Band

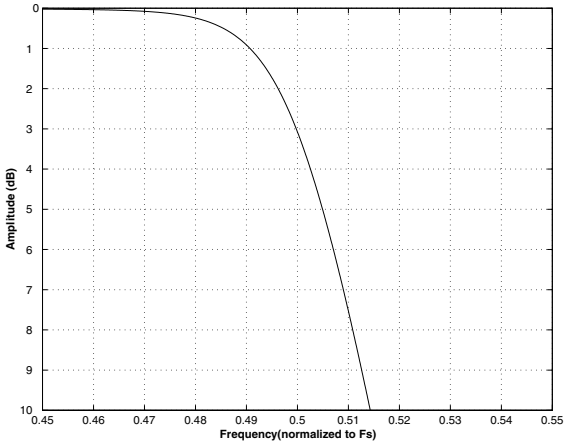


Figure 19. Double Speed (fast) Transition Band (detail)

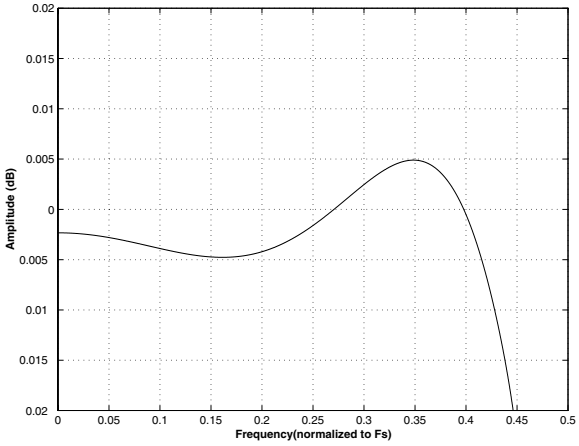


Figure 20. Double Speed (fast) Passband Ripple

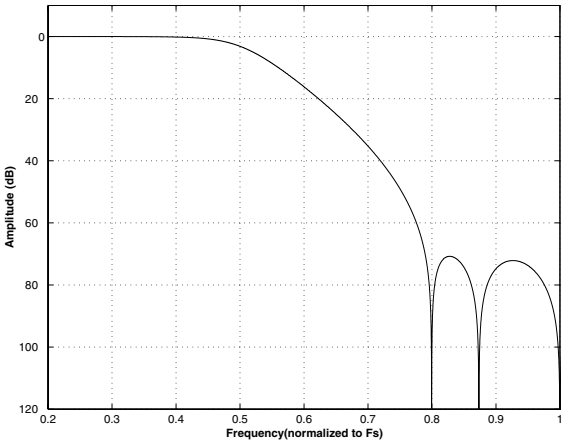


Figure 21. Double Speed (slow) Stopband Rejection

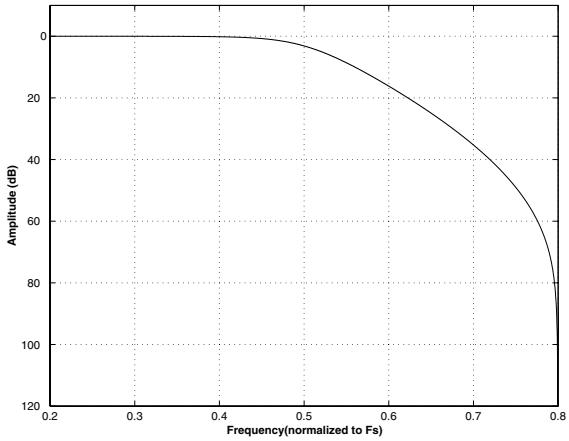


Figure 22. Double Speed (slow) Transition Band

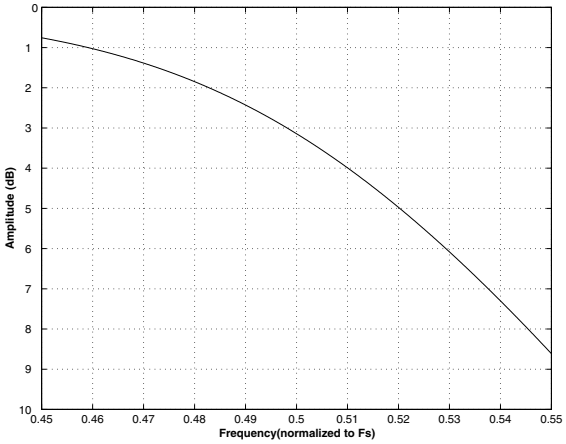


Figure 23. Double Speed (slow) Transition Band (detail)

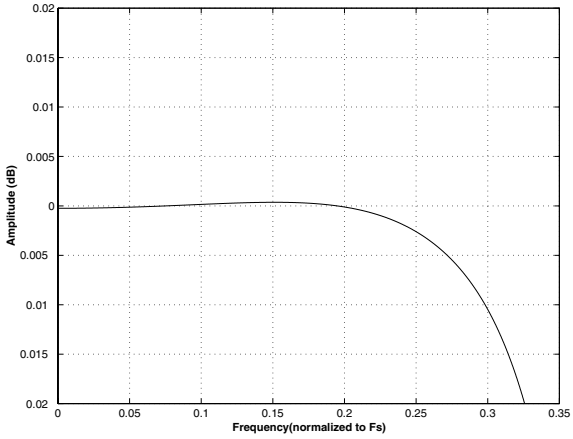


Figure 24. Double Speed (slow) Passband Ripple

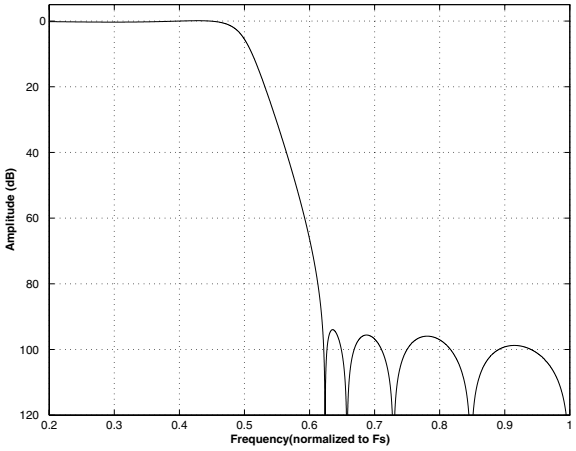


Figure 25. Quad Speed (fast) Stopband Rejection

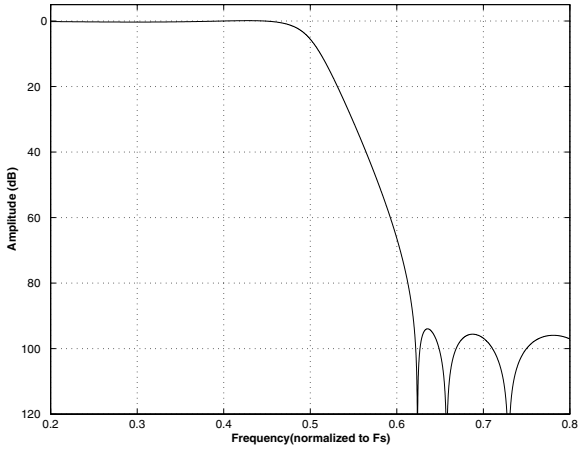


Figure 26. Quad Speed (fast) Transition Band

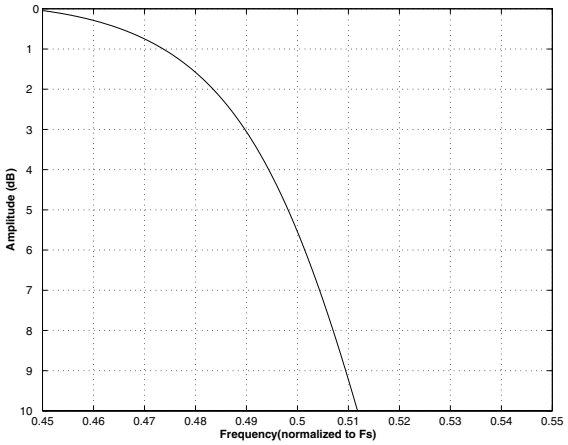


Figure 27. Quad Speed (fast) Transition Band (detail)

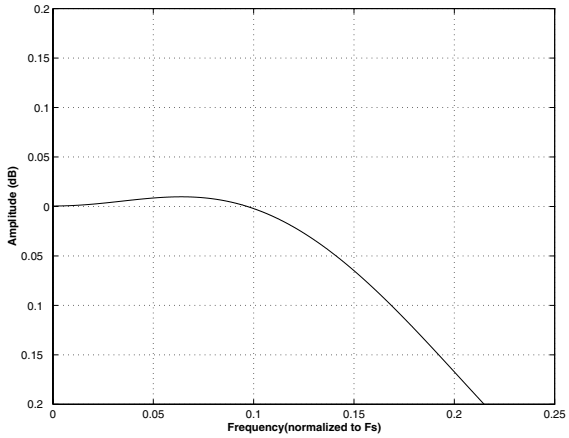


Figure 28. Quad Speed (fast) Passband Ripple

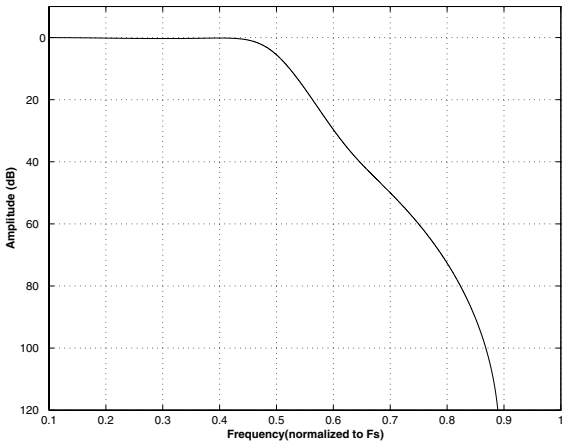


Figure 29. Quad Speed (slow) Stopband Rejection

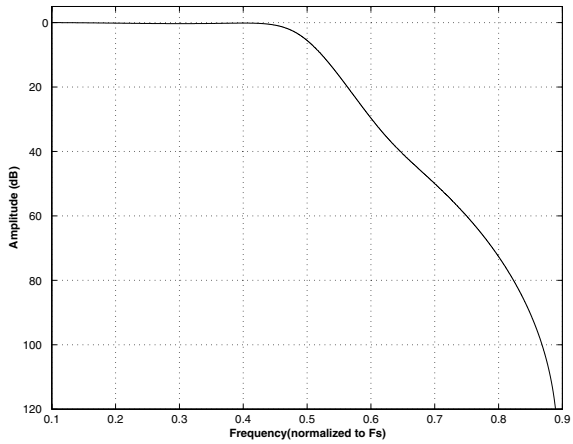


Figure 30. Quad Speed (slow) Transition Band

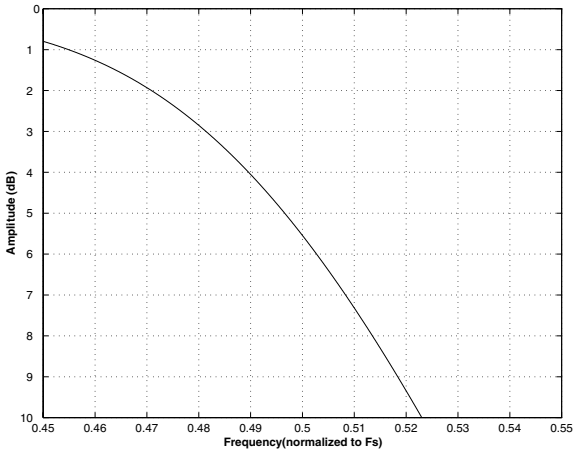


Figure 31. Quad Speed (slow) Transition Band (detail)

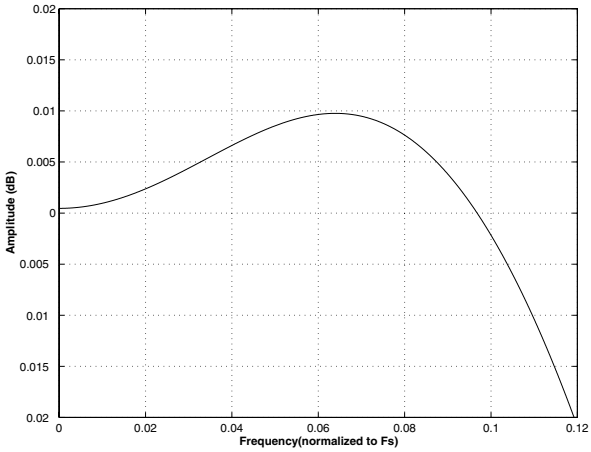


Figure 32. Quad Speed (slow) Passband Ripple

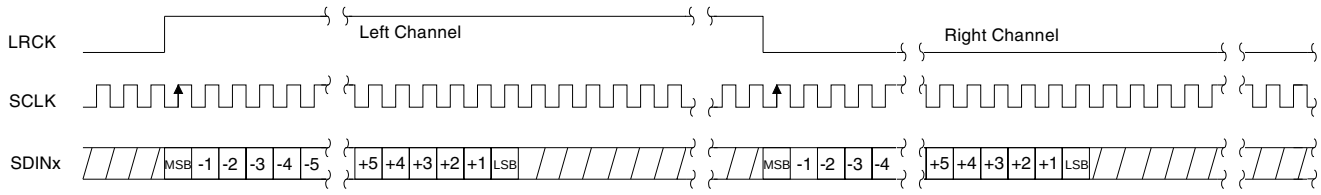


Figure 33. Format 0 - Left Justified up to 24-bit Data

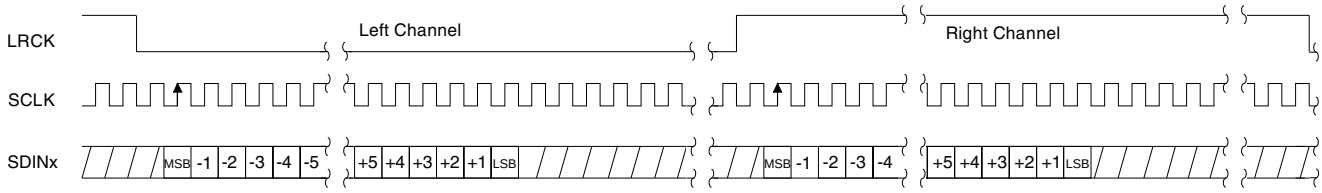


Figure 34. Format 1 - I^2S up to 24-bit Data

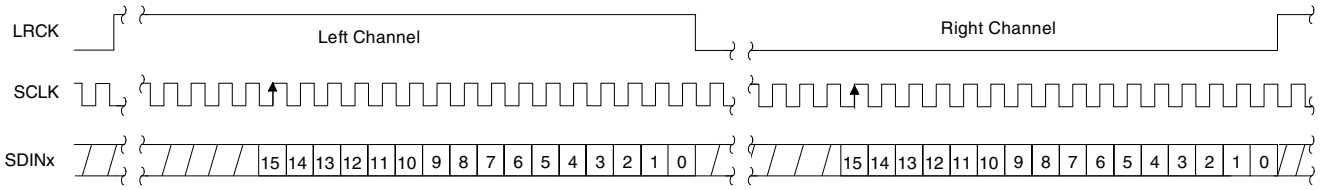


Figure 35. Format 2 - Right Justified 16-bit Data

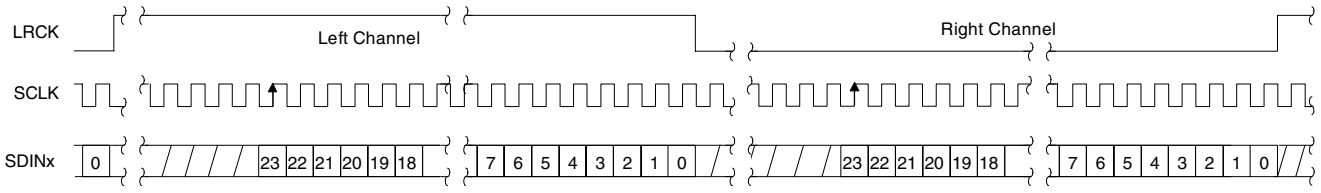


Figure 36. Format 3 - Right Justified 24-bit Data

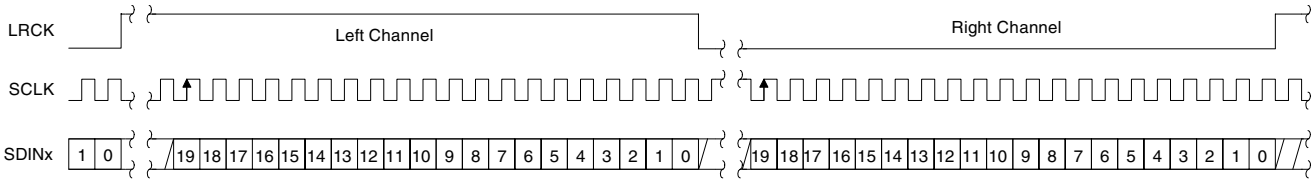


Figure 37. Format 4 - Right Justified 20-bit Data

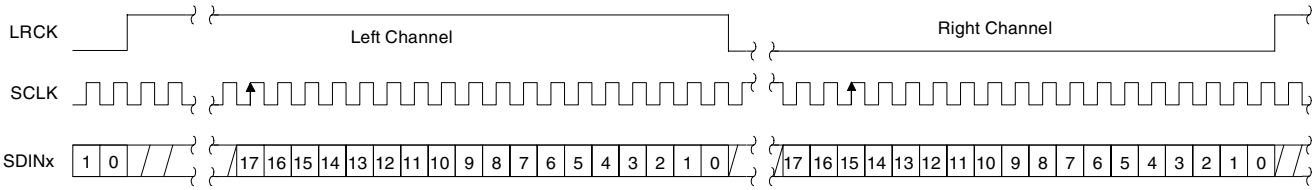


Figure 38. Format 5 - Right Justified 18-bit Data

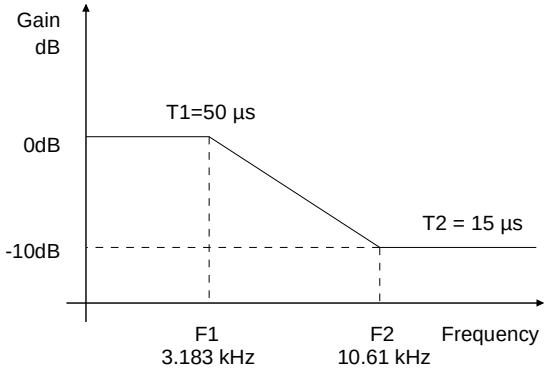


Figure 39. De-Emphasis Curve

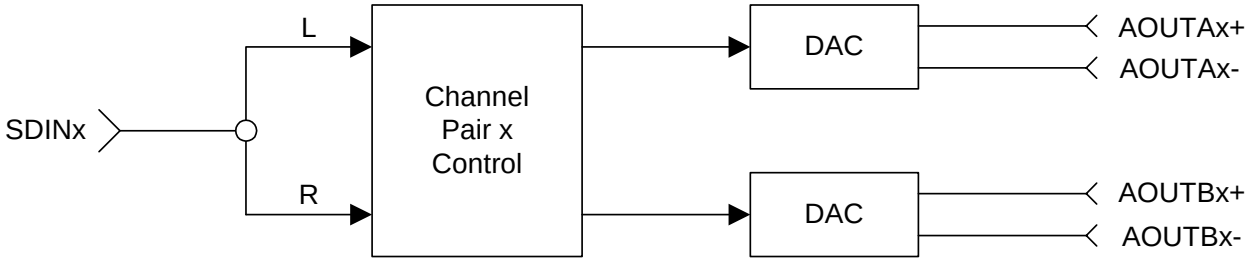


Figure 40. Channel Pair Routing Diagram (x = Channel Pair 1, 2, or

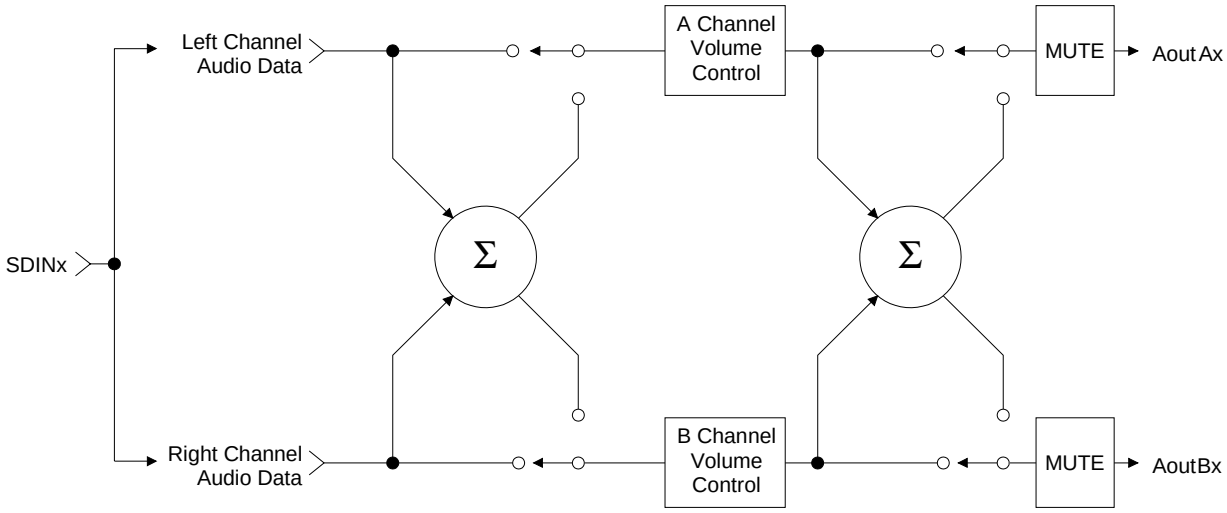


Figure 41. ATAPI Block Diagram (x = channel pair 1, 2, or 3)

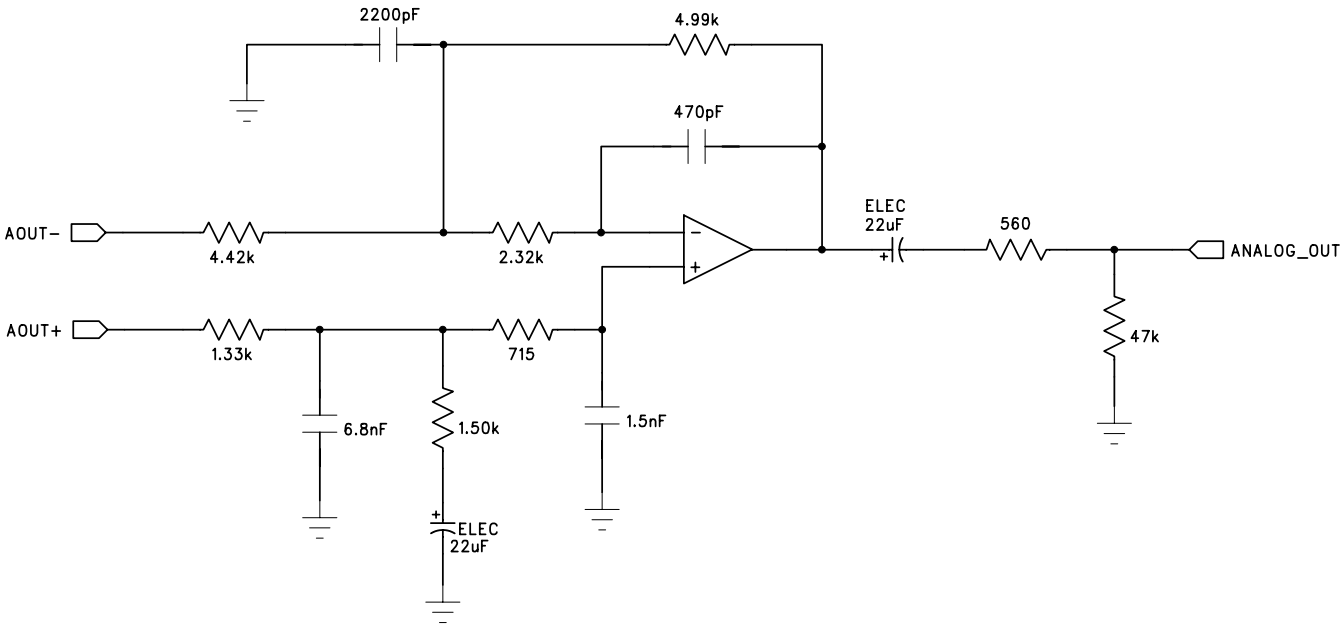


Figure 42. Recommended Output Filter

7. PARAMETER DEFINITIONS

Total Harmonic Distortion + Noise (THD+N)

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels.

Dynamic Range

The ratio of the full scale rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic range is a signal-to-noise measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is then added to the resulting measurement to refer the measurement to full scale. This technique ensures that the distortion components are below the noise level and do not effect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with all zeros to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Gain Error

The deviation from the nominal full scale analog output for a full scale digital input.

Gain Drift

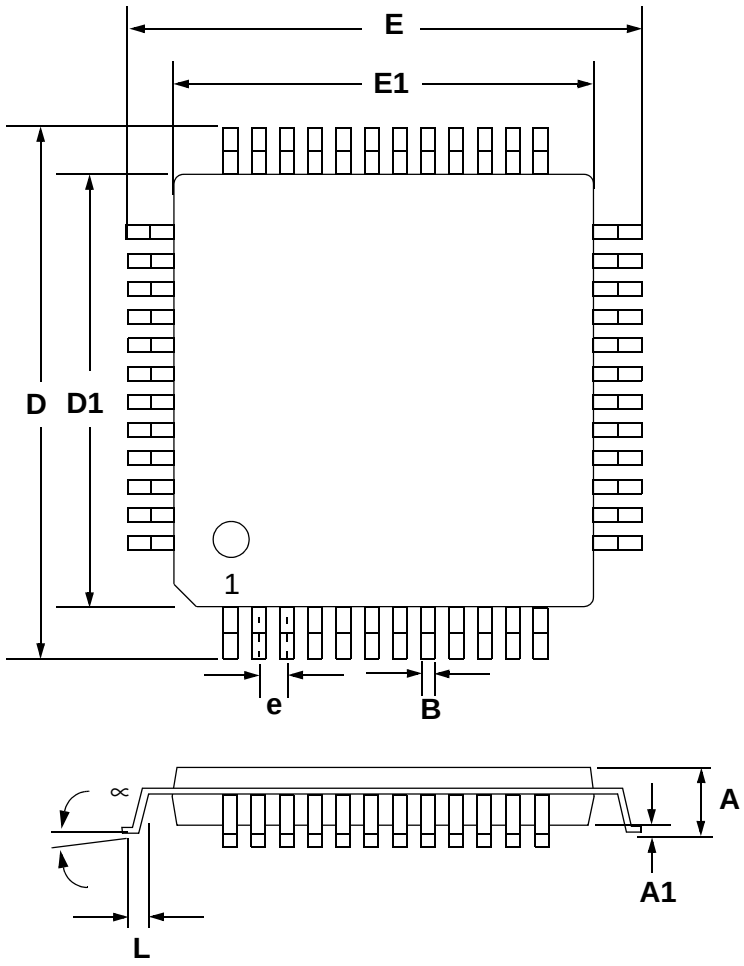
The change in gain value with temperature. Units in ppm/°C.

8. REFERENCES

1. "How to Achieve Optimum Performance from Delta-Sigma A/D & D/A Converters" by Steven Harris. Paper presented at the 93rd Convention of the Audio Engineering Society, October 1992.
2. CDB4362 Evaluation Board Datasheet
3. “Design Notes for a 2-Pole Filter with Differential Input” by Steven Green. Cirrus Logic Application Note AN48
4. “The I^2C-Bus Specification: Version 2.0” Philips Semiconductors, December 1998. http://www.semiconductors.philips.com

9. PACKAGE DIMENSIONS

48L LQFP PACKAGE DRAWING



	INCHES			MILLIMETERS		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	---	0.055	0.063	---	1.40	1.60
A1	0.002	0.004	0.006	0.05	0.10	0.15
B	0.007	0.009	0.011	0.17	0.22	0.27
D	0.343	0.354	0.366	8.70	9.0 BSC	9.30
D1	0.272	0.28	0.280	6.90	7.0 BSC	7.10
E	0.343	0.354	0.366	8.70	9.0 BSC	9.30
E1	0.272	0.28	0.280	6.90	7.0 BSC	7.10
e*	0.016	0.020	0.024	0.40	0.50 BSC	0.60
L	0.018	0.24	0.030	0.45	0.60	0.75
∝	0.000°	4°	7.000°	0.00°	4°	7.00°

* Nominal pin pitch is 0.50 mm

Controlling dimension is mm.
JEDEC Designation: MS022

Table 9. Revision History

Release	Date	Changes
F1	NOV 2004	Removed -BQ ordering option Corrected specifications for Full Scale Differential Output Voltage Updated legal text Incorporated changes outlined in ER257B3 and ER257F1: -corrected pin order for analog outputs in the pin description -corrected mute pin decode in section 3.3.6 -updated description for section 3.6.3 -updated description for 3) in section 5.3 -added section 5.8 -updated Table 2 on page 16 -updated Section 5.7 Using DSD mode

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.

To find the one nearest to you go to www.cirrus.com