# 128K X 36 Dual I/O Dual Address Synchronous SRAM

## Features

- **Fast clock speed: 100 and 83 MHz**
- **Fast access times: 5.0/6.0 ns max.**
- **Single clock operation**
- **Single 3.3V –5% and +5% power supply V$_{CC}$**
- **Separate V$_{CCQ}$ for output buffer**
- **Two chip enables for simple depth expansion**
- **Address, data input, CE1X, CE2X, CE1Y, CE2Y, PTX, PTY, WEX, WEY, and data output registers on-chip**
- **Concurrent Reads and Writes**
- **Two bidirectional data buses**
- **Can be configured as separate I/O**
- **Pass-through feature**
- **Asynchronous output enables (OEX, OEY)**
- **LVTTL-compatible I/O**
- **Self-timed Write**
- **Automatic power-down**
- **176-pin TQFP package**

## Functional Description

The CY7C1300A SRAM integrates 131,072 × 36 SRAM cells with advanced synchronous peripheral circuitry. It employs high-speed, low-power CMOS designs using advanced triple-layer polysilicon, double-layer metal technology. Each memory cell consists of four transistors and two high-valued resistors.

The CY7C1300A allows the user to concurrently perform Reads, Writes, or pass-through cycles in combination on the two data ports. The two address ports (AX, AY) determine the Read or Write locations for their respective data ports (DQX, DQY).

All input pins except output enable pins (OEX, OEY) are gated by registers controlled by a positive-edge-triggered clock (CLK) input. The synchronous inputs include all addresses, data inputs, depth-expansion chip enables (CE1X, CE2X, CE1Y and CE2Y), pass-through controls (PTX and PTY), and Read–Write control (WEX and WEY).
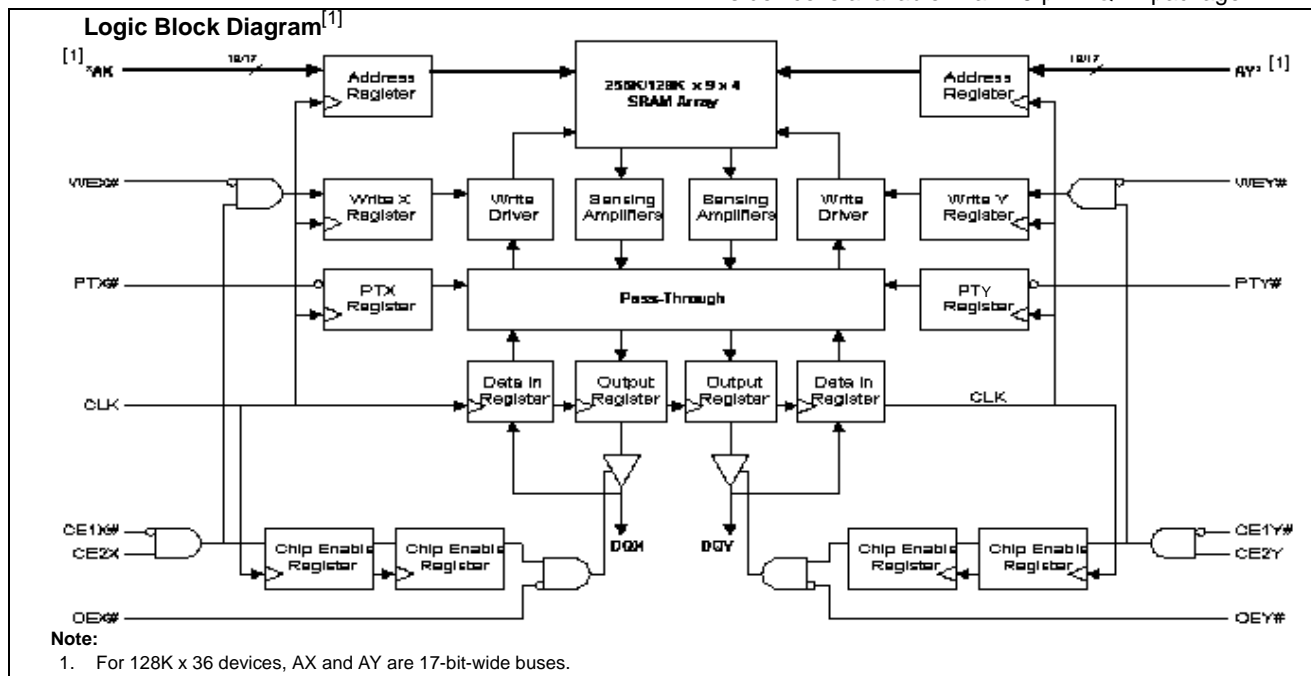
The pass-through feature allows data to be passed from one port to another, in either direction. The PTX input must be asserted to pass data from port X to port Y. The PTY will likewise pass data from port Y to port X. A pass-through operation takes precedence over a Read operation.

When AX and AY are the same, certain protocols are followed. If both ports are Read, the reads occur normally. If one port is written and the other is read, the read from the array will occur before the data is written. If both ports are written, only the data on DQY will be written to the array.

The CY7C1300A operates from a +3.3V power supply. All inputs and outputs are LVTTL-compatible. These dual I/O, dual address synchronous SRAMs are well suited for ATM, Ethernet switches, routers, cell/frame buffers, SNA switches, and shared memory applications.

The CY7C1300A needs one extra cycle after power for proper power-on reset. The extra cycle is needed after V$_{CC}$ is stable on the device.

This device is available in a 176-pin TQFP package.

**Logic Block Diagram**[1]



**Note:**
1. For 128K x 36 devices, AX and AY are 17-bit-wide buses.

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Document #: 38-05075 Rev. *C
Revised January 19, 2003

## Selection Guide

|  | -100 | -83 | Unit |
|---|---|---|---|
| Maximum access time | 5.0 | 6.0 | ns |
| Maximum operating current | 500 | 430 | mA |
| Maximum CMOS standby current | 100 | 100 | mA |

Shaded areas contain advance information.

## Pin Configuration

**176-pin TQFP**

Top side (pins 176–133, left to right):
176 VSS, 175 DQY19, 174 DQX19, 173 VSS, 172 VCCQ, 171 DQY18, 170 DQX18, 169 AX6, 168 AY6, 167 AX7, 166 AY7, 165 VSS, 164 NC, 163 NC, 162 NC, 161 VSS, 160 NC, 159 NC, 158 CE2Y, 157 CE1Y#, 156 CLK, 155 VCC, 154 VSS, 153 OEY#, 152 OEX#, 151 CE2X, 150 CE1X#, 149 WEY#, 148 WEX#, 147 PTY#, 146 PTX#, 145 AX8, 144 AY8, 143 AX9, 142 AY9, 141 AX17*, 140 AY17*, 139 DQX17, 138 DQY17, 137 VCC, 136 VSS, 135 DQX16, 134 DQY16, 133 VSS

Left side (pins 1–44):
1 VSS, 2 DQX20, 3 DQY20, 4 VCCQ, 5 VSS, 6 DQX21, 7 DQY21, 8 DQX22, 9 DQY22, 10 VCCQ, 11 VSS, 12 DQX23, 13 DQY23, 14 DQX24, 15 DQY24, 16 VCCQ, 17 VSS, 18 DQX25, 19 DQY25, 20 DQX26, 21 DQY26, 22 VCC, 23 VSS, 24 DQY27, 25 DQX27, 26 DQY28, 27 DQX28, 28 VCCQ, 29 VSS, 30 DQY29, 31 DQX29, 32 DQY30, 33 DQX30, 34 VCCQ, 35 VSS, 36 DQY31, 37 DQX31, 38 DQY32, 39 DQX32, 40 VCCQ, 41 VSS, 42 DQY33, 43 DQX33, 44 VSS

Right side (pins 132–89):
132 VSS, 131 DQX15, 130 DQY15, 129 VSS, 128 VCCQ, 127 DQX14, 126 DQY14, 125 DQX13, 124 DQY13, 123 VSS, 122 VCCQ, 121 DQX12, 120 DQY12, 119 DQX11, 118 DQY11, 117 VSS, 116 VCCQ, 115 DQX10, 114 DQY10, 113 DQX9, 112 DQY9, 111 VSS, 110 VCC, 109 DQY8, 108 DQX8, 107 DQY7, 106 DQX7, 105 VSS, 104 VCCQ, 103 DQY6, 102 DQX6, 101 DQY5, 100 DQX5, 99 VSS, 98 VCCQ, 97 DQY4, 96 DQX4, 95 DQY3, 94 DQX3, 93 VSS, 92 VCCQ, 91 DQY2, 90 DQX2, 89 VSS

Bottom side (pins 45–88, left to right):
45 VSS, 46 DQY34, 47 DQX34, 48 VSS, 49 VCCQ, 50 DQY35, 51 DQX35, 52 VSS, 53 VSS, 54 AY5, 55 AX5, 56 AY4, 57 AX4, 58 AY3, 59 AX3, 60 AY2, 61 AX2, 62 AY1, 63 AX1, 64 AY0, 65 AX0, 66 VCC, 67 VSS, 68 AX10, 69 AY10, 70 AX11, 71 AY11, 72 AX12, 73 AY12, 74 AX13, 75 AY13, 76 AX14, 77 AY14, 78 AX15, 79 AY15, 80 AX16, 81 AY16, 82 DQX0, 83 DQY0, 84 VCCQ, 85 VSS, 86 DQX1, 87 DQY1, 88 VSS

## Pin Definitions

| Name | I/O | Description |
|---|---|---|
| AX0–AX16 | Input–Synchronous | **Synchronous Address Inputs of Port X**: Do not allow address pins to float. |
| AY0–AY16 | Input–Synchronous | **Synchronous Address Inputs of Port Y**: Do not allow address pins to float. |
| WEX | Input–Synchronous | **Read Write of Port X**: WEX signal is a synchronous input that identifies whether the current loaded cycle is a Read or Write operation. |
| WEY | Input–Synchronous | **Read Write of Port Y**: WEY signal is a synchronous input that identifies whether the current loaded cycle is a Read or Write operation. |
| PTX | Input–Synchronous | **Pass-Through of Port X**: PTX signal is a synchronous input that enables passing Port X input to Port Y output. |
| PTY | Input–Synchronous | **Pass-Through of Port Y**: PTY signal is a synchronous input that enables passing Port Y input to Port X output. |
| OEX | Input | **Asynchronous Output Enable of Port X**: OEX must be LOW to read data. When OEX is HIGH, the DQXx pins are in high-impedance state. |
| OEY | Input | **Asynchronous Output Enable of Port Y**: OEY must be LOW to read data. When OEY is HIGH, the DQYx pins are in high-impedance state. |
| DQX0–DQX35 | Input/Output | **Data Inputs/Outputs of Port X**: Both the data input path and data output path are registered and triggered by the rising edge of CLK. |
| DQY0–DQY35 | Input/Output | **Data Inputs/Outputs of Port Y**: Both the data input path and data output path are registered and triggered by the rising edge of CLK. |
| CLK | Input–Synchronous | **Clock**: This is the clock input to this device. Except for OEX and OEY, all timing references of the address, data in, and all control signals for the device are made with respect to the rising edge of CLK. |
| CE1X | Input–Synchronous | **Synchronous Active LOW Chip Enable Port X**: CE1X is used with CE2X to enable Port X of this device. CE1X sampled HIGH at the rising edge of clock initiates a deselect cycle for Port X. |
| CE2X | Input–Synchronous | **Synchronous Active HIGH Chip Enable Port X**: CE2X is used with CE1X to enable Port X of this device. CE2X sampled LOW at the rising edge of clock initiates a deselect cycle for Port X. |
| CE1Y | Input–Synchronous | **Synchronous Active LOW Chip Enable Port Y**: CE1Y is used with CE2Y to enable Port Y of this device. CE1Y sampled HIGH at the rising edge of clock initiates a deselect cycle for Port Y. |
| CE2Y | Input–Synchronous | **Synchronous Active HIGH Chip Enable Port Y**: CE2Y is used with CE1Y to enable Port Y of this device. CE2Y sampled LOW at the rising edge of clock initiates a deselect cycle for Port Y. |
| $V_{CC}$ | Supply | **Power Supply**: +3.3V –5% and +5%. |
| $V_{SS}$ | Ground | **Ground**: GND. |
| $V_{SS}$ | Ground | **Ground**: GND. No chip current flows through these pins. However, the user needs to connect GND to these pins. |
| $V_{CCQ}$ | I/O Supply | **Output Buffer Supply**: +3.3V -5% and +5%. |
| NC | – | **No Connect**: These signals are not internally connected. The user can connect them to $V_{CC}$, $V_{SS}$, or any signal lines, or simply leave them floating. |

## Cycle Description Truth Table [2, 3, 4, 5, 6, 7, 8, 9]

| Operation | CE1X | CE2X | CE1Y | CE2Y | WEX | WEY | PTX | PTY |
|---|---|---|---|---|---|---|---|---|
| Deselect Cycle | H | X | H | X | X | X | X | X |
| Deselect Cycle | X | L | X | L | X | X | X | X |
| Write Port X | L | H | X | X | 0 | X | X | X |

**Notes:**
2. X means "Don't Care." H means logic HIGH. L means logic LOW.
3. All inputs except OEX and OEY must meet set-up and hold times around the rising edge (LOW to HIGH) of CLK.
4. OEX and OEY must be asserted to avoid bus contention during Write and Pass-through cycles. For Write and Pass-through operations following a Read operation, OEX/OEY must be HIGH before the input data required set-up time plus High-Z time for OEX/OEY and staying HIGH throughout the input data hold time.
5. Operation numbers 3–6 can be used in any combination.
6. Operation numbers 4 and 7, 3 and 8, and 7 and 8 can be combined.
7. Operation numbers 5 can not be combined with operation number 7 or 8 because Pass-through operation has higher priority over a Read operation.
8. Operation number 6 can not be combined with operation number 7 or 8 because Pass-through operation has higher priority over a Read operation.
9. This device contains circuitry that will ensure the outputs will be in High-Z during power-up

## Cycle Description Truth Table (continued)[2, 3, 4, 5, 6, 7, 8, 9]

| Operation | CE1X | CE2X | CE1Y | CE2Y | WEX | WEY | PTX | PTY |
|---|---|---|---|---|---|---|---|---|
| Write Port Y | X | X | L | H | X | 0 | X | X |
| Pass-through from X to Y | L | H | L | H | X | X | 0 | X |
| Pass-through from Y to X | L | H | L | H | X | X | X | 0 |
| Read Port X | L | H | X | X | 1 | X | 1 | 1 |
| Read Port Y | X | X | L | H | X | 1 | 1 | 1 |

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..................................... –55°C to +125°C

Ambient Temperature with
Power Applied.................................................. –10°C to +85°C

Supply Voltage on $V_{DD}$ Relative to GND.........–0.5V to +4.6V

DC Voltage Applied to Outputs
in High-Z State[10] ..................................–0.5V to $V_{CCQ}$ + 0.5V

DC Input Voltage[10] ...............................–0.5V to $V_{CCQ}$ + 0.5V

Current into Outputs (LOW) ........................................ 20 mA

Static Discharge Voltage .......................................... > 1601V
(per MIL-STD-883, Method 3015)

Latch-up Current .................................................. > 200 mA

## Operating Range

| Range | Ambient Temperature[11] | $V_{DD}/V_{DDQ}$[12] |
|---|---|---|
| Commercial | 0°C to +70°C | 3.3V ± 5% |

## Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Power Supply Voltage | | | 3.135 | 3.465 | V |
| $V_{DDQ}$ | I/O Supply Voltage | | | 3.135 | 3.465 | V |
| $V_{OH}$ | Output HIGH Voltage | $V_{DD}$ = Min., $I_{OH}$ = –4.0 mA | | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $V_{DD}$ = Min., $I_{OL}$ = 8.0 mA | | | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage[13] | | | 2.0 | $V_{CC}$ + 0.5V | V |
| $V_{IL}$ | Input LOW Voltage[14] | | | –0.5 | 0.8 | V |
| $I_X$ | Input Load Current | GND ≤ $V_{IN}$ ≤ $V_{DDQ}$ | | –5 | 5 | µA |
| $I_{OZ}$ | Output Leakage Current | GND ≤ $V_{IN}$ ≤ $V_{DDQ}$, Output Disabled | | –5 | 5 | µA |
| $I_{CC}$ | $V_{DD}$ Operating Supply | $V_{DD}$ = Max., $I_{OUT}$ = 0 mA, f = $f_{MAX}$ = 1/$t_{CYC}$ | 10.0 ns cycle, MHz | | 500 | mA |
| | | | 12.0 ns cycle, 83 MHz | | 430 | mA |
| $I_{SB}$ | Automatic CE Power-down Current—CMOS Inputs | Max. $V_{DD}$, Device Deselected[15], $V_{IN}$ ≤ 0.3V or $V_{IN}$ ≥ $V_{DDQ}$ – 0.3V, f = 0 | 10.0 ns cycle, 100 MHz | | 140 | mA |
| | | | 12.0 ns cycle, 83 MHz | | 120 | mA |

## Capacitance[16]

| Parameter | Description | Test Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $T_A$ = 25°C, f = 1 MHz, $V_{CC}$ = 3.3V, $V_{CCQ}$ = 3.3V | 8 | pF |
| $C_{CLK}$ | Clock input capacitance | | 9 | pF |

**Notes:**
10. Minimum voltage equals –2.0V for pulse duration less than 20 ns.
11. $T_A$ is the case temperature.
12. Power supply ramp up should be monotonic.
13. Overshoot: $V_{IH}$ ≤ +6.0V for t ≤ $t_{KC/2}$.
14. Undershoot: $V_{IL}$ ≤ –2.0V for t ≤ $t_{KC/2}$.
15. "Device Deselected" means the device is in power-down mode as defined in the truth table.
16. Tested initially and after any design or process change that may affect these parameters.

## AC Test Loads and Waveforms[17, 18]



(a)                                    (b)                                    (c)
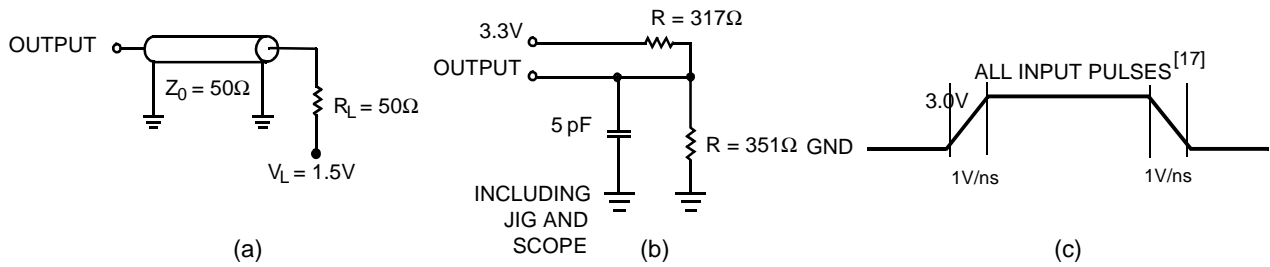
## Thermal Resistance

| Parameter | Description | Test Conditions | TQFP Typ. | Units | Notes |
|-----------|-------------|-----------------|-----------|-------|-------|
| $\Theta_{JA}$ | Thermal Resistance (Junction to Ambient) | (@200lfm) Single-layer printed circuit board | 40 | °C/W | 15 |
| $\Theta_{JC}$ | Thermal Resistance (Junction to Ambient) | (@200lfm) Four-layer printed circuit board | 35 | °C/W | 15 |
| $\Theta_{JA}$ | Thermal Resistance (Junction to Board) | Bottom | 23 | °C/W | 15 |
| $\Theta_{JC}$ | Thermal Resistance (Junction to Case) | Top | 9 | °C/W | 15 |

**Notes:**
17. AC test conditions assume a signal transition time of 1 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading shown in part (a) of AC Test Loads.
18. Overshoot: VIH(AC) <VDD + 1.5V for t <tTCYC/2; undershoot: VIL(AC) < 0.5V for t <tTCYC/2; power-up: VIH < 2.6V and VDD <2.4V and VDDQ < 1.4V for t<200 ms.

## Switching Characteristics Over the Operating Range[17, 19, 20]

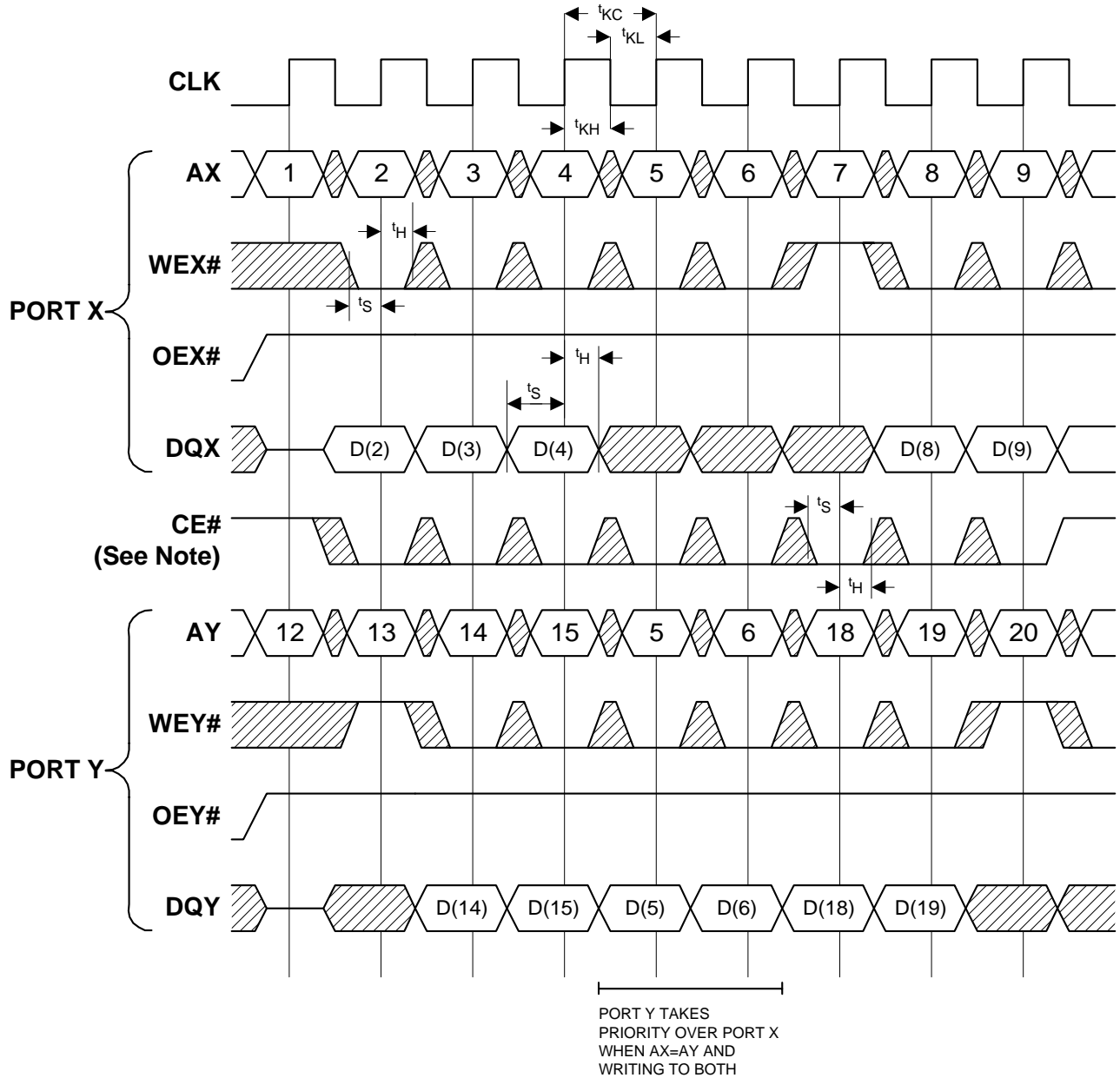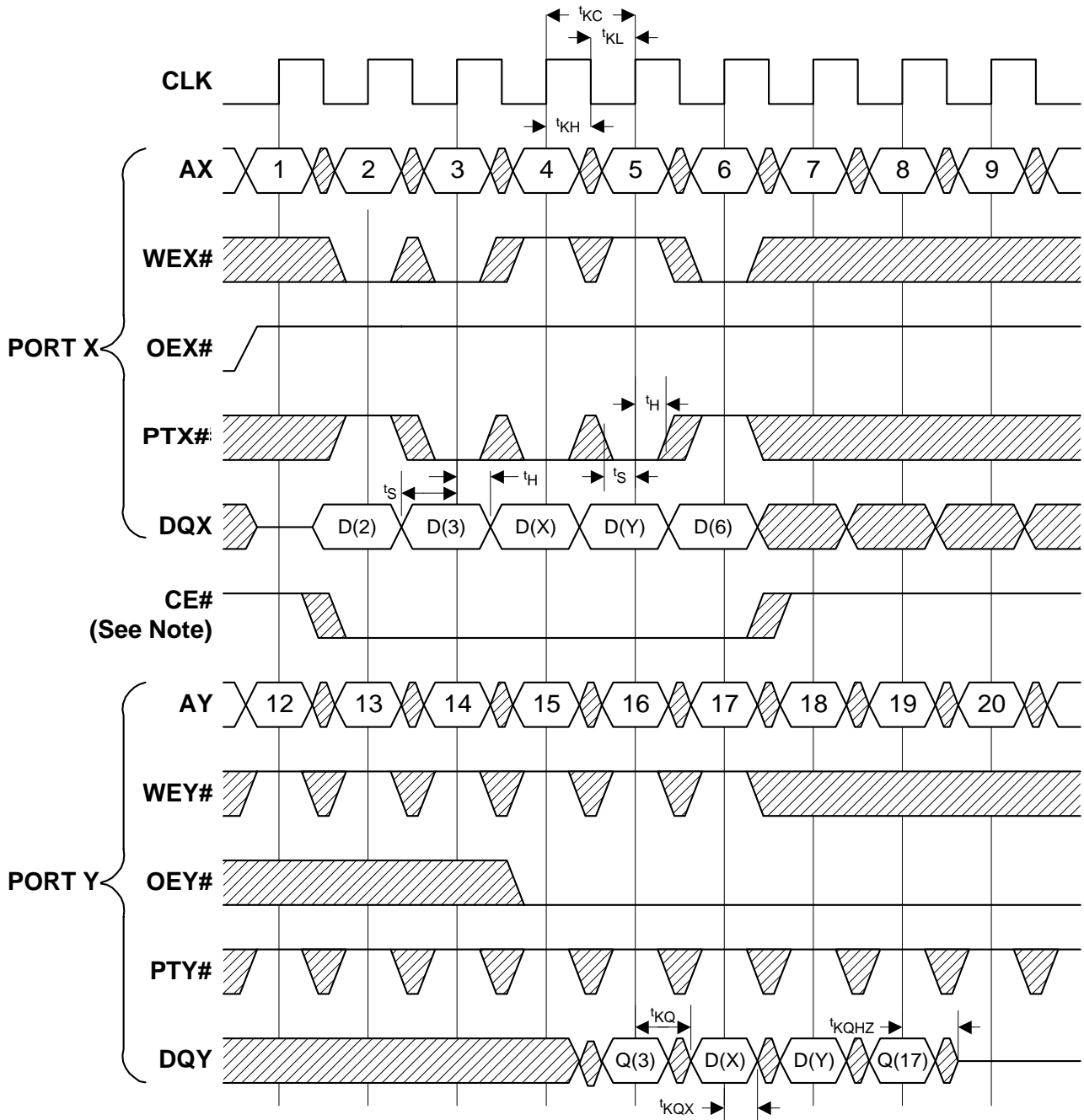| Parameter | Description | -100 Min. | -100 Max. | -83 Min. | -83 Max. | Unit |
|---|---|---|---|---|---|---|
| **Clock** | | | | | | |
| $t_{KC}$ | Clock cycle time | 10 | | 12 | | ns |
| $t_{KH}$ | Clock HIGH time | 3.5 | | 4.0 | | ns |
| $t_{KL}$ | Clock LOW time | 3.5 | | 4.0 | | ns |
| **Output times** | | | | | | |
| $t_{KQ}$ | Clock to output valid | | 5.0 | | 6.0 | ns |
| $t_{KQX}$ | Clock to output invalid | 1.5 | | 1.5 | | ns |
| $t_{KQLZ}$ | Clock to output in Low-Z[21] | 0 | | 0 | | ns |
| $t_{KQHZ}$ | Clock to output in High-Z[21] | | 3.0 | | 3.0 | ns |
| $t_{OEQ}$ | $\overline{OEX}/\overline{OEY}$ to output valid | | 5.0 | | 6.0 | ns |
| $t_{OELZ}$ | $\overline{OEX}/\overline{OEY}$ to output in Low-Z[21] | 0 | | 0 | | ns |
| $t_{OEHZ}$ | $\overline{OEX}/\overline{OEY}$ to output in High-Z[21] | | 3.0 | | 3.0 | ns |
| **Set-up times** | | | | | | |
| $t_S$ | Addresses, controls, and data In | 1.8 | | 2.0 | | ns |
| **Hold times** | | | | | | |
| $t_H$ | Addresses, controls, and data In | 0.5 | | 0.5 | | ns |

**Notes:**

19. $t_{CHZ}$, $t_{CLZ}$, $t_{OEV}$, $t_{EOLZ}$, and $t_{EOHZ}$ are specified with AC test conditions, as shown in part (a) of AC Test Loads. Transition is measured ±200 mV from steady-state voltage.

20. At any given voltage and temperature, $t_{EOHZ}$ is less than $t_{EOLZ}$ and $t_{CHZ}$ is less than $t_{CLZ}$ to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but rather reflect parameters guaranteed over worst-case user conditions. Device is designed to achieve High-Z prior to Low-Z under the same system conditions.

21. This parameter is sampled and not 100% tested.

## Switching Waveforms [22]

### Read Cycle Timing from Both Ports (WEX, WEY, PTX, PTY HIGH)[22]
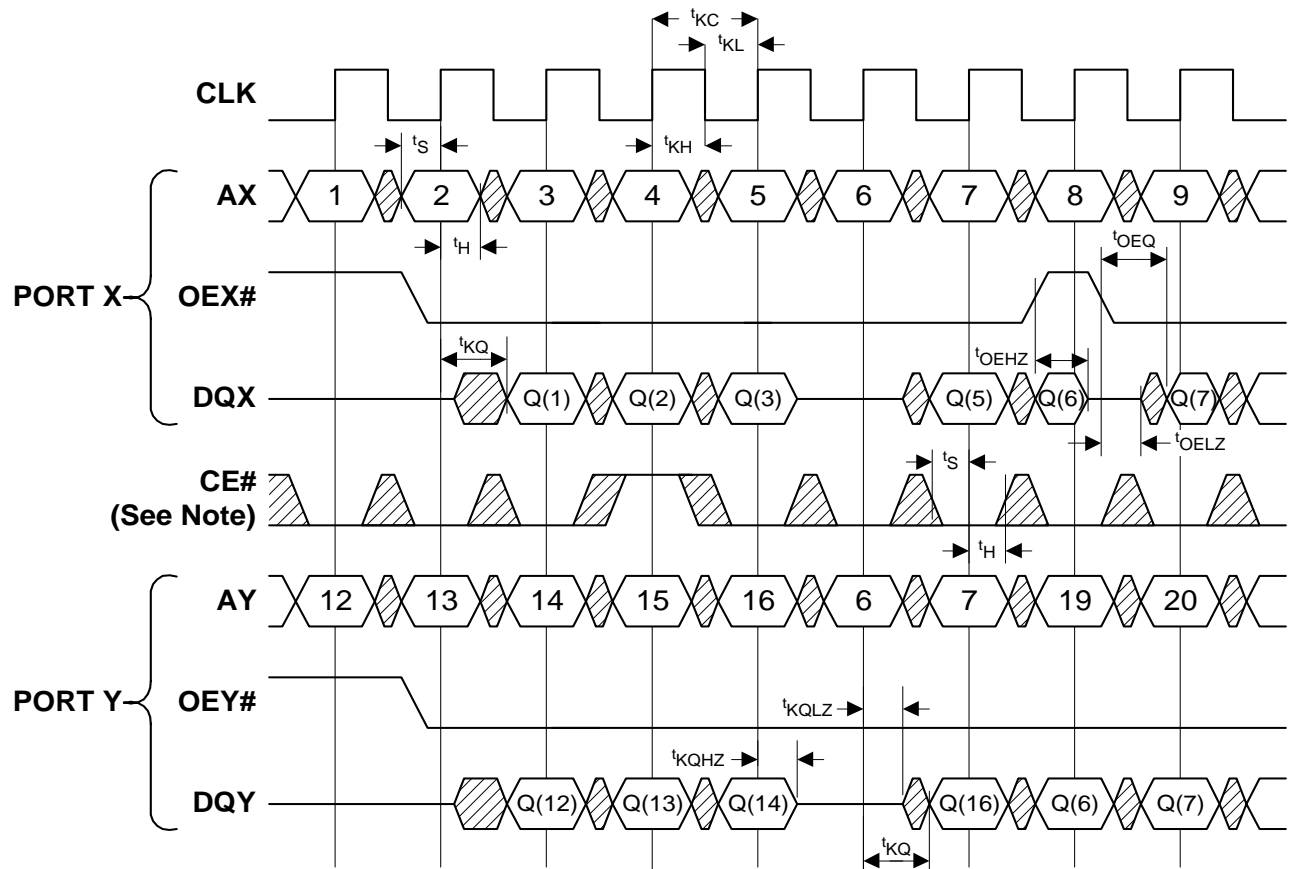


22. $\overline{CE}$ LOW means ($\overline{CE1X}$ and $\overline{CE1Y}$) equals LOW and (CE2X and CE2Y) equals HIGH. $\overline{CE}$ HIGH means ($\overline{CE1X}$ and $\overline{CE1Y}$) equals HIGH or (CE2X and CE2Y) equals LOW.

**Switching Waveforms** (continued)[22]

**Write Cycle Timing to Both Ports (PTX, PTY HIGH)**[21]



PORT Y TAKES
PRIORITY OVER PORT X
WHEN AX=AY AND
WRITING TO BOTH

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## Switching Waveforms (continued)[22]

**Write to Port X and Pass-through to Port Y[21]**

## Switching Waveforms (continued)[22]

### Combination Read/Write with Same Address on Each Port



PORT Y TAKES PRIORITY OVER PORT X WHEN AX=AY AND WRITING TO BOTH PORTS.
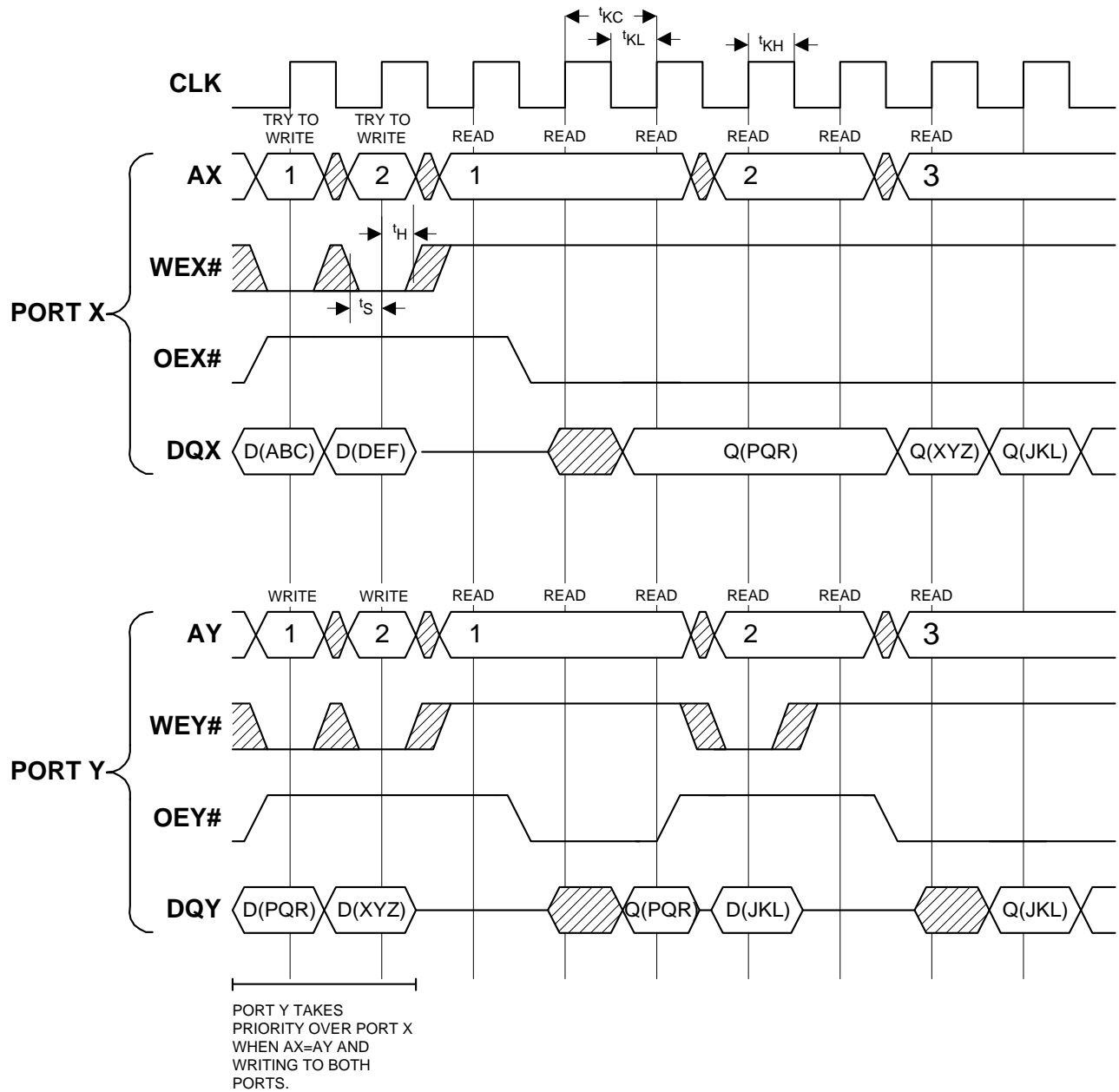
PTX# = PTY# = HIGH
D(Value) = Value is the input of the data port.
Q(Value) = Value is the output of the data port.

## Ordering Information

| Speed (MHz) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 100 | CY7C1300A-100AC | AC | 176-lead TQFP | Commercial |
| 83 | CY7C1300A-83AC | | | |

## Package Diagram

**176-lead Thin Quad Flat Pack (24 × 24 × 1.4 mm) A176**



51-85132
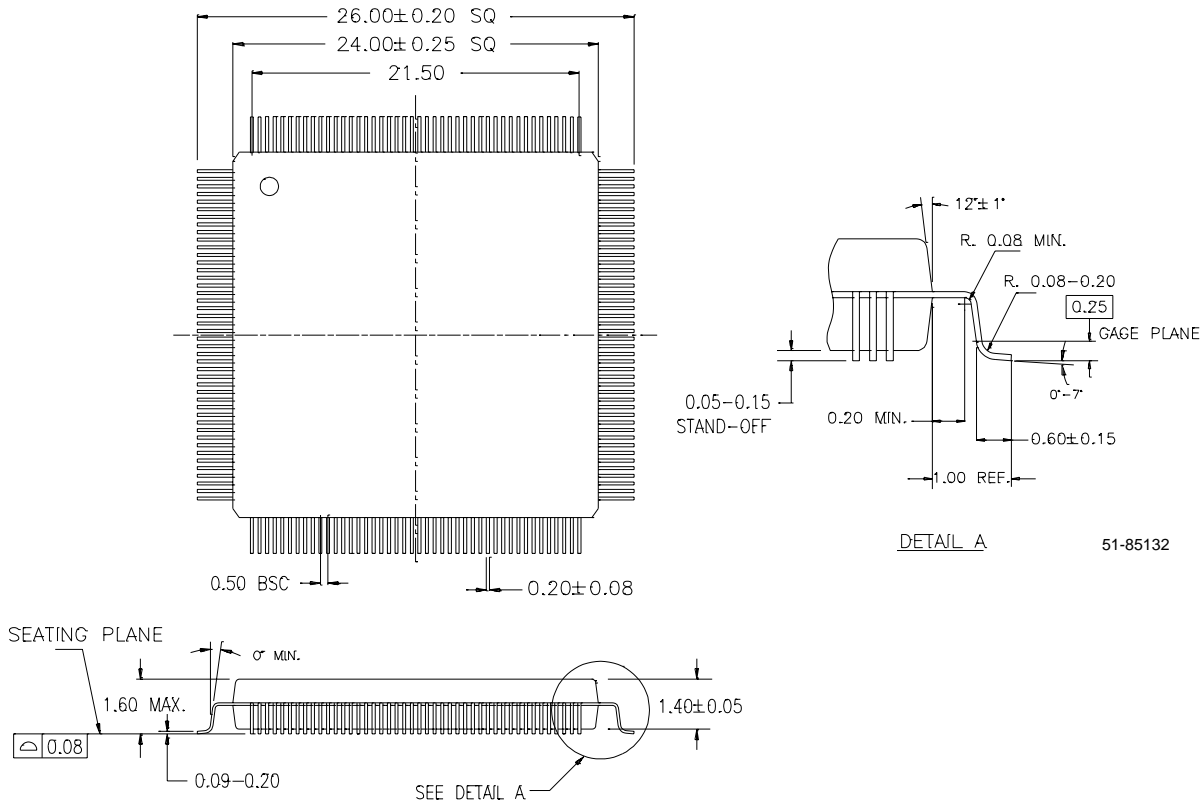
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**Document Title: CY7C1300A 128K x 36 Dual I/O Dual Address Synchronous SRAM**
**Document Number: 38-05075**

| REV. | ECN NO. | Issue Date | Orig. of Change | Description of Change |
|---|---|---|---|---|
| ** | 107304 | 06/08/01 | NSL | New Data Sheet |
| *A | 109296 | 10/31/01 | CJM | 1. Removed 133 MHz speed bin<br>2. Changed ESD voltage from >2001V to >1601V<br>3. Changed $t_S$ from 1.5 ns to 1.8 ns (only 100 MHz)<br>4. Changed $I_{SB}$ from 100 mA to 120 mA (All speeds)<br>5. Changed $C_{IN}$ from 6 pF to 8 pF (All speeds)<br>6. Changed $C_{CLK}$ from 6 pF to 9 pF (All speeds)<br>7. Changed $I_{CC}$ to reflect char data (All speeds)<br>8. Changed ordering code from CY7C1301A to CY7C1300A (All speeds)<br>9. Removed Preliminary |
| *B | 113017 | 04/09/02 | KOM | Changed $I_{CC}$ values on first page to correct value (500 and 430). Also updated Logic Block Diagram. |
| *C | 123844 | 01/19/03 | AJH | Updated power-up requirements in Operating Range and in AC Test Loads and Waveforms. |