LM555QML

LM555QML Timer

Literature Number: SNOSAP2B

National Semiconductor

July 2006

LM555QML
Timer

General Description

The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200mA or drive TTL circuits.

Features

- Direct replacement for SE555/NE555
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per ˚C
- Normally on and normally off output

Applications

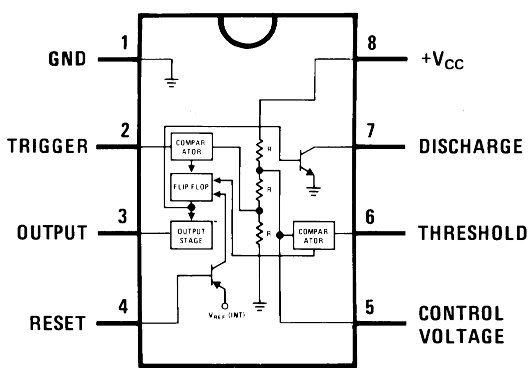
- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

Ordering Information

NS Part Number	SMD Part Number	NS Package Number	Package Description
LM555H/883		H08A	8LD Metal Can
LM555J/883		J08A	8LD Ceramic Dip

Connection Diagrams

Dual-In-Line Package



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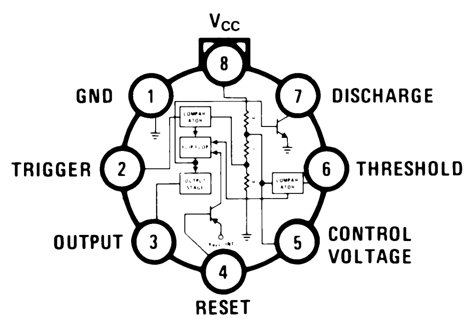
Top View

Metal Can Package



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Top View

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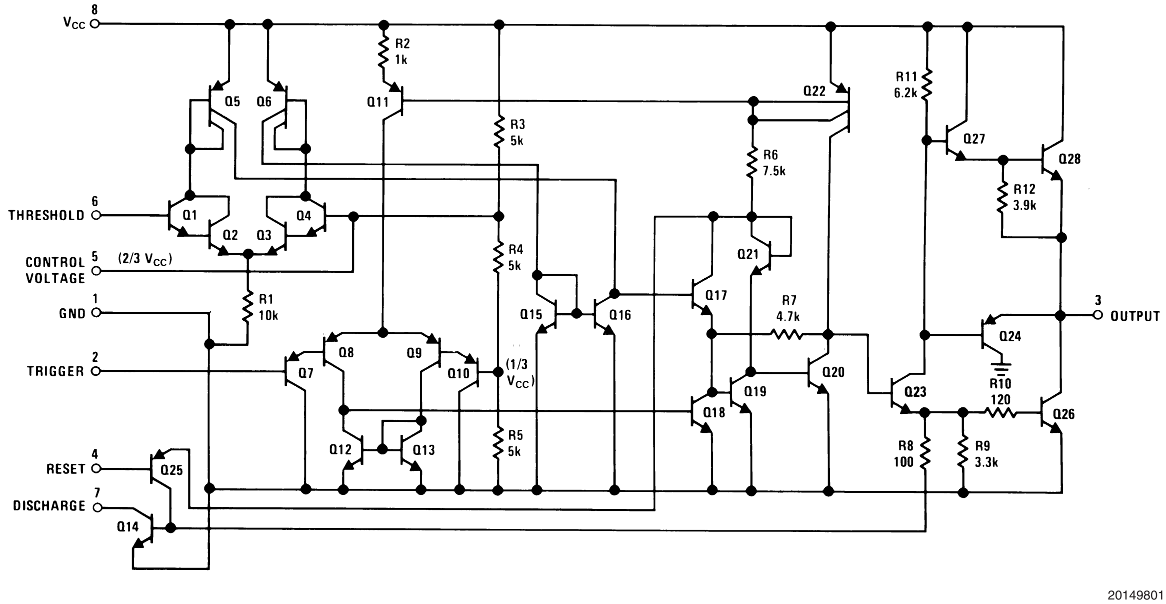
Schematic Diagram



Absolute Maximum Ratings (Note 1)

Supply Voltage	+18V
Power Dissipation (Note 2)	
Metal Can	760 mW
CERDIP	1180 mW
Operating Temperature Range	$-55^\circ C \leq T_A \leq +125^\circ C$
Maximum Junction Temperature (T_{Jmax})	+150˚C
Storage Temperature Range	$-65^\circ C \leq T_A \leq +150^\circ C$
Soldering Information (Soldering 10 Seconds)	260˚C
Thermal Resistance	
θ_{JA}	
CERDIP Still Air	125˚C/W
CERDIP 500LF / Min Air Flow	71˚C/W
Metal Can Still Air	176˚C/W
Metal Can 500LF / Min Air Flow	96˚C/W
θ_{JC}	
CERDIP	20˚C/W
Metal Can	42˚C/W
ESD Tolerance (Note 3)	500V

Quality Conformance Inspection

Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp ˚C
1	Static tests at	25
2	Static tests at	125
3	Static tests at	-55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	-55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	-55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	-55
12	Settling time at	25
13	Settling time at	125
14	Settling time at	-55

Electrical Characteristics

DC Parameters

The following conditions apply to all the following parameters, unless otherwise specified.

DC: $+5V \le V_{CC} \le +15V$

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
I_{CCL}	Supply Current Low State	$V_{CC} = 5V$, $R_L = \infty$			5.0	mA	1
		$V_{CC} = 15V$, $R_L = \infty$			12.0	mA	1
		$V_{CC} = 18V$, $R_L = \infty$, $V_2 = V_6 = 18V$			18.5	mA	1
I_{L7}	Leakage Current Pin 7	$V_{CC} = 18V$, $V_7 = 18V$, $V_2 = V_6 = 0$			100	nA	1
V_{Sat}	Saturation Voltage Pin 7	$V_{CC} = 15V$, $I_7 = 15mA$, $V_2 = V_6 = 12V$	(Note 6)		240	mV	1
		$V_{CC} = 4.5V$, $I_7 = 4.5mA$	(Note 6)		80	mV	1
V_{CO}	Control Voltage	$V_{CC} = 5V$, $V_2 = V_6 = 4V$		2.9	3.8	V	1, 2, 3
		$V_{CC} = 15V$, $V_2 = V_6 = 12V$		9.6	10.4	V	1, 2, 3
V_{Th}	Threshold Voltage			9.5	10.5	V	1
I_{Th}	Threshold Current	$V_6 = V_{Th}$, $V_2 = 7.5V$, $V_{Th} = V_{Th}$ Test Measured Value	(Note 7)		250	nA	1
I_{Trig}	Trigger Current	$V_2 = 0$			500	nA	1
V_{Trig}	Trigger Voltage	$V_{CC} = 15V$		4.8	5.2	V	1
				3.0	6.0	V	2, 3
		$V_{CC} = 5V$	(Note 4)	1.45	1.9	V	1, 2, 3
I_{Reset}	Reset Current	$V_2 = V_6 = Gnd$			0.4	mA	1
V_{Reset}	Reset Voltage			0.4	1.0	V	1
V_{OL}	Output Voltage Drop Low	$V_{CC} = 5V$, $I_{Sink} = +8mA$, $V_7 = 5V$, $V_6 = 5V$			250	mV	1, 2, 3
		$V_{CC} = 15V$, $I_{Sink} = +10mA$, $V_2 = V_6 = 15V$			150	mV	1
					250	mV	2, 3
		$V_{CC} = 15V$, $I_{Sink} = +50mA$, $V_2 = V_6 = 15V$			500	mV	1
					800	mV	2, 3
		$V_{CC} = 15V$, $I_{Sink} = +85mA$, $V_2 = V_6 = 15V$			2.2	V	1, 2, 3
V_{OH}	Output Voltage Drop High	$V_{CC} = 15V$, $I_{Source} = 85mA$		13		V	1
				12.75		V	2, 3
		$V_{CC} = 5V$, $I_{Source} = 85mA$		3		V	1
				2.75		V	2, 3
Af	A Stable Frequency		(Note 5)	45	51	KHz	1
tE	Timing Error	$V_{CC} = 5V$	(Note 5)		±2	%	1, 2, 3
		$V_{CC} = 15V$, $1K\Omega \le R_A \le 100K\Omega$, Timing error decreases with an increase in V_{CC}	(Note 5)		±2	%	1, 2, 3
$\Delta tE / \Delta V_{CC}$	Timing Drift with Supply	$5V \le V_{CC} \le 15V$	(Note 5)		0.2	% / V	1, 2, 3

Electrical Characteristics (Continued)

AC Parameters

The following conditions apply to all the following parameters, unless otherwise specified.

AC: $+5V \le V_{CC} \le +15V$

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
tR	Rise Time	$V_{Trig} = 5V$	(Note 5)		250	nS	9, 10
			(Note 5)		400	nS	11
tF	Fall Time	$V_{Trig} = 5V$	(Note 5)		250	nS	9, 10
			(Note 5)		400	nS	11

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: Human body model, 1.5KΩ in series with 100pF.

Note 4: Guaranteed by tests at V_{CC} = 15V.

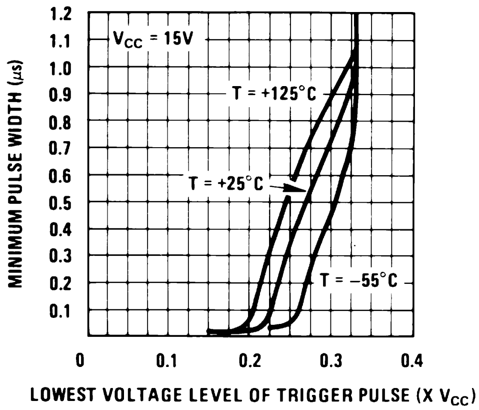
Note 5: Guaranteed parameter, not tested.

Note 6: No protection against excessive pin 7 current is necessary providing the package dissipation rating will not be exceeded.

Note 7: This will determine the maximum value of $R_A + R_B$ for 15V operation. The maximum total ($R_A + R_B$) is 20MΩ.

Typical Performance Characteristics

Minimum Pulse Width Required for Triggering



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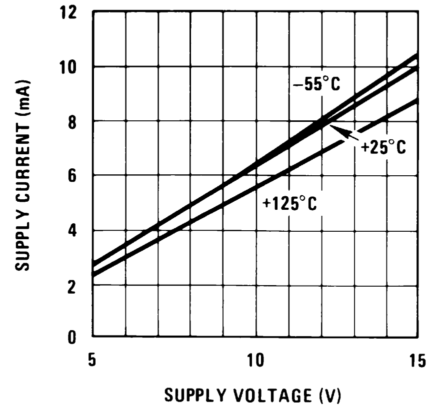
Supply Current vs. Supply Voltage



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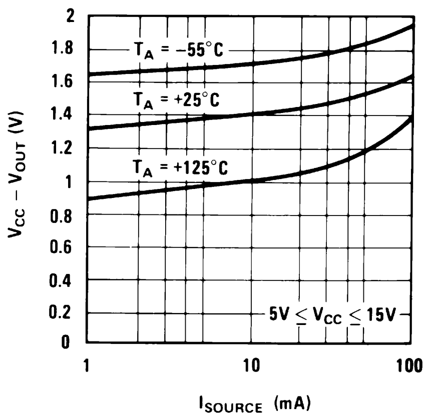
High Output Voltage vs. Output Source Current



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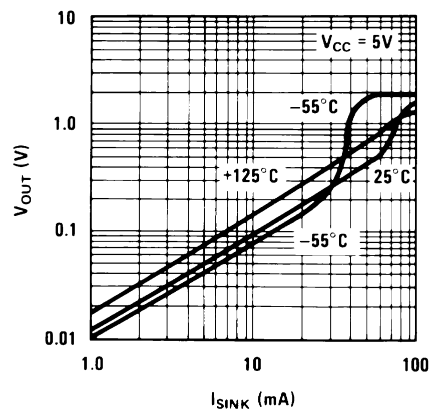
Low Output Voltage vs. Output Sink Current



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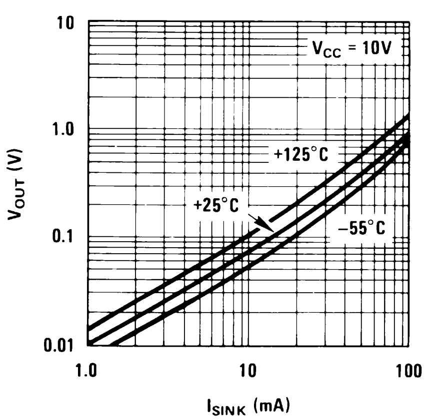
Low Output Voltage vs. Output Sink Current



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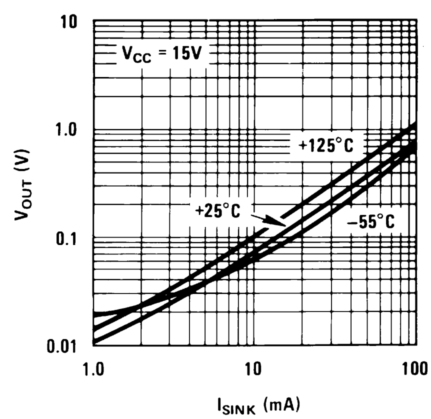
Low Output Voltage vs. Output Sink Current



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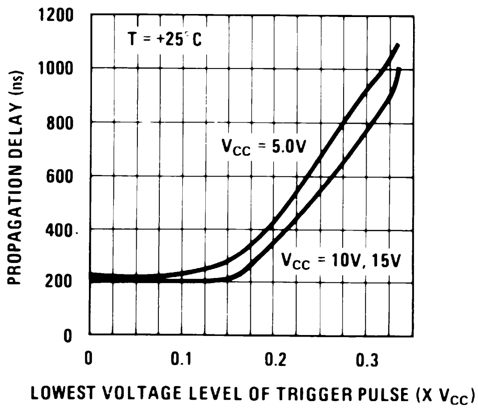
Typical Performance Characteristics (Continued)

Output Propagation Delay vs. Voltage Level of Trigger Pulse



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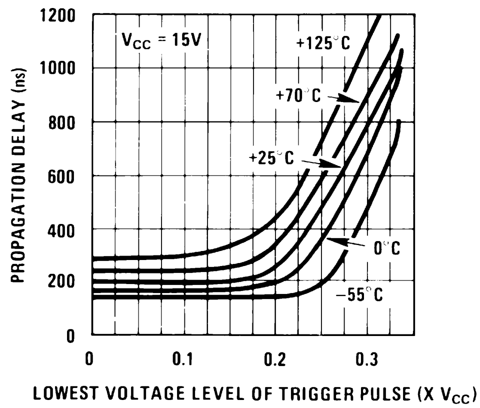
Output Propagation Delay vs. Voltage Level of Trigger Pulse



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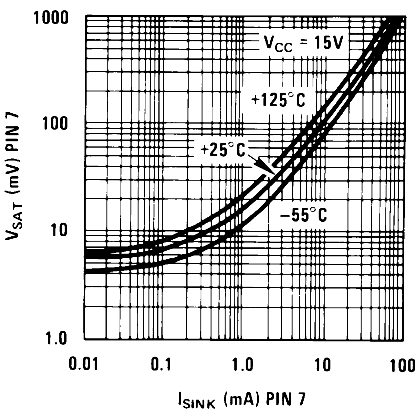
Discharge Transistor (Pin 7) Voltage vs. Sink Current



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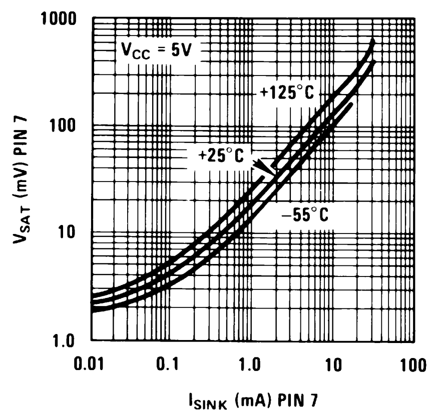
Discharge Transistor (Pin 7) Voltage vs. Sink Current



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Applications Information

MONOSTABLE OPERATION

In this mode of operation, the timer functions as a one-shot (*Figure 1*). The external capacitor is initially held discharged by a transistor inside the timer. Upon application of a negative trigger pulse of less than 1/3 V_{CC} to pin 2, the flip-flop is set which both releases the short circuit across the capacitor and drives the output high.

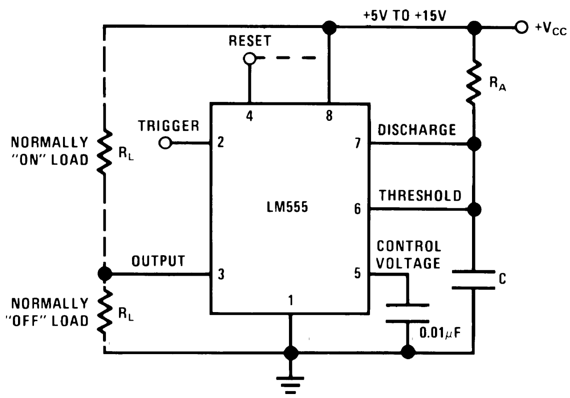

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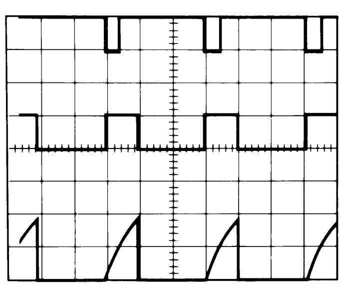
FIGURE 1. Monostable

The voltage across the capacitor then increases exponentially for a period of $t = 1.1\ R_A\ C$, at the end of which time the voltage equals 2/3 V_{CC}. The comparator then resets the flip-flop which in turn discharges the capacitor and drives the output to its low state. *Figure 2* shows the waveforms generated in this mode of operation. Since the charge and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply.



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V_{CC} = 5V — Top Trace: Input 5V/Div.
TIME = 0.1 ms/DIV. — Middle Trace: Output 5V/Div.
R_A = 9.1kΩ — Bottom Trace: Capacitor Voltage 2V/Div.
C = 0.01μF

FIGURE 2. Monostable Waveforms

During the timing cycle when the output is high, the further application of a trigger pulse will not effect the circuit so long as the trigger input is returned high at least 10μs before the end of the timing interval. However the circuit can be reset during this time by the application of a negative pulse to the reset terminal (pin 4). The output will then remain in the low state until a trigger pulse is again applied.

When the reset function is not in use, it is recommended that it be connected to V_{CC} to avoid any possibility of false triggering.

Figure 3 is a nomograph for easy determination of R, C values for various time delays.

NOTE: In monostable operation, the trigger should be driven high before the end of timing cycle.

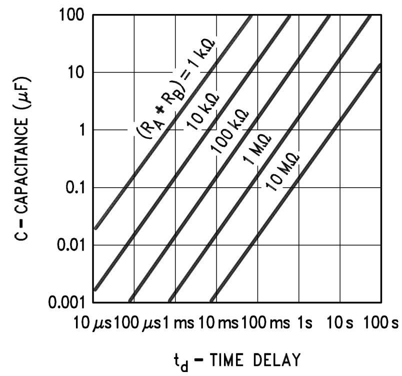

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FIGURE 3. Time Delay

ASTABLE OPERATION

If the circuit is connected as shown in *Figure 4* (pins 2 and 6 connected) it will trigger itself and free run as a multivibrator. The external capacitor charges through $R_A + R_B$ and discharges through R_B. Thus the duty cycle may be precisely set by the ratio of these two resistors.

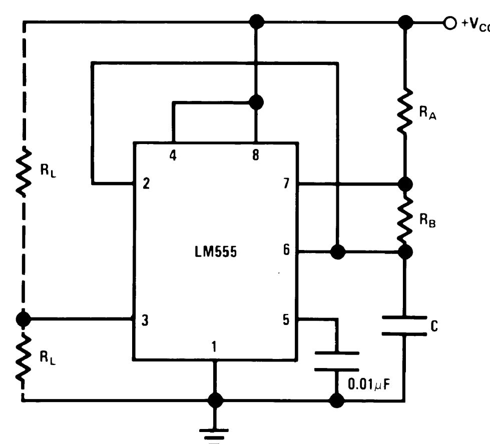

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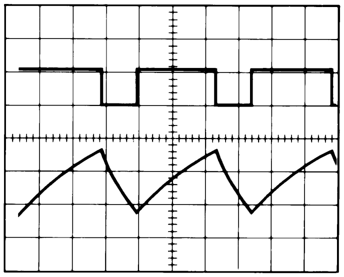
FIGURE 4. Astable

In this mode of operation, the capacitor charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Applications Information (Continued)

Figure 5 shows the waveforms generated in this mode of operation.



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V_{CC} = 5V Top Trace: Output 5V/Div.
TIME = 20μs/DIV. Bottom Trace: Capacitor Voltage 1V/Div.
R_A = 3.9kΩ
R_B = 3kΩ
C = 0.01μF

FIGURE 5. Astable Waveforms

The charge time (output high) is given by:

$$t_1 = 0.693\ (R_A + R_B)\ C$$

And the discharge time (output low) by:

$$t_2 = 0.693\ (R_B)\ C$$

Thus the total period is:

$$T = t_1 + t_2 = 0.693\ (R_A + 2R_B)\ C$$

The frequency of oscillation is:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2\,R_B)\,C}$$

Figure 6 may be used for quick determination of these RC values.

The duty cycle is:

$$D = \frac{R_B}{R_A + 2R_B}$$

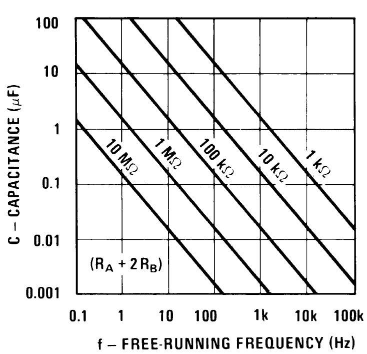

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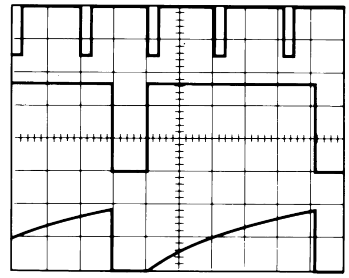
FIGURE 6. Free Running Frequency

FREQUENCY DIVIDER

The monostable circuit of *Figure 1* can be used as a frequency divider by adjusting the length of the timing cycle. *Figure 7* shows the waveforms generated in a divide by three circuit.



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V_{CC} = 5V Top Trace: Input 4V/Div.
TIME = 20μs/DIV. Middle Trace: Output 2V/Div.
R_A = 9.1kΩ Bottom Trace: Capacitor 2V/Div.
C = 0.01μF

FIGURE 7. Frequency Divider

PULSE WIDTH MODULATOR

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to pin 5. *Figure 8* shows the circuit, and in *Figure 9* are some waveform examples.

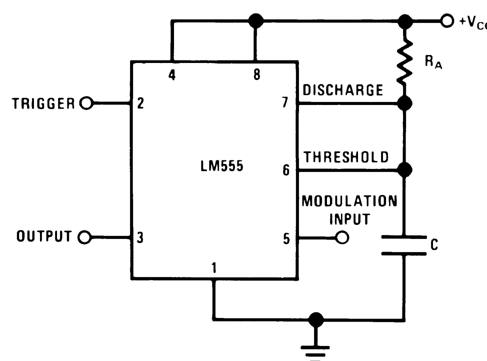

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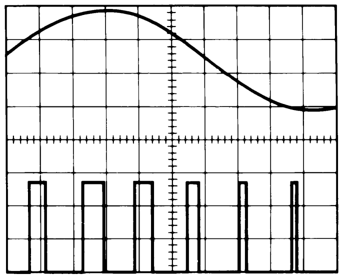
FIGURE 8. Pulse Width Modulator

Applications Information (Continued)



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V_{CC} = 5V Top Trace: Modulation 1V/Div.
TIME = 0.2 ms/DIV. Bottom Trace: Output Voltage 2V/Div.
R_A = 9.1kΩ
C = 0.01µF

FIGURE 9. Pulse Width Modulator

PULSE POSITION MODULATOR

This application uses the timer connected for astable operation, as in *Figure 10*, with a modulating signal again applied to the control voltage terminal. The pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied. *Figure 11* shows the waveforms generated for a triangle wave modulation signal.

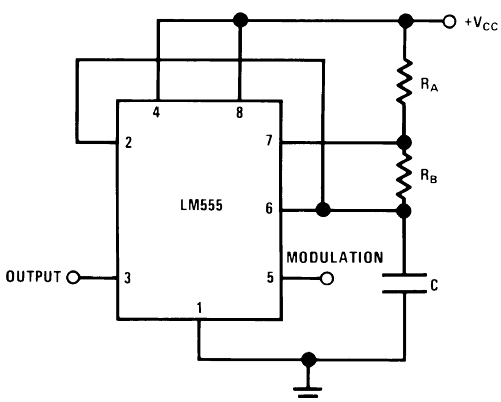

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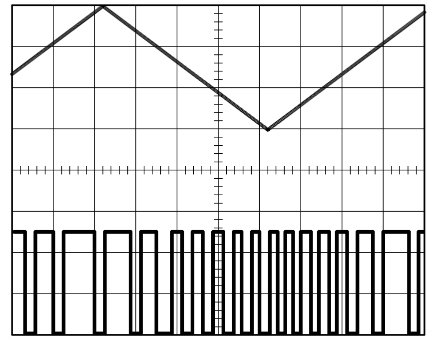
FIGURE 10. Pulse Position Modulator



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V_{CC} = 5V Top Trace: Modulation Input 1V/Div.
TIME = 0.1 ms/DIV. Bottom Trace: Output 2V/Div.
R_A = 3.9kΩ
R_B = 3kΩ
C = 0.01µF

FIGURE 11. Pulse Position Modulator

LINEAR RAMP

When the pullup resistor, R_A, in the monostable circuit is replaced by a constant current source, a linear ramp is generated. *Figure 12* shows a circuit configuration that will perform this function.

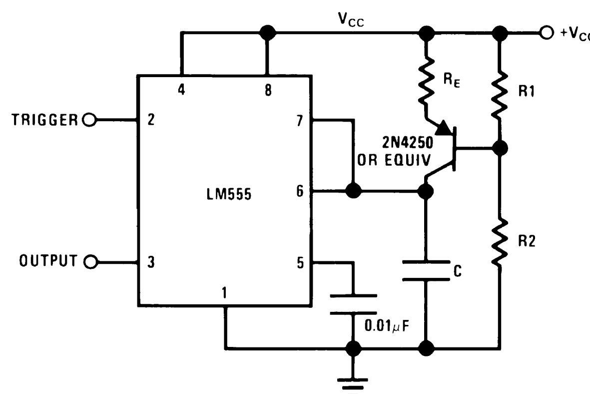

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FIGURE 12.

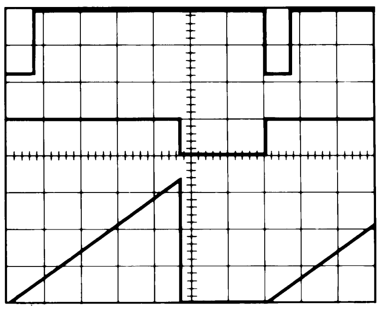
Figure 13 shows waveforms generated by the linear ramp.

The time interval is given by:

$$T = \frac{2/3\, V_{CC}\, R_E\, (R_1 + R_2)\, C}{R_1\, V_{CC} - V_{BE}\, (R_1 + R_2)}$$

$$V_{BE} \cong 0.6V$$

$$V_{BE} \simeq 0.6V$$



V_{CC} = 5V | Top Trace: Input 3V/Div.
TIME = 20μs/DIV. | Middle Trace: Output 5V/Div.
R_1 = 47kΩ | Bottom Trace: Capacitor Voltage 1V/Div.
R_2 = 100kΩ
R_E = 2.7 kΩ
C = 0.01 μF

FIGURE 13. Linear Ramp

50% DUTY CYCLE OSCILLATOR

For a 50% duty cycle, the resistors R_A and R_B may be connected as in *Figure 14*. The time period for the output high is the same as previous, $t_1 = 0.693\ R_A\ C$. For the output low it is t_2 =

$$\left[(R_A R_B)/(R_A + R_B)\right] C\ \ell n \left[\frac{R_B - 2R_A}{2R_B - R_A}\right]$$

Thus the frequency of oscillation is

$$f = \frac{1}{t_1 + t_2}$$

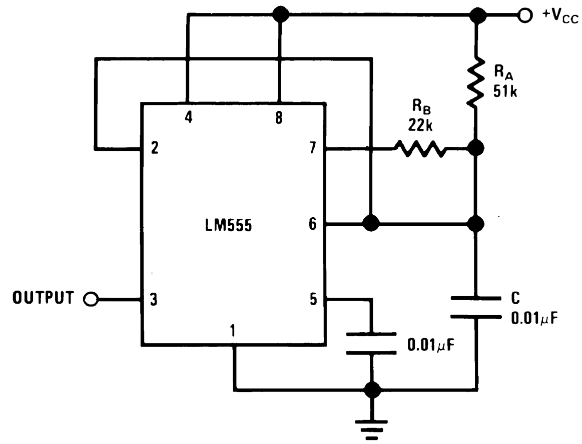


FIGURE 14. 50% Duty Cycle Oscillator

Note that this circuit will not oscillate if R_B is greater than 1/2 R_A because the junction of R_A and R_B cannot bring pin 2 down to 1/3 V_{CC} and trigger the lower comparator.

ADDITIONAL INFORMATION

Adequate power supply bypassing is necessary to protect associated circuitry. Minimum recommended is 0.1μF in parallel with 1μF electrolytic.

Lower comparator storage time can be as long as 10μs when pin 2 is driven fully to ground for triggering. This limits the monostable pulse width to 10μs minimum.

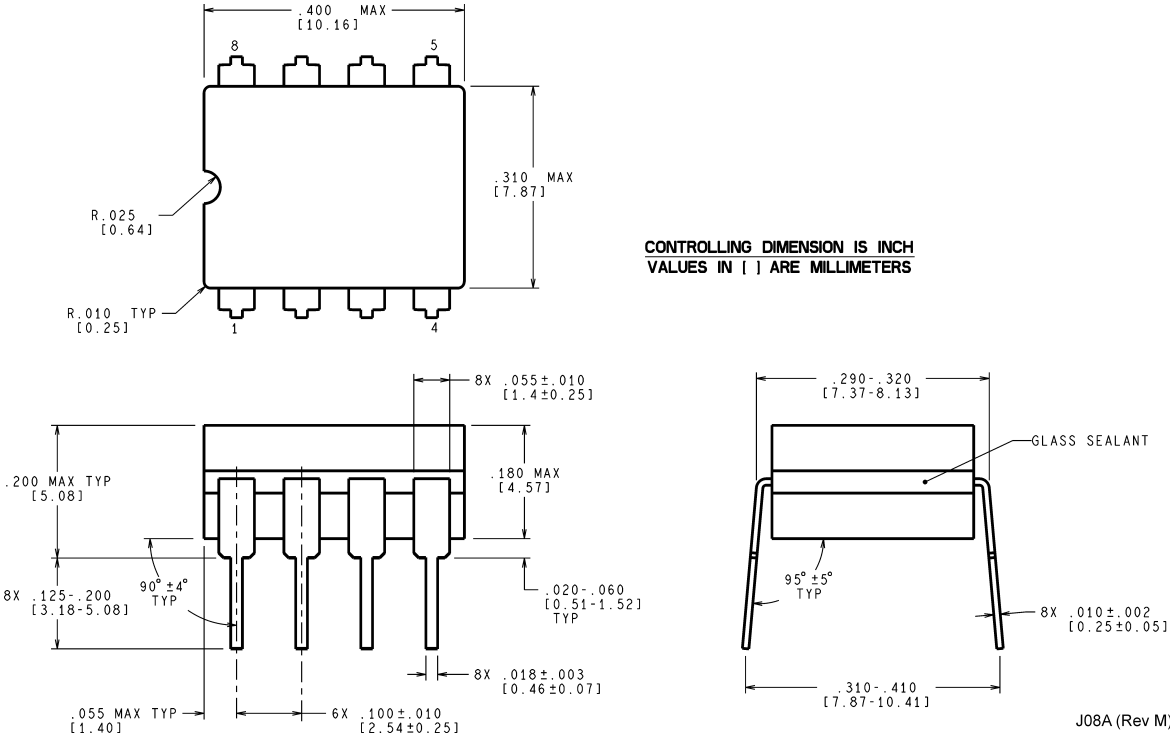
Delay time reset to output is 0.47μs typical. Minimum reset pulse width must be 0.3μs, typical.

Pin 7 current switches within 30ns of the output (pin 3) voltage.

Revision History

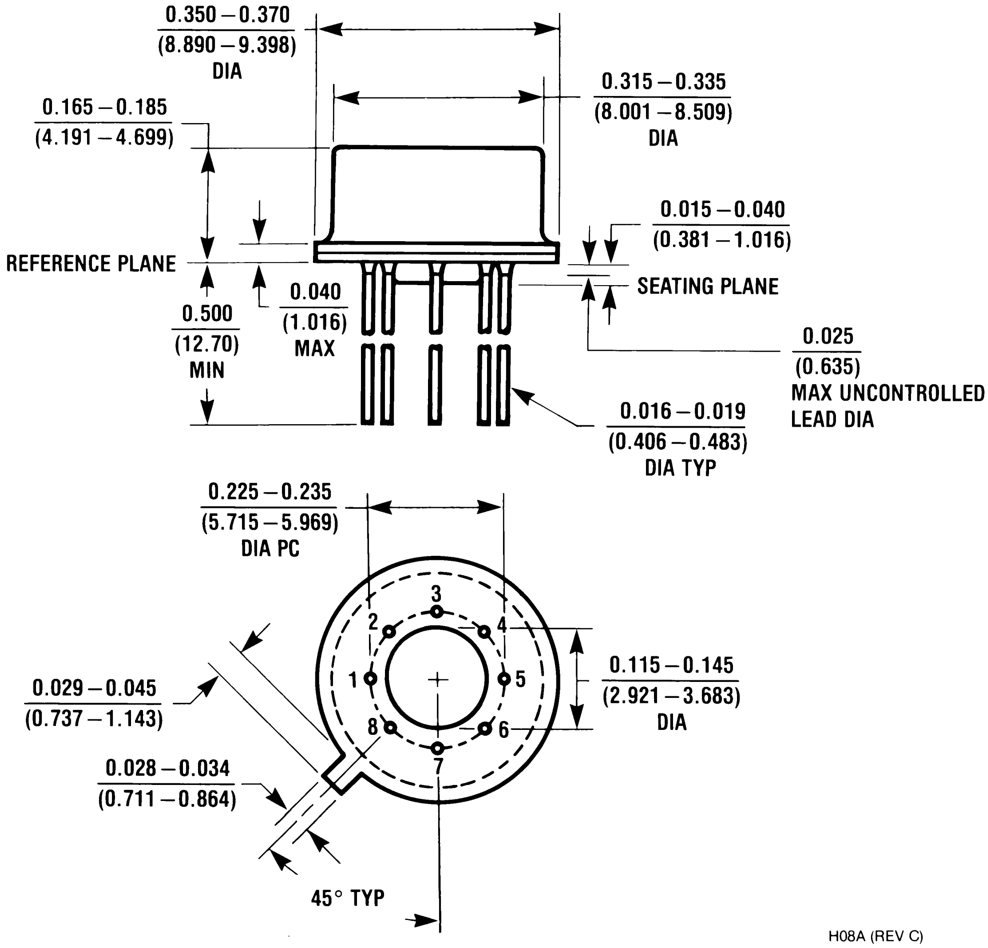
Date Released	Revision	Section	Originator	Changes
08/04/05	A	New Release to corporate format	L. Lytle	1 MDS datasheet converted into once datasheet in the corporate format. Removed drift endpoints since not performed on 883 product. MNLM555-X Rev 0B0 to be archived
04/10/06	B	Ordering Information Table	R. Malone	NS Package Number and Description was referenced incorrectly. Revision A will be Archived.
07/25/06	C	Applications Information, page 8	R. Malone	Correct a typo in the paragraph after figure 1 (change the word internal to interval) to reflect same change made to Commercial data sheet. Revision B will be Archived.

Physical Dimensions inches (millimeters) unless otherwise noted



8LD Ceramic Dip Package (J)
NS Package Number J08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



8LD Metal Can Package (H)
NS Package Number H08A

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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