CY7C340 EPLD Family

Multiple Array Matrix High-Density EPLDs

Features

- **Erasable, user-configurable CMOS EPLDs capable of implementing high-density custom logic functions**
- **0.8-micron double-metal CMOS EPROM technology (CY7C34X)**
- **Advanced 0.65-micron CMOS technology to increase performance (CY7C34XB)**
- **Multiple Array MatriX architecture optimized for speed, density, and straightforward design implementation**
  - **— Programmable Interconnect Array (PIA) simplifies routing**
  - **— Flexible macrocells increase utilization**
  - **— Programmable clock control**
  - **— Expander product terms implement complex logic functions**

General Description

The Cypress Multiple Array Matrix (MAX®) family of EPLDs provides a user-configurable, high-density solution to general-purpose logic integration requirements. With the combination of innovative architecture and state-of-the-art process, the MAX EPLDs offer LSI density without sacrificing speed.

The MAX architecture makes it ideal for replacing large amounts of TTL SSI and MSI logic. For example, a 74161 counter utilizes only 3% of the 128 macrocells available in the CY7C342B. Similarly, a 74151 8-to-1 multiplexer consumes less than 1% of the over 1,000 product terms in the CY7C342B. This allows the designer to replace 50 or more TTL packages with just one MAX EPLD. The family comes in a range of densities, shown below. By standardizing on a few MAX building blocks, the designer can replace hundreds of different 7400 series part numbers currently used in most digital systems.

The family is based on an architecture of flexible macrocells grouped together into Logic Array Blocks (LABs). Within the LAB is a group of additional product terms called expander product terms. These expanders are used and shared by the macrocells, allowing complex functions of up to 35 product terms to be easily implemented in a single macrocell. A Programmable Interconnect Array (PIA) globally routes all signals within devices containing more than one LAB. This architecture is fabricated on the Cypress 0.8-micron, double-layer-metal CMOS EPROM process, yielding devices with significantly higher integration, density and system clock speed than the largest of previous generation EPLDs. The CY7C34XB devices are 0.65-micron shrinks of the original 0.8-micron family. The CY7C34XBs offer faster speed bins for each device in the Cypress MAX family.

The density and performance of the CY7C340 family is accessed using Cypress's *Warp*™, *Warp* Professional™, or *Warp* Enterprise™ design software. *Warp* provides state-of-the-art synthesis, fitting, simulation and other development tools at a very low cost. *Warp* Professional or *Warp* Enterprise are sophisticated CAE tool that include behavioral simulation, graphical waveform editing and more. Consult the datasheets for *Warp*, *Warp* Professional and *Warp* Enterprise™ for more information about these development tools.

Max Family Members

Feature	CY7C344(B)	CY7C343(B)	CY7C342B	CY7C346(B)	CY7C341B
Macrocells	32	64	128	128	192
MAX Flip-Flops	32	64	128	128	192
MAX Latches[1]	64	128	256	256	384
MAX Inputs[2]	23	35	59	84	71
MAX Outputs	16	28	52	64	64
Packages	28H,J,W,P	44H,J	68H,J,R	84H,J 100R,N	84H,J,R

Key: P—Plastic DIP; H—Windowed Ceramic Leaded Chip Carrier; J—Plastic J-Lead Chip Carrier; R—Windowed Pin Grid Array; W—Windowed Ceramic DIP; N—Plastic Quad Flat Pack

Notes:

1. When all expander product terms are used to implement latches.
2. With one output.

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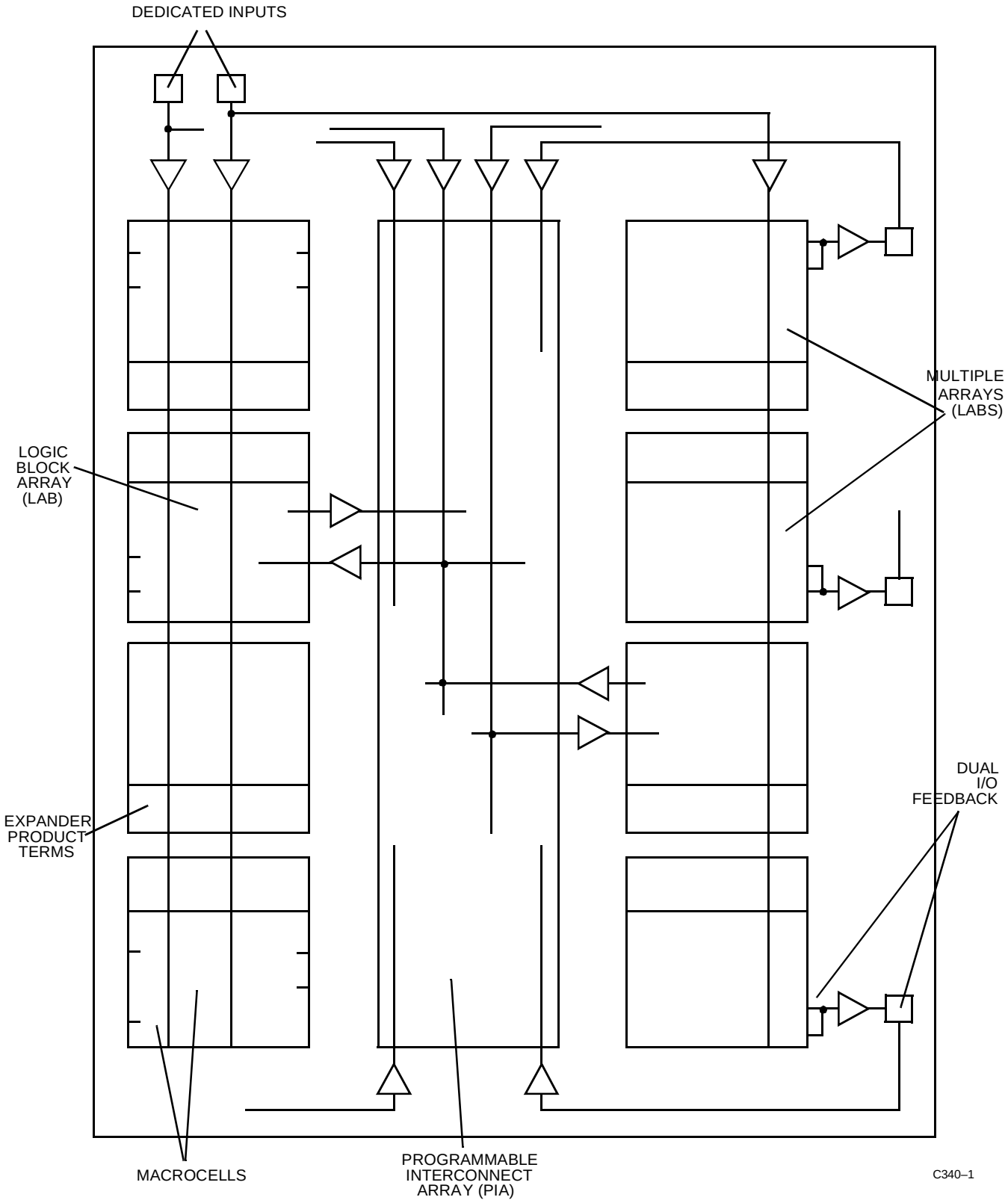

Figure 1. Key MAX Features

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Functional Description

The Logic Array Block

The logic array block, shown in *Figure 2*, is the heart of the MAX architecture. It consists of a macrocell array, expander product term array, and an I/O block. The number of macrocells, expanders, and I/O vary, depending upon the device used. Global feedback of all signals is provided within a LAB, giving each functional block complete access to the LAB resources. The LAB itself is fed by the programmable interconnect array and dedicated input bus. The feedbacks of the macrocells and I/O pins feed the PIA, providing access to them through other LABs in the device. The members of the CY7C340 family of EPLDs that have a single LAB use a global bus, so a PIA is not needed (see *Figure 3*).

The MAX Macrocell

Traditionally, PLDs have been divided into either PLA (programmable AND, programmable OR), or PAL® (programmable AND, fixed OR) architectures. PLDs of the latter type provide faster input-to-output delays, but can be inefficient due to fixed allocation of product terms. Statistical analysis of PLD logic designs has shown that 70% of all logic functions (per macrocell) require three product terms or less.

The macrocell structure of MAX has been optimized to handle variable product term requirements. As shown in *Figure 4*, each macrocell consists of a product term array and a configurable register. In the macrocell, combinatorial logic is implemented with three product terms ORed together, which then feeds an XOR gate. The second input to the XOR gate is also controlled by a product term, providing the ability to control active HIGH or active LOW logic and to implement T- and JK-type flip-flops.

If more product terms are required to implement a given function, they may be added to the macrocell from the expander product term array. These additional product terms may be added to any macrocell, allowing the designer to build gate-intensive logic, such as address decoders, adders, comparators, and complex state machines, without using extra macrocells.

The register within the macrocell may be programmed for either D, T, JK, or RS operation. It may alternately be configured as a flow-through latch for minimum input-to-output delays, or bypassed entirely for purely combinatorial logic. In addition, each register supports both asynchronous preset and clear, allowing asynchronous loading of counters of shift registers, as found in many standard TTL functions. These registers may be clocked with a synchronous system clock, or clocked independently from the logic array.

Expander Product Terms

The expander product terms, as shown in *Figure 5*, are fed by the dedicated input bus, the programmable interconnect array, the macrocell feedback, the expanders themselves, and the I/O pin feedbacks. The outputs of the expanders then go to each and every product term in the macrocell array. This allows expanders to be “shared” by the product terms in the logic array block. One expander may feed all macrocells in the LAB, or even multiple product terms in the same macrocell. Since these expanders feed the secondary product terms (preset, clear, clock, and output enable) of each macrocell, complex logic functions may be implemented without utilizing another macrocell. Likewise, expanders may feed and be shared by other expanders, to implement complex multilevel logic and input latches.

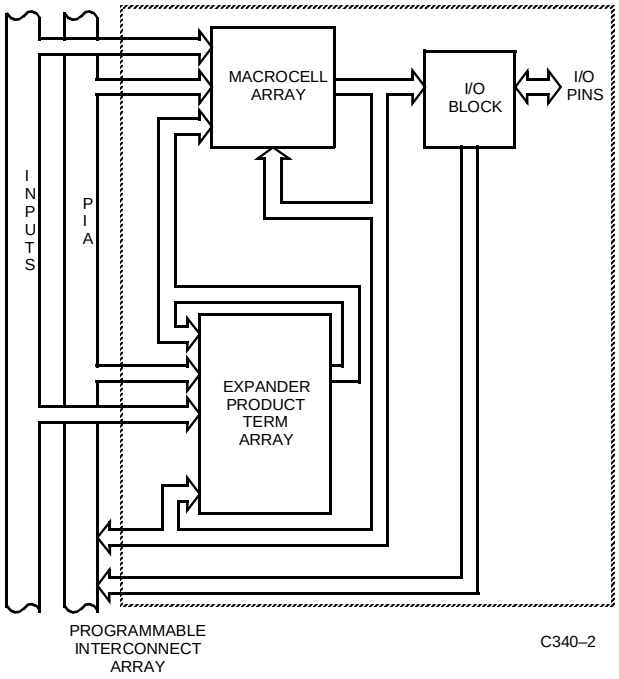

Figure 2. Typical LAB Block Diagram

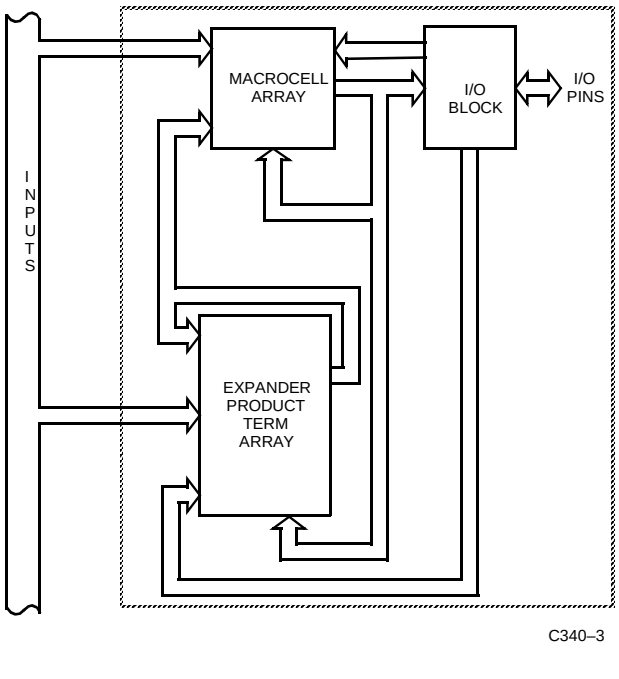

Figure 3. 7C344 LAB Block Diagram

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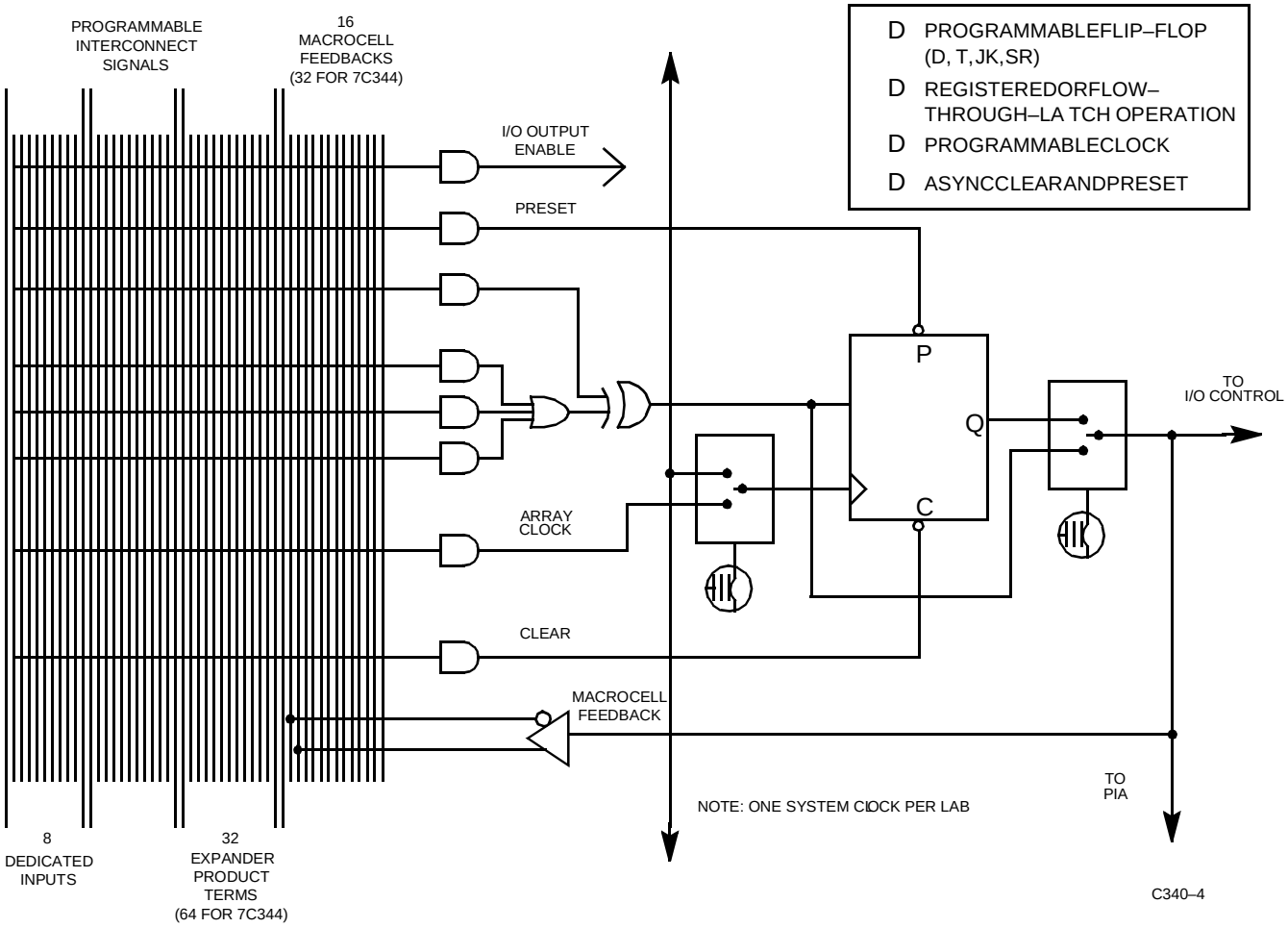

Figure 4. Macrocell Block Diagram

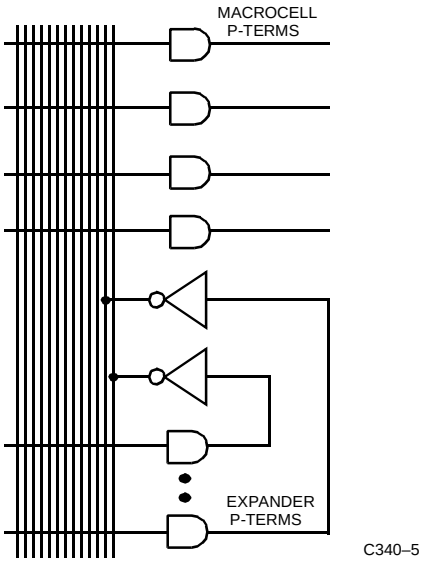

Figure 5. Expander Product Terms

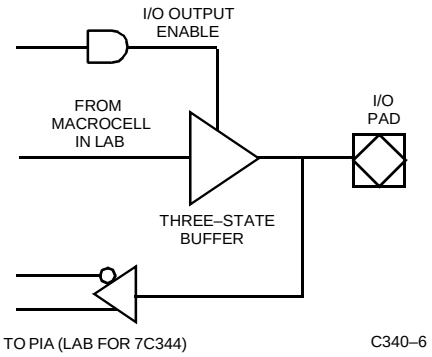

Figure 6. I/O Block Diagram

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I/O Block

Separate from the macrocell array is the I/O control block of the LAB. *Figure 6* shows the I/O block diagram. The three-state buffer is controlled by a macrocell product term and the drives the I/O pad. The input of this buffer comes from a macrocell within the associated LAB. The feedback path from the I/O pin may feed other blocks within the LAB, as well as the PIA. By decoupling the I/O pins from the flip-flops, all the registers in the LAB are "buried," allowing the I/O pins to be used as dedicated outputs, bidirectional outputs, or as additional dedicated inputs. Therefore, applications requiring many buried flip-flops, such as counters, shift registers, and state machines, no longer consume both the macrocell register and the associated I/O pin, as in earlier devices.

The Programmable Interconnect Array

PLD density and speed has traditionally been limited by signal routing; i.e., getting signals from one macrocell to another. For smaller devices, a single array is used and all signals are available to all macrocells. But as the devices increase in density, the number of signals being routed becomes very large, increasing the amount of silicon used for interconnections. Also, because the signal must be global, the added loading on the internal connection path reduces

the overall speed performance of the device. The MAX architecture solves these problems. It is based on the concept of small, flexible logic array blocks that, in the larger devices, are interconnected by a PIA.

The PIA solves interconnect limitations by routing only the signals needed by each LAB. The architecture is designed so that every signal on the chip is within the PIA. The PIA is then programmed to give each LAB access to the signals that it requires. Consequently, each LAB receives only the signals needed. This effectively solves any routing problems that may arise in a design without degrading the performance of the device. Unlike masked or programmable gate arrays, which induce variable delays dependent on routing, the PIA has a fixed delay from point to point. This eliminates undesired skews among logic signals, which may cause glitches in internal or external logic.

Development Software Support

Warp

Warp is a state-of-the-art compiler and complete CPLD design tool. For design entry, *Warp* provides an IEEE-STD-1076/1164 VHDL text editor, an IEEE-STD-1364 Verilog text editor and a graphical finite state machine editor. It provides optimized synthesis and fitting by replacing basic circuits with ones pre-optimized for the target device, by implementing logic in unused memory and by perfect communication between fitting and synthesis. *Warp* provides other tools such as graphical timing simulation and analysis.

Warp Professional

Warp Professional contains several additional features. It provides an extra method of design entry with its graphical block diagram editor. It allows up to 5 ms timing simulation instead of only 2 ms. It allows comparing of waveforms before and after design changes.

Warp Enterprise

Warp Enterprise provides even more features. It provides unlimited timing simulation and source-level behavioral simulation as well as a debugger. It has the ability to generate graphical HDL blocks from HDL text. It can even generate testbenches.

Warp is available for PC and UNIX platforms. Some features are not available in the UNIX version. For further information see the *Warp* for PC*, Warp* for UNIX, *Warp* Professional and *Warp* Enterprise datasheets.

Third-Party Software

Although *Warp* is a complete CPLD development tool on its own, it interfaces with nearly every third party EDA tool. All major third-party software vendors provide support for the MAX family of devices. To expedite this support, Cypress supplies vendors with all pertinent architectural information as well as design fitters for our products.

Programming

The *Impulse3*™ device programmers from Cypress will program all Cypress PLDs, CPLDs, FPGAs, and PROMs. The unit is a standalone programmer that connects to any IBM-compatible PC via the printer port.

Third-Party Programmers

As with development software, Cypress strongly supports third-party programmers. All major third-party programmers support the MAX family.

Cross Reference

ALTERA	CYPRESS
PREFIX EPM	PREFIX: CY
PREFIX: EP	PREFIX: PALC
22V10–10C	PALC22V10D–7C
22V10–10C	PALC22V10D–10C
22V10–10C	PAL22V10C–7C+
22V10–10C	PAL22V10C–10C+
22V10–15C	PALC22V10B–15C
22V10–15C	PALC22V10D–15C
5032DC	7C344–25WC
5032DC–2	7C344–20WC
5032DC–15	7C344–15WC
5032DC–17	Call Factory
5032DC–20	7C344–20WC
5032DC–25	7C344–25WC
5032DM	7C344–25WMB
5032DM–25	7C344–25WMB
5032JC	7C344–25HC
5032JC–2	7C344–20HC
5032JC–15	7C344–15HC
5032JC–17	Call Factory
5032JC–20	7C344–20HC

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Cross Reference (continued)

ALTERA	CYPRESS
5032JC–25	7C344–25HC
5032JM	7C344–25HMB
5032JM–25	7C344–25HMB
5032LC	7C344–25JC
5032LC–2	7C344–20JC
5032LC–15	7C344–15JC
5032LC–17	Call Factory
5032LC–20	7C344–20JC
5032LC–25	7C344–25JC
5032PC	7C344–25PC
5032PC–2	7C344–20PC
5032PC–15	7C344–15PC
5032PC–17	Call Factory
5032PC–20	7C344–20PC
5032PC–25	7C344–25PC
5064JC	7C343–35HC
5064JC–1	7C343–25HC
5064JC–2	7C343–30HC
5064JI	7C343–35HI
5064JM	7C343–35HMB
5064LC	7C343–35JC
5064LC–1	7C343–25JC
5064LC–2	7C343–30JC
5128AGC–12	7C342B–12RC
5128AGC–15	7C342B–15RC
5128AGC–20	7C342B–20RC
5128AJC–12	7C342B–12HC
5128AJC–15	7C342B–15HC
5128AJC–20	7C342B–20HC
5128ALC–12	7C342B–12JC
5128ALC–15	7C342B–15JC
5128ALC–20	7C342B–20JC
5128GC	7C342–35RC
5128GC–1	7C342–25RC
5128GC–2	7C342–30RC
5128GM	7C342–35RMB
5128JC	7C342–35HC
5128JC–1	7C342–25HC
5128JC–2	7C342–30HC
5128JI	7C342–35HI
5128JI–2	7C342–30HI
5128JM	7C342–35HMB
5128LC	7C342–35JC
5128LC–1	7C342–25JC

Cross Reference (continued)

ALTERA	CYPRESS
5128LC–2	7C342–30JC
5128LI	7C342–35JI
5128LI–2	7C342–30HI
5130GC	7C346–35RC
5130GC–1	7C346–25RC
5130GC–2	7C346–30RC
5130GM	7C346–35RM
5130JC	7C346–35HC
5130JC–1	7C346–25HC
5130JC–2	7C346–30HC
5130JM	7C346–35HM
5130LC	7C346–35JC
5130LC–1	7C346–25JC
5130LC–2	7C346–30JC
5130LI	7C346–35JI
5130LI–2	7C346–30JI
5130QC	7C346–35NC
5130QC–1	7C346–25NC
5130QC–2	7C346–30NC
5130QI	7C346–35NI
5192AGC–15	7C341B–15RC
5192AGC–20	7C341B–20RC
5192AJC–15	7C341B–15HC
5192AJC–20	7C341B–20HC
5192ALC–1	7C341B–15JC
5192ALC–2	7C341B–20JC
5192GC	7C341–35RC
5192GC–1	7C341–25RC
5192GC–2	7C341–30RC
5192JM	7C341–35HM
5192JC	7C341–35HC
5192JC–1	7C341–25HC
5192JC–2	7C341–30HC
5192GM	7C341–35RM
5192JI	7C341–35HI
5192LC	7C341–35JC
5192LC–1	7C341–25JC
5192LC–2	7C341–30JC

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