Intel® 80960KA/KB

Specification Update

August 2004

Notice: The Intel® 80960KA/KB may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this specification update.

Order Number: 272851-004

Contents

Revision History

Intel has manufactured the Intel® 80960KA/KB under two series of steppings, known respectively as "Non-Shrink" and "Shrink" to denote manufacturing processes. Intel currently manufactures all 80960KA/KB devices using the "Shrink" Process 648. Therefore, the complete name of the C stepping is "Shrink C" stepping.

The C stepping corrected a number of errata and incorporated other changes to improve manufacturability in plastic packages. Minor changes have since been made via segmentation and metal line organization for manufacturability. There have been no further logic modifications.

Date	Version	Description
8/20/04	004	To address the fact that many of the package prefix variables have changed, all package prefix variables in this document are now indicated with an "x".
6/07/00	003	Removed EOLed devices from Table 1.
6/30/97	002	Added Errata #4. Added Document Change #1. Added Document Change #2.
07/01/96	001	This is the new Specification Update document. It contains all identified errata published prior to this date.

Preface

As of July, 1996, Intel's Computing Enhancement Group has consolidated available historical device and documentation errata into this new document type called the Specification Update. We have endeavored to include all documented errata in the consolidation process, however, we make no representations or warranties concerning the completeness of the Specification Update.

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Order
Electrical specifications for these products are found in the following documents:	
80960KA Embedded 32-Bit Processor datasheet	270775
80960KB Embedded 32-Bit Processor with Integrated Floating-Point Unit datasheet	270565
Functional descriptions for these products are found in the following documents:	
i960® KA/KB Microprocessor Programmer’s Reference Manual	270567
80960KB Hardware Designer’s Reference Manual	270564

Nomenclature

Errata are design defects or errors. These may cause the Product Name's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

Note: Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the Product Name product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

▌	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

No.	Steppings				Page	Status	Errata
	A	B	C	C-2			
1			X		10	NoFix	ALE# Does Not Function in Secondary Bus Master Mode
2			X		10	NoFix	Problem Using HLDA and ADS# with Asynchronous Logic
3			X		10	NoFix	Breakpoint Register Initialization
4	X	X	X	X	11	NoFix	Undocumented Register Flushes on Interrupt Return for the 80960KA/KB Microprocessors

Specification Changes

No.	Steppings		Page	Status	Specification Changes
	A	B			
					None for this revision of this specification update.

Specification Clarifications

No.	Steppings			Page	Status	Specification Clarifications
	#	#	#			
						None for this revision of this specification update.

Documentation Changes

No.	Document Revision	Page	Status	Documentation Changes
1	270775-005 270565-007	14		Page 8, Table 3
2	270775-005 270565-007	14		Page 22, Figure 18

Identification Information

Markings

As of January 1994, all 80960KA/KB, x80960KA/KB, x80960KA/KB, and x80960KA devices will be marked with stepping numbers.

Unless otherwise documented, 80960KA/KB devices marked with other specification numbers belong to different steppings. Be sure you have a correct technical bulletin for the devices at hand.

Stepping Register

Table 1 applies to all C stepping devices:

Table 1. Identification Information for All C Stepping Devices

Part Number	Specification Number	Package	Status
x80960KA	C	PGA-132	Current
x80960KB	C	PGA-132	Current
x80960KA	C	PGA-132 Extended Temp.	Current
x80960KB	C	PGA-132 Extended Temp.	Current
x80960KA	C	PQFP-132	Current
x80960KB	C	PQFP-132	Current
x80960KA	C	PQFP-132 Extended Temp	Current
x80960KB	C	PQFP-132 Extended Temp	Current

Notes: 1. Refer to the 80960KA Datasheet (270775) and the 80960KB Datasheet (270565) for specifics on frequency offerings.

2. To address the fact that many of the package prefix variables have changed, all package prefix variables in this document are now indicated with an "x".

Errata

1. ALE# Does Not Function in Secondary Bus Master Mode

Problem: When two 80960KA/KB processors share the same local bus in a Primary Bus Master (PBM)/ Secondary Bus Master (SBM) relationship, ALE# does not work on the Secondary Bus Master.

Implication: This erratum effectively makes "bus re-enter" operation impossible.

Workaround: None.

Status: NoFix. Refer to Summary Table of Changes to determine the affected stepping(s).

2. Problem Using HLDA and ADS# with Asynchronous Logic

Problem: Asynchronous logic connected to the HLDA and ADS# pins may malfunction due to ground bounce on these outputs. The problem occurs when address/data buffers switch from a high state to a low state.

This problem exists on devices in both the PGA and PQFP packages. On the 80960KA/KB device, the LAD bus buffers share a ground with the buffers for the ADS#, HLDA, DT/R#, W/R#, ALE#, BE2#, BE1#, BE0#, CACHE and INTA pins. In addition to ground bounce on the ADS# and HLDA pins, it may be possible to observe ground bounce, undershoot and overshoot on other pins from this group.

The problem depends on how many outputs switch, proximity to the switching outputs and proximity to ground pads on the die. The worst case situation occurs when all address/data outputs switch simultaneously.

Implication: None.

Workaround: Logic external to the 80960KA/KB processor should sample HLDA synchronously on an "A" or "D" clock edge. ADS# can be sampled synchronously on an "A", "C", or "D" clock edge. Check setup and hold times carefully.

All 80960KA/KB processor designs must consider good power and ground distribution and decoupling techniques. As with all i960 family designs, a multi-layer circuit board is recommended. Use of a multi-layer board will not eliminate this problem, but may lessen its effects.

Status: NoFix. Refer to Summary Table of Changes to determine the affected stepping(s).

3. Breakpoint Register Initialization

Problem: There are two breakpoint registers on the 80960Kx. These registers can be written using the Set Breakpoint Register IAC only, and they cannot be read. Bits 2-31 of the register contain the address on which to break, and bit 1 enables or disables the breakpoint. These registers are not set to a specific value during initialization, and may be enabled upon powerup. This could cause sporadic breakpoints to occur if tracing is enabled in the process controls and breakpoint trace mode is enabled in the trace controls.

Implication: This errata does not affect the normal function of the breakpoint registers.

Workaround: Disable breakpoints using Set Breakpoint Register IAC to set bit 1 of both registers to 1. Alternatively, if breakpoints are not being used, do not set breakpoint trace mode bit in the trace controls.

Status: NoFix. Refer to Summary Table of Changes to determine the affected stepping(s).

4. Undocumented Register Flushes on Interrupt Return for the 80960KA/KB Microprocessors

Problem: The 80960Kx processors may execute unnecessary local register set flushes on interrupt return. The flushes occur when the working register belongs to an interrupt service routine (isr), and a *return* instruction is executed. The interrupt return flushes every register set in the cache excluding the set belonging to the procedure that was interrupted.

Example One: (A) function #1 is the only register set in the cache and is interrupted by isr #1. (B) on the return from interrupt, the function #1 register set is reinstated as the working set with no sets flushed to the stack.

Example Two: (A) function #1 calls function #2, which calls function #3; function #3 is interrupted by isr #1. On the return from interrupt, function #1 and function #2 are flushed to the stack. (B) function #3 is reinstated as the working register set.

Example Three: (A) function #3 is interrupted by isr #1 which is interrupted by an isr of higher priority, isr #2. On return from interrupt, function #3 is flushed to the procedure stack. Isr #1 is reinstated as the working register. (B) On the interrupt return from isr #1, there are no sets in the cache to flush. (C) The processor must perform a register cache fill from the procedure stack.

Notice that on return from the only active isr, the working register set belongs to the first interrupted procedure and the remainder of the cache is invalid.

Implication: The flushes are transparent to the user; however, they will cause an unexpected increase in interrupt latency.

Workaround: Accommodate the longer interrupt return latency. Otherwise, prevent any combination of nested functions and/or interrupts.

Status: NoFix. Refer to Summary Table of Changes to determine the affected stepping(s).

Specification Changes

None for this revision of this specification update.

Specification Clarifications

None for this revision of this specification update.

Documentation Changes

1. Page 8, Table 3

Issue: $\overline{\text{DEN}}$ pin description omitted.

Affected Docs: *80960KA Embedded 32-Bit Microprocessor* Data Sheet, #270775-005 and *80960KB Embedded 32-Bit Microprocessor with Integrated Floating-Point Unit* Data Sheet, #270565-007.

2. Page 22, Figure 18

Issue: Pins M2 and M13 are incorrectly shown:

"M2 was NC and M13 was V_{CC}"

The corrected text shows:

"M2 is V_{CC} and M13 is NC"

Affected Docs: *80960KA Embedded 32-Bit Microprocessor* Data Sheet, #270775-005 and *80960KB Embedded 32-Bit Microprocessor with Integrated Floating-Point Unit* Data Sheet, #270565-007.