MC14001B Series

B-Suffix Series CMOS Gates

MC14001B, MC14011B, MC14023B, MC14025B, MC14071B, MC14073B, MC14081B, MC14082B

The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

Features

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low–power TTL Loads or One Low–power Schottky TTL Load Over the Rated Temperature Range.
- Double Diode Protection on All Inputs Except: Triple Diode Protection on MC14011B and MC14081B
- Pin-for-Pin Replacements for Corresponding CD4000 Series B Suffix Devices
- Pb–Free Packages are Available*

MAXIMUM RATINGS (Voltages Referenced to VSS)

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage Range	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage Range (DC or Transient)	–0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
PD	Power Dissipation, per Package (Note 1)	500	mW
T _A	Ambient Temperature Range	-55 to +125	°C
T _{stg}	Storage Temperature Range	-65 to +150	°C
TL	Lead Temperature (8–Second Soldering)	260	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Temperature Derating:

Plastic "P and D/DW" Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in} \text{ or } V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



ON Semiconductor[®]

http://onsemi.com

		MARKING DIAGRAMS
	PDIP-14 P SUFFIX CASE 646	14 A A A A A A A A MC140xxBCP O AWLYYWW V V V V V V V 1
Sectored.	SOIC-14 D SUFFIX CASE 751A	¹⁴ ∄ ∄ ∄ ∄ ∄ ∄ ∄ ∄ ∄ 140xxB <u>○ AWLYWW</u> 1 월 8 8 8 8 8 8
and the second s	TSSOP-14 DT SUFFIX CASE 948G	14 14 0xxB • ALYW 1000000
Period Mark	SOEIAJ-14 F SUFFIX CASE 965	14 MC140xxB AWLYWW 1
xx A WL, L YY, Y	= Specific = Assembl = Wafer Lo = Year	

- YY, Y = Year
- WW, W = Work Week

DEVICE INFORMATION

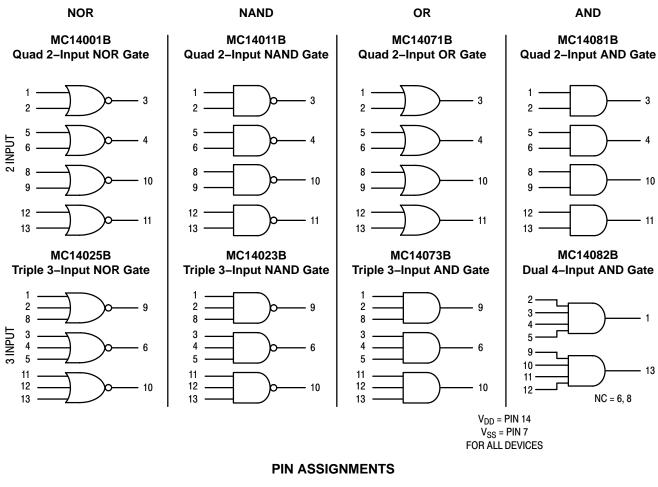
Device	Description
MC14001B	Quad 2–Input NOR Gate
MC14011B	Quad 2–Input NAND Gate
MC14023B	Triple 3–Input NAND Gate
MC14025B	Triple 3–Input NOR Gate
MC14071B	Quad 2–Input OR Gate
MC14073B	Triple 3–Input AND Gate
MC14081B	Quad 2–Input AND Gate
MC14082B	Dual 4–Input AND Gate

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

MC14001B Series

LOGIC DIAGRAMS



	MC1400 2–Input		Gate	Quad 2	MC14011 -Input N		D Gate	Triple 3		C14023B nput NAN	D Gate	Triple		14025B put NOF	R Gate
IN 1 _A [1•	14 🛛	V _{DD}	in 1 _a C	1•	14	0 v _{dd}	in 1 _a C	1	• 14] v _{dd}	in 1 _a C	1•	14	D v _{dd}
IN 2 _A [2	13 🛛	IN 2 _D	IN 2 _A [2	13] IN 2 _D	IN 2 _A [2	13] IN 3 _C	IN 2 _A [2	13] IN 3 _C
OUT _A [3	12	IN 1 _D	OUT _A [3	12] IN 1 _D	IN 1 _B [3	12] IN 2 _C	IN 1 _B [3	12] IN 2 _C
out _b [4	11	OUTD	OUT _B [4	11] OUT _D	IN 2 _B [4	11] IN 1 _C	IN 2 _B [4	11] IN 1 _C
IN 1 _B [5	10	OUT _C	IN 1 _B [5	10] оит _с	in 3 _b [5	10] OUT _C	in 3 _b [5	10] OUT _C
IN 2 _B [6	9 🛛	IN 2 _C	IN 2 _B	6	9] IN 2 _C	out _b [6	9] OUT _A	out _b [6	9] OUT _A
v _{ss} [7	8]	IN 1 _C	v _{ss} E	7	8	IN 1 _C	v _{ss} E	7	8] IN 3 _A	v _{ss} [7	8] IN 3 _A

Quad	Tri			
in 1 _a C	1•	14	D V _{DD}	IN
IN 2 _A [2	13] IN 2 _D	IN
out _a [3	12] IN 1 _D	IN
out _b [4	11] OUT _D	IN
IN 1 _b [5	10] оит _с	IN
IN 2 _B [6	9] IN 2 _C	OU
v _{ss} [7	8] IN 1 _C	۷

MC14073B Triple 3–Input AND Gate								
in 1 _a C	1•	14	D v _{dd}					
IN 2 _A [2	13] IN 3 _C					
IN 1 _B [3	12] IN 2 _C					
IN 2 _B [4	11] IN 1 _C					
in 3 _b [5	10] оит _с					
out _b [6	9] OUT _A					
v _{ss} [7	8	IN 3 _A					

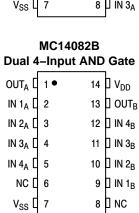
-							
MC14081B Quad 2–Input AND Gate							
in 1 _a [1•	14] v _{dd}				
IN 2 _A [2	13					
out _a [3	12] IN 1 _D				
out _b [4	11]out _d				
in 1 _b [5	10]out _c				

9 |] IN 2_C

8 | IN 1_C

IN 2_B [6

V_{SS} [7



NC = NO CONNECTION