DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD75004, 75006, 75008

4-BIT SINGLE-CHIP MICROCOMPUTER

DESCRIPTION

The μPD75008 is one of the 75X Series 4-bit single-chip microcomputer.

In addition to high-speed operation with 0.95 μs minimum instruction execution time for the CPU, the μPD75008 employs a serial bus interface with standard NEC format, the μPD75004 is a powerful product with a high cost/performance ratio.

The μPD75P008 with PROM, which is provided with μPD75008, is applicable for evaluating systems under development, or for small-scale production of developed systems.

Detailed functions are described in the following user's manual. Be sure to read it for designing.
μPD7500X Series User's Manual: IEM-5033

FEATURES

- Capable of high-speed operation and variable instruction execution time to power save
  - 0.95 μs, 1.91 μs, 15.3 μs (Main system clock: operating at 4.19 MHz)
  - 122 μs (Subsystem clock: operating at 32.768 kHz)
- 75X architecture comparable to that for an 8-bit microcomputer is employed
- Built-in NEC standard serial bus interface (SBI)
- Clock operation at reduced power dissipation (5 μA TYP. : operating at 3 V)
- Enhanced timer function (3 channels)
- Interrupt functions especially enhanced for applications, such as remote control receiver

APPLICATIONS

VCRs, CD players, telephones, cameras, blood pressure gauges, etc.

Unless otherwise specified, μPD75008 is treated as the representative model throughout this manual.

The information in this document is subject to change without notice.

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Date Published November 1993 P
Printed in Japan.

The mark ★ shows major revised points.

ORDERING INFORMATION

Part Number	Package	Quality Grade
μPD75004CU-xxx	42-pin plastic shrink DIP (600 mil)	Standard
μPD75004GB-xxx-3B4	44-pin plastic QFP (□10 mm)	Standard
μPD75006CU-xxx	42-pin plastic shrink DIP (600 mil)	Standard
μPD75006GB-xxx-3B4	44-pin plastic QFP (□10 mm)	Standard
μPD75008CU-xxx	42-pin plastic shrink DIP (600 mil)	Standard
μPD75008GB-xxx-3B4	44-pin plastic QFP (□10 mm)	Standard

Remarks: xxx is ROM code number.

Please refer to "Quality Grade on NEC Semiconductor Devices" (Document Number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

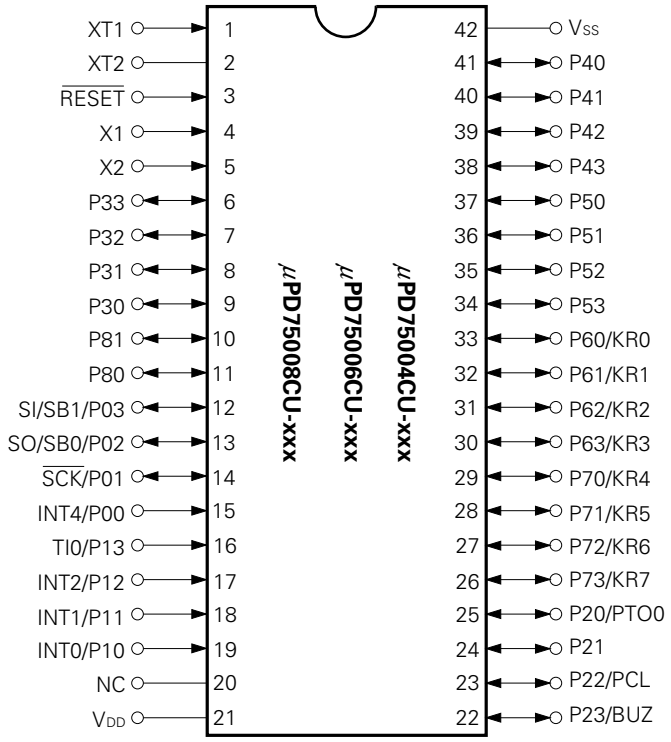
FUNCTIONAL OUTLINE

Item		Function			
Instruction Execution Time		0.95, 1.91, and 15.3 μs, (Main system clock: operating at 4.19 MHz) 122 μs (Subsystem clock: operating at 32.768 kHz)			
Internal Memory	ROM	4096 × 8-bit (μPD75004)			
		6016 × 8-bit (μPD75006)			
		8064 × 8-bit (μPD75008)			
	RAM	512 × 4-bit			
General-Purpose Registers		• 4-bit manipulation: 8 • 8-bit manipulation: 4			
I/O Port		34	8	CMOS Input pins	Internal pull-up resistor specification by software is possible. : 25
			18	CMOS input/output pins Can directly drive LED: 4	
			8	N-ch open-drain input/output Can directly drive LED: 8	Withstand voltage: 10V Internal pull-up resistor specification by mask option is possible.
Timer		3 chs	Timer/event counter Basic interval timer: Also serves as watchdog timer Watch timer: Buzzer output possible		
Serial Interface		3-line serial I/O mode 2-line serial I/O mode SBI mode			
Bit Sequential Buffer		16 bits			
Clock Output Function		Φ, $f_X/2^3$, $f_X/2^4$, $f_X/2^6$			
Vector Interrupt		External: 3, Internal: 3			
Test Input		External: 1, Internal: 1			
System Clock Oscillator		Main system clock oscillation ceramic/crystal oscillator Subsystem clock oscillation crysal ocillator			
Standby Function		STOP/HALT mode			
Operating Temperature Range		–40 to +85°C			
Operating Supply Voltage		2.7 to 6.0 V			
Package		42-pin plastic shrink DIP (600 mil) 44-pin plastic QFP (□10 mm)			

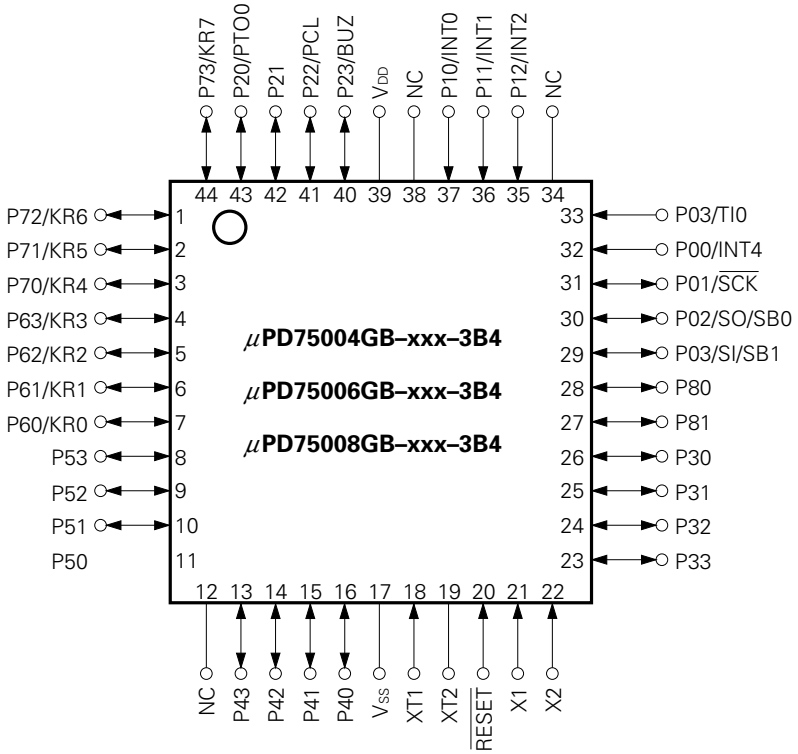
CONTENTS

1. PIN CONFIGURATION (Top View)

• 42-pin plastic shrink DIP (600 mil)

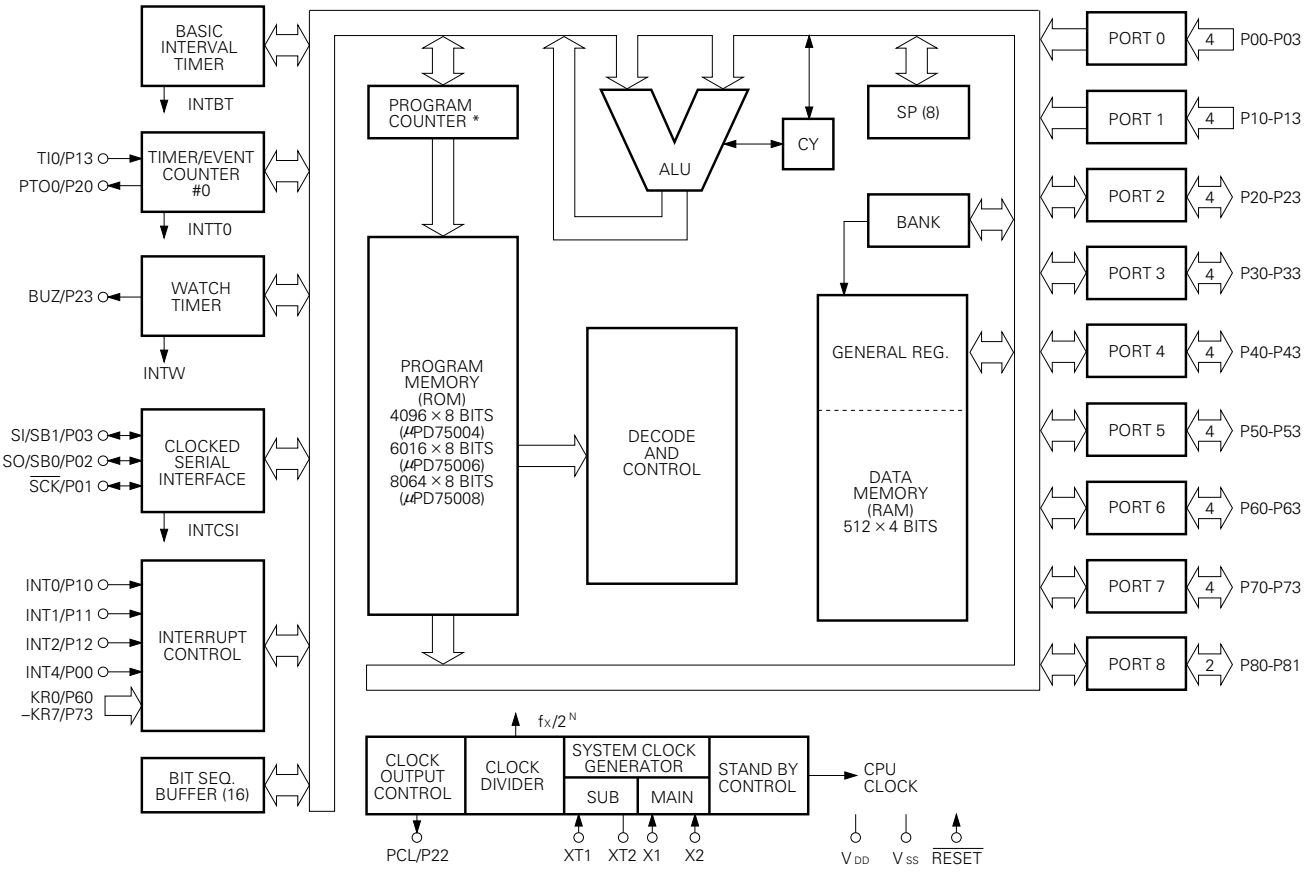


• 44-pin plastic QFP (□ 10 mm)



Pin names

P00-P03	: Port 0	SO	: Serial Output
P10-P13	: Port 1	SB0,SB1	: Serial Bus 0,1
P20-P23	: Port 2	$\overline{\text{RESET}}$	: Reset Input
P30-P33	: Port 3	TI0	: Timer Input 0
P40-P43	: Port 4	PTO0	: Programmable Timer Output 0
P50-P53	: Port 5	BUZ	: Buzzer Clock
P60-P63	: Port 6	PCL	: Programmable Clock
P70-P73	: Port 7	INT0, 1, 4	: External Test Interrupt 0,1,4
P80-P81	: Port 8	INT2	: External Test Input 2
KR0-KR7	: Key Return	X1, 2	: Main System Clock Oscillation 1,2
$\overline{\text{SCK}}$	: Serial Clock	XT1, 2	: Subsystem Clock Oscillation 1,2
SI	: Serial Input	NC	: No Connection



*: For μPD75004, 12 bits. For μPD75006 and μPD75008, 13 bits.

3. PIN FUNCTIONS

3.1 PORT PINS (1/2)

Pin Name	Input/Output	Also Served As	Function	8-Bit I/O	When Reset	Input/ Output Circuit TYPE*1
P00	Input	INT4	4-bit input port (PORT0) Pull-up resistors can be specified in 3-bit units for the P01 to P03 pins by software.	X	Input	Ⓑ
P01	Input/ Output	$\overline{\text{SCK}}$				Ⓕ-A
P02	Input/ Output	SO/SB0				Ⓕ-B
P03	Input/ Output	SO/SB1				Ⓜ-C
P10	Input	INT0	With noise elimination function	X	Input	Ⓑ-C
P11		INT1	4-bit input port (PORT1) Internal pull-up resistors can be specified in 4-bit units by software.			
P12		INT2				
P13		TI0				
P20	Input/ Output	PTO0	4-bit input/output port (PORT2) Internal pull-up resistors can be specified in 4-bit units by software.	X	Input	E-B
P21		—				
P22		PCL				
P23		BUZ				
P30*2	Input/ Output	—	Programmable 4-bit input/output port (PORT3) This port can be specified for input/ output in bit units. Internal pull-up resistors can be specified in 4-bit units by software.	X	Input	E-B
P31*2		—				
P32*2		—				
P33*2		—				
P40-43*2	Input/ Output	—	N-ch open-drain 4-bit input/output port (PORT4) Internal pull-up resistors can be specified in bit units. (mask option) Resistive voltage is 10 V in the open-drain mode.	○	High level (with internal pull-up resistor) or high impedance	M
P50-53*2	Input/ Output	—	N-ch open-drain 4-bit input/output port (PORT5) Internal pull-up resistors can be specified in bit units. (mask option) Resistive voltage is 10 V in the open-drain mode.		High level (with internal pull-up resistor) or high impedance	M

*1: Circles indicate Schmitt trigger inputs.

2: Can directly drive LED.

3.1 PORT PINS (2/2)

Pin Name	Input/Output	Also Served As	Function	8-Bit I/O	When Reset	Input/ Output Circuit TYPE*1
P60	Input/ Output	KR0	Programmable 4-bit input/output port (PORT6) This port can be specified for input/ output in bit units. Internal pull-up resistors can be specified in 4-bit units by software.	○	Input	Ⓕ-A
P61		KR1				
P62		KR2				
P63		KR3				
P70	Input/ Output	KR4	4-bit input/output port (PORT7) Internal pull-up resistors can be specified in 4-bit units by software.		Input	Ⓕ-A
P71		KR5				
P72		KR6				
P73		KR7				
P80	Input/ Output	—	2-bit input/output port (PORT8) Internal pull-up resistors can be specified in 2-bit units by software.	X	Input	E-B
P81		—				

*1: Circles indicate Schmitt trigger inputs.

2: Can directly drive LED.

3.2 NON PORT PINS

Pin Name	Input/Output	Also Served As	Functon		When Reset	Input/ Output Circuit TYPE*1
TI0	Input	P13	Timer/event counter external event pulse Input		Input	Ⓑ-C
PTO0	Input/ Output	P20	Timer/event counter output		Input	E-B
PCL	Input/ Output	P22	Clock output		Input	E-B
BUZ	Input/ Output	P23	Fixed frequency output (for buzzer or for trimming the system clock)		Input	E-B
$\overline{SCK}$	Input/ Output	P01	Serial clock input/output		Input	Ⓕ-A
SO/SB0	Input/ Output	P02	Serial data output Serial bus input/output		Input	Ⓕ-B
SI/SB1	Input/ Output	P03	Serial data input Serial bus input/output		Input	Ⓜ-C
INT4	Input	P00	Edge detection vector interrupt input (both rising and falling edge detection are effective)		Input	Ⓑ
INT0	Input	P10	Edge detection vector interrupt input (detection edge can be selected)	Clock synchronous	Input	Ⓑ-C
INT1		P11		Asynchronous		
INT2	Input	P12	Edge detection testable input (rising edge detection)	Asynchronous	Input	Ⓑ-C
KR0-KR3	Input/ Output	P60-P63	Parallel falling edge detection testable input		Input	Ⓕ-A
KR4-KR7	Input/ Output	P70-P73	Parallel falling edge detection testable input		Input	Ⓕ-A
X1, X2	Input	—	To connect the crystal/ceramic oscillator to the main system clock generator. When inputting the external clock, input the external clock to pin X1, and the reverse phase of the external clock to pin X2.		Input	—
XT1	Input	—	To connect the crystal oscillator to the subsystem clock generator. When the external clock is used, pin XT1 inputs the external clock. In this case, pin XT2 must be left open.		Input	—
XT2	—				—	
$\overline{RESET}$	Input	—	System reset input		—	Ⓑ
NC *2	—	—	No connection		—	—
V_{DD}	—	—	Positive power supply		—	—
V_{SS}	—	—	GND		—	—

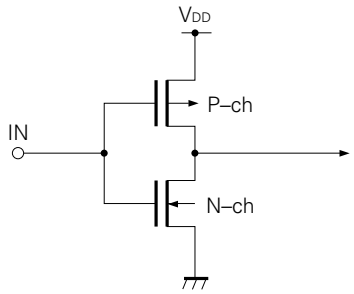
*1: Circles indicate Schmitt trigger inputs.

2: When sharing the printed circut board with the μPD75P008, the NC pin must be directly connected to V_{DD}.

3.3 PIN INPUT/OUTPUT CIRCUITS

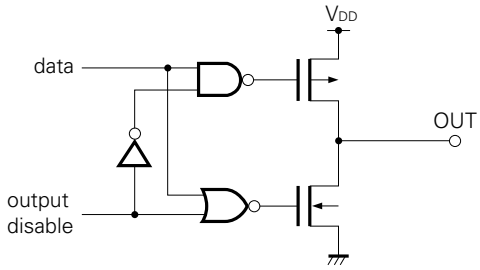
The following shows a simplified input/output circuit diagram for each pin of the μPD75008.

TYPE A (for TYPE E–B)



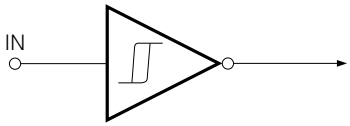
Input buffer of CMOS standard

TYPE D (for TYPE E–B, F–A)



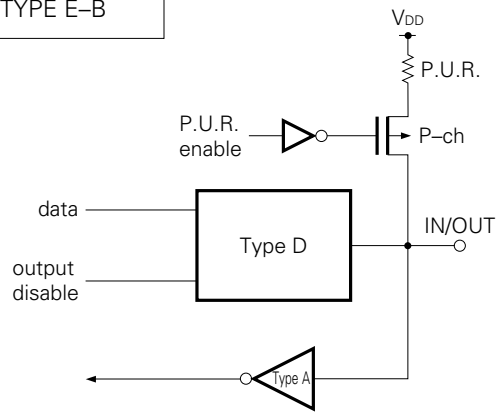
Push–pull output that can be set in a output high–impedance state (both P–ch and N–ch are off)

TYPE B



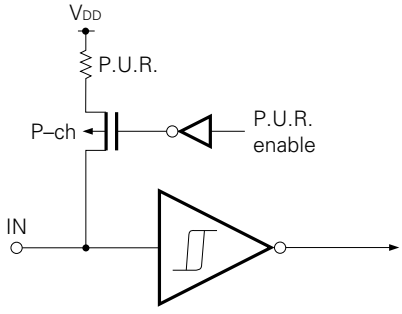
Schmitt trigger input with hysteresis characteristics

TYPE E–B



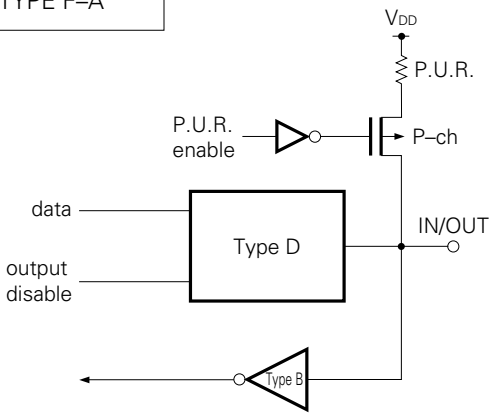
P.U.R. : Pull–Up Resistor

TYPE B–C

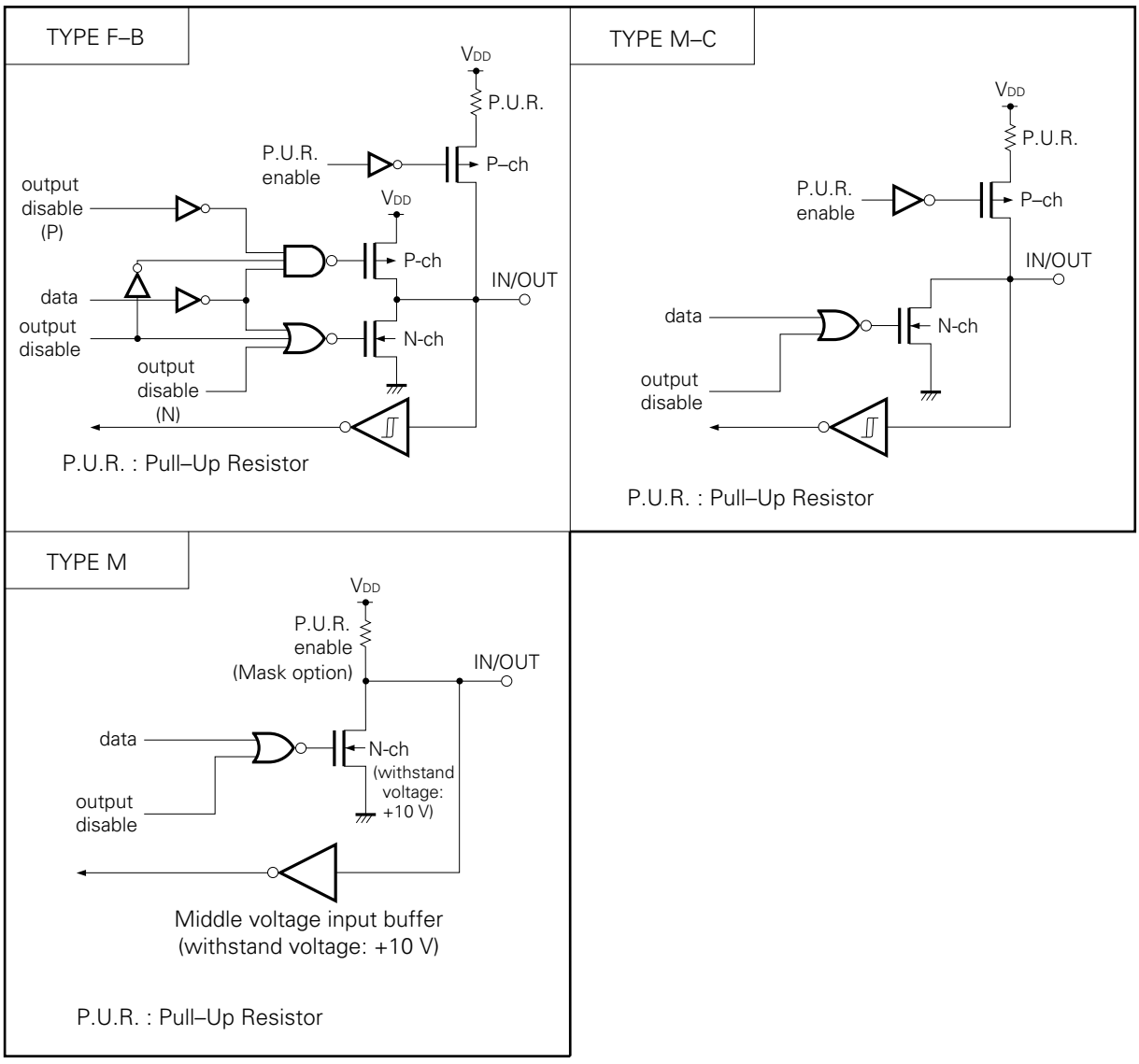


P.U.R. : Pull–Up Resistor

TYPE F–A



P.U.R. : Pull–Up Resistor



3.4 SELECTION OF MASK OPTION

The following mask operations are available and can be specified for each pin.

Table 3-1 Mask Option Selection

Pin	Mask Option	
P40-P43, P50-P53	• With pull-up resistor	• Without pull-up resistor

*: Mask option can be specified in bit units.

★ 3.5 RECOMMENDED PROCESSING OF UNUSED PINS

Table 3-2 Processing of Unused Pins

Pin	Recommended Connections
P00/INT4	Connect to V_{SS}
P01/$\overline{SCK}$	Connect to V_{SS} or V_{DD}
P02/SO/SB0	
P03/SI/SB1	
P10/INT0-P12/INT2	Connect to V_{SS}
P13/TI0	
P20/PTO0	Input : Connect to V_{SS} or V_{DD} Output: Open
P21	
P22/PCL	
P23/BUZ	
P30-P33	
P40-P43	
P50-P53	
P60-P63	
P70-P73	
P80-P81	
XT1	Connect to V_{SS} or V_{DD}
XT2	Open

3.6 NOTES ON USING THE P00/INT4, AND $\overline{\text{RESET}}$ PINS ★

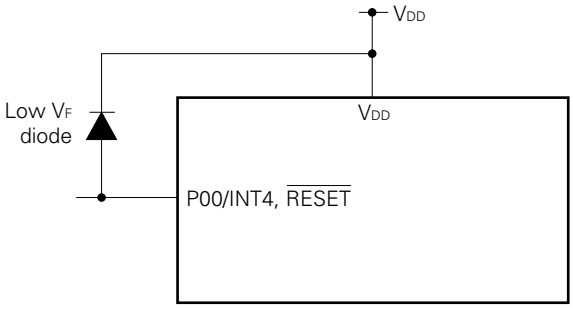
In addition to the functions described in Sections 3.1 PORT PINS and 3.2 NON PORT PINS, an exclusive function for setting the test mode, in which the internal fuctions of the μPD75008 are tested (solely used for IC tests), is provided to the P00/INT4 and $\overline{\text{RESET}}$ pins.

If a voltage exceeding V_{DD} is applied to either of these pins, the μPD75008 is put into test mode. Therefore, even when the μPD75008 is in normal operation, if noise exceeding the V_{DD} is input into any of these pins, the μPD75008 will enter the test mode, and this will cause problems for normal operation.

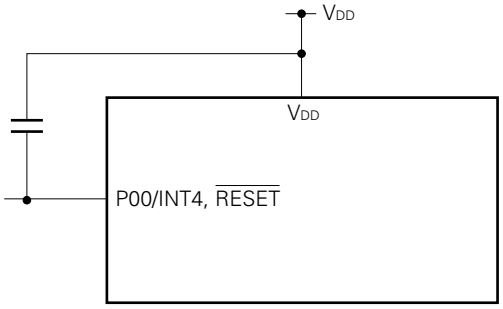
As an example, if the wiring to the P00/INT4 pin or the $\overline{\text{RESET}}$ pin is long, stray noise may be picked up and the above montioned problem may occur.

Therefore, all wiring to these pins must be made short enough to not pick up stray noise. If noise cannot be avoided, suppress the noise using a capacitor or diode as shown in the figure below.

- Connect a diode having a low V_F across P00/INT4 and $\overline{\text{RESET}}$, and V_{DD}. (0.3 V max.)



- Connect a capacitor across P00/INT4 and $\overline{\text{RESET}}$, and V_{DD}.



4. MEMORY CONFIGURATION

- Program memory (ROM) ... 4096 × 8 bits (0000H-0FFFH) : μPD75004
  ... 6016 × 8 bits (0000H-177FH) : μPD75006
  ... 8064 × 8 bits (0000H-1F7FH) : μPD75008
  - 0000H-0001H: Vector table to which address from which program is started is written after reset
  - 0002H-000BH: Vector table to which address from which program is started is written after interrupt
  - 0020H-007FH: Table area referenced by GETI instruction

- Data memory (RAM)
  - Data area .... 512 × 4 bits (000H–1FFH)
  - Peripheral hardware area .... 128 × 4 bits (F80H–FFFH)

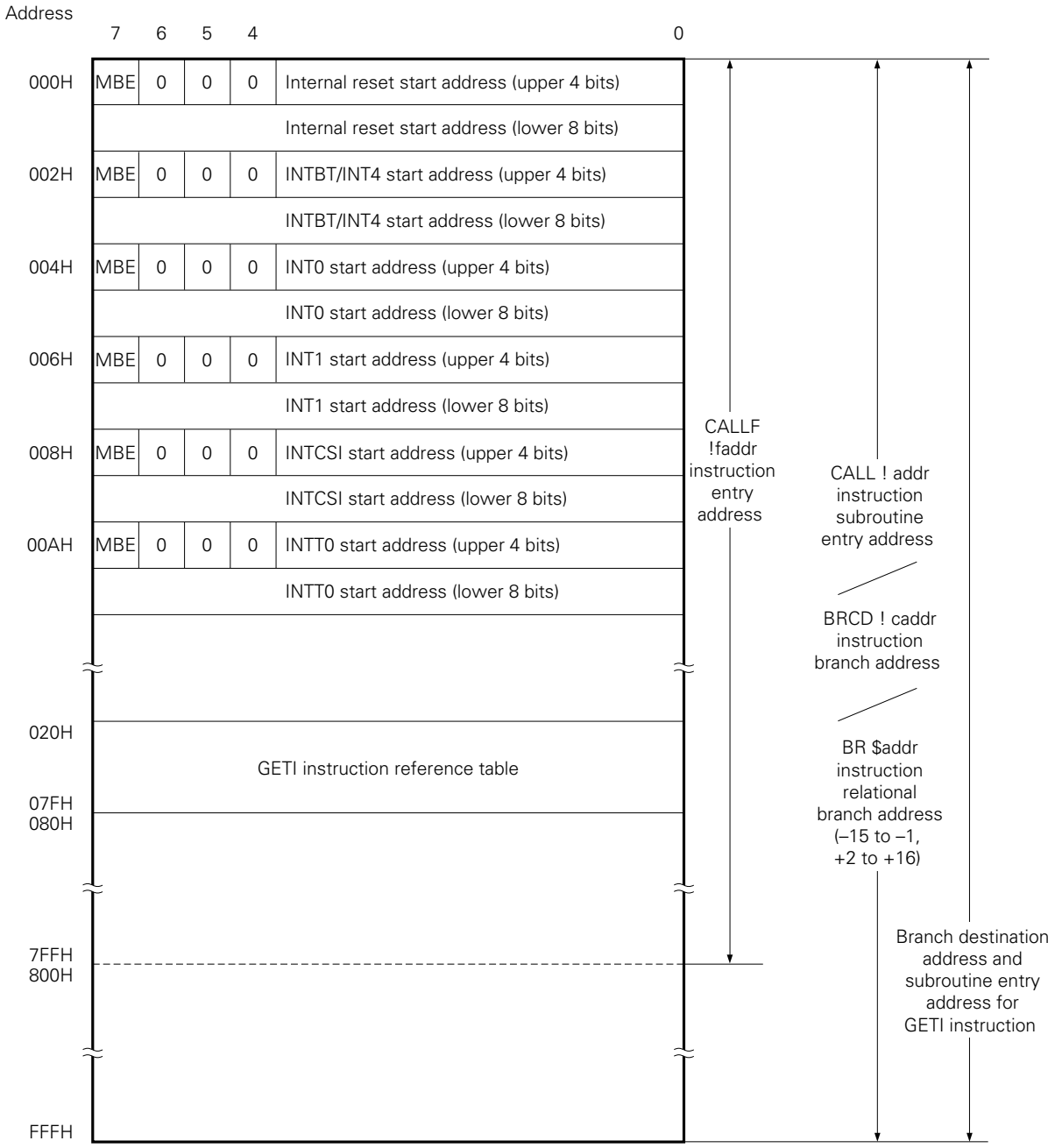


Fig. 4-1 Program Memory Map (μPD75004)

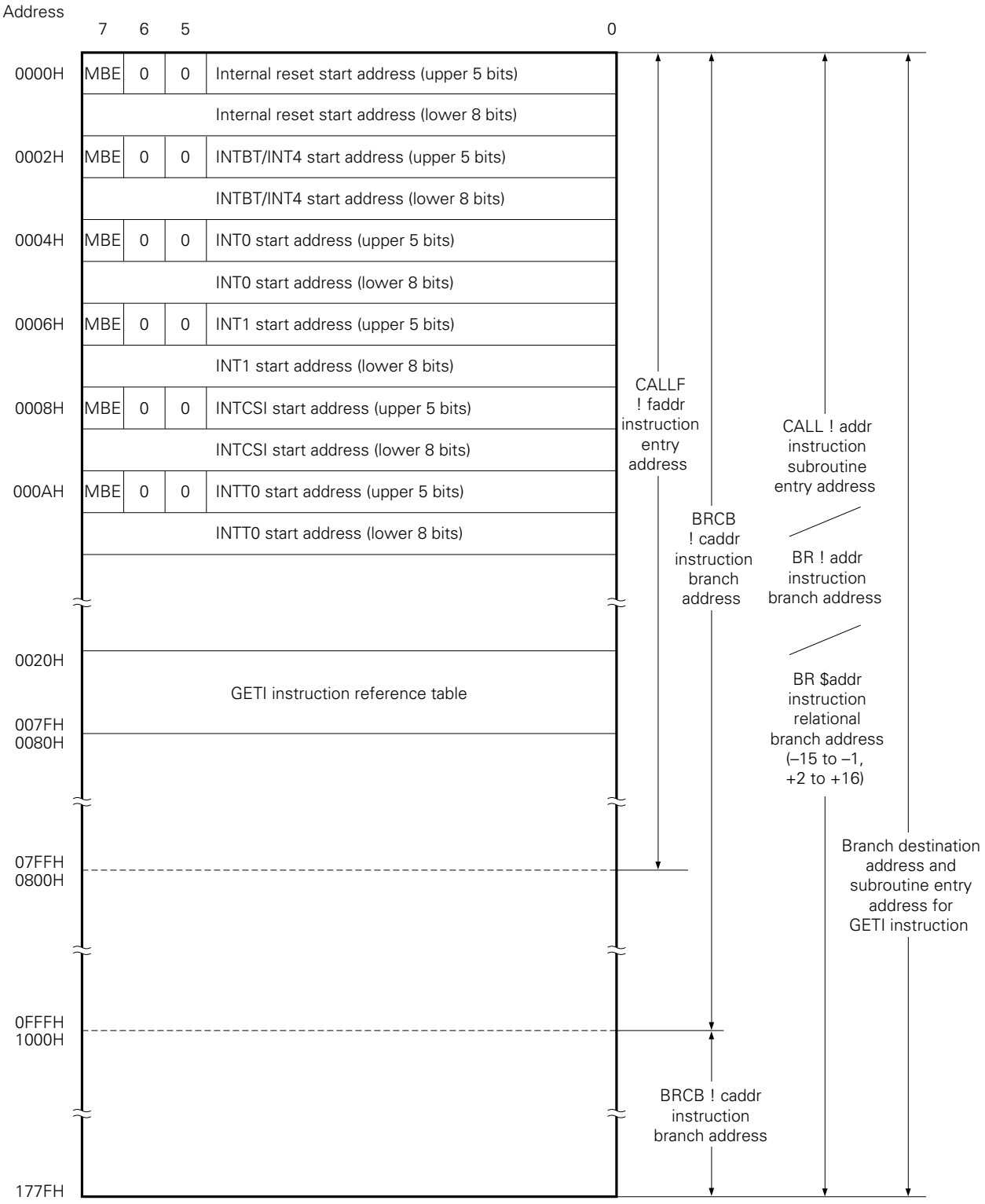


Fig. 4-2 Program Memory Map (μPD75006)

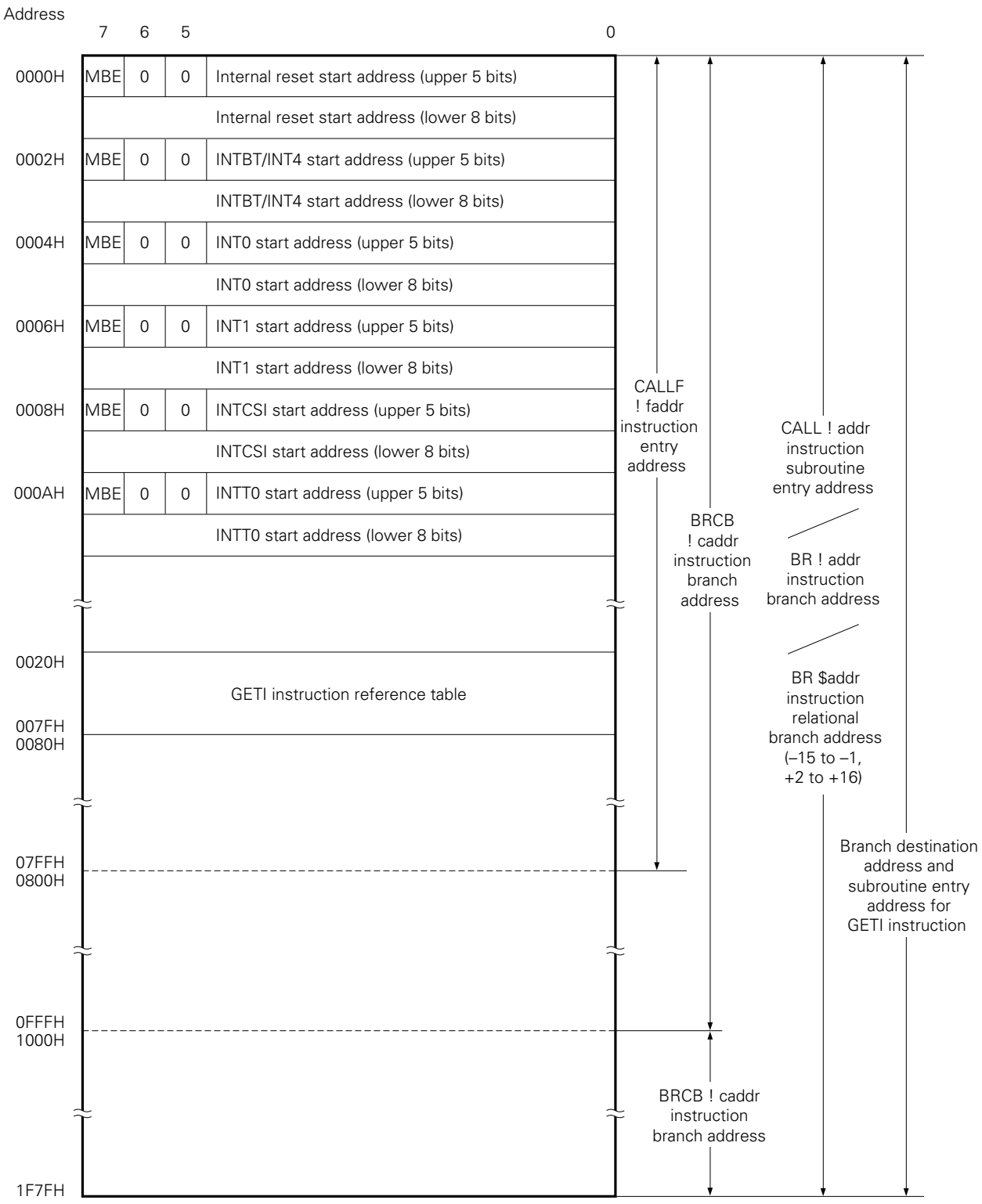


Fig. 4-3 Program Memory Map (μPD75008)

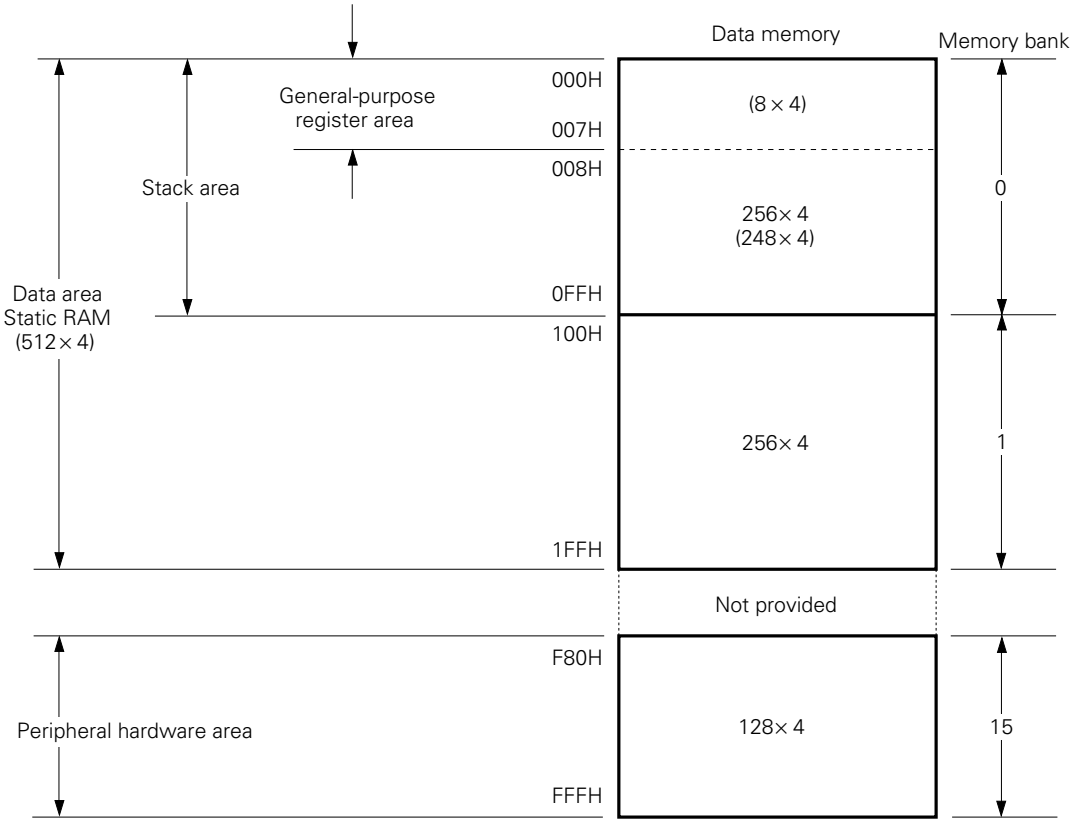


Fig. 4-4 Data Memory Map

5. PERIPHERAL HARDWARE FUNCTIONS

5.1 PORTS

I/O ports are classified into the following 3 kinds:

- CMOS input (PORT0, 1) : 8
- CMOS input/output (PORT2, 3, 6, 7, and 8) : 18
- N-ch open-drain input/output (PORT4, 5) : 8

Total : 34

Table 5-1 Port Function

Port Name (Symbol)	Function	Operation and Feature	Remarks
PORT0 PORT1	4-bit input	Can be always read or tested regardless of operation mode of multiplexed pin.	Multiplexed with SO/SB0, SI/SB1, SCK, INT0-2, 4, and TIO
PORT3* PORT6	4-bit input/output	Can be set in input or output mode in 1-bit units.	Port 6 is multiplexed with KR0 to KR3.
PORT2		Can be set in input or output mode in 4-bit units. Ports 6 and 7 are used in pairs to input/output data in 8-bit units.	Port 2 is multiplexed with PTO0, PCL, and BUZ.
PORT7			Port 7 is multiplexed with KR4-KR7.
PORT4* PORT5*	4-bit input/output (N-ch open-drain, 10 V)	Can be set in input or output mode in 4-bit units. Ports 4 and 5 are used in pairs to input/output data in 8-bit units.	Can be connected to a pull-up resistor in 1-bit units by using mask option.
PORT8	2-bit input/output	Can be set input or output mode in 2-bit units.	—

*: Can directly drive LED.

5.2 CLOCK GENERATOR CIRCUIT

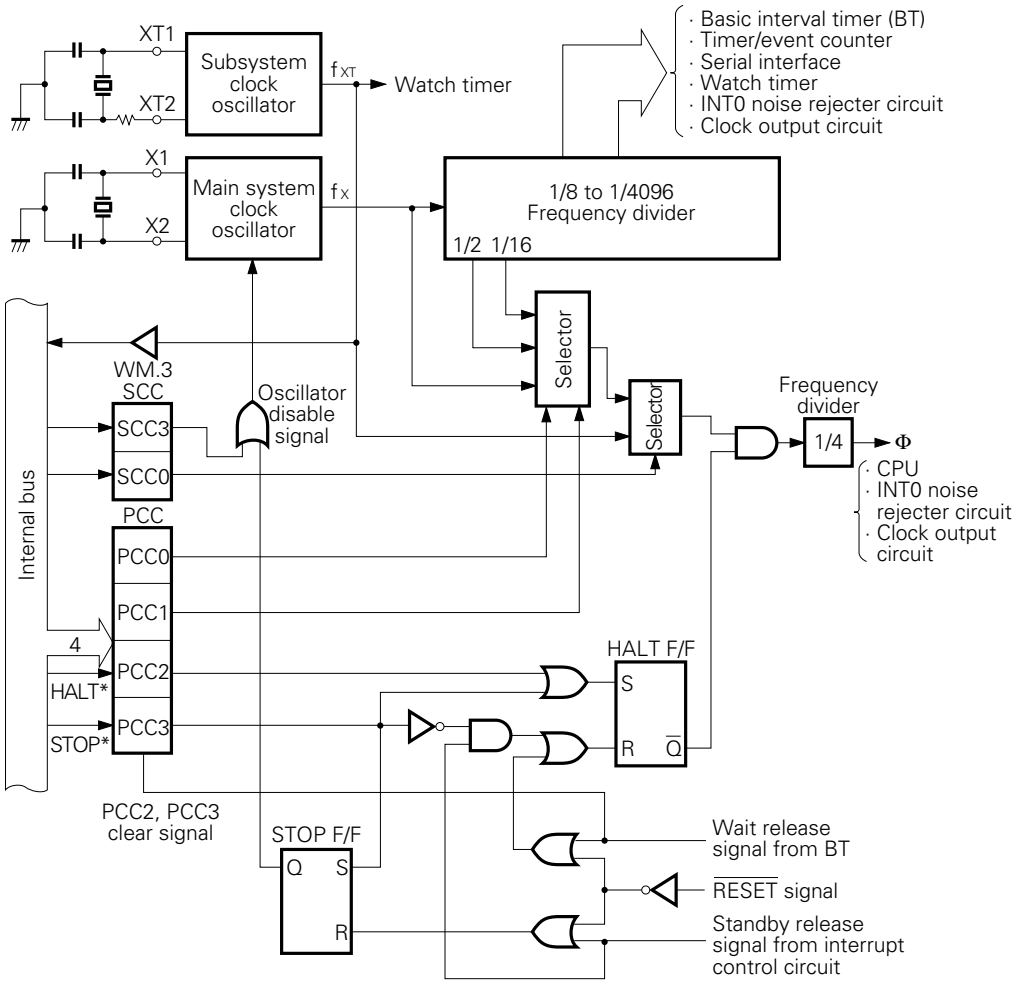
The operation of the clock generator circuit is determined by the processor clock control regiser (PPC) and system clock control register (SCC).

This circuit can generate two types of clocks: main system clock and subsystem clock.

In addition, it can also change the instruction execution time.

- 0.95 μs, 1.91 μs, 15.3 μs (main system clock: 4.19 MHz)
- 122 μs (subsystem clock: 32.768 kHz)

★



*: instruction execution.

Remarks 1: f_X = Main system clock frequency

2: f_{XT} = Subsystem clock frequency

3: Φ = CPU clock

4: PCC: Processor clock control register

5: SCC: System clock control register

6: One clock cysle (t_{CY}) of Φ is one machine cycle of an instruction. For t_{CY}, refer to AC characteristics in 10. ELECTRICAL SPECIFICATIONS.

Fig. 5-1 Clock Generator Block Diagram

5.3 CLOCK OUTPUT CIRCUIT

The clock output circuit outputs clock pulse from the P22/PCL pin. This clock output circuit is used to output clock pulses to the remote control output, peripheral LSIs, etc.

- Clock output (PCL) : Φ, 524, 262, 65.5 kHz (operating at 4.19 MHz)
- Buzzer output (BUZ) : 2 kHz (operating at 4.19 MHz, or 32.768 kHz)

Fig. 5-2 shows the clock output circuit configuration.

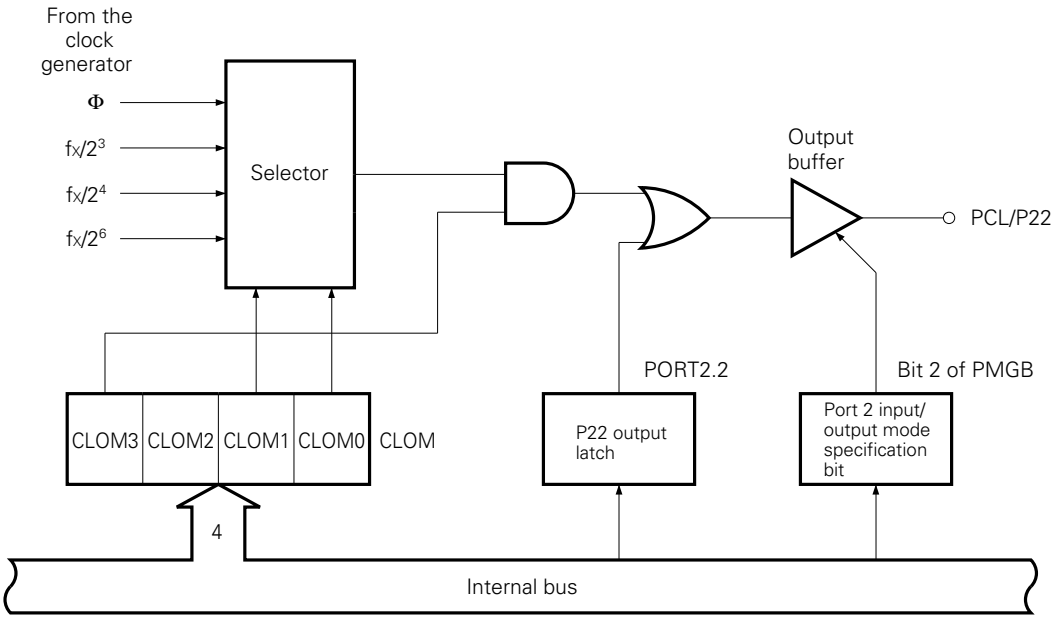


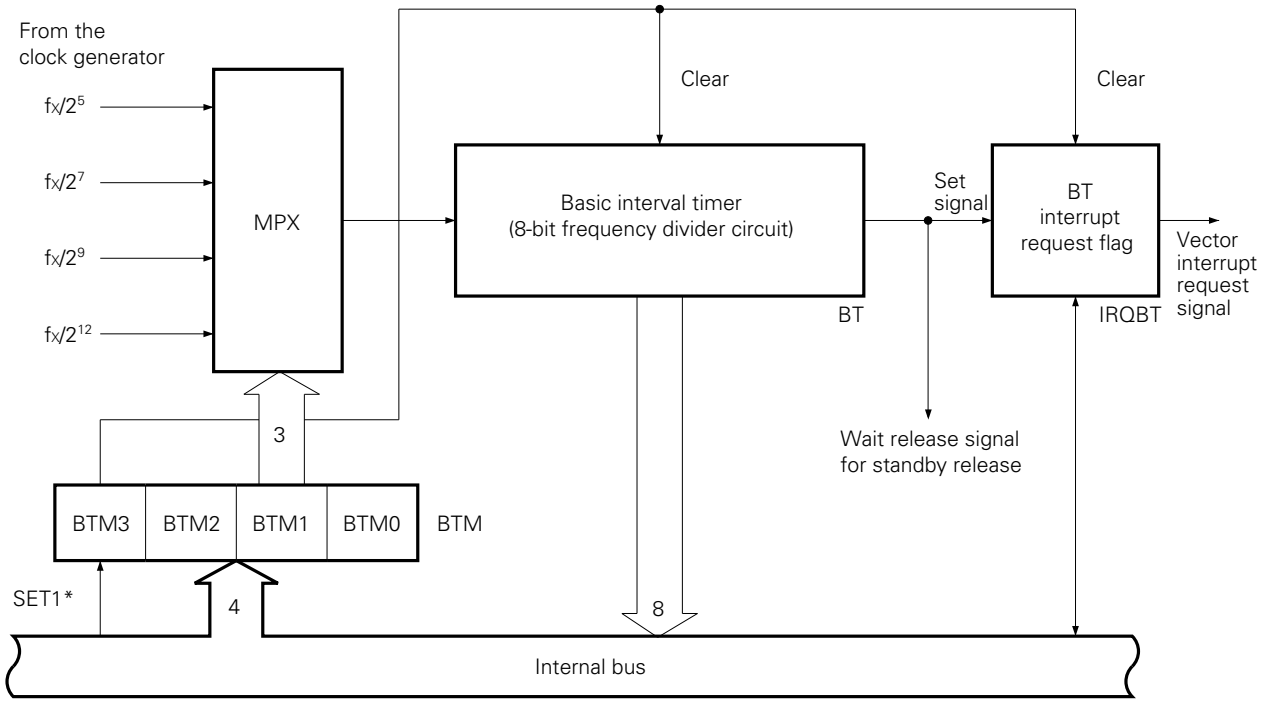
Fig. 5-2 Clock Output Circuit Configuration

Remarks: A measures to prevent outputting narrow width pulse when selecting clock output enable/ disable is taken.

5.4 BASIC INTERVAL TIMER

The basic interval timer has these functions:

- Interval timer operation which generates a reference time interrupt
- Watchdog timer application which detects a program runaway
- Selects the wait time for releasing the standby mode and counts the wait time
- Reads out the count value



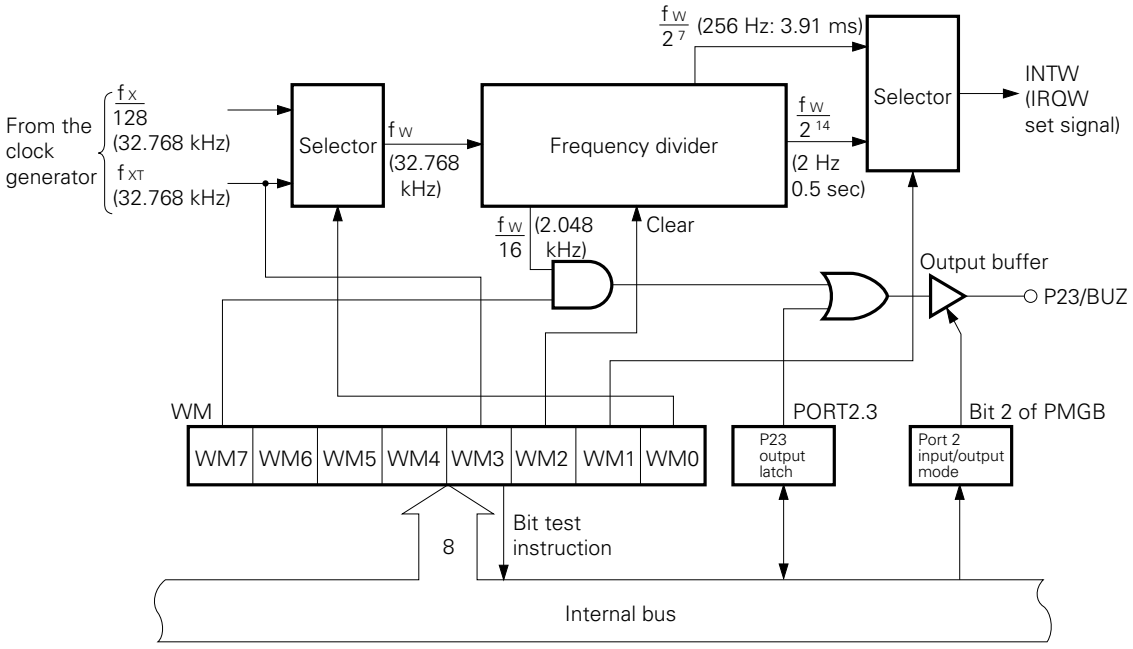
Remarks : *: Instruction execution

Fig. 5-3 Basic Interval Timer Configuration

5.5 WATCH TIMER

The μPD75008 has a built-in 1-ch watch timer. The watch timer is configured as shown in Fig. 5-4.

- Sets the test flag (IRQW) with 0.5 sec interval.
  The standby mode can be released by IRQW.
- 0.5 second interval can be generated either from the main system clock or subsystem clock.
- Time interval can be advanced to 128 times faster (3.91 ms) by setting the fast mode. This is convenient for program debugging, test, etc.
- Fixed frequency (2.048 kHz) can be output to the P23/BUZ pin. This can be used for beep and system clock frequency trimming.
- The frequency divider circuit can be cleared so that zero second watch start is possible.



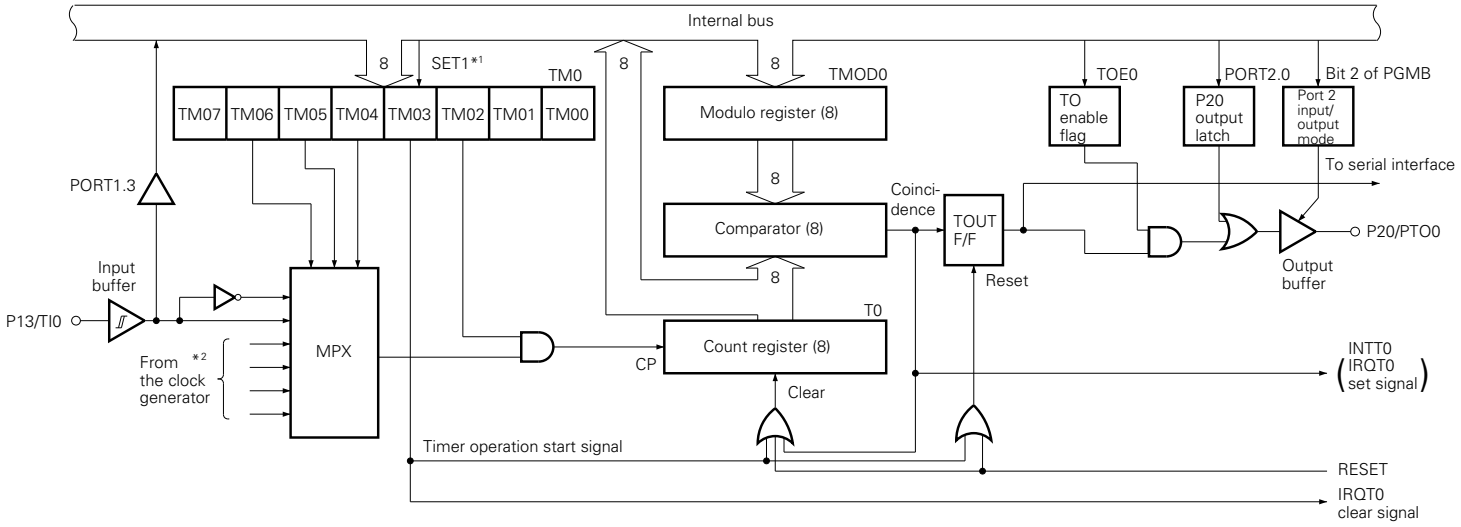
( ) is for fx = 4.194304 MHz, fxT = 32.768 kHz.

Fig. 5-4 Watch Timer Block Diagram

5.6 TIMER/EVENT COUNTER

The μPD75008 has a built-in 1-ch timer/event counter. The timer/even counter has these functions:

- Programmable interval timer operation
- Outputs square-wave signal of an arbitrary frequency to the PTO0 pin.
- Event counter operation
- Divides the TI0 pin input in N and outputs to the PTO0 pin (frequency divider operation).
- Supplies serial shift clock to the serial interface circuit.
- Count condition read out function



*1: SET1: Instruction execution
*2: Refer to Fig. 5-1.

Fig. 5-5 Timer/Event Counter Block Diagram

5.7 SERIAL INTERFACE

The μPD75008 is equipped with a serial interface that operates in the following modes:

- Three-line serial I/O mode (MSB/LSB first selectable)
- Two-line serial I/O mode (MSB first)
- SBI mode (MSB first)

In the three-line I/O mode, the microcomputer can be connected to a microcomputer in the 75X series or 78K series devices, or various I/O devices. In the two-line serial mode and SBI mode, communication can be established with two or more devices.

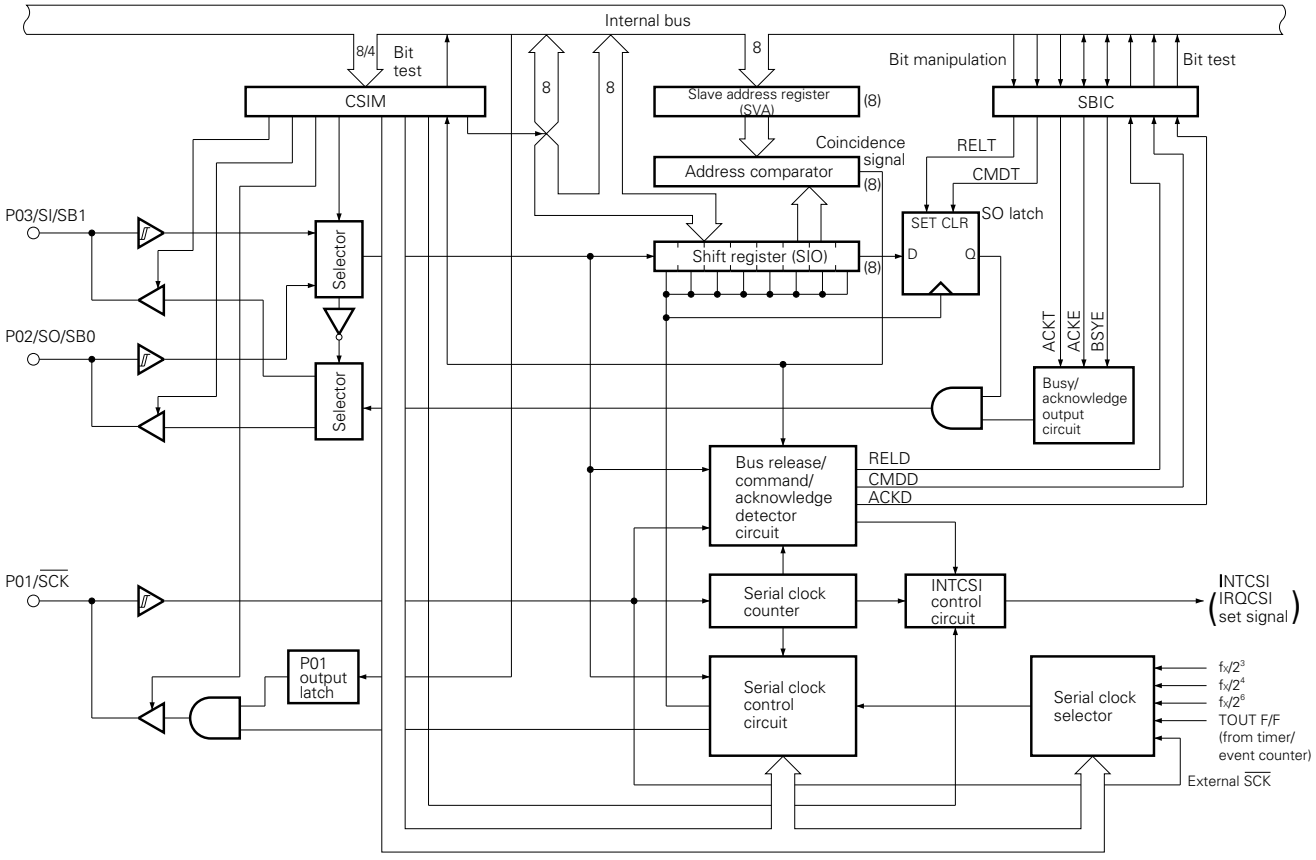
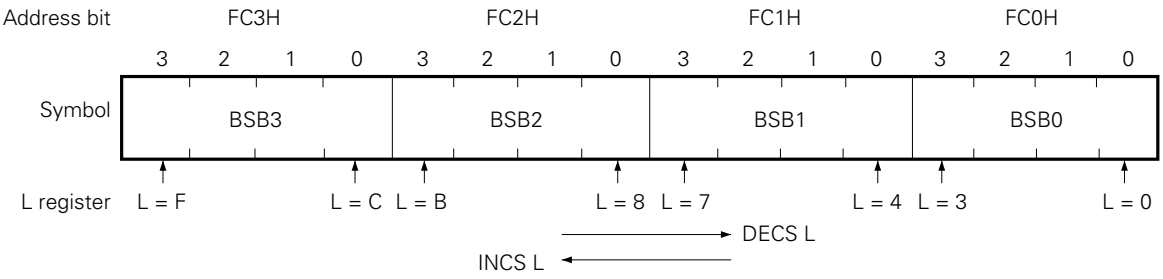


Fig. 5-6 Serial Interface Block Diagram

5.8 BIT SEQUENTIAL BUFFER .... 16 BITS

The bit sequential buffer is a data memory specifically provided for bit manipulation. With this buffer, addresses and bit specifications can be sequentially up-dated in bit manipulation operation. Therefore, this buffer is very useful for processing long data in bit units.



Remarks: For the pmem.@L addressing, the specification bit is shifted according to the L register.

Fig. 5-7 Bit Sequential Buffer Format

6. INTERRUPT FUNCTIONS

The μPD75008 has 8 different interrupt sources and multiplexed interrupt through the software control. In addition to that, the μPD75008 is also provided with two types of edge detection testable inputs.
The interrupt control circuit of the μPD75008 has these functions:

- Hardware controlled vector interrupt function which can control whether or not to accept an interrupt by using the interrupt flag (IExxx) and interrupt master enable flag (IME).
- The interrupt start address can be arbitrarily set.
- Interrupt request flag (IRQxxx) test function (an interrupt generation can be confirmed by means of software).
- Standby mode release (Interrupts to be released can be selected by the interrupt enable flag).

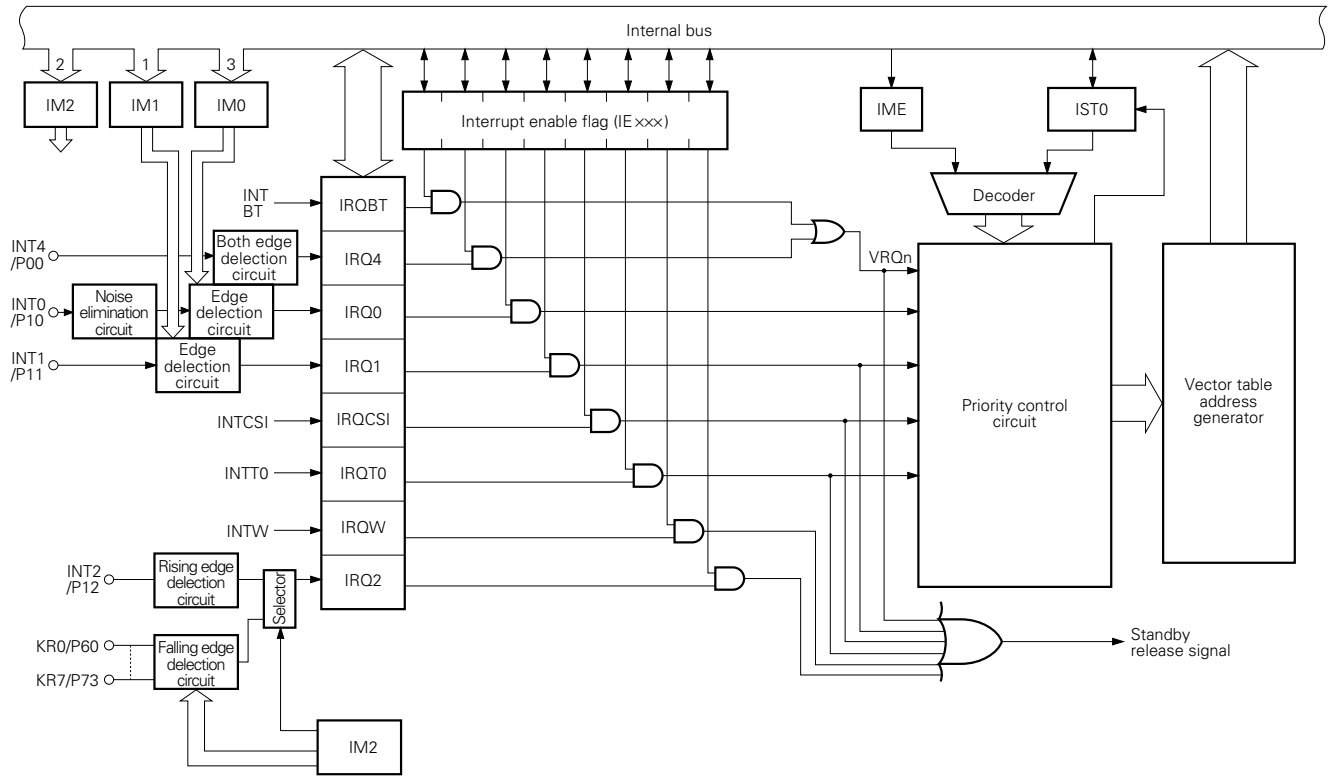


Fig. 6-1 Interrupt Control Block Diagram

7. STANDBY FUNCTIONS

The μPD75008 has two different standby modes (STOP mode and HALT mode) to reduce the power consumption while waiting for program execution.

Table 7-1 Each Status in Standby Mode

		STOP Mode	HALT Mode
Setting Instruction		STOP instrtuction	HALT instruction
System Clock for Setting		Can be set only when operating on the main system clock	Can be set either with the main system clock or the subsystem clock
Operation Status	Clock Generator	Only the main system clock stops its operation.	Only the CPU clock Φ stops its operation. (oscillation continues)
	Basic Interval Timer	No operation	Can operate only when main system clock oscillates (Sets IRQBT at reference time interval)
	Serial Interface	Can operate only when the external $\overline{SCK}$ input is selected for the serial clock	Can operate only when external $\overline{SCK}$ input is selected as serial clock, or when main system clock oscillates
	Timer/Event Counter	Can operate only when the TI0 pin input is selected for the count clock	Can operate only when TI0 pin input is selected as count clock, or when main system clock oscillates
	Watch Timer	Can operate when f_{XT} is selected as the count clock	Can operate
	External Interrupt	INT1, INT2, and INT4 can operate. Only INT0 can not operate.	
	CPU	No operation	
Release Signal		An interrupt request signal from a hardware whose operation is enabled by the interrupt enable flag or the $\overline{RESET}$ signal input	An interrupt request signal from a hardware whose operation is enabled by the interrupt enable flag or the $\overline{RESET}$ signal input

8. RESET FUNCTION

When the $\overline{\text{RESET}}$ signal is input, the μPD75008 is reset and each hardware is initialized as indicated in Table 8-1. Fig. 8-1 shows the reset operation timing.

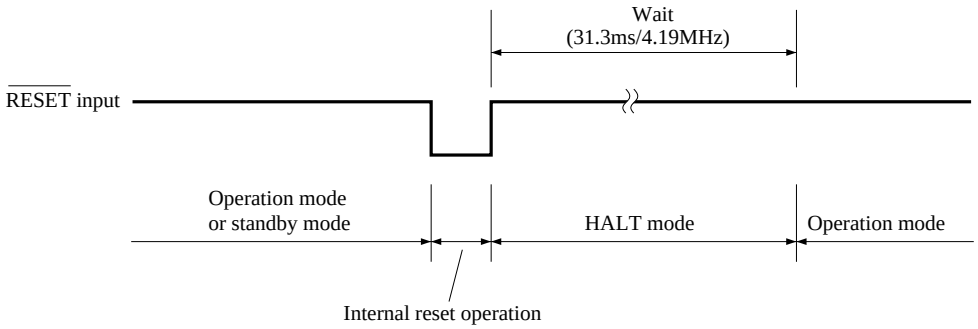


Fig. 8-1 Reset Operation by $\overline{\text{RESET}}$ Input

Table 8-1 Status of Each Hardware after Reset (1/2)

Hardware		$\overline{\text{RESET}}$ Input in Standby Mode	$\overline{\text{RESET}}$ Input during Operation
Program Counter (PC)		The contents of the lower 4 bits of address 000H of the program memory are set to PC11-8, and the contents of address 001H are set to PC7-0.	Same as at left
PSW	Carry Flag (CY)	Retained	Undefined
	Skip Flag (SK0-2)	0	0
	Interrupt Status Flag (IST0)	0	0
	Bank Enable Flag (MBE)	The contents of bit 7 of address 000H of the program memory is set to MBE.	Same as at left
Stack Pointer (SP)		Undefined	Undefined
Data Memory (RAM)		Retained*	Undefined
General-Purpose Register (X, A, H, L, D, E, B, C)		Retained	Undefined
Bank Selection Register (MBS)		0	0
Basic Interval Timer	Counter (BT)	Undefined	Undefined
	Mode Register (BTM)	0	0
Timer/Event Counter	Counter (T0)	0	0
	Module Register (TMOD0)	FFH	FFH
	Mode Register (TM0)	0	0
	TOE0, TOUT F/F	0, 0	0, 0
Watch Timer	Mode Register (WM)	0	0

*: Data of address 0F8H to 0FDH of the data memory becomes undefined when a $\overline{\text{RESET}}$ signal is input.

Table 8-1 Status of Each Hardware after Reset (2/2)

Hardware		$\overline{\text{RESET}}$ Input in Standby Mode	$\overline{\text{RESET}}$ Input during Operation
Serial Interface	Shift Register (SIO)	Retained	Undefined
	Operation Mode Register (CSIM)	0	0
	SBI Control Register (SBIC)	0	0
	Slave Address Register (SVA)	Retained	Undefined
Clock Generator, Clock Output Circuit	Processor Clock Control Register (PCC)	0	0
	System Clock Control Register (SCC)	0	0
	Clock Output Mode Register (CLOM)	0	0
Interrupt Function	Interrupt Enable Flag (IExxx)	0	0
	Interrupt Master Enable Flag (IME)	0	0
	INT0, INT1, INT2 Mode Registers (IM0, 1, 2)	0, 0, 0	0, 0, 0
Digital Port	Output Buffer	Off	Off
	Output Latch	Clear (0)	Clear (0)
	Input/Output Mode Register (PMGA, B, C)	0	0
	Pull-Up Resistor Specification Register (POGA, B)	0	0
Bit sequential buffer (BSB0-3)		Retained	Specified

9. INSTRUCTION SET

(1) Operand representation and description

Describe one or more operands in the operand field of each instruction according to the operand representation and description methods of the instruction (for details, refer to RA75X Assembler Package User's Manual - Language (EEU-730)). With some instructions, only one operand should be selected from several operands. The uppercase characters, +, and – are keywords and must be described as is.

Describe an appropriate numeric value or label as immediate data.

The symbols in the register and flag symbols can be described as labels in the places of mem, fmem, pmem, and bit (for details, refer to μPD7500X Series User's Manual (IEM-5033)). However, fmem and pmem restricts the label that can be described.

Representation	Description	
reg reg1	X, A, B, C, D, E, H, L X, B, C, D, E, H, L	
rp rp1 rp2	XA, BC, DE, HL BC, DE, HL BC, DE	
rpa rpa1	HL, DE, DL DE, DL	
n4 n8	4-bit immediate data or label 8-bit immediate data or label	
mem* bit	8-bit immediate data or label 2-bit immediate data or label	
fmem pmem	FB0H to FBFH,FF0H to FFFH immediate data or label FC0H to FFFH immediate data or label	
addr	μPD75004	0000H to 0FFFH immediate data or label
	μPD75006	0000H to 177FH immediate data or label
	μPD75008	0000H to 1F7FH immediate data or label
caddr	12-bit immediate data or label	
faddr	11-bit immediate data or label	
taddr	20H to 7FH immediate data (where bit0 = 0) or label	
PORTn IExxx MBn	PORT0 to PORT8 IEBT, IECSI, IET0, IE0, IE1, IE2, IE4, IEW MB0, MB1, MB15	

*: Only even address can be described as mem for 8-bit data processing.

(2) Legend of operation field

A	:	A register; 4-bit accumulator
B	:	B register; 4-bit accumulator
C	:	C register; 4-bit accumulator
D	:	D register; 4-bit accumulator
E	:	E register; 4-bit accumulator
H	:	H register; 4-bit accumulator
L	:	L register; 4-bit accumulator
X	:	X register; 4-bit accumulator
XA	:	Register pair (XA); 8-bit accumulator
BC	:	Register pair (BC); 8-bit accumulator
DE	:	Register pair (DE); 8-bit accumulator
HL	:	Register pair (HL); 8-bit accumulator
PC	:	Program counter
SP	:	Stack pointer
CY	:	Carry flag; or bit accumulator
PSW	:	Program status word
MBE	:	Memory bank enable flag
PORTn	:	Port n (n = 0 to 8)
IME	:	Interrupt mask enable flag
IExxx	:	Interrupt enable flag
MBS	:	Memory bank selector register
PCC	:	Processor clock control register
·	:	Delimiter of address and bit
(xx)	:	Contents addressed by xx
xxH	:	Hexadecimal data

(3) Symbols in addressing area field

*1	MB = MBE · MBS (MBS = 0, 1, 15)	Data memory addressing
*2	MB = 0	
*3	MBE = 0 : MB = 0 (00H-7FH) MB = 15 (80H-FFH) MBE = 1 : MB = MBS (MBS = 0, 1, 15)	
*4	MB = 15, fmem = FB0H-FBFH, FF0H-FFFH	
*5	MB = 15, pmem = FC0H-FFFH	
*6	addr = 000H-FFFH (μPD75004) 0000H-177FH (μPD75006) 0000H-1F7FH (μPD75008)	Program memory addressing
*7	addr = (Current PC) – 15 to (Current PC) – 1 (Current PC) + 2 to (Current PC) + 16	
*8	caddr = 000H-FFFH (μPD75004) 0000H-0FFFH (PC_{12} = 0 : μPD75006, 75008) 0000H-177FH (PC_{12} = 1 : μPD75006) 0000H-1F7FH (PC_{12} = 1 : μPD75008)	
*9	faddr = 0000H-07FFH	
*10	taddr = 0020H-007FH	

Remarks 1: MB indicates memory bank that can be accessed.

2: In *2, MB = 0 regardless of MBE and MBS.

3: In *4 and *5, MB = 15 regardless of MBE and MBS.

4: *6 to *10 indicate areas that can be addressed.

(4) Machine cycle field

In this field, S indicates the number of machine cycles required when an instruction having a skip function skips. The value of S varies as follows:

- When no instruction is skipped ..... S = 0
- When 1-byte or 2-byte instruction is skipped ..... S = 1
- When 3-byte instruction (BR ! addr or CALL ! addr) is skipped ..... S = 2

Note: The GETI instruction is skipped in one machine cycle.

One machine cycle equals to one cycle of the CPU clock Φ, ($=t_{CY}$), and can be changed in three steps depending on the setting of the processor clock control register (PCC).

Instructions	Mnemonics	Operand	Bytes	Machine Cycles	Operation	Addressing Area	Skip Conditions
Transfer	MOV	A, #n4	1	1	A ← n4		String effect A
		reg1, #n4	2	2	reg1 ← n4		
		XA, #n8	2	2	XA ← n8		String effect A
		HL, #n8	2	2	HL ← n8		String effect B
		rp2, #n8	2	2	rp2 ← n8		
		A, @HL	1	1	A ← (HL)	*1	
		A, @rpa1	1	1	A ← (rpa1)	*2	
		XA, @HL	2	2	XA ← (HL)	*1	
		@HL, A	1	1	(HL) ← A	*1	
		@HL, XA	2	2	(HL) ← XA	*1	
		A,mem	2	2	A ← (mem)	*3	
		XA, mem	2	2	XA ← (mem)	*3	
		mem, A	2	2	(mem) ← A	*3	
		mem, XA	2	2	(mem) ← XA	*3	
		A, reg	2	2	A ← reg		
		XA, rp	2	2	XA ← rp		
		reg1, A	2	2	reg1 ← A		
		rp1, XA	2	2	rp1 ← XA		
	XCH	A, @HL	1	1	A ↔ (HL)	*1	
		A, @rpa1	1	1	A ↔ (rpa1)	*2	
		XA, @HL	2	2	XA ↔ (HL)	*1	
		A, mem	2	2	A ↔ (mem)	*3	
		XA, mem	2	2	XA ↔ (mem)	*3	
		A, reg1	1	1	A ↔ reg1		
		XA, rp	2	2	XA ↔ rp		
	MOVT	XA, @PCDE	1	3	• μPD75004 XA ← $(PC_{11-8}+DE)_{ROM}$ • μPD75006, 75008 XA ← $(PC_{12-8}+DE)_{ROM}$		
		XA, @PCXA	1	3	• μPD75004 XA ← $(PC_{11-8}+XA)_{ROM}$ • μPD75006, 75008 XA ← $(PC_{12-8}+XA)_{ROM}$		
Arithmetic Operation	ADDS	A, #n4	1	1+S	A ← A+n4		carry
		A, @HL	1	1+S	A ← A+(HL)	*1	carry
	ADDC	A, @HL	1	1	A, CY ← A+(HL)+CY	*1	
	SUBS	A, @HL	1	1+S	A ← A-(HL)	*1	borrow
	SUBC	A, @HL	1	1	A, CY ← A-(HL)-CY	*1	
	AND	A, #n4	2	2	A ← A ∧ n4		
		A, @HL	1	1	A ← A ∧ (HL)	*1	
	OR	A, #n4	2	2	A ← A ∨ n4		
		A, @HL	1	1	A ← A ∨ (HL)	*1	
	XOR	A, #n4	2	2	A ← A ⊻ n4		
		A, @HL	1	1	A ← A ⊻ (HL)	*1	
Accumulator Manipulation	RORC	A	1	1	CY ← A_0, A_3 ← CY, A_{n-1} ← A_n		
	NOT	A	2	2	A ← $\overline{A}$		

Instructions	Mnemonics	Operand	Bytes	Machine Cycles	Operation	Addressing Area	Skip Conditions
Increment/ Decrement	INCS	reg	1	1+S	reg ← reg+1		reg = 0
		@HL	2	2+S	(HL) ← (HL)+1	*1	(HL) = 0
		mem	2	2+S	(mem) ← (mem)+1	*3	(mem) = 0
	DECS	reg	1	1+S	reg ← reg-1		reg = FH
Compare	SKE	reg, #n4	2	2+S	Skip if reg = n4		reg = n4
		@HL, #n4	2	2+S	Skip if (HL) = n4		*1(HL) = n4
		A, @HL	1	1+S	Skip if A = (HL)	*1	A = (HL)
		A, reg	2	2+S	Skip if A = reg		A = reg
Carry flag Manipulation	SET1	CY	1	1	CY ← 1		
	CLR1	CY	1	1	CY ← 0		
	SKT	CY	1	1+S	Skip if CY = 1		CY = 1
	NOT1	CY	1	1	CY ← $\overline{CY}$		
Memory/ Bit Manipulation	SET1	mem.bit	2	2	(mem.bit) ← 1	*3	
		fmem.bit	2	2	(fmem.bit) ← 1	*4	
		pmem.@L	2	2	(pmem$_{7-2}$ + L$_{3-2}$.bit(L$_{1-0}$)) ← 1	*5	
		@H+mem.bit	2	2	(H + mem$_{3-0}$.bit) ← 1	*1	
	CLR1	mem.bit	2	2	(mem.bit) ← 0	*3	
		fmem.bit	2	2	(fmem.bit) ← 0	*4	
		pmem.@L	2	2	(pmem$_{7-2}$ + L$_{3-2}$.bit(L$_{1-0}$)) ← 0	*5	
		@H+mem.bit	2	2	(H+mem$_{3-0}$.bit) ← 0	*1	
	SKT	mem.bit	2	2+S	Skip if (mem.bit) = 1	*3	(mem.bit) = 1
		fmem.bit	2	2+S	Skip if (fmem.bit) = 1	*4	(fmem.bit) = 1
		pmem.@L	2	2+S	Skip if (pmem$_{7-2}$+L$_{3-2}$.bit (L$_{1-0}$)) = 1	*5	(pmem.@L) = 1
		@H+mem.bit	2	2+S	Skip if (H + mem$_{3-0}$.bit) = 1	*1	(@H+mem.bit) = 1
	SKF	mem.bit	2	2+S	Skip if (mem.bit) = 0	*3	(mem.bit) = 0
		fmem.bit	2	2+S	Skip if (fmem.bit) = 0	*4	(fmem.bit) = 0
		pmem.@L	2	2+S	Skip if (pmem$_{7-2}$ +L$_{3-2}$.bit (L$_{1-0}$)) = 0	*5	(pmem.@L) = 0
		@H+mem.bit	2	2+S	Skip if (H + mem$_{3-0}$.bit) = 0	*1	(@H+mem.bit) = 0
	SKTCLR	fmem.bit	2	2+S	Skip if (fmem.bit) = 1 and clear	*4	(fmem.bit) = 1
		pmem.@L	2	2+S	Skip if (pmem$_{7-2}$+L$_{3-2}$.bit (L$_{1-0}$)) = 1 and clear	*5	(pmem.@L) = 1
		@H+mem.bit	2	2+S	Skip if (H+mem$_{3-0}$.bit) = 1 and clear	*1	(@H+mem.bit) = 1
	AND1	CY,fmem.bit	2	2	CY ← CY ∧ (fmem.bit)	*4	
		CY,pmem.@L	2	2	CY ← CY ∧ (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))	*5	
		CY,@H+mem.bit	2	2	CY ← CY ∧ (H+mem$_{3-0}$.bit)	*1	
	OR1	CY,fmem.bit	2	2	CY ← CY ∨ (fmem.bit)	*4	
		CY,pmem.@L	2	2	CY ← CY ∨ (pmem$_{7-2}$+L$_{3-2}$.bit (L$_{1-0}$))	*5	
		CY,@H+mem.bit	2	2	CY ← CY ∨ (H+mem$_{3-0}$.bit)	*1	
	XOR1	CY,fmem.bit	2	2	CY ← CY ⊻ (fmem.bit)	*4	
		CY,pmem.@L	2	2	CY ← CY ⊻ (pmem$_{7-2}$+L$_{3-2}$.bit (L$_{1-0}$))	*5	
		CY,@H+mem.bit	2	2	CY ← CY ⊻ (H+mem$_{3-0}$.bit)	*1	

Instructions	Mnemonics	Operand	Bytes	Machine Cycles	Operation	Addressing Area	Skip Conditions
Branch	BR	addr	—	—	• μPD75004 $PC_{11-0} \leftarrow$ addr (The most suitable instruction is selectable from among BRCB !caddr, and BR $addr depending on the assembler.)	*6	
					• μPD75006, 75008 $PC_{12-0} \leftarrow$ addr (The most suitable instruction is selectable from among BR !addr, BRCB !caddr, and BR $addr depending on the assembler.)		
		!addr	3	3	• μPD75006, 75008 $PC_{12-0} \leftarrow$ addr	*6	
		$addr	1	2	• μPD75004 $PC_{11-0} \leftarrow$ addr	*7	
					• μPD75006, 75008 $PC_{12-0} \leftarrow$ addr		
	BRCB	!caddr	2	2	• μPD75004 $PC_{11-0} \leftarrow caddr_{11-0}$	*8	
					• μPD75006, 75008 $PC_{12-0} \leftarrow PC_{12} + caddr_{11-0}$		
Subroutine/ Stack Control	CALL	!addr	3	3	• μPD75004 $(SP-4)(SP-1)(SP-2) \leftarrow PC_{11-0}$ $(SP-3) \leftarrow$ MBE, 0, 0, 0 $PC_{11-0} \leftarrow$ addr, $SP \leftarrow SP-4$	*6	
					• μPD75006, 75008 $(SP-4)(SP-1)(SP-2) \leftarrow PC_{11-0}$ $(SP-3) \leftarrow$ MBE, 0, 0, PC_{12} $PC_{12-0} \leftarrow$ addr, $SP \leftarrow SP-4$		
	CALLF	!faddr	2	2	• μPD75004 $(SP-4)(SP-1)(SP-2) \leftarrow PC_{11-0}$ $(SP-3) \leftarrow$ MBE, 0, 0, 0 $PC_{11-0} \leftarrow 0$, faddr, $SP \leftarrow SP-4$	*9	
					• μPD75006, 75008 $(SP-4)(SP-1)(SP-2) \leftarrow PC_{11-0}$ $(SP-3) \leftarrow$ MBE, 0, 0, PC_{12} $PC_{12-0} \leftarrow$ 0, 0, faddr, $SP \leftarrow SP-4$		
	RET		1	3	• μPD75004 MBE, x, x, x $\leftarrow$ (SP+1) $PC_{11-0} \leftarrow$ (SP)(SP+3)(SP+2) $SP \leftarrow SP+4$		
					• μPD75006, 75008 MBE, x, x, $PC_{12} \leftarrow$ (SP+1) $PC_{11-0} \leftarrow$ (SP)(SP+3)(SP+2) $SP \leftarrow SP+4$		
	RETS		1	3+S	• μPD75004 MBE, x, x, x $\leftarrow$ (SP+1) $PC_{11-0} \leftarrow$ (SP)(SP+3)(SP+2) $SP \leftarrow SP+4$, then skip unconditionally		Undefined
					• μPD75006, 75008 MBE, x, x, $PC_{12} \leftarrow$ (SP+1) $PC_{11-0} \leftarrow$ (SP)(SP+3)(SP+2) $SP \leftarrow SP+4$, then skip unconditionally		

Instructions	Mnemonics	Operand	Bytes	Machine Cycles	Operation	Addressing Area	Skip Conditions
Subroutine/ Stack Control (Cont'd)	RETI		1	3	• μPD75004 MBE, x, x, x ← (SP+1) PC_{11-0} ← (SP)(SP+3)(SP+2) PSW ← (SP+4)(SP+5), SP ← SP+6		
					• μPD75006, 75008 MBE, x, x, PC_{12} ← (SP+1) PC_{11-0} ← (SP)(SP+3)(SP+2) PSW ← (SP+4)(SP+5), SP ← SP+6		
	PUSH	rp	1	1	(SP-1)(SP-2) ← rp, SP ← SP-2		
		BS	2	2	(SP-1) ← MBS, (SP-2) ← 0, SP ← SP-2		
	POP	rp	1	1	rp ← (SP+1)(SP), SP ← SP+2		
		BS	2	2	MBS ← (SP+1), SP ← SP+2		
Interrupt Control	EI		2	2	IME ← 1		
		IExxx	2	2	IExxx ← 1		
	DI		2	2	IME ← 0		
		IExxx	2	2	IExxx ← 0		
I/O	IN *	A, PORTn	2	2	A ← $PORT_n$ (n = 0-8)		
		XA, PORTn	2	2	XA ← $PORT_{n+1}$,$PORT_n$ (n = 4, 6)		
	OUT *	PORTn, A	2	2	$PORT_n$ ← A (n = 2-8)		
		PORTn, XA	2	2	$PORT_{n+1}$, $PORT_n$ ← XA (n = 4, 6)		
CPU Control	HALT		2	2	Set HALT Mode (PCC.2 ← 1)		
	STOP		2	2	Set STOP Mode (PCC.3 ← 1)		
	NOP		1	1	No Operation		
Special	SEL	MBn	2	2	MBS ← n (n = 0, 1, 15)		
	GETI	taddr	1	3	• μPD75004 Where TBR instruction, PC_{11-0} ← $(taddr)_{3-0}$+(taddr+1)	*10	
					Where TCALL instruction, (SP-4)(SP-1)(SP-2) ← PC_{11-0} (SP-3) ← MBE, 0, 0, 0 PC_{11-0} ← $(taddr)_{3-0}$+(taddr+1) SP ← SP-4		
					Except for TBR and TCALL instructions, Instruction execution of (taddr)(taddr+1)		Depends on referenced instruction
					• μPD75006, 75008 Where TBR instruction, PC_{12-0} ← $(taddr)_{4-0}$+(taddr+1)		
					Where TCALL instruction, (SP-4)(SP-1)(SP-2) ← PC_{11-0} (SP-3) ← MBE, 0, 0, PC_{12} PC_{12-0} ← $(taddr)_{4-0}$+(taddr+1) SP ← SP-4		
					Except for TBR and TCALL instructions, Instruction execution of (taddr)(taddr+1)		Depends on referenced instruction

*: When executing the IN/OUT instruction, MBE = 0, or MBE = 1, and MBS = 15.

10. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Supply Voltage	V_{DD}			-0.3 to +7.0	V
Input Voltage	V_{I1}	Other than ports 4, 5		-0.3 to V_{DD}+0.3	V
	V_{I2}	Ports 4, 5	w/pull-up resistor	-0.3 to V_{DD}+0.3	V
			Open drain	-0.3 to +11	V
Output Voltage	V_O			-0.3 to V_{DD}+0.3	V
High-Level Output Current	I_{OH}	1 pin		-10	mA
		All pins		-30	mA
Low-Level Output Current	I_{OL}*	Ports 0, 3, 4, 5	Peak	30	mA
		1 pin	rms	15	mA
		Other than ports 0, 3, 4, 5	Peak	20	mA
		1 pin	rms	10	mA
		Total of ports 0, 3, 4, 5, 8	Peak	160	mA
			rms	120	mA
		Total of ports 2, 6, 7	Peak	66	mA
			rms	33	mA
Operating Temperature	T_{opt}			-40 to +85	°C
Storage Temperature	T_{stg}			-65 to +150	°C

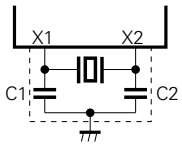
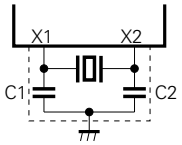
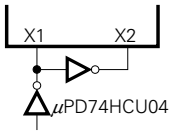
*: rms = Peak value x $\sqrt{\text{Duty}}$

CAPACITANCE (T_a = 25°C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input Capacitance	C_{IN}	f = 1 MHz			15	pF
Output Capacitance	C_{OUT}	Pins other than thosemeasured are at 0 V			15	pF
Input/Output Capacitance	C_{IO}				15	pF

MAIN SYSTEM CLOCK OSCILLATOR CIRCUIT CHARACTERISTICS

(T_a = -40 to +85°C, V_{DD} = 2.7 to 6.0 V)

Oscillator	Recommended Constants	Item	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic		Oscillation frequency(f_{XX})*1	V_{DD} = Oscillation voltage range	1.0		5.0*3	MHz
		Oscillation stabilization time*2	After V_{DD} come to MIN. of oscillation voltage range			4	ms
Crystal		Oscillation frequency (f_{XX})*1		1.0	4.19	5.0*3	MHz
		Oscillation stabilization time*2	V_{DD} = 4.5 to 6.0 V			10	ms
						30	ms
External Clock		X1 input frequency (f_X)*1		1.0		5.0*3	MHz
		X1 input high-, low-level widths (t_{XH}, t_{XL})		100		500	ns

*1: The oscillation frequency and X1 input frequency are indicated only to express the characteristics of the oscillator circuit. For instruction execution time, refer to AC Characteristics.

2: Time required for oscillation to stabilize after V_{DD} has been applied or the STOP mode has been released.

3: When the oscillation frequency is 4.19 MHz < fx ≤ 5.0 MHz, do not select PCC = 0011 as the instruction execution time: otherwise, one machine cycle is set to less than 0.95 μs, falling short of the rated minimum value of 0.95 μs. ★

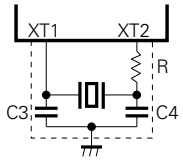
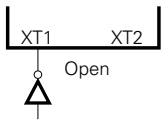
★

Note: When using the oscillation circuit of the main system clock, wire the portion enclosed in dotted line in the figures as follows to avoid adverse influences on the wiring capacity:

- Keep the wiring length as short as possible.
- Do not cross the wiring over the other signal lines.
- Do not route the wiring in the vicinity of lines through which a high alternating current flows.
- Always keep the ground point of the capacitor of the osccillator circuit at the same potential as V_{SS}. Do not connect the ground pattern through which a high current flows.
- Do not extract signals from the oscillation circuit.

SUBSYSTEM CLOCK OSCILLATOR CIRCUIT CHARACTERISTICS

(T_a = -40 to +85°C, V_{DD} = 2.7 to 6.0 V)

Oscillator	Recommended Constants	Item	Conditions	MIN.	TYP.	MAX.	Unit
Crystal		Oscillation frequency (f_{XT})*1		32	32.768	35	kHz
		Oscillation stabilization time*2	V_{DD} = 4.5 to 6.0 V		1.0	2	s
						10	s
External Clock		XT1 input frequency (f_{XT})*1		32		100	kHz
		XT1 input high-, low-level widths (t_{XTH}, t_{XTL})		5		15	μs

*1: Express the characteristcs of the oscillator circuit.

2: Time required for oscillator to stabilize after V_{DD} has been applied.

★ **Note:** When using the oscillation circuit of the subsystem clock, wire the portion enclosed in dotted line in the figures as follows to avoid adverse influences on the wiring capacity:

- Keep the wiring length as short as possible.
- Do not cross the wiring over the other signal lines.
- Do not route the wiring in the vicinity of lines through which a high alternating current flows.
- Always keep the ground point of the capacitor of the oscillator circuit at the same potential as V_{SS}. Do not connect the ground pattern through which a high current flows.
- Do not extract signals from the oscillation circuit.

The amplification factor of the subsystem clock oscillation circuit is designed to be low to reduce the current dissipation and therefore, the subsystem clock oscillation circuit is influenced by noise more easily than the main system clock oscillation circuit. When using the subsystem clock, therefore, exercise utmost care in wiring the circuit.

RECOMMENDED OSCILLATION CIRCUIT CONSTANTS

MAIN SYSTEM CLOCK: CERAMIC OSCILLATOR (T_a = -40 to +85°C)

Manufacturer	Product Name	Frequency (MHz)	Recommended Circuit Constants		Operating Voltage Range	
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)
Murata Mfg.	CSA x.xxMK*	1.00 to 1.99	30	30	2.7	6.0
	CSA x.xxMG093*	2.00 to 2.44	30	30	2.7	
	CST x.xxMG093*		—	—	2.7	
	CSA x.xxMGU*	2.45 to 5.00	30	30	2.7	
	CST x.xxMGU*		—	—	2.7	
	CSA x.xxMG*	2.00 to 5.00	30	30	3.0	
	CST x.xxMG*		—	—	3.0	
Kyoto Ceramic	KBR-1000H	1.00	100	100	2.7	6.0
	KBR-2.0MS	2.00	47	47	2.7	
	KBR-4.0MS	4.00	33	33	2.7	
	KBR-5.0M	5.00	33	33	3.0	
Toko	CRHB4.00M	4.00	27	27	3.0	

*: x.xx indicates frequency.

MAIN SYSTEM CLOCK: XTAL (T_a = -20 to +70°C)

Manufacturer	Product Name	Frequency (MHz)	Recommended Circuit Constants		Operating Voltage Range	
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)
Kinseki	HC-6U	1.0 to 2.0	20 *	22	2.7	6.0
	HC-18U HC-43U, 49/U	2.0 to 5.0				

*: Adjust the oscillation frequency in a range of C_1 = 15 to 33 pF.

SUBSYSTEM CLOCK: XTAL (T_a = -10 to +60°C)

Manufacturer	Product Name	Frequency (MHz)	Recommended Circuit Constants			Operating Voltage Range	
			C3 (pF)	C4 (pF)	R (kΩ)	MIN. (V)	MAX. (V)
Kinseki	P-3	32.768	18 *	18	330	2.7	6.0

*: Adjust the oscillation frequency in a range of C3 = 10 to 33 pF.

DC CHARACTERISTICS (T_a = -40 to +85°C, V_{DD} = 2.7 to 6.0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-Level Input Voltage	V_{IH1}	Ports 2, 3, 8		0.7V_{DD}		V_{DD}	V
	V_{IH2}	Ports 0, 1, 6, 7, $\overline{RESET}$		0.8V_{DD}		V_{DD}	V
	V_{IH3}	Ports 4, 5	w/pull-up resistor	0.7V_{DD}		V_{DD}	V
			Open-drain	0.7V_{DD}		10	V
	V_{IH4}	X1, X2, XT1		V_{DD}-0.5		V_{DD}	V
Low-level Input Voltage	V_{IL1}	Ports 2, 3, 4, 5, 8		0		0.3V_{DD}	V
	V_{IL2}	Ports 0, 1, 6, 7, $\overline{RESET}$		0		0.2V_{DD}	V
	V_{IL3}	X1, X2, XT1		0		0.4	V
High-Level Output Voltage	V_{OH1}	Ports 0, 2, 3, 6, 7, 8	V_{DD} = 4.5 to 6.0 V, I_{OH} = -1 mA	V_{DD}-1.0			V
			I_{OH} = -100 μA	V_{DD}-0.5			V
Low-Level Output Voltage	V_{OL1}	Ports 0, 2, 3, 4, 5, 6, 7, 8	Ports 4 and 5 V_{DD} = 4.5 to 6.0 V I_{OL} = 15 mA		0.4	2.0	V
			Ports 3 V_{DD} = 4.5 to 6.0 V I_{OL} = 15 mA		0.6	2.0	V
			V_{DD} = 4.5 to 6.0 V I_{OL} = 1.6 mA			0.4	V
			I_{OL} = 400 μA			0.5	V
	V_{OL2}	SB0, 1 Open-drain	Pull-up ≥ 1 kΩ V_{DD} = 4.5 to 6.0 V			0.2V_{DD}	V
			Pull-up ≥ 5 kΩ			0.2V_{DD}	V
High-Level Input Leakage Current	I_{LIH1}	V_{IN} = V_{DD}	Other than below			3	μA
	I_{LIH2}		X1, X2, XT1			20	μA
	I_{LIH3}	V_{IN} = 10 V	Ports 4, 5 (open-drain)			20	μA
Low-Level Input Leakage Current	I_{LIL1}	V_{IN} = 0 V	Other than below			-3	μA
	I_{LIL2}		X1, X2, XT1			-20	μA
High-Level Output Leakage Current	I_{LOH1}	V_{OUT} = V_{DD}	Other than below			3	μA
	I_{LOH2}	V_{OUT} = 10 V	Ports 4, 5 (open-drain)			20	μA
Low-Level Output Leakage Current	I_{LOL}	V_{OUT} = 0 V				-3	μA
Internal Pull-Up Resistor	R_{L1}	Ports 0, 1, 2, 3, 6, 7, 8 (except P00) V_{IN} = 0V	V_{DD} = 5.0 V±10%	15	40	80	kΩ
			V_{DD} = 3.0 V±10%	30		300	kΩ
	R_{L2}	Ports 4, 5 V_{OUT} = V_{DD}-2.0 V	V_{DD} = 5.0 V±10%	15	40	70	kΩ
			V_{DD} = 3.0 V±10%	10		60	kΩ

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Supply Current *1	I_{DD1}	4.19 MHz*4 crystal oscillator C1 = C2 = 22pF	V_{DD} = 5.0 V±10%*2			2.5	8	mA
			V_{DD} = 3.0 V±10%*3			0.35	1.2	mA
	I_{DD2}		HALT mode	V_{DD} = 5 V±10%		500	1500	μA
				V_{DD} = 3 V±10%		150	450	μA
	I_{DD3}	32.768 kHz*5 crystal oscillator		V_{DD} = 3 V±10%		30	90	μA
	I_{DD4}		HALT mode	V_{DD} = 3 V±10%		5	15	μA
	I_{DD5}	XT1 = 0 V STOP mode		V_{DD} = 5 V±10%		0.5	20	μA
			V_{DD} = 3 V±10%			0.1	10	μA
				T_a = 25°C		0.1	5	μA

*1: Current for the built-in pull-up resistor is not included.

2: When operand in the high-speed mode with the processor clock control register (PCC) set to 0011.

3: When operated in the low-speed mode with the PCC set to 0000.

4: Including when the subsystem clock is operated.

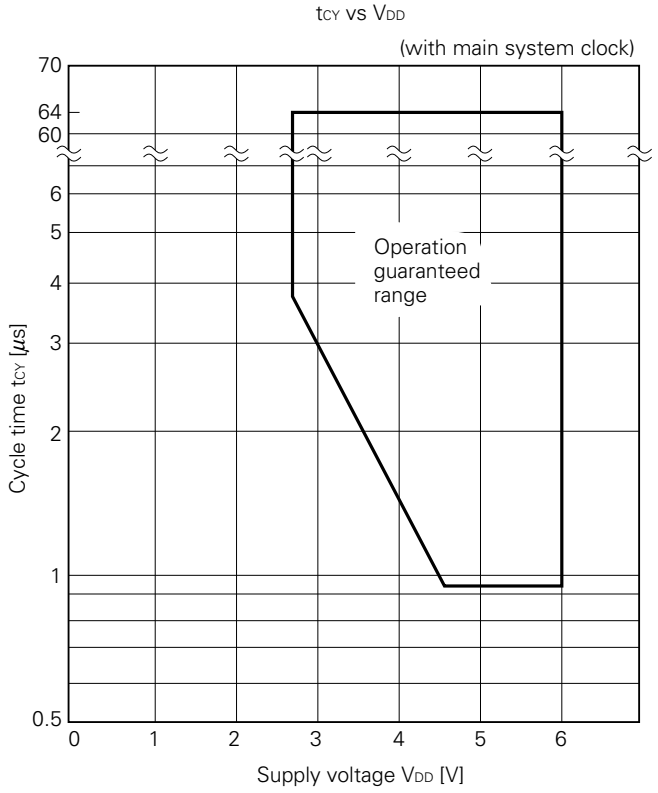
5: When operated with the subsystem clock by setting the system clock control register (SCC) to 1011 to stop the main system clock operation.

AC CHARACTERISTICS (T_a = -40 to +85°C, V_{DD} = 2.7 to 6.0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
CPU Clock Cycle Time*1 (Minimum Instruction Execution Time = 1 Machine Cycle)	t_{CY}	w/main system clock	V_{DD} = 4.5 to 6.0 V	0.95		64	μs
				3.8		64	μs
		w/subsystem clock		114	122	125	μs
TI0 Input Frequency	f_{TI}	V_{DD} = 4.5 to 6.0 V		0		1	MHz
				0		275	kHz
TI0 Input High-, Low-Level Widths	t_{TIH}, t_{TIL}	V_{DD} = 4.5 to 6.0 V		0.48			μs
				1.8			μs
Interrupt Input High-, Low-Level Widths	t_{INTH}, t_{INTL}	INT0		*2			μs
		INT1, 2, 4		10			μs
		KR0-7		10			μs
$\overline{\text{RESET}}$ Low-Level Width	t_{RSL}			10			μs

*1: The CPU clock (Φ) cycle time (minimum instruction execution time) is determined by the oscillation frequency of the connected oscillator, system clock control register (SCC), and processor clock control register (PCC).
The figure on the right is cycle time t_{CY} vs. supply voltage V_{DD} characteristics at the main system clock.

2: $2t_{CY}$ or $128/f_X$ depending on the setting of the interrupt mode register (IM0).



SERIAL TRANSFER OPERATION

Two-Line and Three-Line Serial I/O Modes ($\overline{SCK}$: internal clock output):

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ Cycle Time	t_{KCY1}	V_{DD} = 4.5 to 6.0 V		1600			ns
				3800			ns
$\overline{SCK}$ High-, Low-Level Widths	t_{KL1}	V_{DD} = 4.5 to 6.0 V		t_{KCY1}/2-50			ns
	t_{KH1}			t_{KCY1}/2-150			ns
SI Set-Up Time (vs. $\overline{SCK}$ ↑)	t_{SIK1}			150			ns
SI Hold Time (vs. $\overline{SCK}$ ↑)	t_{KSI1}			400			ns
$\overline{SCK}$ ↓→ SO Output Delay Time	t_{KSO1}	R = 1 kΩ, C = 100 pF*	V_{DD} = 4.5 to 6.0 V	0		250	ns
				0		1000	ns

TWO-LINE AND THREE-LINE SERIAL I/O MODES ($\overline{SCK}$: external clock input):

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ Cycle Time	t_{KCY2}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ High-, Low-Level Widths	t_{KL2}	V_{DD} = 4.5 to 6.0 V		400			ns
	t_{KH2}			1600			ns
SI Set-Up Time (vs. $\overline{SCK}$ ↑)	t_{SIK2}			100			ns
SI Hold Time (vs. $\overline{SCK}$ ↑)	t_{KSI2}			400			ns
$\overline{SCK}$ ↓→ SO Output Delay Time	t_{KSO2}	R = 1 kΩ, C = 100 pF*	V_{DD} = 4.5 to 6.0 V	0		300	ns
				0		1000	ns

*: R and C are load resistance and load capacitance of the SO output line.

SBI MODE ($\overline{SCK}$: internal clock output (master)):

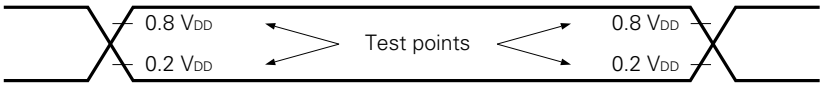
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ Cycle Time	t_{KCY3}	V_{DD} = 4.5 to 6.0 V		1600			ns
				3800			ns
$\overline{SCK}$ High-, Low-Level Widths	t_{KL3} t_{KH3}	V_{DD} = 4.5 to 6.0 V		t_{KCY3}/2-50			ns
				t_{KCY3}/2-150			ns
SB0, 1 Set-Up Time (vs. $\overline{SCK}$ ↑)	t_{SIK3}			150			ns
SB0, 1 Hold Time (vs. $\overline{SCK}$ ↑)	t_{KSI3}			t_{KCY3}/2			ns
$\overline{SCK}$ ↓→ SB0, 1 Output Delay Time	t_{KSO3}	R = 1 kΩ, C = 100 pF*	V_{DD} = 4.5 to 6.0 V	0		250	ns
				0		1000	ns
$\overline{SCK}$ ↑→ SB0, 1 ↓	t_{KSB}			t_{KCY3}			ns
SB0,1 ↓→ $\overline{SCK}$	t_{SBK}			t_{KCY3}			ns
SB0, 1 Low-Level Width	t_{SBL}			t_{KCY3}			ns
SB0, 1 High-Level Width	t_{SBH}			t_{KCY3}			ns

SBI MODE ($\overline{SCK}$: external clock input (slave)):

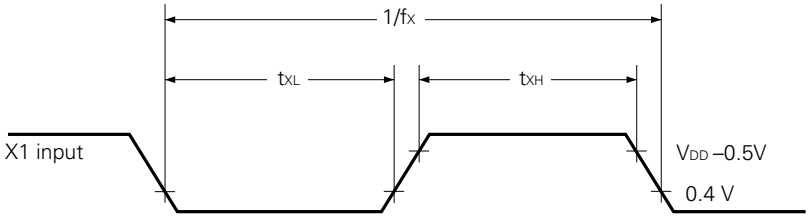
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ Cycle Time	t_{KCY4}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ High-, Low-Level Widths	t_{KL4} t_{KH4}	V_{DD} = 4.5 to 6.0 V		400			ns
				1600			ns
SB0, 1 Set-Up Time (vs. $\overline{SCK}$ ↑)	t_{SIK4}			100			ns
SB0, 1 Hold Time (vs. $\overline{SCK}$ ↑)	t_{KSI4}			t_{KCY4}/2			ns
$\overline{SCK}$ ↓→ SB0, 1 Output Delay Time	t_{KSO4}	R = 1 kΩ, C = 100 pF*	V_{DD} = 4.5 to 6.0 V	0		300	ns
				0		1000	ns
$\overline{SCK}$ ↑→ SB0, 1 ↓	t_{KSB}			t_{KCY4}			ns
SB0,1 ↓→ $\overline{SCK}$ ↓	t_{SBK}			t_{KCY4}			ns
SB0, 1 Low-Level Width	t_{SBL}			t_{KCY4}			ns
SB0, 1 High-Level Width	t_{SBH}			t_{KCY4}			ns

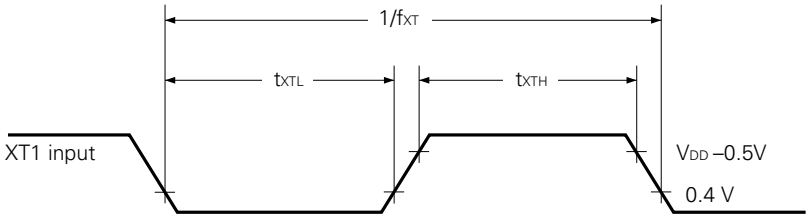
*: R and C are load resistance and load capacitance of the SB0 and SB1 output lines.

AC TIMING TEST POINT (excluding X1 and XT1 inputs)

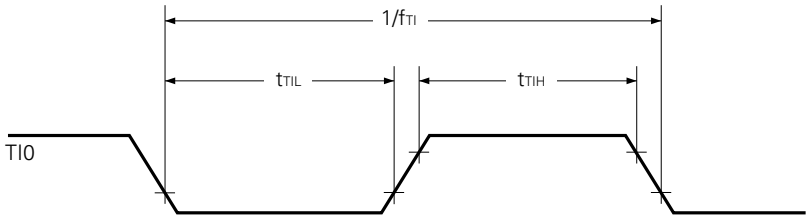


CLOCK TIMING



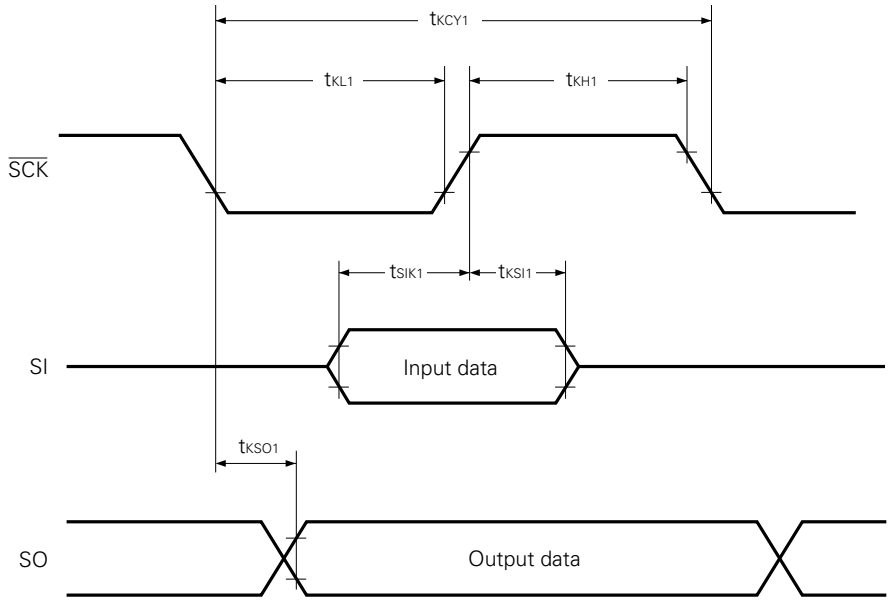


TI0 TIMING

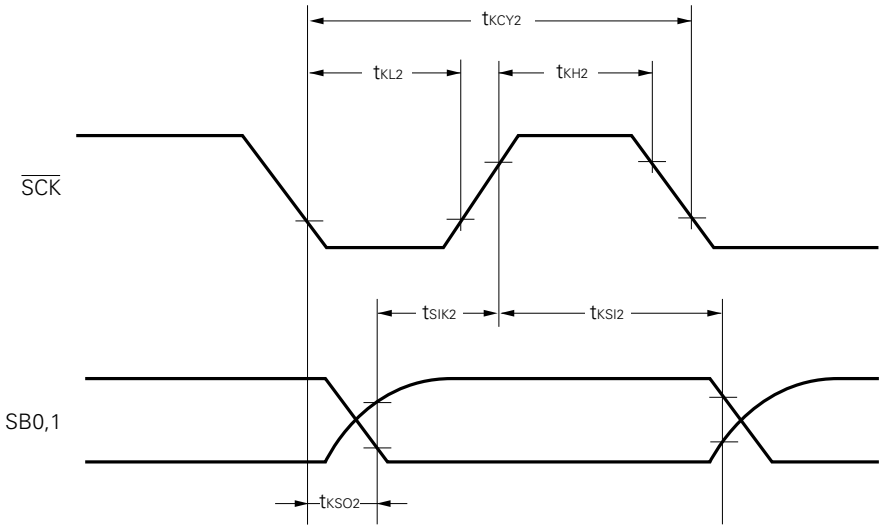


SERIAL TRANSFER TIMING

THREE-LINE SERIAL I/O MODE:

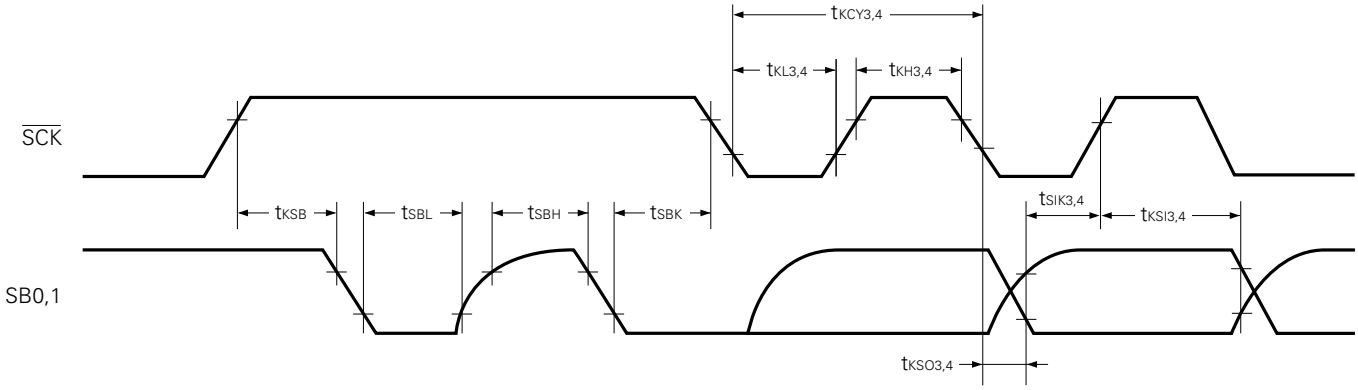


TWO-LINE SERIAL I/O MODE:

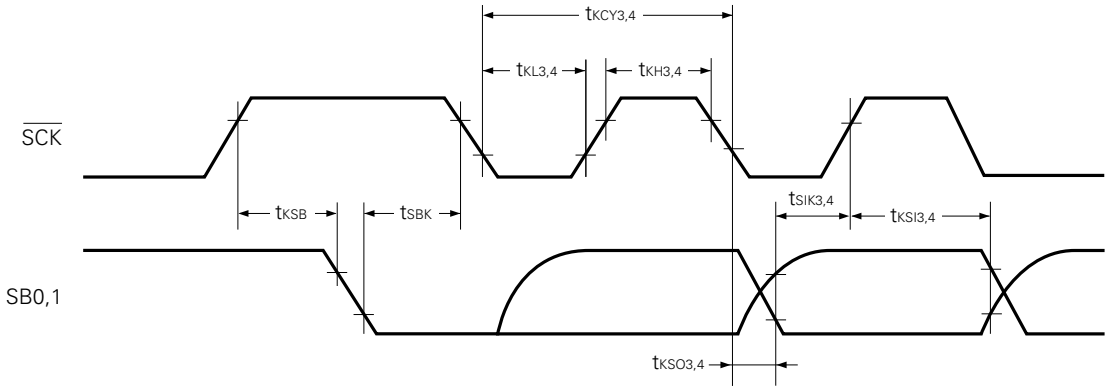


SERIAL TRANSFER TIMING

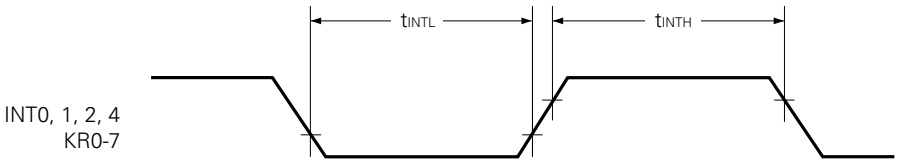
BUS RELEASE SIGNAL TRANSFER:



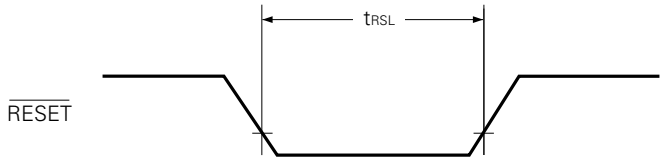
COMMAND SIGNAL TRANSFER:



INTERRUPT INPUT TIMING:



RESET INPUT TIMING:



LOW-VOLTAGE DATA RETENTION CHARACTERISTICS OF DATA MEMORY IN STOP MODE

(T_a = −40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data Retention Supply Voltage	V_{DDDR}		2.0		6.0	V
Data Retention Supply Current*1	I_{DDDR}	V_{DDDR} = 2.0 V		0.1	10	μA
Release Signal Set Time	t_{SREL}		0			μs
Oscillation Stabilization Wait Time*2	t_{WAIT}	Released by $\overline{RESET}$		$2^{17}/f_X$		ms
		Released by interrupt request		*3		ms

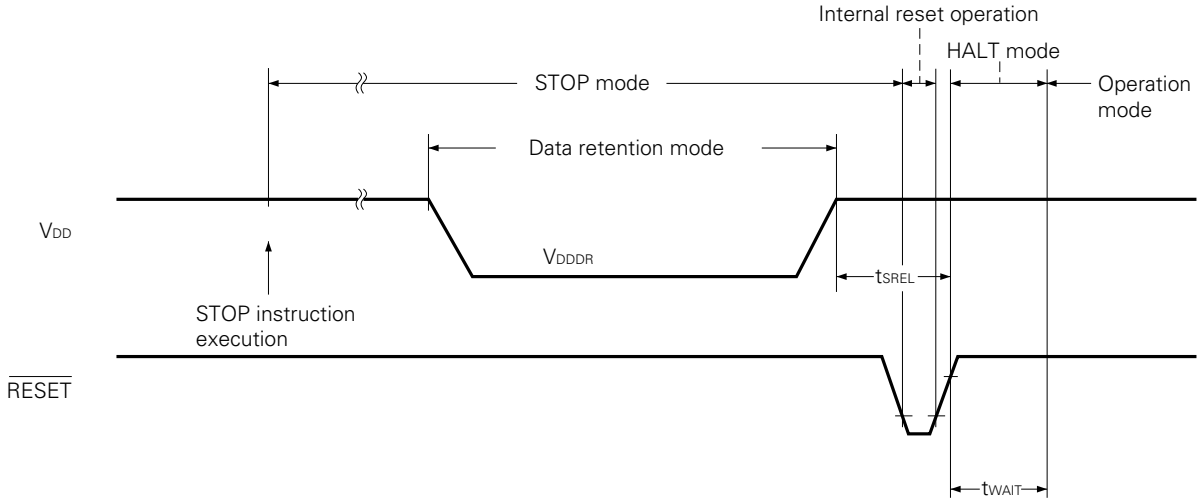
*1: Does not include current flowing through internal pull-up resistor

2: The oscillation stabilization wait time is the time during which the CPU is stopped to prevent unstable operation when oscillation is started.

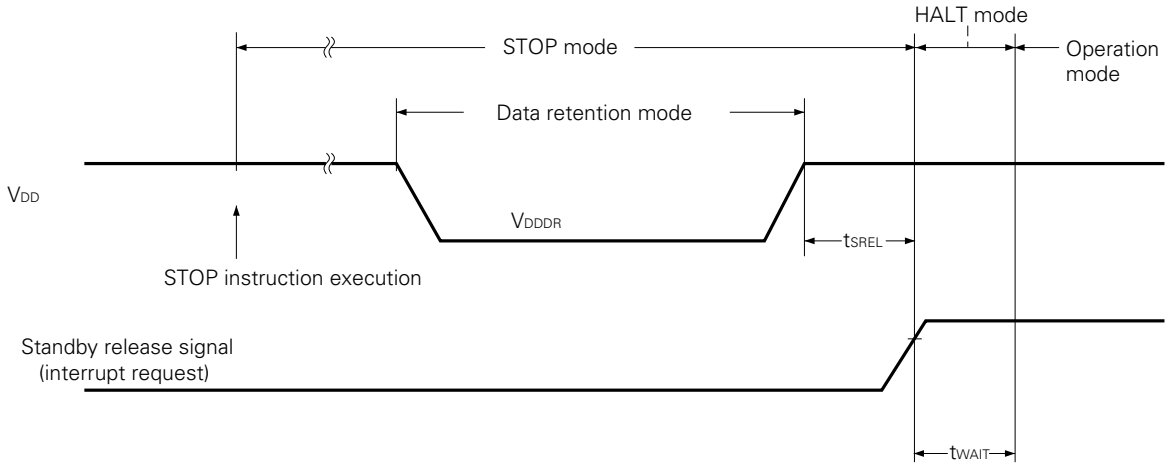
3: Depends on the setting of the basic interval timer mode register (BTM) as follows:

BTM3	BTM2	BTM1	BTM0	WAIT time ( ): f_{XX} = 4.19 MHz
–	0	0	0	$2^{20}/f_{XX}$ (approx. 250 ms)
–	0	1	1	$2^{17}/f_{XX}$ (approx. 31.3 ms)
–	1	0	1	$2^{15}/f_{XX}$ (approx. 7.82 ms)
–	1	1	1	$2^{13}/f_{XX}$ (approx. 1.95 ms)

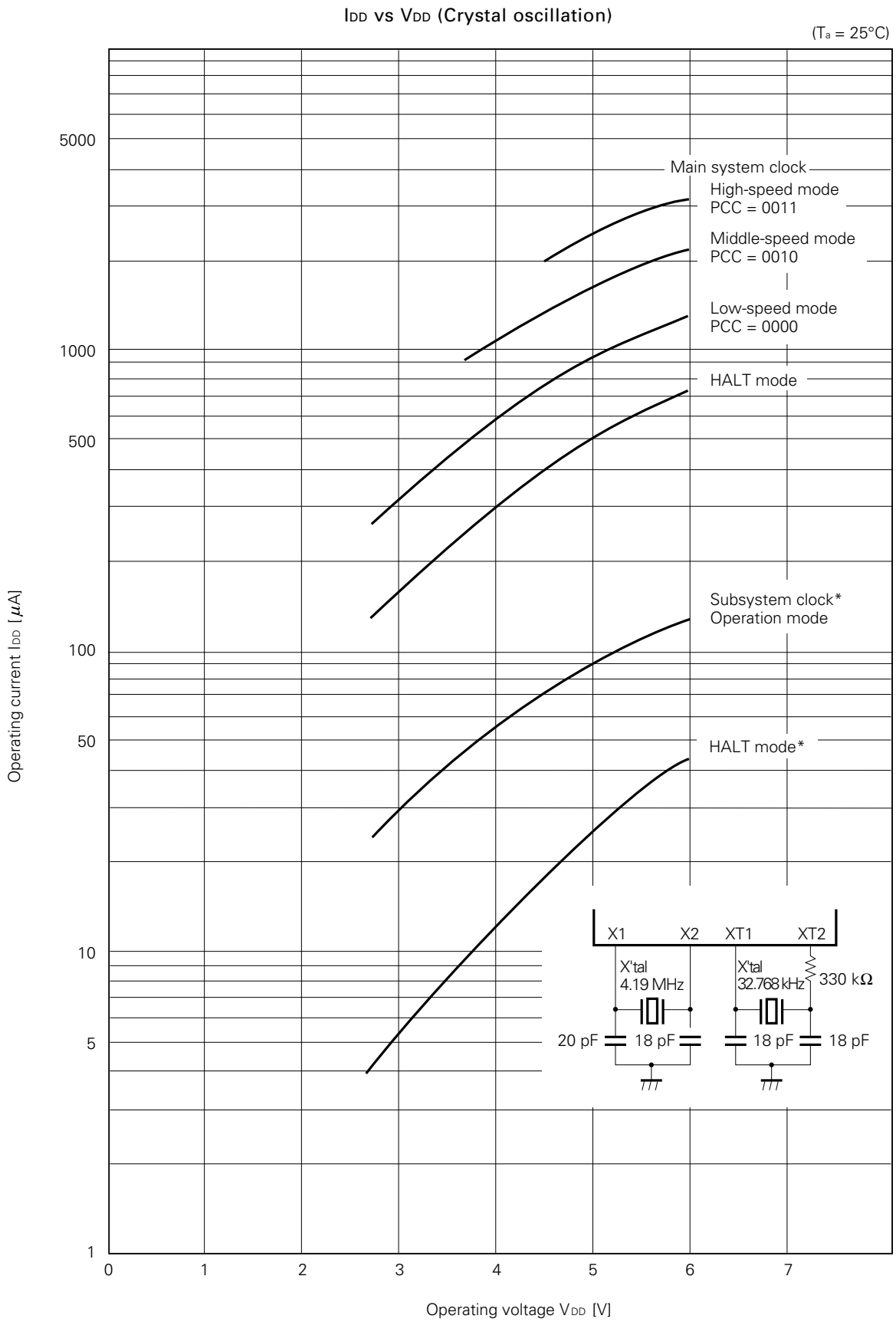
DATA RETENTION TIMING (releasing STOP mode by $\overline{RESET}$)



DATA RETENTION TIMING (standby release signal: releasing STOP mode by interrupt)



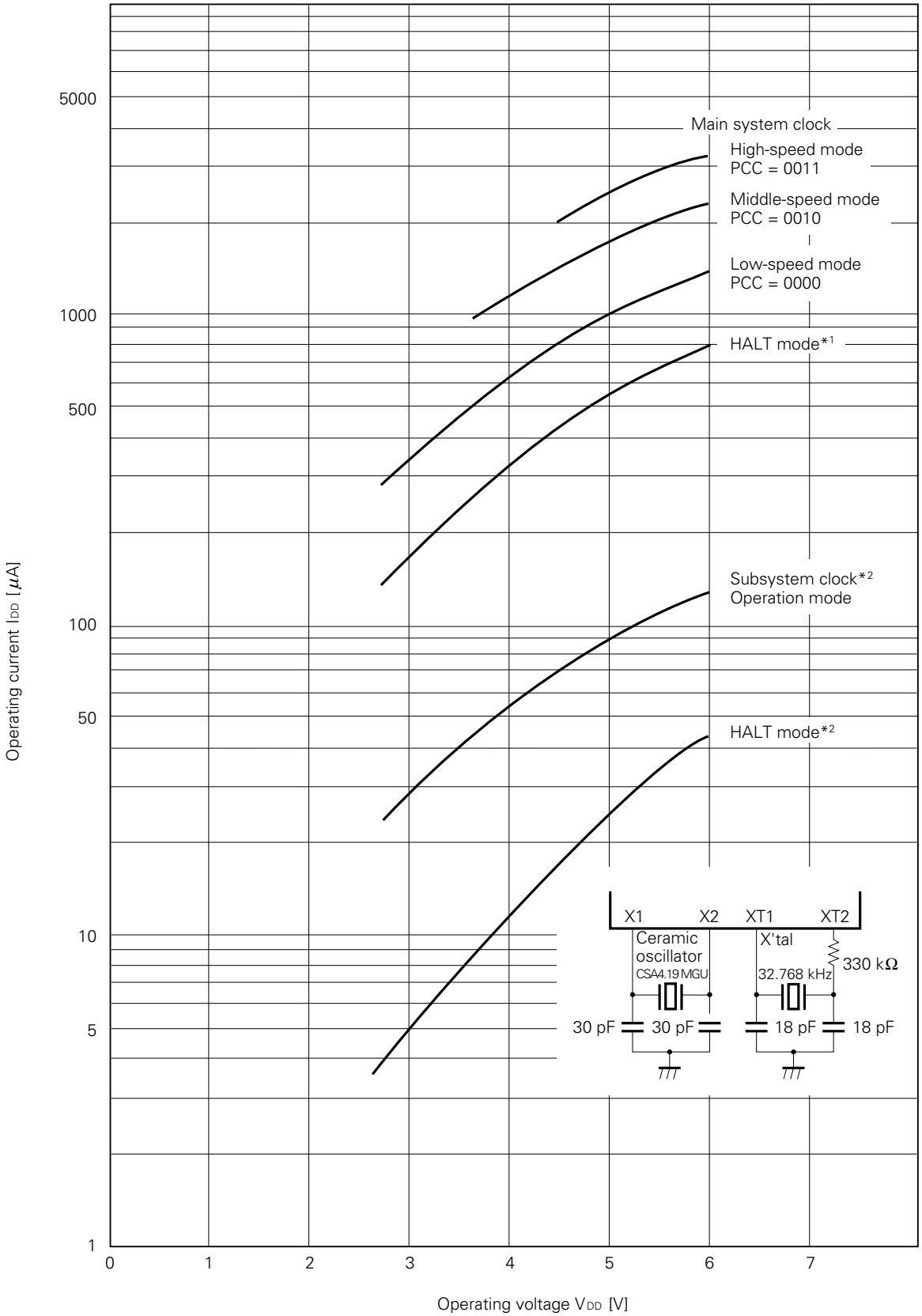
11. CHARACTERISTIC CURVES



*: Main system clock halts.

I_{DD} vs V_{DD} (Ceramic oscillation)

(T_a = 25°C)

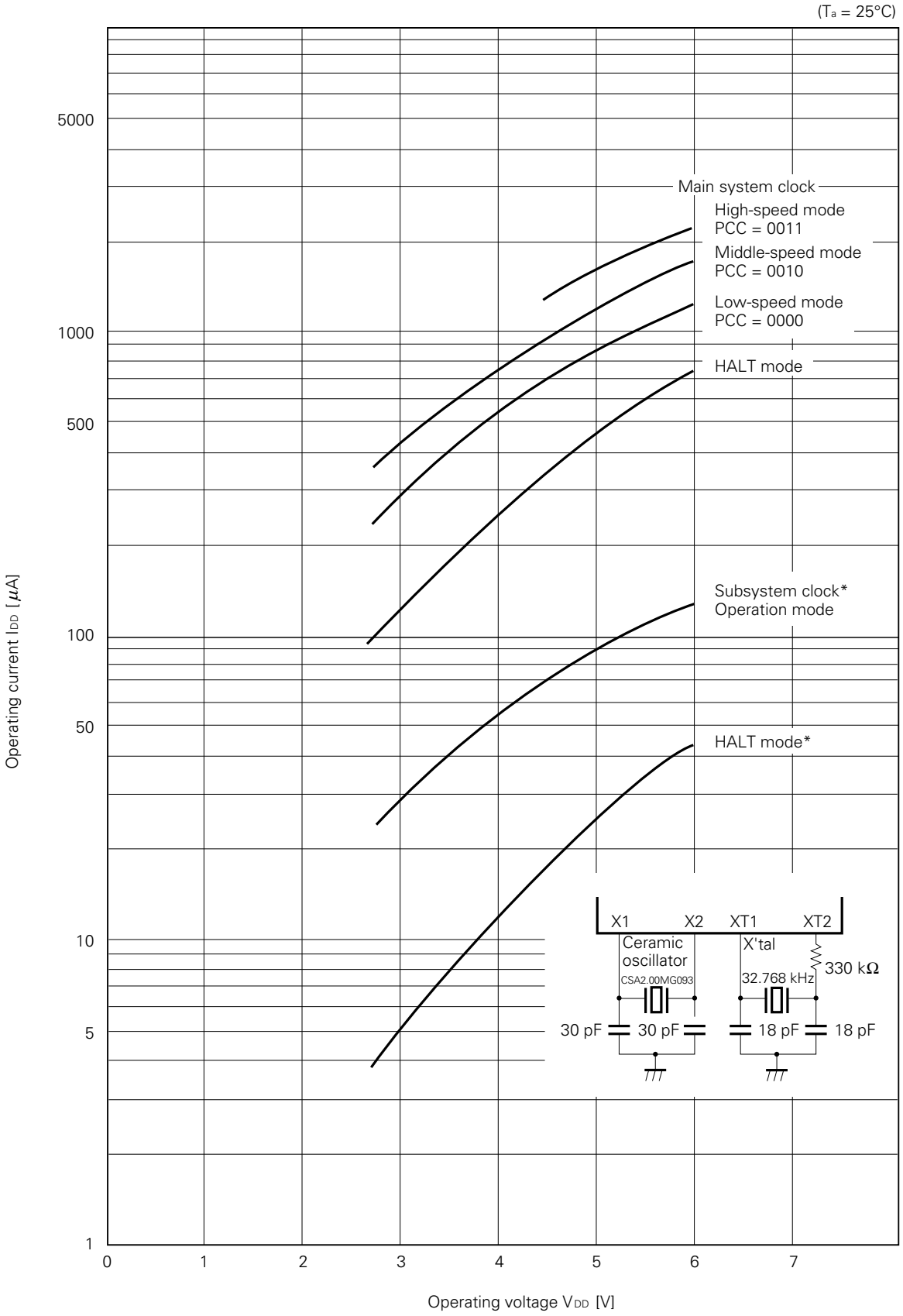


*1: When compared to crystal oscillation, increased by approximately 10%.

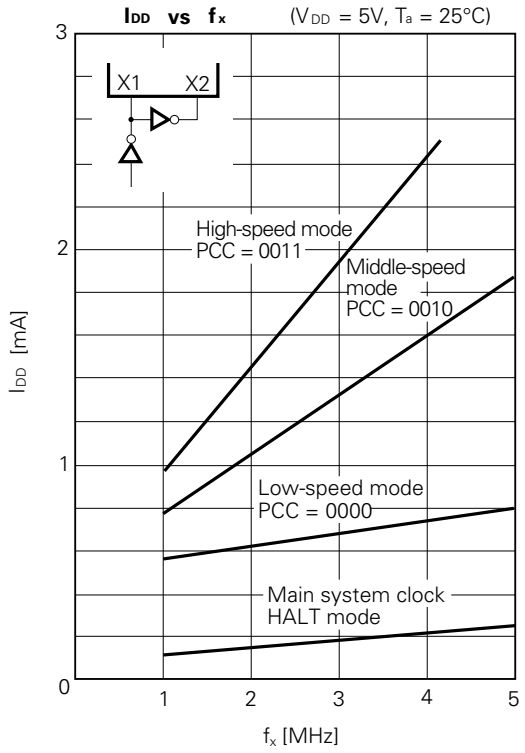
2: Main system clock halts.

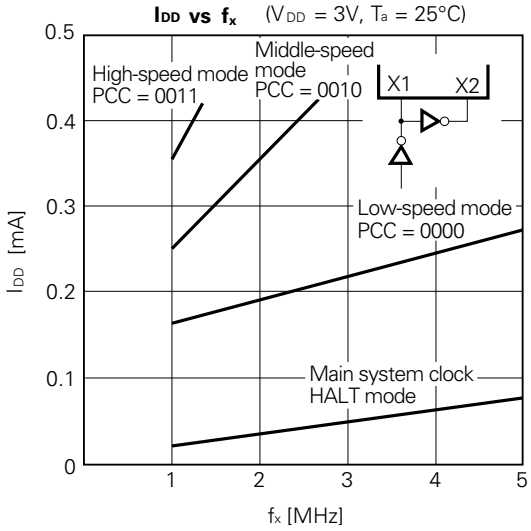
I_{DD} vs V_{DD} (Ceramic oscillation)

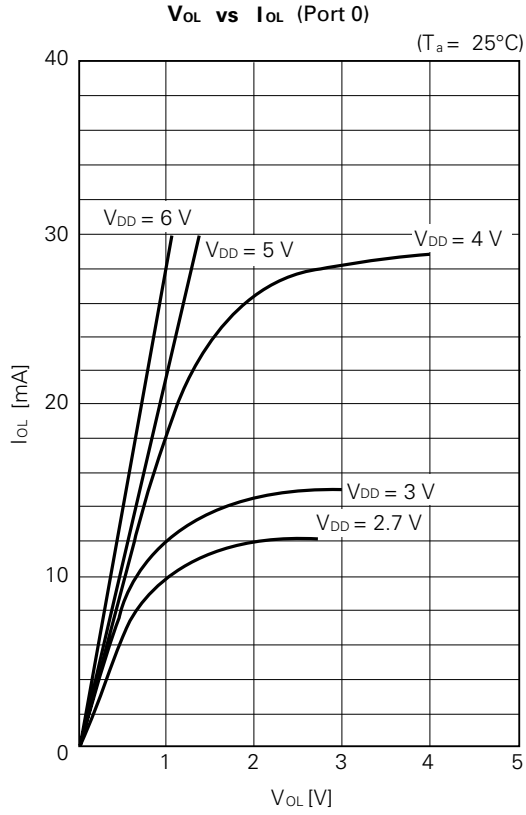
(T_a = 25°C)

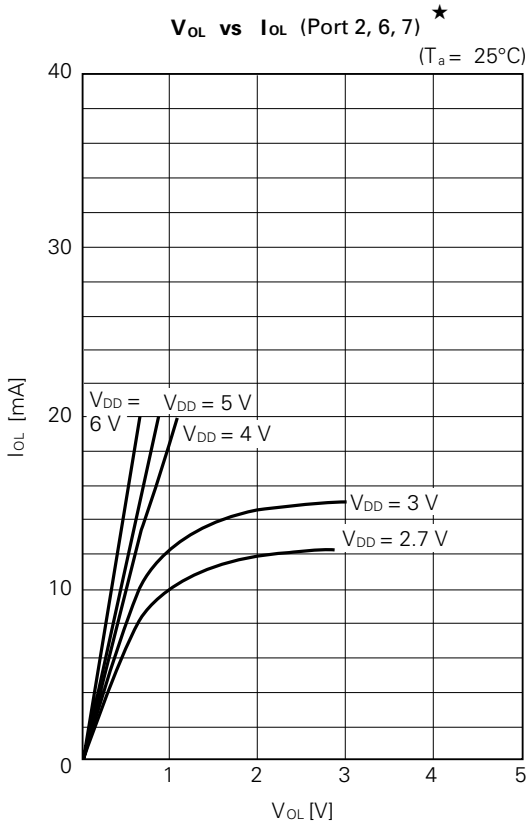


*: Main system clock halts.

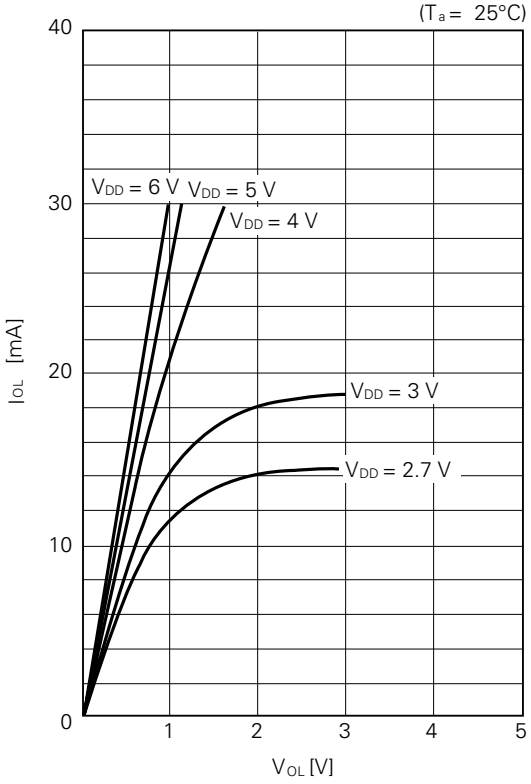




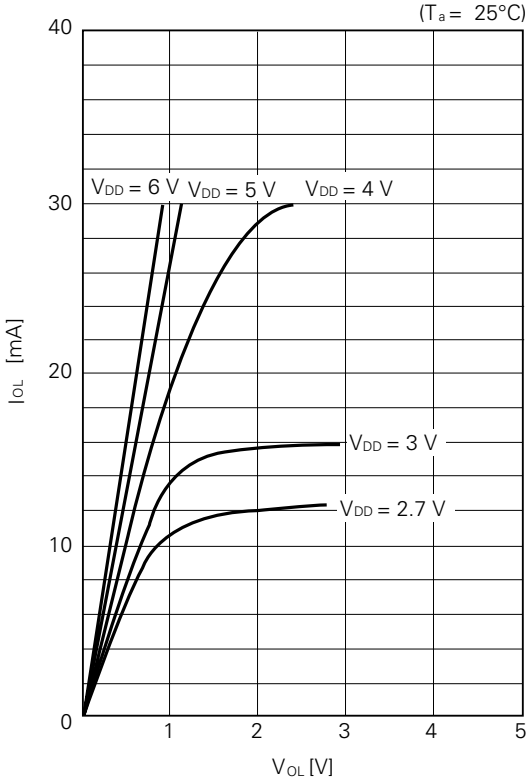




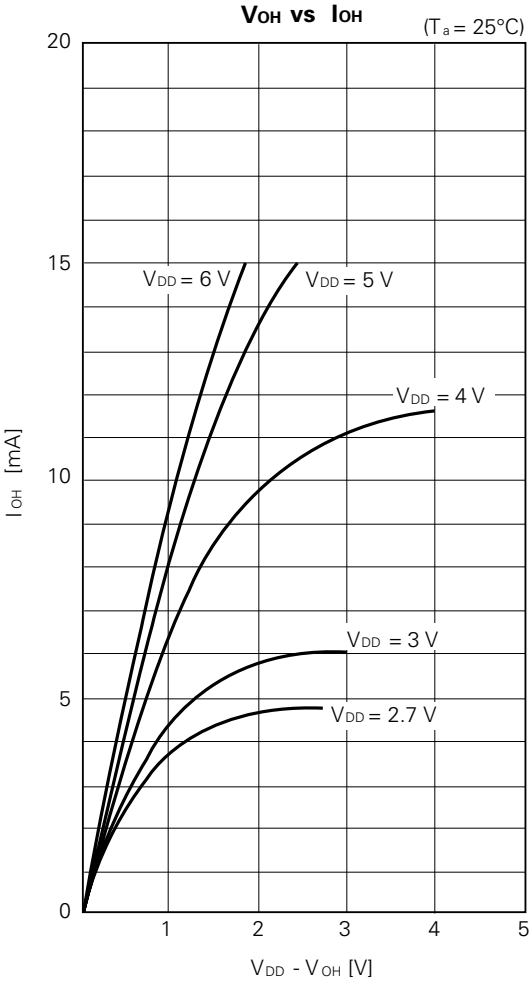
V_{OL} vs I_{OL} (Port 4, 5)



V_{OL} vs I_{OL} (Port 3)

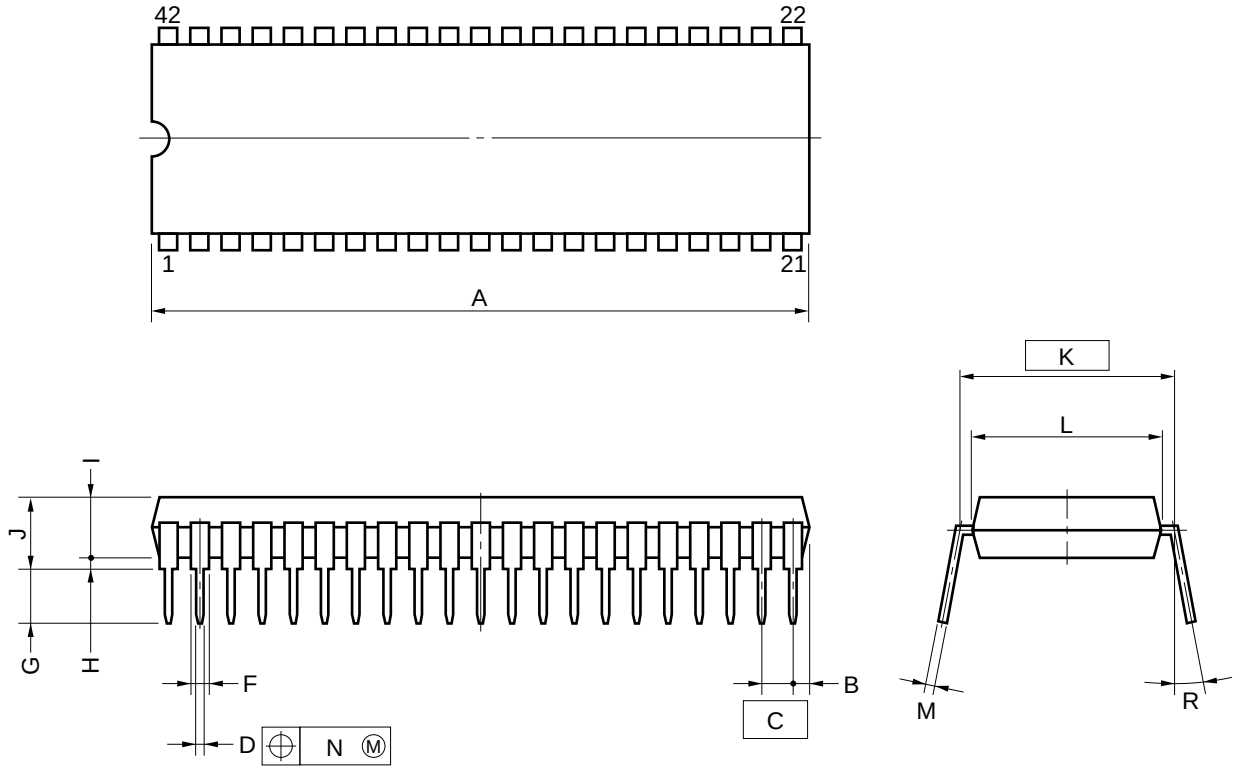


V_{OH} vs I_{OH}



12. PACKAGE DRAWINGS

42PIN PLASTIC SHRINK DIP (600 mil)



NOTES

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

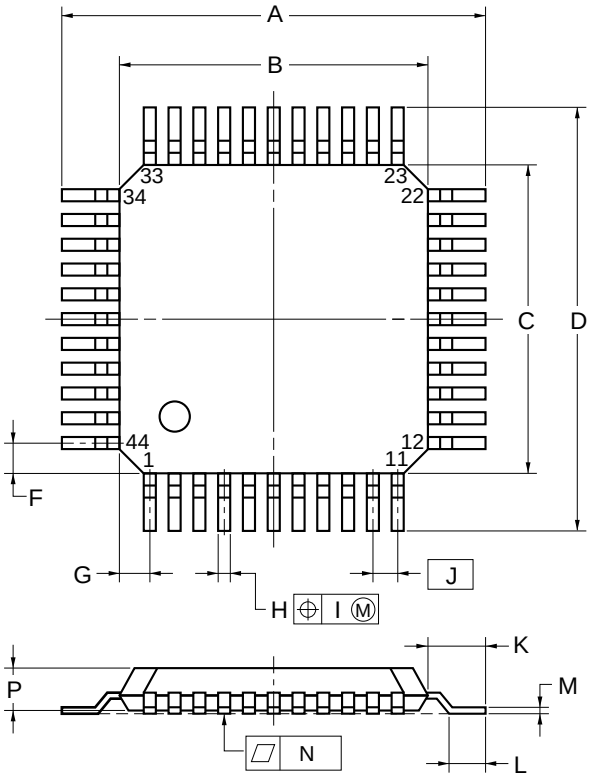
2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	39.13 MAX.	1.541 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50 ± 0.10	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	3.2 ± 0.3	0.126 ± 0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	15.24 (T.P.)	0.600 (T.P.)
L	13.2	0.520
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0~15°	0~15°

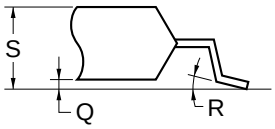
P42C-70-600A-1

44 PIN PLASTIC QFP (□10)

★



detail of lead end



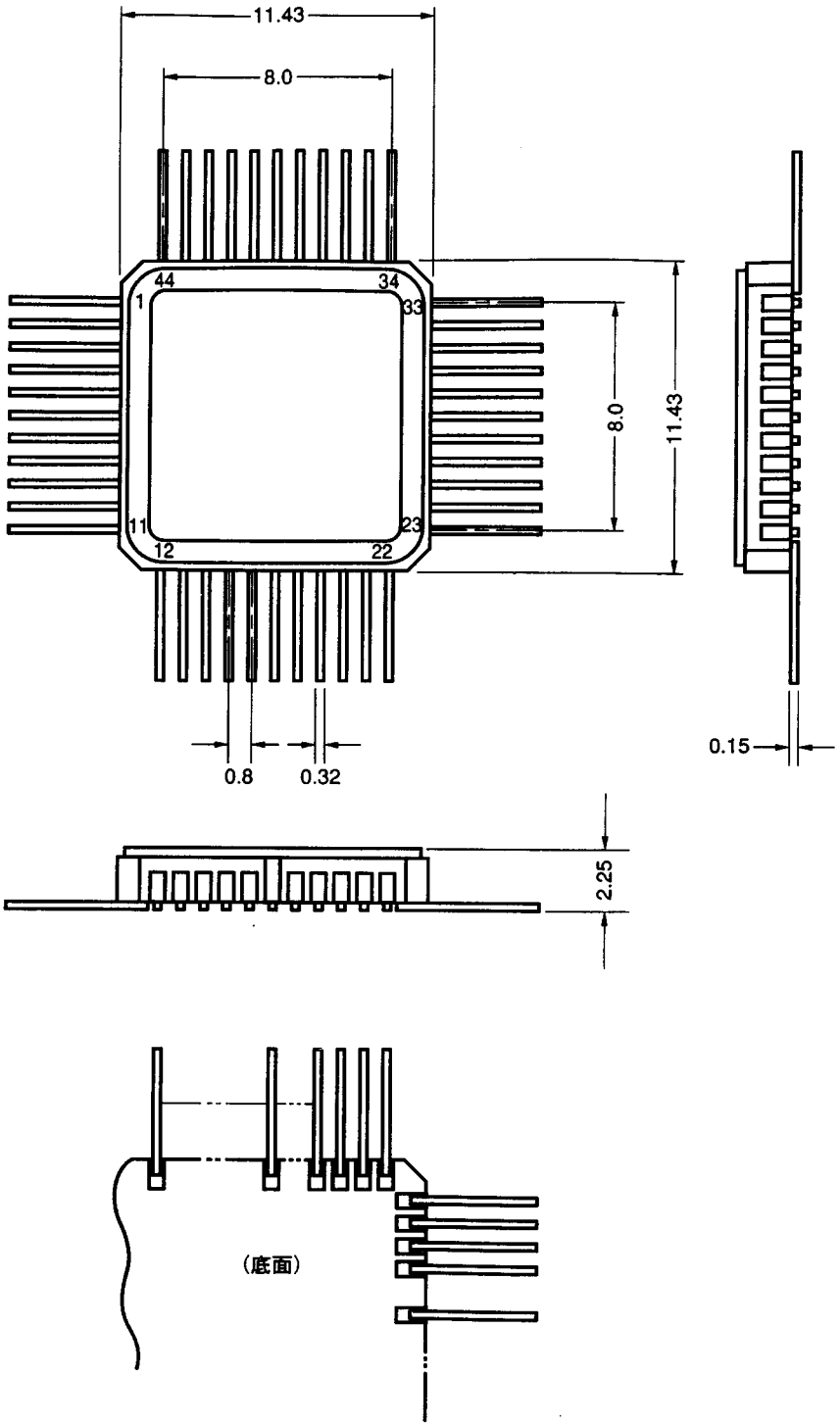
NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	13.6±0.4	$0.535^{+0.017}_{-0.016}$
B	10.0±0.2	$0.394^{+0.008}_{-0.009}$
C	10.0±0.2	$0.394^{+0.008}_{-0.009}$
D	13.6±0.4	$0.535^{+0.017}_{-0.016}$
F	1.0	0.039
G	1.0	0.039
H	0.35±0.10	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

P44GB-80-3B4-3

44-PIN CERAMIC QFP FOR ES (UNITS IN mm)



Note 1: Determine the position of pin 1 from the position of pin 17 which is connected to a metal cap.

2: A metal cap is connected to 17-pin and is Vss (GND) level.

3: Lead wire length is not stipulated because cutting process of lead ends is out of production control.

13. RECOMMENDED SOLDERING CONDITIONS ★

It is recommended that μPD75004, 75006, and 75008 be soldered under the following conditions.

For details on the recommended soldering conditions, refer to Information Document "Semiconductor Devices Mounting Manual" (IEI-616).

The soldering methods and conditions are not listed here, consult NEC.

Table 13-1 Soldering Conditions

μPD75004GB - xxx - 3B4: 44-pin plastic QFP (□10 mm)
μPD75006GB - xxx - 3B4: 44-pin plastic QFP (□10 mm)
μPD75008GB - xxx - 3B4: 44-pin plastic QFP (□10 mm)

Soldering Method	Soldering Conditions	Symbol for Recommended Condition
Infrared Reflow	Package peak temperature: 230°C, time: 30 seconds max. (210°C min.), number of times: 1, number of days: 7 days*, (afterwards, 10 hours of prebaking at 125°C is required.)	IR30-107-1
VPS	Package peak temperature: 215°C, time: 40 seconds max. (200°C min.), number of times: 1, number of days: 7 days*, (afterwards, 10 hours of prebaking at 125°C is required.)	VP15-107-1
Wave Soldering	Soldering bath temperature: 260°C max., time: 10 seconds max., number of times: 1, number of days: 7 days*, (afterwards, 10 hours of prebaking at 125°C is required.) pre-heating temperature: 120°C max. (package surface temperature)	WS60-00-1
Pin Partial Heating	Pin temperature: 300°C max., time: 3 seconds max. (per side)	—

*: This means the number of days after unpacking the dry pack. Storage conditions are 25°C and 65% RH max.

Caution: Do not use two or more soldering methods in combination (except the pin partial heating method).

Table 13-2 Soldering Conditions of Through-Hole Type

μPD75004CU - xxx : 42-pin plastic shrink DIP (600 mil)
μPD75006CU - xxx : 42-pin plastic shrink DIP (600 mil)
μPD75008CU - xxx : 42-pin plastic shrink DIP (600 mil)

Soldering Method	Soldering Conditions
Wave Soldering (Only for lead part)	Soldering bath temperature: 260°C max., Time: 10 seconds max.
Pin Partial Heating	Pin temperature: 260°C max., Time: 10 seconds max.

Notice

A model that can be soldered under the more stringent conditions (infrared reflow peak temperature: 235°C, number of times: 2, and an extended number of days) is also available.
For details, consult NEC.

APPENDIX A. DEVELOPMENT TOOLS

The following development support tools are readily available to support development of systems using μPD75008:

Hardware	IE-75000-R *1 IE-75001-R	In-circuit emulator for 75X series
	IE-75000-R-EM *2	Emulation board for IE-75000-R and IE-75001-R
	EP-75008CU/GB-R	Emulation prove for μPD75004CU/GB, 75006CU/GB, 75008CU/GB
	PG-1500	PROM programmer
	PA-75P008CU	PROM programmer adapter solely used for μPD75P008CU/GB. It is connected to PG-1500.
Software	IE Control Program	Host machine • PC-9800 series (MS-DOS™ Ver.3.30 to Ver.5.00A*3) • IBM PC/AT™ (PC DOS™ Ver.3.1)
	PG-1500 Controller	
	RA75X Relocatable Assembler	

*1: Maintenance product

2: Not provided with IE-75001-R.

3: Ver.5.00/5.00A has a task swap function, but this function cannot be used with this function.

Remarks: For development tools from other companies, refer to 75X Series Selection Guide (IF-151).

APPENDIX B. RELATED DOCUMENTS ★

[MEMO]

GENERAL NOTES ON CMOS DEVICES

① STATIC ELECTRICITY (ALL MOS DEVICES)

Exercise care so that MOS devices are not adversely influenced by static electricity while being handled.

The insulation of the gates of the MOS device may be destroyed by a strong static charge. Therefore, when transporting or storing the MOS device, use a conductive tray, magazine case, or conductive buffer materials, or the metal case NEC uses for packaging and shipment, and use grounding when assembling the MOS device system. Do not leave the MOS device on a plastic plate and do not touch the pins of the device.

Handle boards on which MOS devices are mounted similarly .

② PROCESSING OF UNUSED PINS (CMOS DEVICES ONLY)

Fix the input level of CMOS devices.

Unlike bipolar or NMOS devices, if a CMOS device is operated with nothing connected to its input pin, intermediate level input may be generated due to noise, and an inrush current may flow through the device, causing the device to malfunction. Therefore, fix the input level of the device by using a pull-down or pull-up resistor. If there is a possibility that an unused pin serves as an output pin (whose timing is not specified), each pin should be connected to V_{DD} or GND through a resistor.

Refer to “Processing of Unused Pins” in the documents of each devices.

③ STATUS BEFORE INITIALIZATION (ALL MOS DEVICES)

The initial status of MOS devices is undefined upon power application.

Since the characteristics of an MOS device are determined by the quantity of injection at the molecular level, the initial status of the device is not controlled during the production process. The output status of pins, I/O setting, and register contents upon power application are not guaranteed. However, the items defined for reset operation and mode setting are subject to guarantee after the respective operations have been executed.

When using a device with a reset function, be sure to reset the device after power application.

[MEMO]

M4 92.6